PR2000: A 90-W, High-Efficiency, LLC Series-Resonant Converter with Secondary-Side Synchronous Rectification

Power Management – Consumer Isolated Power

1 INTRODUCTION

This guide documents the design of a low-profile, high-efficiency, LLC series-resonant DC/DC converter that incorporates secondary-side synchronous rectifiers (SR). The converter is optimized for a 90-W laptop adapter application and designed to operate from the high-voltage output produced by an upstream AC/DC boost power factor correction (PFC) converter. The boost PFC converter would allow this adapter to operate from a universal line-voltage input. The LLC resonant converter provides an isolated output of 19.5 VDC from an input voltage range of 320–420 VDC. At a rating of 90 W the circuit has a maximum continuous load of 4.6 A.

Off-line ac adapters used for powering laptop PCs demand increasingly higher operating efficiencies in ever smaller packages. The combination of high efficiency operation and a low-profile package reduces the adapter's overall size, weight and cost by minimizing the need for thermal management. The improved efficiency of this design is made possible by replacing the Schottky rectifiers that are normally used in the secondary circuit with synchronously controlled MOSFETs. Due to their low drain-source 'on' resistance, synchronously switched MOSFETs can operate with a much lower voltage drop than regular diode rectifiers. Depending on the combination of load current and output voltage the power dissipation of an adapter can be reduced by several watts using this design.

The circuit features four integrated circuit devices from Texas Instruments. They include the UCC25600; a low-cost resonant converter controller, and the UCC24610; a green rectifier controller. Other parts used include the TL431A shunt regulator and the TPS71550 low drop-out linear regulator. The circuit requires a 12-VDC external bias supply to operate. In a regular adapter design the bias power would be produced by the boost PFC AC/DC converter stage that would normally precede this circuit.

2 SCOPE

The UCC24610 Green Rectifier Controller is optimized for 5-V systems and can be used for LLC outputs up to 15 V when a separate 5-V supply is available. Above 15 V the UCC24610 is limited by the 50-V maximum voltage rating of the VD pin. This is because in a conventional secondary rectifier arrangement, that employs two rectifiers with a center-tapped secondary winding, each rectifier sees a peak reverse voltage equal to twice the regulated output.

The scope of this reference design guide is to describe the design and performance of a functional circuit that extends the application of the UCC24610 to systems with output voltages up to 30 V. This is achieved using an alternate topology for secondary rectification and addressing the design constraints that the topology presents. Two configurations are described for synchronizing the turn-off of each SR circuit using the gate-drive signals on the primary side of the converter.

An area not addressed by this guide is electromagnetic compatibility (EMC). For most applications, EMI filter components are added so that the design meets applicable environmental and system compatibility requirements. To comply with EMC standards, components such as input and output filters are required to suppress electromagnetic interference (EMI).

3 ELECTRICAL PERFORMANCE

Table 1 Performance Specifications

Symbol	Parameter	Notes and Conditions	Min	Nom	Max	Units
INPUT CHARACTERSTICS						
V_I	Input Voltage		320		420	VDC
I_I	Input Current				0.5	A
V_{CC}	Bias supply voltage		11.5		16	V
I_{CC}	Bias supply current	Output enabled		20		mA
OUTPUT CHARACTERSTICS						
V_O	Output Voltage		19.2	19.5	19.8 (1)	V
I_O	Output Current		1 (2)		4.6	A
P_O	Output Power				90	W
I_{LIM}	Current Limit	ΔV_O = -2 V		6		A
ΔV_{LOAD}	Load Regulation	V_I =390 V		0.05		$\%V_O$
ΔV_{LINE}	Line Regulation	I_O =3 A		0.1		
V_O(ripple)	Output Voltage Ripple	V_I =390 V, I_O =3 A		150		mV_{PP}
SYSTEM CHARACTERSTICS						
η	Efficiency	V_I =390 V, I_O =3 A		94		%
	Overall thickness (3)				18	mm
	Temp. Range	Nat'l Conv. airflow	0		50	°C

(1) Equivalent to an output voltage tolerance of ±1.5%.

(2) Operates at no load with reduced regulation and burst mode operation.

(3) Excludes terminal blocks for power input and output connections.

4 BACKGROUND

4.1 LLC Series-Resonant Topology

Figure 1 shows the topology of this LLC series-resonant converter. The input is powered from a high-voltage DC source. This is normally the regulated output of the boost PFC pre-regulator. The circuit comprises of a ½-bridge power stage (Q1, Q2), which is connected to the series elements of an LLC resonant circuit. The LLC resonant circuit is formed by the series combination of the magnetizing inductance (L_M) and low-value leakage inductance of the main transformer (L_R), and the combined capacitance on the passive side of the bridge (C_R). The resonant frequency is set by the low-value leakage inductance of the main transformer (approx. 80 µH) and total bridge capacitance (0.02 µF). These values set the resonant frequency at approximately 123 kHz.

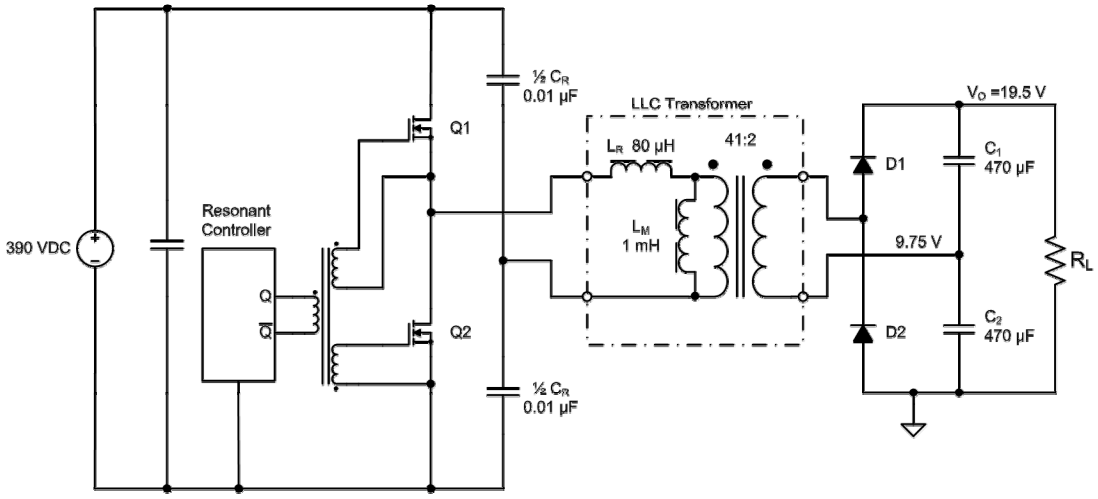

Figure 1 LLC Series-Resonant Converter

The ½-bridge power stage operates at a fixed 50% duty and varying frequency. At resonant frequency the voltages across the resonant components of the circuit cancel, allowing the full peak-peak voltage from the power stage to be applied across the transformer primary. This is the unity gain operating condition. By varying the frequency either below or above the circuit's resonance, the output voltage of the converter, can be increased or decreased respectively. The operating frequency is the control parameter that regulates the output of a resonant converter.

In this design the resonant inductor is integrated into the main transformer as a leakage component. The magnetizing inductance (L_M) also affects the gain of the circuit versus frequency and plays an important role in limiting the switching losses of the MOSFET drivers. Energy stored in the magnetizing inductance forces current to circulate during the short period when both MOSFET switches are 'off'. The phase of this current has the effect of reducing the voltage across each MOSFET prior to it turning on. This is referred to as zero-voltage switching (ZVS). ZVS improves efficiency by reducing the switching losses of the converter. It also reduces the electrical noise produced by the circuit compared to the rapid collapse of the MOSFET drain voltage with normal switching.

4.2 Secondary Rectifier Configuration

LLC converters generally use a center-tapped transformer secondary winding with two rectifiers; one at each end of the winding. This allows the rectifiers and each half winding to share the load current by conducting alternate half cycles. However the rectifiers must be rated at more than 2× the output voltage.

To limit the peak voltage to the VD pin of the UCC24610 SR controller, the rectifiers in this design are stacked in a voltage doubling arrangement. This reduces the voltage seen by each rectifier to 1× the output voltage, allowing MOSFETS with a lower V_{DS} (max) and on resistance to be used. It also eliminates the requirement for a center tap on the main transformer secondary winding, reducing manufacturing cost. However there are compromises. Both rectifiers are now required to conduct the full load current. This doubles the peak current in the secondary winding, which must now pass current in both half cycles. The combination of twice the current magnitude and full-cycle conduction increases the rms current in the secondary winding by a factor of $2 \times \sqrt{2}$. Secondly the rectifiers no longer share a common anode, requiring the control circuit for the upper rectifier (D1 in Figure 2) to float on the ac-voltage end of the transformer secondary winding. This is the switch node between the two rectifiers.

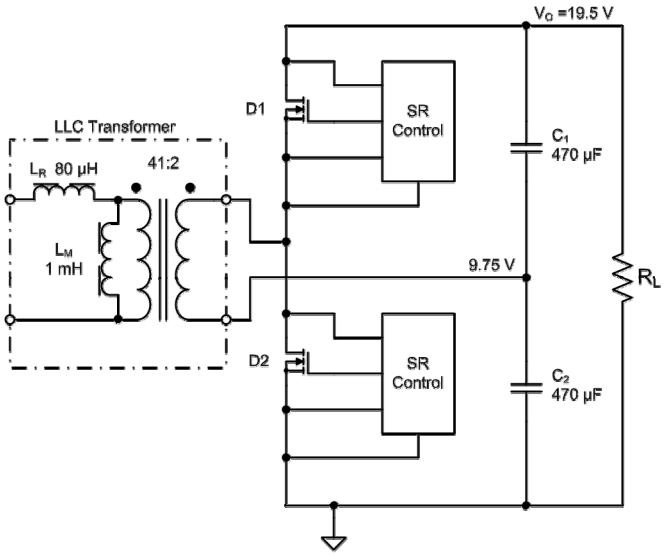

Figure 2 Voltage-Doubling Rectifier Circuit with Synchronously Switched MOSFETs

5 SCHEMATICS AND CIRCUIT DESCRIPTION

The schematics provided in this section are for reference only. For the purposes of clarity some of the detailed component parameters are not shown. Consult the list of materials for additional information.

Three versions of the schematic are presented. The choice depends on the desired synchronization method for turning the UCC24610 SR controllers off, using the gate-drive signals from the primary side of the converter. The synchronization configurations are described in detail in the section 5.2, Secondary-Side Synchronous Rectifier Circuit. The primary circuit and feedback control is the same for all three synchronization methods. The following description refers to Figure 3, Figure 4, and Figure 5.

5.1 Primary Circuit and Feedback Control

The half-bridge power stage is comprised of the MOSFETs Q1, Q2. These are controlled by the UCC25600 via an isolated gate drive, T2. The UCC25600 is a very simple and low-cost part to use. In addition to providing a variable drive frequency for the ½-bridge power stage, it includes a soft-start feature, over-current shutdown protection, and adjustment of the switch dead time between Q1 and Q2.

Load current is sensed through the resonant capacitance using a parallel 0.001-µF capacitor to ground (C7). This capacitor is in parallel with the 0.02-µF of resonant capacitance (C5+C6) to form a 1:21 impedance divider. Current through C7 is half-wave rectified (D3) and then passed through a sense resistor (R19). The resulting signal is then filtered (R18 and C25) and fed to the OC pin (pin 3) of the UCC25600 (U1). This method of sensing current provides less variation in the sensed current versus the switching frequency.

The resonant current is susceptible to a high surge current during converter start-up. For this reason it is recommended that the sensitivity of the current sense circuit is reduced during converter start up. This circuit accomplishes this using a p-channel JFET (Q6) and a divider resistor (R20). The gate of the JFET is connected to the SS pin (pin 4) of the UCC25600, which is initially low during converter start up. The JFET places the divider resistor in circuit during the period that its gate voltage is low. When the soft-start period is complete the rising gate voltage to the JFET pinches off its channel. This isolates the divider resistor and returns the current sense gain to normal.

A limitation of LLC series-resonant converters is that they operate over a limited input voltage range. This is because below a certain operating frequency the frequency-gain relationship of the converter is reversed. The operating frequency of the UCC25600 is controlled by the magnitude of current flowing from the RT pin (pin 2). A resistor to ground, R22, sets the minimum operating frequency to approximately 70 kHz.

To help limit the surge current during start-up the UCC25600 incorporates a soft-start feature. The maximum control frequency is set by R23. The value of this resistor sets the maximum frequency of the UCC25600 above 360 kHz. Above 360 kHz the device will enter burst-mode in order to maintain control of the output at light loads.

The converter output voltage is regulated by a TL431A shunt regulator (U7) located in the secondary. The error signal generated from the TL431A is passed back to the converter primary using a coupler (U6). A decrease in the voltage at the output of the coupler increases the current pulled from RC pin (pin 2) of the UCC25600. This increases the switching frequency of the converter to reduce its gain and output voltage.

5.2 Secondary-Side Synchronous Rectifier Circuit

The control circuit for the two synchronous rectifiers (SRs) in the secondary is identical. The only difference is the method by which the circuits are powered. The upper SR circuit formed by U2, U4, Q3 and C19 effectively sits on top of the lower SR circuit formed by U3, U5, Q4, and C20. The voltage developed across each circuit's capacitor (C19 and C20) is approximately 9.75 VDC, producing a total of 19.5 VDC across both capacitors. The supply voltage to each UCC24610 controller (U4, U5) is tightly regulated to 5 VDC by a low-cost linear regulator (U2, U3).

The lower SR circuit is referenced to secondary ground (SECGND) and can be powered directly from the steady-state 9.75 VDC produced across C20. However the upper SR circuit floats on the 10 VAC produced at one end of the transformer secondary winding. The voltage at this node swings approximately ±10 V with respect to the junction of C19 and C20, requiring the upper circuit to be powered using the bootstrap diode (D1). During operation

the upper SR circuit common swings 10 V below the C19/C20 junction, allowing D1 to charge the capacitor (C9) at the input to the linear regulator, U2.

It is important that the SR FETs turn off correctly without any conduction overlap. This is especially when the rate of change in voltage (dv/dt) produced across secondary winding is high. The reference circuit offers two methods for synchronizing the turn off of the UCC24610 SR controllers using a gate-drive signal on the primary side of the converter.

5.2.1 Self-Synchronization Configuration

Figure 3 shows the schematic for the "self-synchronizing"' circuit configuration. This synchronization method has the minimum component count but relies on the UCC24610 SR controllers to turn themselves off after sensing that the FET drain current has decayed. The method is made possible by the device's ability to sense milli-volts of voltage drop across the FET. Each FET must turn off prior to the reversal in the main transformer secondary voltage. Otherwise the transformer output is shorted. The most vulnerable condition occurs when the converter is operating at a frequency well above resonance at relatively high input voltages; 390-420 VDC. Above resonance the primary current is interrupted prior to completing the resonant half-cycle and drops dramatically. The rate of decay is limited only be the relatively low resonant inductance provided by the transformer's leakage. The ability for the SR controllers to turn off in a timely manner is conditional on a moderate rate of decay of the resonant current.

5.2.2 Pulse Transformer Synchronization

One reliable method of passing synchronization signals between the primary and secondary circuit is with a small pulse transformer. Not only are the primary and secondary circuits isolated, but the zero-volt reference to the upper SR FET and control circuit (Q3, U4) floats on a switch node. This switch node is stepped up and down by 10 V with respect to the primary and secondary ground at the switch frequency of the converter.

The schematic for this method is detailed in Figure , and the additional components are listed in Table 3. They include the pulse transformer, T3. The external pull-up resistors, R32 and R33 are added to dampen oscillations from each primary transition due to the pulse transformer's leakage inductance.

5.2.3 Synchronization Using 'Y' Type Safety-Rated Capacitors

Figure 5 shows how 'Y' type, safety-rated capacitors (C15, C16), can be used to provide synchronization signals to the UCC24610 SR controllers. This works fairly well but results in a shorter conduction period for the upper SR FET. As the 0-V reference for the upper SR-FET and controller (Q3, U4) floats on a switch node, a false negative pulse is produced due to the 0-V to the upper SR circuit rising sharply at the start of this rectifier's conduction period. This "false" pulse momentarily inhibits the upper SR controller from turning on its FET (Q3) by approximately 0.2 µs.

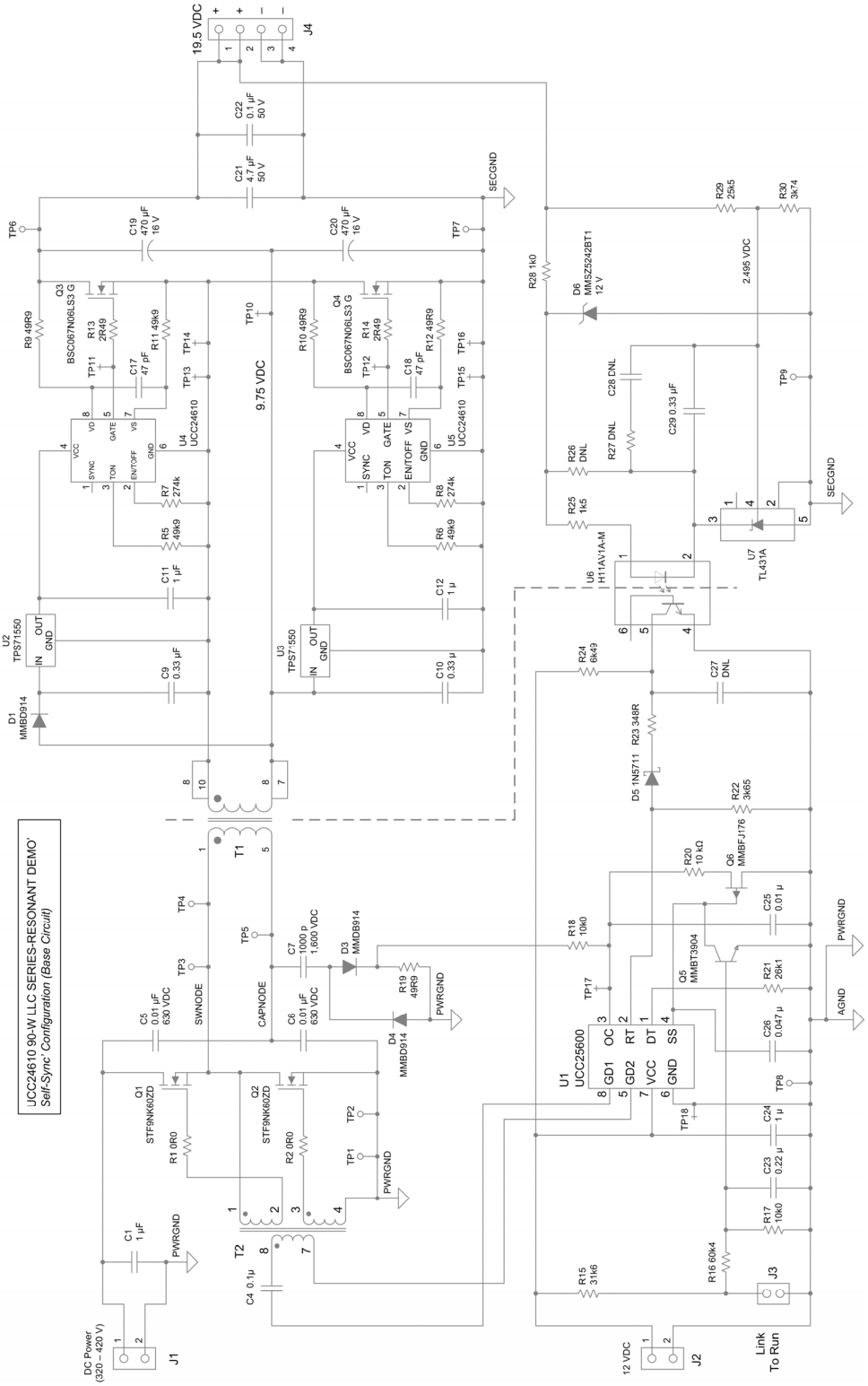

Figure 3 Schematic, UCC24610 LLC Series-Resonant Converter – Self Synchronization Configuration

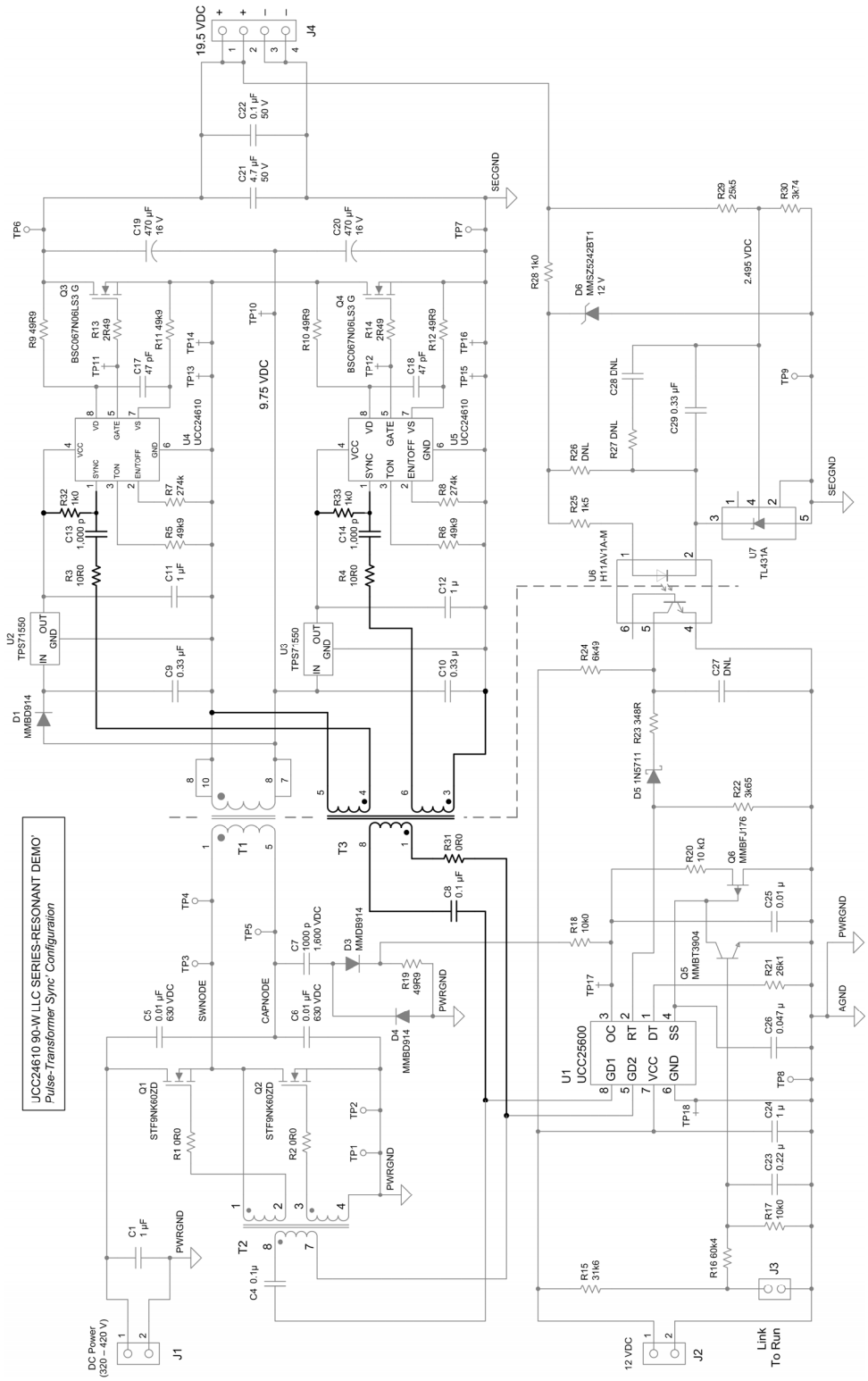

Figure 4 Schematic, UCC24610 LLC Series-Resonant Converter – Transformer Configuration

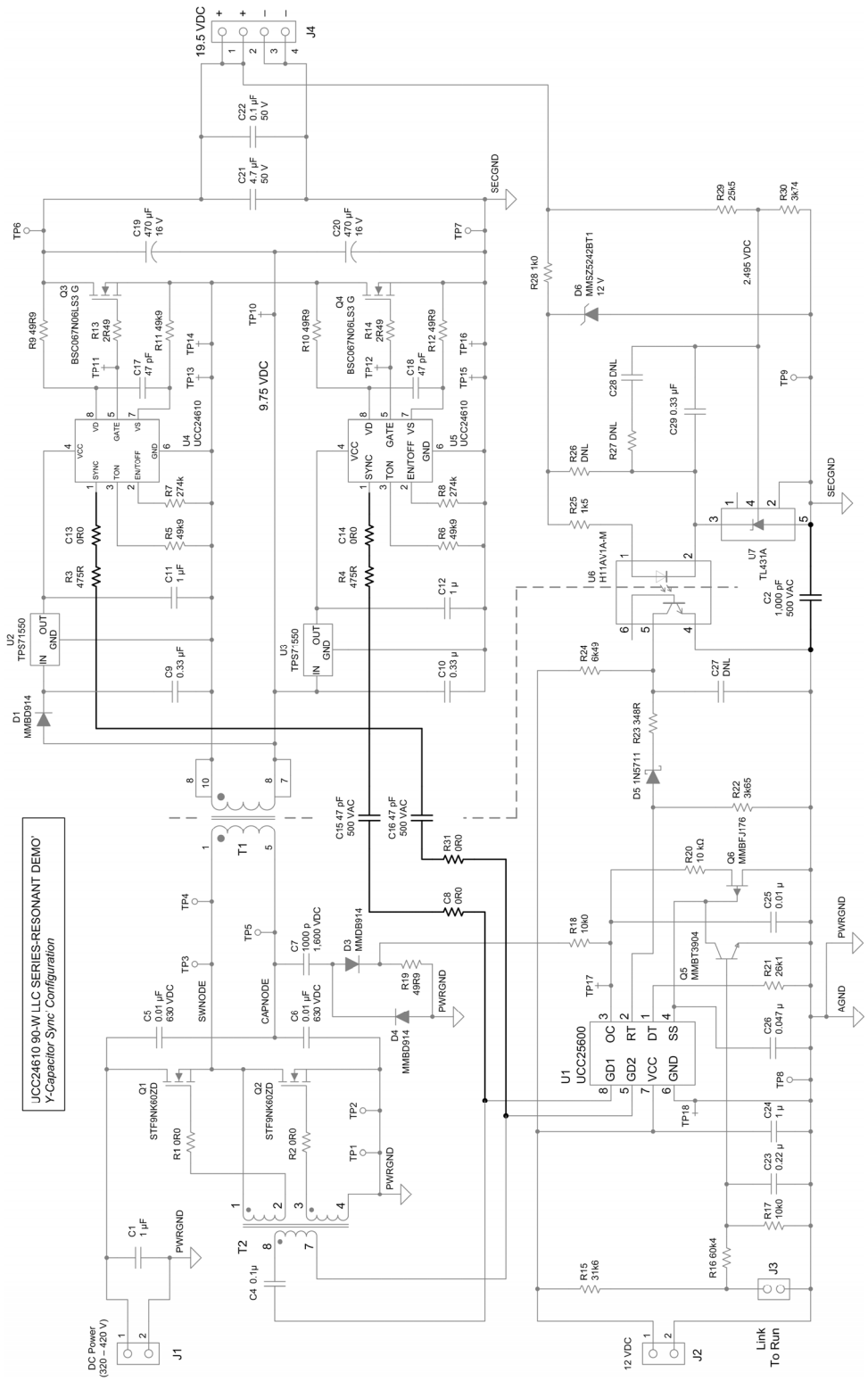

Figure 5 Schematic, UCC24610 LLC Series-Resonant Converter – Capacitor Configuration

6 LIST OF MATERIALS

The component list for the three build configurations described herein is defined by combining the contents of up to two of the three tables in this section. Table 2 lists the components for the "self-synchronization" configuration. The self-synchronization configuration has the minimum component count and is common to all three configurations. For this reason it is defined as the *base circuit* for the "Transformer Synchronization" and "Capacitor Synchronization" configurations. The following summary identifies the material list for each configuration.

1. Self-Synchronization: Use only Table 2
2. Transformer Synchronization: Combine Table 2 with the changes outlined in Table 3.
3. Capacitor Synchronization: Combine Table 2 with the changes outlined in Table 4.

Table 2 Components for Self-Synchronization Configuration (Base Circuit)

Ref.	Value	Tol.	Description	Part Number	Manufacturer
C1	1.0 µF	10%	Capacitor, Film (PP), 630 V	B32674D6105K	EPCOS
C2	N/A		Not Fitted		
C4	0.1 µF	10%	Capacitor, MLC, 0805, 25 V	Generic	Multi-Sourced
C5	0.01 µF	5%	Capacitor, Film (PP), 630 V	B32621A6103J	EPCOS
C6	0.01 µF	5%	Capacitor, Film (PP), 630 V	B32621A6103J	EPCOS
C7	0.001 µF	10%	Capacitor, Film, (PP), 1600 V	MKP10 1000/1600/10	WIMA
C8	N/A		Not Fitted		
C9	0.33 µF	20%	Capacitor, MLC, 0805, 50 V	Generic	Multi-Sourced
C10	0.33 µF	20%	Capacitor, MLC, 0805, 50 V	Generic	Multi-Sourced
C11	1 µF	10%	Capacitor, MLC, 0805, 16 V	Generic	Multi-Sourced
C12	1 µF	10%	Capacitor, MLC, 0805, 16 V	Generic	Multi-Sourced
C13	N/A		Not Fitted		
C14	N/A		Not Fitted		
C15	N/A		Not Fitted		
C16	N/A		Not Fitted		
C17	47 pF	5%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C18	47 pF	5%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C19	470 µF	20%	Capacitor, Electrolytic, 16 V	ORZ471M1CSA-10127S	Surge Components Inc.
C20	470 µF	20%	Capacitor, Electrolytic, 16 V	ORZ471M1CSA-10127S	Surge Components Inc.
C21	4.7 µF	20%	Capacitor, MLC, 1210, 50 V	Generic	Multi-Sourced
C22	0.1 µF	20%	Capacitor, MLC, 1206, 50 V	Generic	Multi-Sourced
C23	0.22 µF	10%	Capacitor, MLC, 0603, 10 V	Generic	Multi-Sourced
C24	1 µF	10%	Capacitor, MLC, 0805, 16 V	Generic	Multi-Sourced
C25	0.01 µF	10%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C26	0.047 µF	10%	Capacitor, MLC, 0603, 25 V	Generic	Multi-Sourced
C27	N/A		Not Fitted		
C28	N/A		Not Fitted		
C29	0.33 µF	5%	Capacitor, MLC, 0805, 50 V	Generic	Multi-Sourced

Ref.	Value	Tol.	Description	Part Number	Manufacturer
D1			Diode, Switching, 100 V, 200 mA	MMBD914	Multi-Sourced
D3			Diode, Switching, 100 V, 200 mA	MMBD914	Multi-Sourced
D4			Diode, Switching, 100 V, 200 mA	MMBD914	Multi-Sourced
D5			Diode, Schottky, 70 V, 15 mA	1N5711	ST Microelectronics
D6			Diode, Zener, 0.5-W, 12 V	MMSZ5242BT1	ON Semiconductor
J1			Term Block, Eurostyle, 3-Way	39390-0103	Molex
J2			Terminal Block, 2-Way	ED120/2DS	On-Shore Technology
J3			Header, 0.025 Sq., 2-Way	68001-203HLF	FCI BergStik
J4			Terminal Block, 4-Way	ED120/4DS	On Shore Technology
Q1			N-MOSFET, TO-220, 600 V, 7 A	STF9NK60ZD	ST Microelectronics
Q2			N-MOSFET, TO-220, 600 V, 7 A	STF9NK60ZD	ST Microelectronics
Q3			N-MOSFET, LF-PACK, 60 V, 50 A	BSC067N06LS3 G	Infineon
Q4			N-MOSFET, LF-PACK, 60 V, 50 A	BSC067N06LS3 G	Infineon
Q5			TRANSISTOR, NPN, 40 V, 200 mA	MMBT3904	Multi-Sourced
Q6			JFET, P-CHL, 30 V, 50 mA	MMBFJ176	Fairchild
R1	15R0	1%	Resistor, SMD, 0805	Generic	Multi-Sourced
R2	15R0	1%	Resistor, SMD, 0805	Generic	Multi-Sourced
R3	N/A		Not Fitted		
R4	N/A		Not Fitted		
R5	49k9	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R6	49k9	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R7	274k	1%	Resistor, SMD, 0603	RK73H1JTTD2743F	KOA
R8	274k	1%	Resistor, SMD, 0603	RK73H1JTTD2743F	KOA
R9	49R9	1%	Resistor, SMD, 0805	RK73H2ATTD49R9F	KOA
R10	49R9	1%	Resistor, SMD, 0805	RK73H2ATTD49R9F	KOA
R11	49R9	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R12	49R9	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R13	2R49	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R14	2R49	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R15	31k6	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R16	60k4	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R17	10k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R18	10k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R19	49R9	1%	Resistor, SMD, 0805	RK73H2ATTD49R9F	KOA
R20	10k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R21	26k1	1%	Resistor, SMD, 0603	RK73H1JTTD2612F	
R22	3k65	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R23	348R	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R24	6k49	1%	Resistor, SMD, 0603	Generic	Multi-Sourced

Ref.	Value	Tol.	Description	Part Number	Manufacturer
R25	1k5	1%	Resistor, SMD, 0805	Generic	Multi-Sourced
R26	DNL	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R27	N/A		Not Fitted		
R28	1k	1%	Resistor, T/H, 0.25 W	271-1K/AP-RC	Xicon
R29	25k5	1%	Resistor, SMD, 0805	Generic	Multi-Sourced
R30	3k74	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R31	N/A		Not Fitted		
R32	N/A		Not Fitted		
R33	N/A		Not Fitted		
T1			LLC Power Transformer	YS01361903	Taiwan Transmore Elect.
T2			Transformer, Gate Drive, 1:1:1	HA3858-AL	Coilcraft
T3	N/A		Not Fitted		
TP1			Test Point, Loop w/ Insulator	5012	Keystone
TP2			Test Point, Loop w/ Insulator	5012	Keystone
TP3			Test Point, Loop w/ Insulator	5012	Keystone
TP4			Test Point, Loop w/ Insulator	5012	Keystone
TP5			Test Point, Loop w/ Insulator	5012	Keystone
TP6			Test Point, Loop w/ Insulator	5012	Keystone
TP7			Test Point, Loop w/ Insulator	5012	Keystone
TP8			Test Point, Loop w/ Insulator	5012	Keystone
TP9			Test Point, Loop w/ Insulator	5012	Keystone
U1			Resonant-Mode Controller	UCC25600D	Texas Instruments
U2			Linear Regulator	TPS71550DCKR	Texas Instruments
U3			Linear Regulator	TPS71550DCKR	Texas Instruments
U4			SR Controller	UCC24610D	Texas Instruments
U5			SR Controller	UCC24610D	Texas Instruments
U6			Opto-Coupler	H11AV1A-M	Fairchild
U7		1%	Shunt Regulator, 2.495 V	TL431AIDBV	Texas Instruments
Q1, Q2			Heat Sink, Low-Profile, TO-220	274-1AB	Wakefield
Q1, Q2			Screw, Panhead, #4-40 x 3/8	#4-40 x 3/8	Fastener Supply
Q1, Q2			Nut, Stainless Steel, #4-40	#4-40	Fastener Supply

Table 3 Component Changes for Transformer Synchronization Configuration

Ref.	Value	Tol.	Description	Part Number	Manufacturer
C2	N/A		Not Fitted		
C8	0.1 µF	10%	Capacitor, MLC, 0805, 25 V	Generic	Multi-Sourced
C13	1000 pF	10%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C14	1000 pF	10%	Capacitor, MLC, 0603, 50 V	Generic	Multi-Sourced
C15	N/A		Not Fitted		
C16	N/A		Not Fitted		
R3	10R0	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R4	10R0	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R31	0R0		Link, SMD, 0805	Generic	Multi-Sourced
R32	1k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R33	1k	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
T3			Pulse Transformer (2:1:1), SMD	PA2008NL	Pulse

Table 4 Component Changes for Capacitor Synchronization Configuration

Ref.	Value	Tol.	Description	Part Number	Manufacturer
C2	1,000 pF	20%	Capacitor, Ceramic T/H, 500 VAC	VY1102M35Y5UQ63V0	Vishay-BCcomponents
C8	0R0		Link, SMD, 0805	Generic	Multi-Sourced
C13	0R0		Link, SMD, 0603	Generic	Multi-Sourced
C14	0R0		Link, SMD, 0603	Generic	Multi-Sourced
C15	47 pF	10%	Capacitor, Ceramic T/H, 500 VAC	VY1470K31Y5SQ63V0	Vishay-BCcomponents
C16	47 pF	10%	Capacitor, Ceramic T/H, 500 VAC	VY1470K31Y5SQ63V0	Vishay-BCcomponents
R3	475R	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R4	475R	1%	Resistor, SMD, 0603	Generic	Multi-Sourced
R31	0R0		Link, SMD, 0805	Generic	Multi-Sourced
R32	N/A		Not Fitted		
R33	N/A		Not Fitted		
T3	N/A		Not Fitted		

7 PCB DESIGN

7.1 General

Figure 6 and Figure 7 show the component placement and copper routing of the printed circuit board (PCB) used to test and characterize this design. The PCB design is based on a double-sided 2-oz. copper-foil layout. A double-sided PCB provides the flexibility to optimize the layout of the SR FETs and control circuitry. A combination of both through-hole (T/H) and surface mount devices (SMD) were placed on the top side, and SMD parts on the foil side.

7.2 Grounding

High-frequency transient current associated with switched-power converters induce differential noise voltages in the ground system. Any voltage differential in the ground can cause spurious operation of the control circuits. The design dedicates large areas of copper to power ground (PWRGND) and analog ground (AGND). PWRGND provides the return path for the power circuitry on the primary side of the converter. AGND is used by the control circuits as the primary-side zero-volt reference. To prevent the AGND from being used as current path by high-frequency power signals, AGND is referenced to PWRGND at just one location. This single-point grounding technique forces the high-frequency ground currents generated by the power circuitry to be directed around (as opposed to through) the quiet ground area of the sensitive control circuits.

It is important to keep the ground connections contiguous. Ground connections should take priority over the routing of other signals. Where necessary, use vias and T/H components to pass signals to other areas of the board. These techniques minimize the impedance to high-frequency ground currents to ensure low-noise and reliable operation.

7.3 Creepage and Clearance

Both the component placement and spacing between the copper areas or the PCB were designed to comply with the creepage and clearance requirements defined in the UL 60950 safety standard. The board was designed to meet the requirements for functional isolation for the high-voltage nodes on the primary (ac-line) side of the power supply, and reinforced isolation between all primary and secondary circuits. To comply with the UL standard 4 mm of separation was used for the primary-side high-voltage traces, and 8 mm between all primary and secondary side traces. The default trace separation for low-voltage nodes, as used for control circuits, was 0.3 mm.

7.4 Thermal Considerations

Although this circuit and topology operates with high efficiency, some components on the PCB assembly dissipate a moderate amount of heat. This may require thermal management initiatives to be implemented when the converter operates in an enclosure. A thermally conductive path to the surfaces of the enclosure may be required for these components. Table 5 provides a list of the components that have significant heat dissipation.

Table 5 Parts with High Thermal Dissipation

Reference Designator	Description	Dissipation (1)/
Q3, Q4	Secondary SR FETs	1 W
T1	LLC converter transformer	3 W

(1) Estimated dissipation at maximum load and 390 V input voltage.

7.5 Board Layout

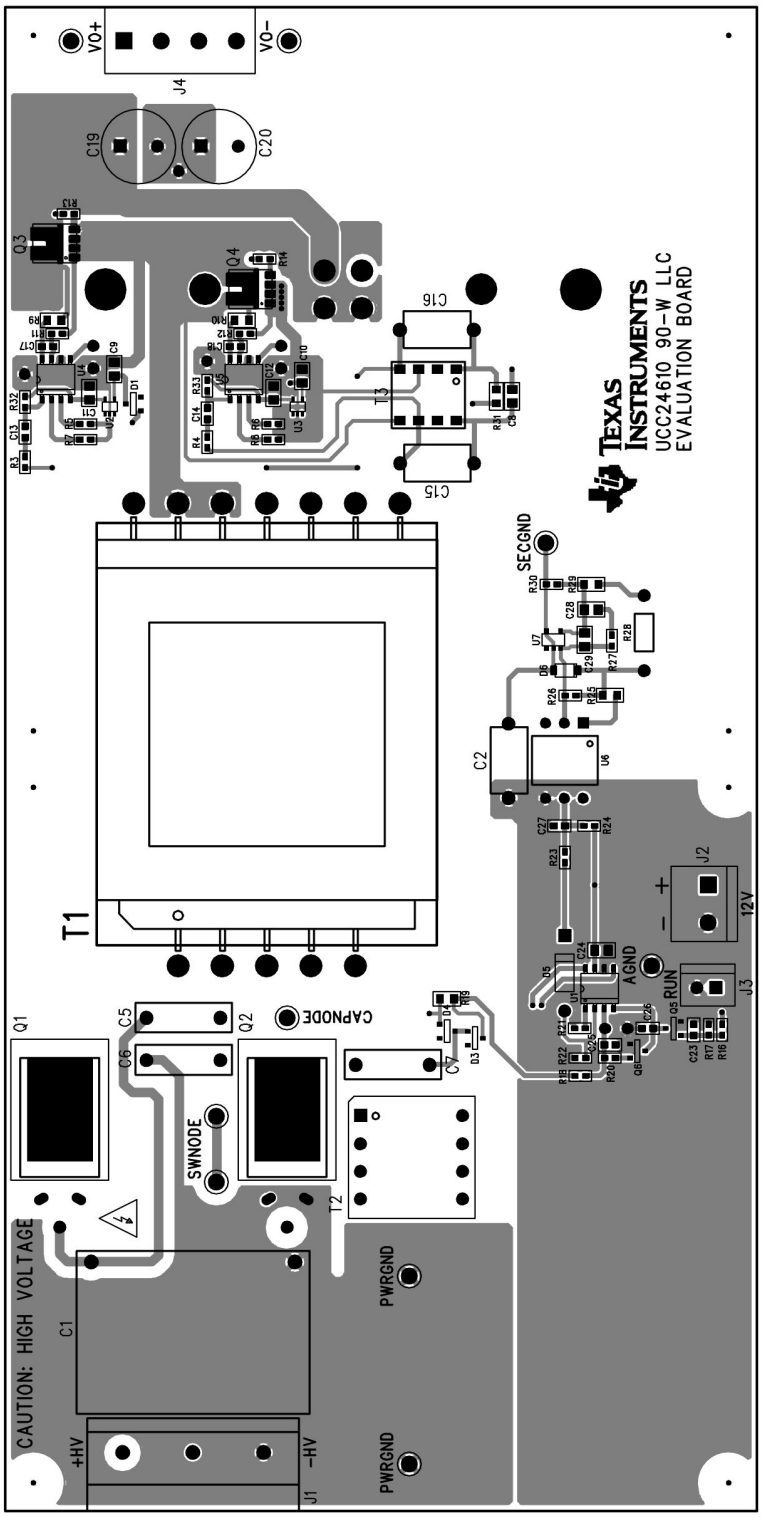

Figure 6 PCB Layout; Component-Side View

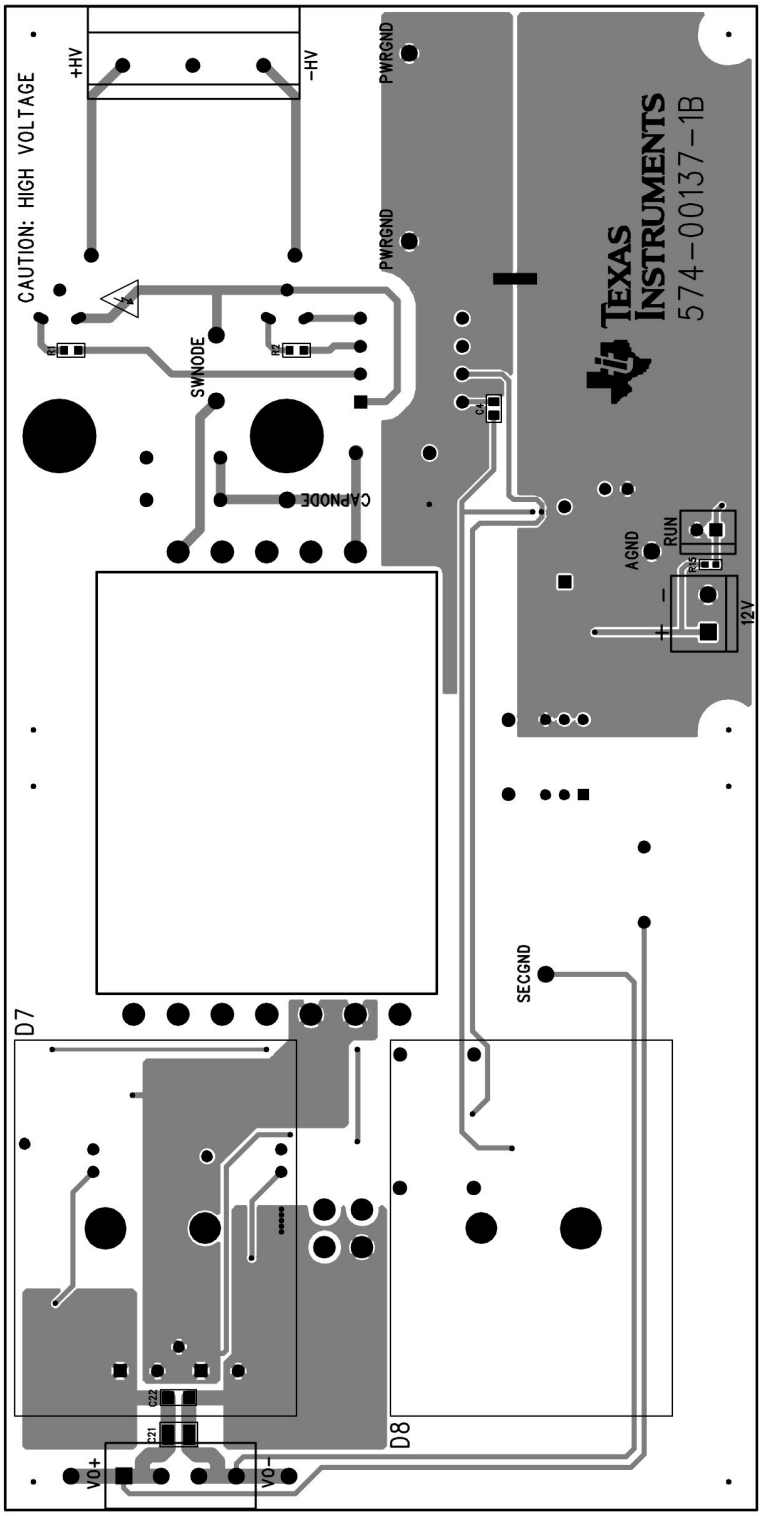

Figure 7 PCB Layout; Foil-Side View

7.6 Power Inputs

7.6.1 HVDC Input

The power input to the circuit requires a high-voltage DC source, capable of supplying up to 420 VDC at 0.5 A max. This can be provided by a high-voltage adjustable bench supply, the output from a boost PFC circuit, or the rectified output from a 0–280 V, 1-kVA rated power rheostat. Ensure that the source is either current limited or is fitted with a fuse with a rating of no more than 1 A.

The HVDC power can be safely applied without the bias supply being present.

7.6.2 Bias Supply

A bias supply of 12–16 VDC at 50 mA is required to operate the converter. The bias power is applied to the J2 terminal block and can be supplied from a small adjustable bench supply or 12-V lamp battery. The current consumption is typically 20 mA when the converter is operating. The polarity is correct when the negative connection is closest to the J3 connector.

7.7 J3 Header

The PCB design includes a 0.1-in spaced pin header, J3. This header provides on/off control of the converter when both HVDC input and bias power is applied. This interface can be used to hold down the SS pin (pin 4) until there is sufficient output voltage for the converter to produce a regulated output. The converter runs only when the open-circuit voltage at pin 1 of J3 is pulled to GND (J3/Pin 2) using either a jumper or NPN bipolar transistor.

Place a standard 2-pin shorting jumper at J3 to enable the converter to run and produce a DC output. When the converter is enabled the UCC25600 resonant controller initiates a soft start. Removal of the J3 jumper promptly shuts down the converter.

The application and removal of the bias supply has the same effect as the removal and replacement of the shorting jumper at J3.

7.8 Monitoring Primary Current

By making a small modification to the PCB the primary current can be monitored using a current probe. This is also the current flowing between the series-resonant components, L_R and C_R.

The PCB layout in Figure 6 shows two test points labeled “SWNODE” located close to and just above the primary switch, Q2. They are identified TP3 and TP4 on the schematic. The 0.05-in trace connecting these two test points carries the transformer primary current. This trace can easily be cut, and replaced with a loop of wire connecting TP3 and TP4. The primary current can then be measured using a clip-on current probe.

8 PERFORMANCE VERSUS SCHOTTKY RECTIFIERS

Figure 8 through Figure 13 compares the typical performance of the 90-W LLC series-resonant converter, when operating with the UCC24610 synchronous rectifier controller versus regular Schottky rectifiers. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

8.1 Typical Operating Efficiency

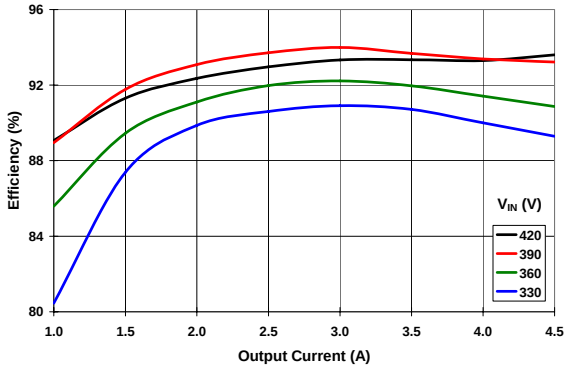

Figure 8 Operating Efficiency with UCC24610 Rectifier Controllers and FETs

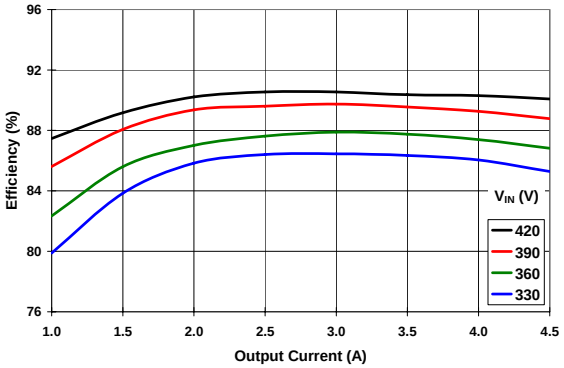

Figure 9 Operating Efficiency with MBR1645 Schottky Rectifiers

8.2 Typical Power Dissipation

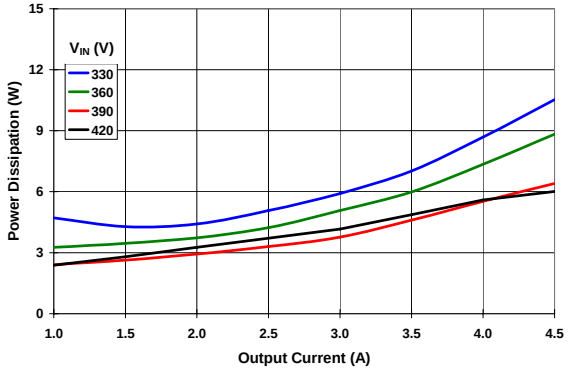

Figure 10 Power Dissipation with UCC24610 Rectifier Controllers and FETs (1)

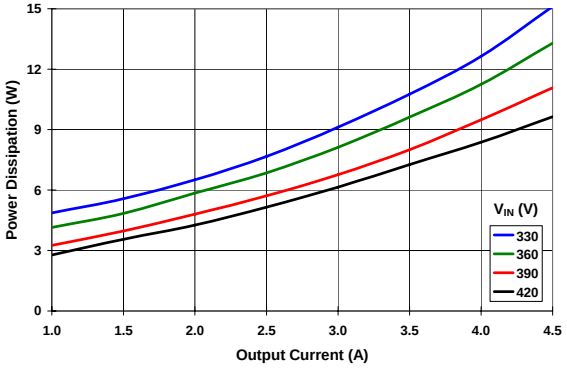

Figure 11 Power Dissipation with MBR1645 Schottky Rectifiers (1)

(1) When operating at 390-V input and at 3-A load, the converter dissipates 3.75 W using the UCC24610 rectifier controllers and FETs, compared to 6.75 W using regular Schottky rectifiers.

8.3 Typical Output AC Ripple Voltage

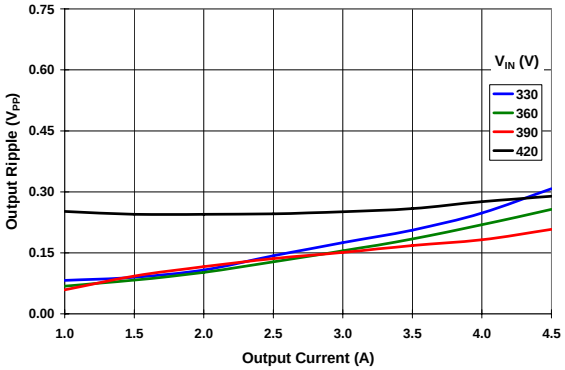

Figure 12 Output AC-Ripple with UCC24610 Rectifier Controllers and FETs (2)

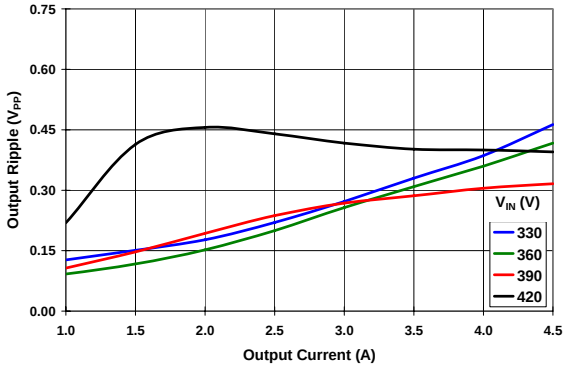

Figure 13 Output AC-Ripple with MBR1645 Schottky Rectifiers (2), (3)

(2) Peak-to-peak output ripple derived from V_{OUT} rms measurement using an oscilloscope with 20-MHz bandwidth limit.

(3) The Schottky diode rectifiers show a higher magnitude of ac rippled at high input voltage (420 V). This is due to an increase in high-frequency ringing from these devices at this input voltage.

9 CIRCUIT WAVEFORMS

The oscilloscope waveforms in this section, captured in Figure 14 through Figure 29, can be identified using the same color for source identification. The color key to the signals is provided in Table 6.

Table 6 Color Key for Oscilloscope Waveforms

Trace Color	Signal Description
Black	Main transformer secondary winding output voltage
Blue	Main transformer primary current
Green	Upper SR GATE signal waveform (U4/pin 5)
Brown	Upper SR SYNC signal waveform (U4/pin 1)
Red	Lower SR GATE signal waveform (U5/pin 5)
Orange	Lower SR SYNC signal waveform (U5/pin 1)

9.1 SR Synchronization with Pulse Transformer

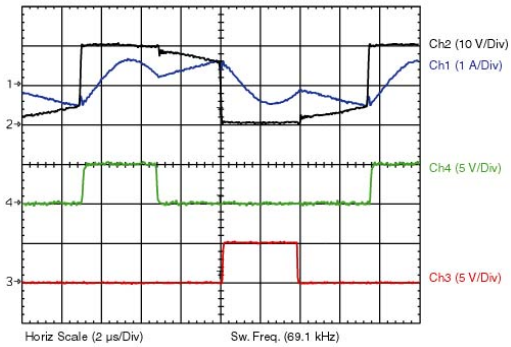

Figure 14 Upper and Lower SR Gate Signals at 320-VDC and 1-A Load ($f_{SW} < f_R$)

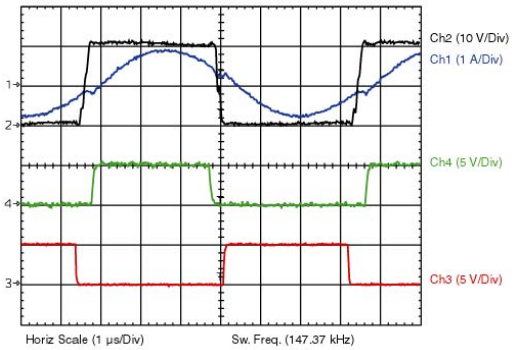

Figure 15 Upper and Lower Gate Signals at 400-VDC Input and 4.6-A Load ($f_{SW} \approx f_R$)

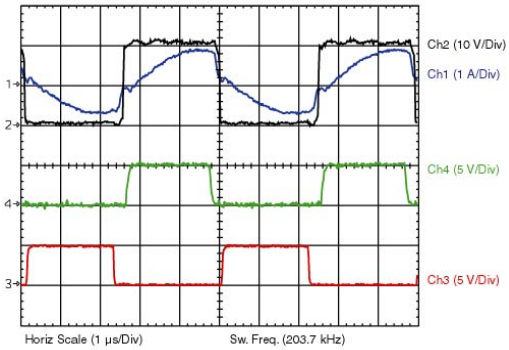

Figure 16 Upper and Lower SR Gate Signals at 420-VDC Input and 4.6-A Load ($f_{SW} > f_R$)

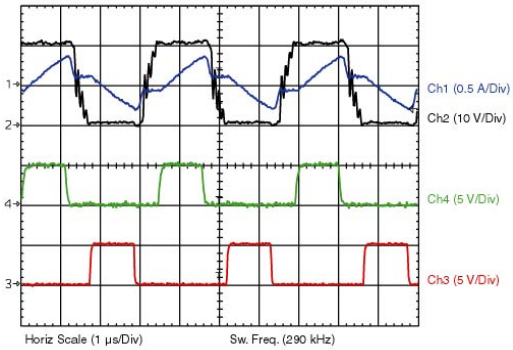

Figure 17 Upper and Lower SR Gate Signals at 420-VDC Input and 1-A Load ($f_{SW} > f_R$)

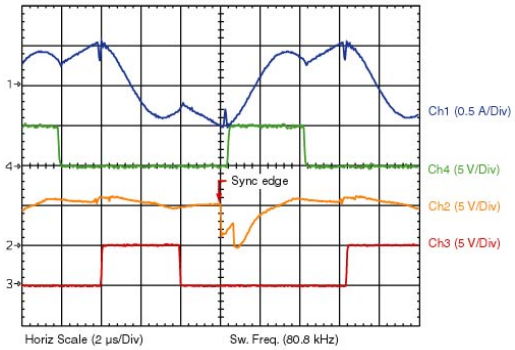

Figure 18 Upper/Lower SR Gate and Lower SYNC Signals at 340-VDC Input and 1-A Load (1)/

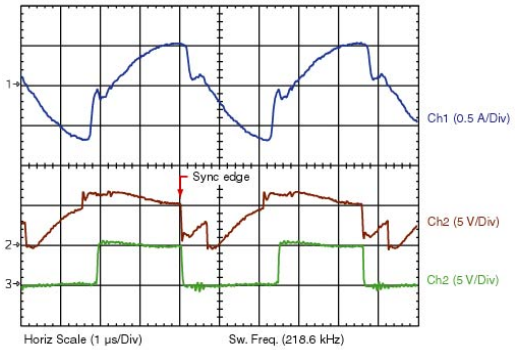

Figure 19 Upper SR Gate and SYNC Signals at 420-VDC and 3-A Load (2)/

(1) Below resonance the lower SR controller has set the gate signal (Red) low before the negative SYNC pulse (Orange).

(2) Above resonance the upper SR controller sets the gate signal (Green) low about the same time as the SYNC pulse (Brown). This forces the gate output low irrespective of whether the UCC24610 controller has sensed the FET is no longer conducting.

9.2 SR Synchronization with Capacitors

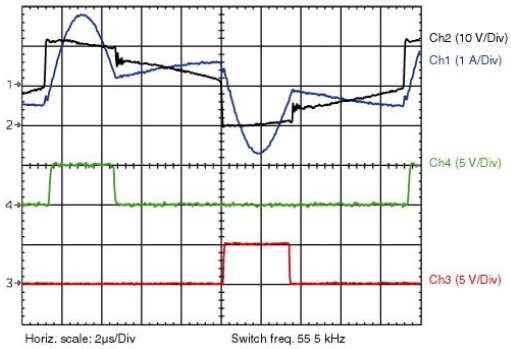

Figure 20 Upper and Lower SR Gate Signals at 320-VDC Input and 4.6-A Load ($f_{SW} < f_R$)

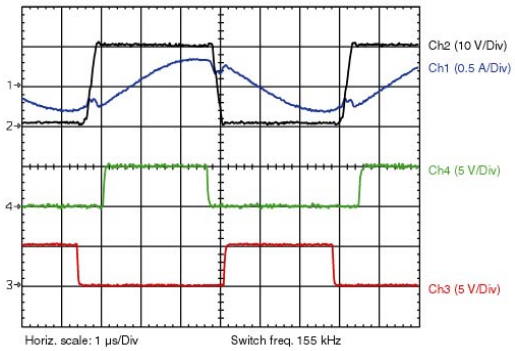

Figure 21 Upper and Lower Gate Signals at 390-VDC Input and 1-A Load ($f_{SW} \approx f_R$)

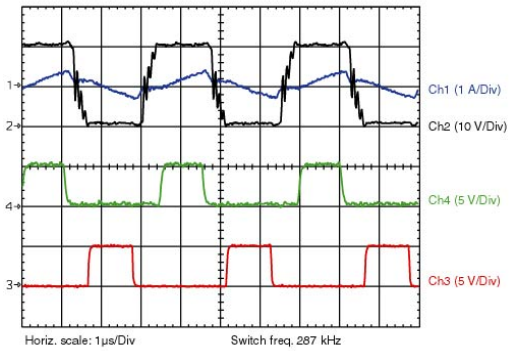

Figure 22 Upper and Lower SR Gate Signals at 420-VDC and 1-A Load ($f_{SW} > f_R$)

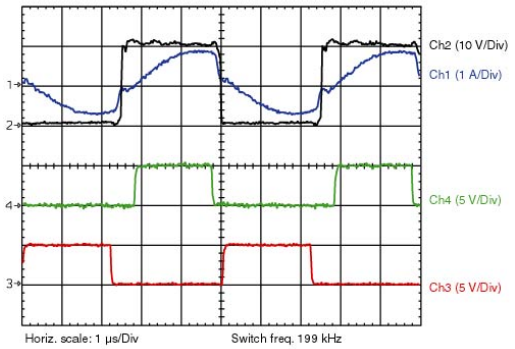

Figure 23 Upper and Lower SR Gate Signals at 420-VDC Input and 4.6-A Load ($f_{SW} > f_R$)

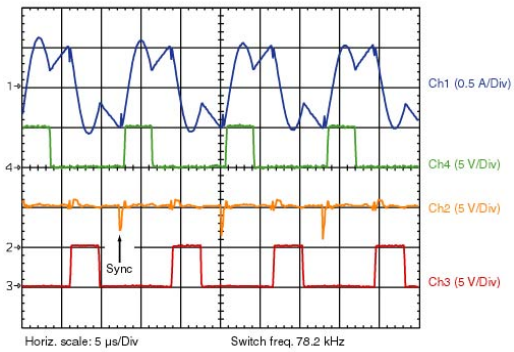

Figure 24 Upper/Lower SR Gate and Lower SYNC Signals at 340-VDC Input and 1-A Load (3)

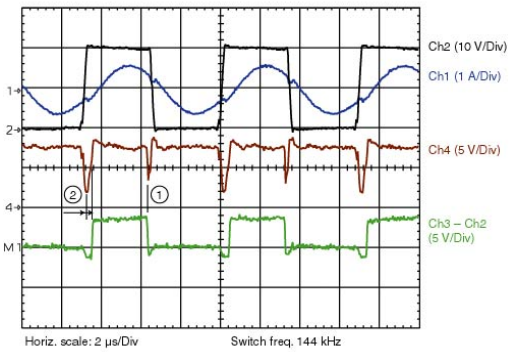

Figure 25 Upper SR Gate and SYNC Signals at 393-VDC Input and 3-A Load (4) ($f_{SW} \approx f_R$)

(3) The SYNC signal negative pulse for the lower SR circuit is generated by the high-to-low transition of the gate signal that drives the low-side MOSFET in the converter primary (U1/pin 8).

(4) Because the upper SR floats on the transformer secondary winding, it sees two negative pulses. The smaller, identified ①, is generated by the high-to-low transition of the gate signal that drives the high-side primary MOSFET (U1/pin 5). This is the edge that the controller should respond to. The larger, ②, is produced when the 0-V return of the circuit rises with the secondary winding voltage. The additional pulse delays (and thus shortens) the length of the gate signal from the upper controller by as much as 0.3 µs.

9.3 Self-Synchronization Configuration

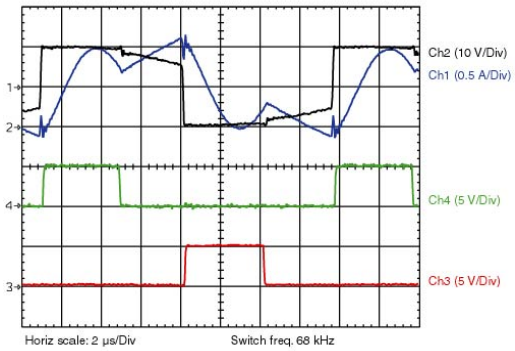

Figure 26 Upper and Lower SR Gate Signals at 320-VDC and 1-A Load

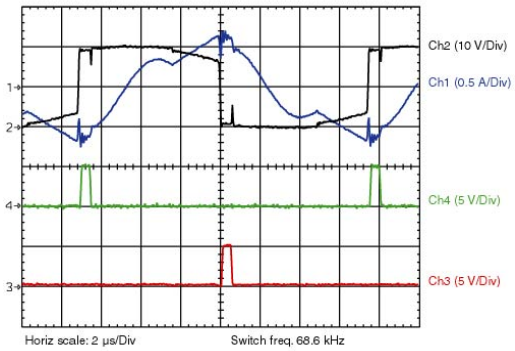

Figure 27 Upper and Lower SR Gate Signals at 340-VDC Input and 1-A Load (5)/

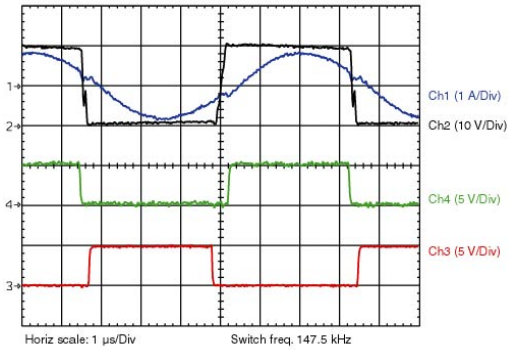

Figure 28 Upper and Lower SR Gate Signals at 400-VDC and 4.6-A Load

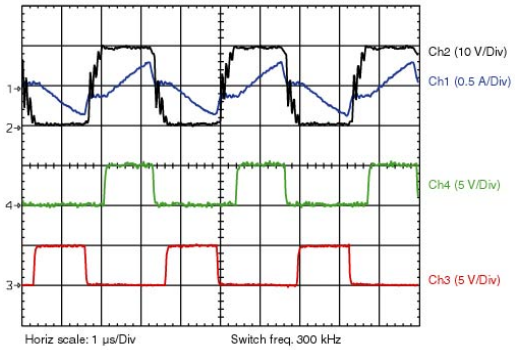

Figure 29 Upper and Lower SR Gate Signals at 420-VDC and 1-A Load

(5) Under the conditions of low input voltage and output load the drain-source voltage produced across the SR FETs does not always rise fast enough to keep each FET turned on. In this case the gate-drive outputs from both SR controllers (UCC24610) have turned off early, requiring the body diode of each FET to conduct for the rest of the cycle.

10 Performance Observations and Comments

The UCC24610 performs well in an LLC series-resonant converter application. This is especially when required to operate in a voltage-doubling rectifier configuration, which requires the upper SR circuit to float on the AC side of the transformer secondary winding.

The UC24610 is a single independent synchronous rectifier controller that includes features such as light-load management control. The threshold of this function is subject to both component tolerances and circuit variances. So when two devices are employed in either a center-tapped or voltage-doubling full-wave bridge rectifier they cannot make coordinated decisions. This was noted with all three circuit configurations; synchronization with a pulse transformer, capacitors, or without any synchronization (self-synchronization configuration).

There is always a risk of cross conduction when using two UCC24610 devices in a full-wave rectifier configuration. This risk is minimized, or even eliminated, when the devices are provided a synchronization signal. Synchronization prevents cross conduction by not only ensuring that an SR FET turns off at the end of its conduction period, but that it does not turn on at that point. The negative pulses at the UCC24610 SYNC pin occur just prior to the converter beginning its transition to the opposite half cycle. This has the effect of inhibiting the GATE output from each device at a point when it is subject to being turned on due to circuit noise generated during the phase transition.

Only when the SR circuits are operated *without* an external synchronization signal can cross conduction occur, and then only at low input voltages and load. The conduction overlap is extremely short (<10 ns) as reverse FET current is quickly detected by one of the SR controllers, which promptly turns off its gate drive. Series-resonant LLC converters also tend to be very robust as fault current is limited by the series-resonant inductance. Whenever cross-conduction occurred during testing of this design the over-current limit was promptly triggered. This allowed the converter to recover without any significant drop in the output voltage. The problem was eliminated by placing just 47 pF of capacitance across pins 7 and 8 of U4 and U5.

At zero loads the magnitude of current through the SR FETs can be sufficiently low that the SR controllers may periodically operate in either no-load mode or with the minimum t_{ON} gate period (0.5 µs). To maintain regulation the feedback control loop forces the converter frequency higher. The frequency is highest when the input voltage is also at a maximum (420 VDC). If the switch frequency rises above 350 kHz the UCC25600 can revert to burst-mode operation. This further helps keep the output voltage in regulation.

11 References

The following is a list of data sheets, evaluation guides, and papers that were used to design of the UCC24610 90-W LLC series-resonant converter.

[1] UCC24610 Data Sheet, Texas Instruments Ref. SLUSA87

[2] UCC25600 Data Sheet; Texas Instruments Ref. SLUS846

[3] TPS715xx Data Sheet, Texas Instruments Ref. SLVS338

[4] Bing Lu, Wenduo Liu,Yan Liang, Fred C. Lee, and Jacobus D. van Wyk, “Optimal Design Methodology for LLC Resonant Converter,” IEEE APEC 2006.

12 Additional Information

The PCB layout for this reference design was created using PADS version 9 CAD software by Mentor Graphics. PADS Logic was used for schematic capture, and PADS Layout was used to design the PCB. The Gerber file, silk screen, solder mask, and drill drawing files produced by PADS, including the program files that created them, are available to customers and designers. Enquiries should be made to the regional Texas Instruments Product Information Center (PIC), or a local TI sales representative. Use the prototype reference design number, PR2000, for this request.

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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		Wireless	www.ti.com/wireless-apps

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AN-6208

Secondary-Side Synchronous Rectifier (SR) for LLC Resonant Converter Using FAN6208

Introduction

The LLC resonant converter has drawn a lot of attention recently due to its advantages over a conventional series resonant converter and parallel resonant converter: narrow frequency variation over wide load, input variation, and Zero Voltage Switching (ZVS) for the entire load range.

In an LLC resonant converter, rectifier diodes are typically used to obtain DC output voltage from the transformer secondary winding. The conduction loss of diode rectifier contributes significantly to the overall power losses in an LLC resonant converter; especially in low output voltage applications. The conduction loss of a rectifier is proportional to the product of its forward-voltage drop and the forward conduction current. Using synchronous rectification (SR) where the rectifier diode is replaced by MOSFET with a small on resistance (R_{DSON}), the forward-voltage drop of a synchronous rectifier can be lower than that of a diode rectifier and, consequently, the rectifier conduction loss can be reduced.

FAN6208 is a synchronous rectification controller for isolated LLC or LC resonant converters that can drive two individual SR MOSFETs emulating the behavior of rectifier diodes. FAN6208 measures the SR conduction time of each switching cycle by monitoring the drain-to-source voltage of each SR and determines the optimal timing of SR gate drive. FAN6208 also uses the change of opto-coupler diode current to adaptively shrink the duration of SR gate drive signals during load transients to prevent shoot-through. To improve light-load efficiency, Green Mode disables the SR drive signals, minimizing gate drive power consumption at light-load conditions.

This application note describes the design procedure for a SR circuit using FAN6208. The guidelines for printed circuit board (PCB) layout and a design example with experiment results are also presented. Figure 1 shows the typical application circuit of FAN6208.

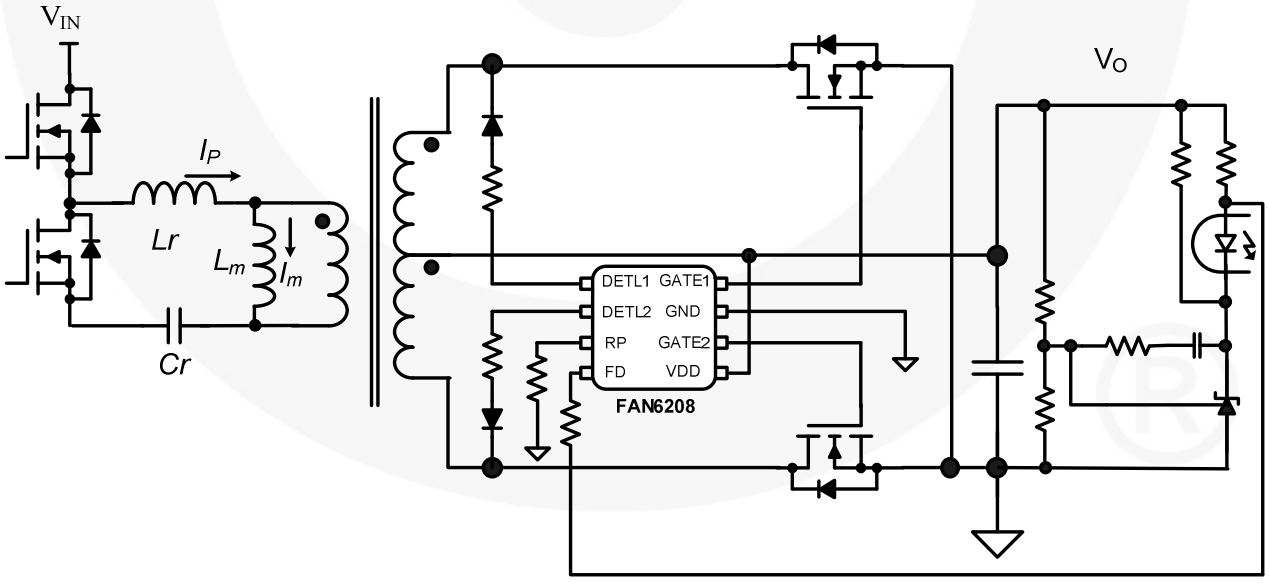

Figure 1. Typical Application

LLC Resonance Converter with SR

Figure 2 shows the simplified schematic of a half-bridge LLC resonant converter, where L_m is the magnetizing inductance that acts as a shunt inductor, L_r is the series resonant inductor, and C_r is the resonant capacitor. Since the magnetizing inductor is relatively small, a considerable amount of magnetizing current (I_m) exists, which freewheels in the primary side without being involved in the power transfer. The primary-side current (I_p) is sum of the magnetizing current and the secondary-side current referred to the primary.

Figure 3 shows the typical gain curve of the half-bridge LLC resonant converter. To allow Zero Voltage Switching (ZVS) for the primary-side switches, gain curves with inductive impedance characteristics should be used, where the gain decreases as frequency increases. The resonant network has a resonant frequency determined by the resonance between L_r and C_r. When the switching frequency is lower than the resonant frequency (below resonance), the half resonance of reflected secondary-side current (diode current) finishes before the primary-side switch is turned off, as shown in Figure 4. When the switching frequency is higher than the resonant frequency (above resonance) the primary-side switch is turned off before the half resonance of reflected secondary-side current (diode current) is completed, as shown in Figure 5.

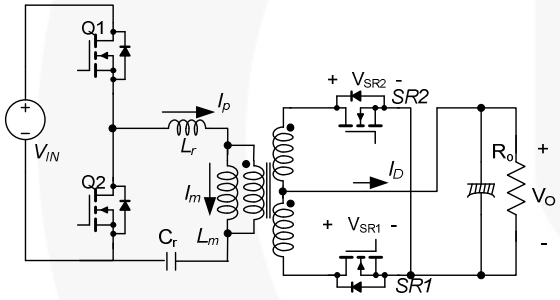

Figure 2. Schematic of LLC Resonant Converter with SR

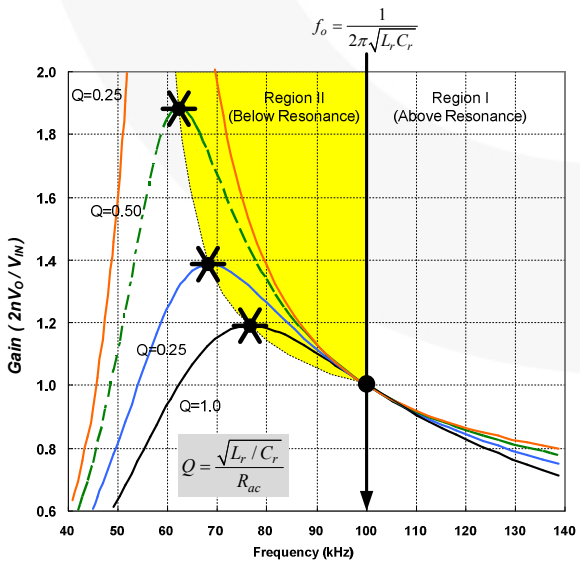

Figure 3. Typical Gain Curves of LLC Resonant Converter

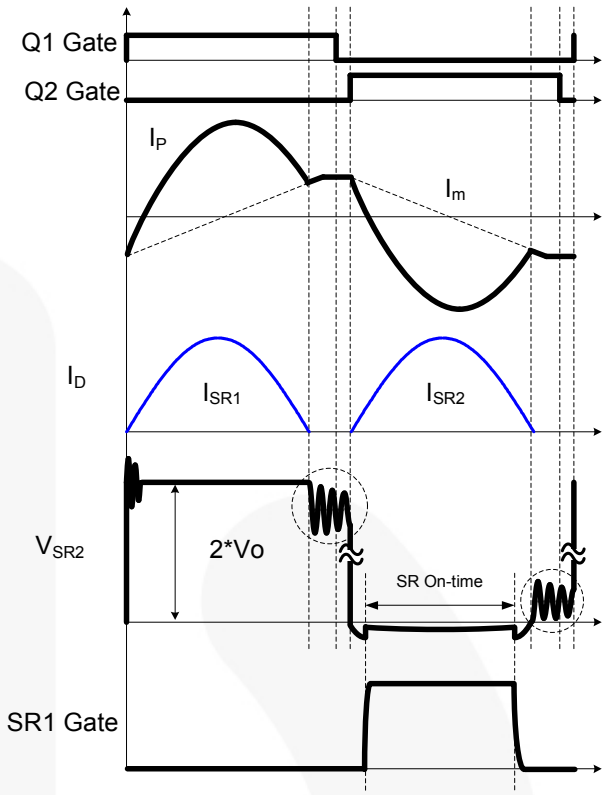

Figure 4. Key Waveforms Below -Resonance Operation

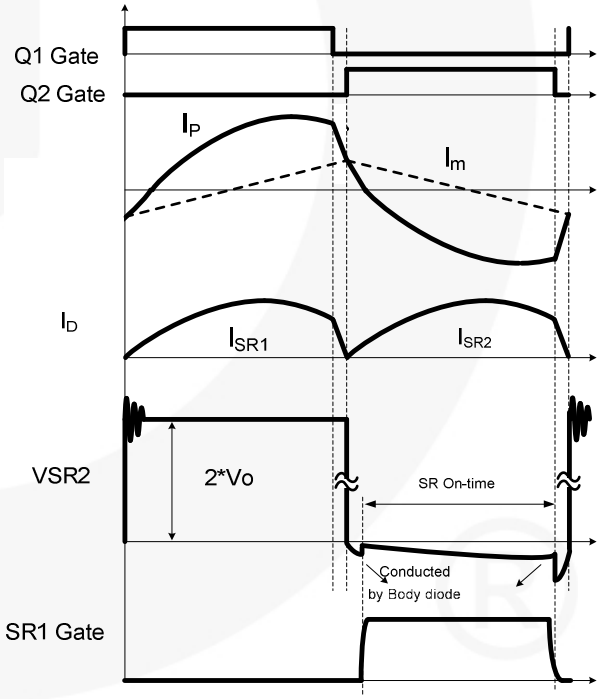

Figure 5. Key Waveforms of Above-Resonance Operation

Application Circuit

Figure 6 shows the typical application circuit of FAN6208 and Figure 7 shows the typical timing diagram of SR gate drive signal. FAN6208 senses the drain-to-source voltage of each SR to determine the gate drive timing. Once the body diode of SR begins conducting, the drain-to-source voltage drops to zero, which causes low detection (DETL) pin voltage to drop to zero. FAN6208 turns on the MOSFET after $t_{ON-ON-DETL}$ (about 350ns), when the voltage on DETL drops below 2V. As depicted in Figure 8, the turn -on delay (after $t_{SR-ON-DETL}$) is a sum of debounce time (150ns) and propagation delay (200ns).

FAN6208 measures the SR conduction duration (t_{DETL}), during which DETL voltage stays lower than 2V, and uses this information to determine the turn-off instant of SR gates of the next switching cycle, as shown in Figure 7. The turn-off instant is obtained by subtracting a dead time (t_{DEAD}) from the measured SR conduction duration of the previous switching cycle.

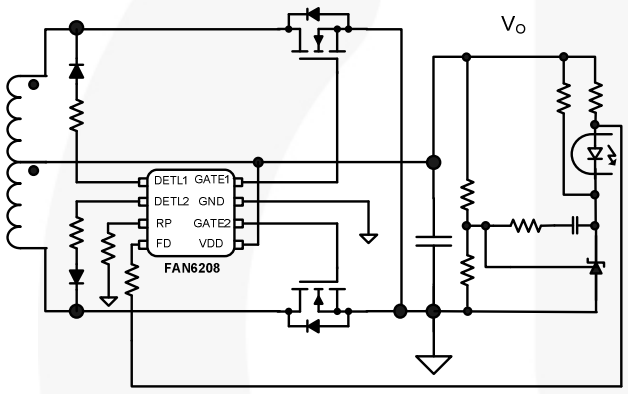

Figure 6. Application Circuit of FAN6208

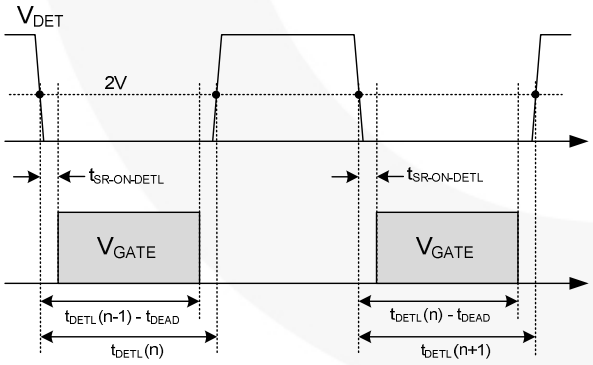

Figure 7. SR Conduction Time Determination

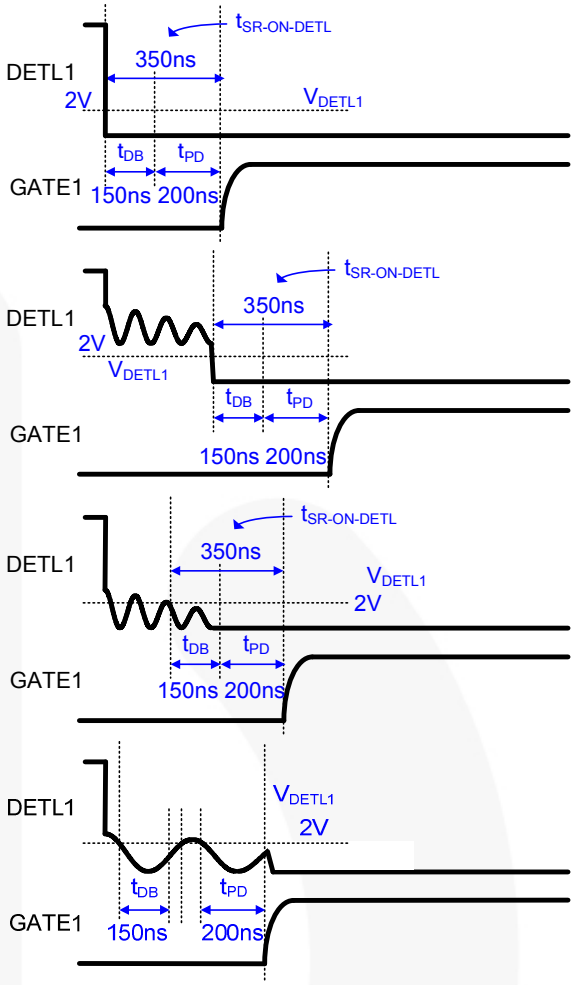

Figure 8. Timing Diagram for Turning On SR

DETL Pin Configuration

Allowable voltage on the DETL pin is from -0.3V to 7V. Since the maximum voltage of the SR drain-to-source voltage is twice that of the output voltage, a diode (D_{DETL}) is required for the DETL pin to prevent high voltage. Diode 1N4148 is typically used for D_{DETL}. Since the DETL internal current source is 50μA, R_{DETL} should be determined such that the DETL voltage is lower than the low detection threshold (2V) with enough margin when the SR conducts. Since the forward-voltage drop of SR can be as low as zero when SR current is small, the DETL resistor should be:

$$R_{DETL} < \frac{(2 - V_{FD})}{50\mu A} \quad (1)$$

where V_{FD} is the forward-voltage drop of DETL diode.

R_{DETL} larger than 20kΩ is not typically recommended for proper low-voltage detection on DETL pin.

R_{DETL} should be determined such that the DETL voltage is higher than -0.3V when the maximum voltage drop occurs across SR, such as:

$$R_{DETL} > \frac{I_{SR}^{max} R_{DS.ON} - V_{FD} - 0.3}{50\mu A} \quad (2)$$

where I_{SR}^{max} is the maximum current of SR and $R_{DS.ON}$ is the maximum on-resistance of the SR MOSFET at high temperature.

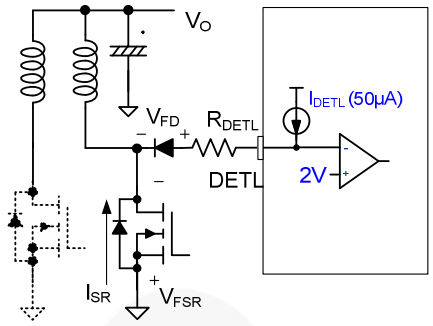

Figure 9. Application Circuit of DETL Pin

RP Pin Configuration

The dead time can be programmed using a resistor on the RP pin. The relationship between the dead time and SR conduction duration (t_{DETL}) for different resistor values on the RP pin are given in Figure 10 and Figure 11. Since the SR conduction time is shrunk by the protection function (gate-shrink function) when t_{DEAD} is smaller than 125ns, R_p should be properly selected such that the gate-shrink function does not operate at maximum switching frequency.

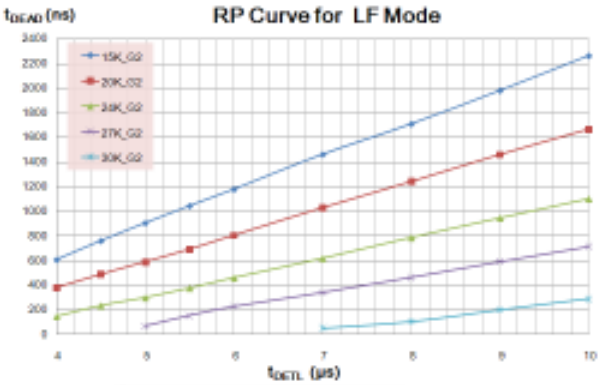

Figure 10. t_{DEAD} vs. t_{DETL} for Different R_P (Low Frequency)

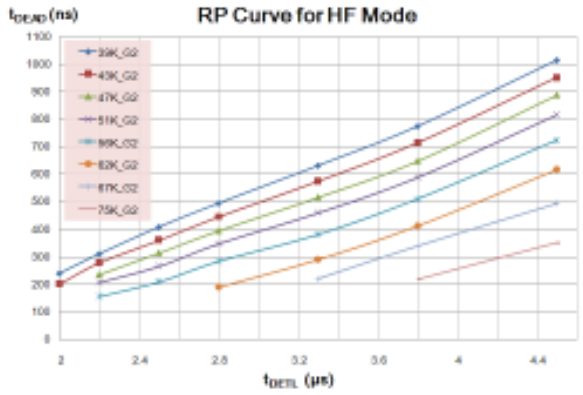

Figure 11. t_{DEAD} vs. t_{DETL} for Different R_P (High Frequency)

The RP pin has an internal constant current source (41.5μA) and the pin voltage is determined by the R_p resistor. Depending on the RP pin voltage, the Green Mode threshold of t_{DETL} is determined as shown in Figure 12. When R_{RP} is less than 36KΩ, FAN6208 operates in Low-Frequency Mode, where Green Mode is enabled when t_{DETL} is smaller than 3.75μs. When R_{RP} is larger than 36KΩ, High-Frequency Mode is selected and Green Mode is enabled for t_{DETL} smaller than 1.90μs.

The RP pin also has two internal thresholds for pin-open / short protection. Using RP pin short protection, remote on / off control can be implemented as shown in Figure 13.

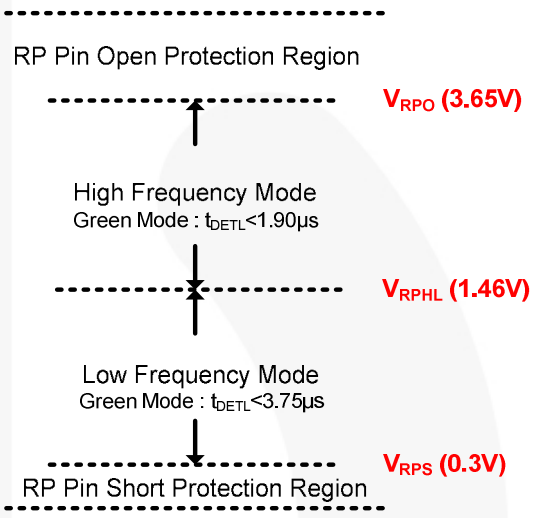

Figure 12. RP Pin Operation

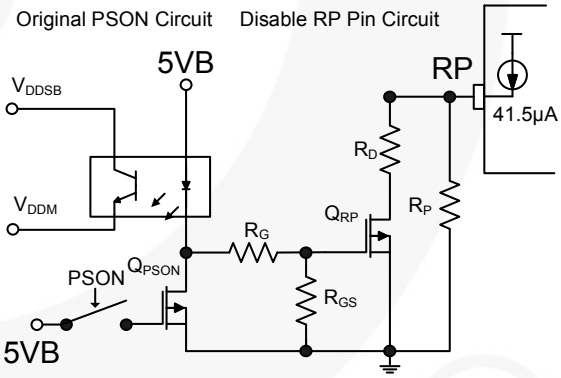

Figure 13. Application Circuit of RP Pin for Remote ON / OFF

Gate-Shrink Functions

In normal operation, the turn-off instant is determined by subtracting a dead time (t_{DEAD}) from the measured SR conduction duration of the previous switching cycle, as shown in Figure 7. This allows proper driving timing for the SR MOSFETS when the converter is in steady state and the switching frequency does not change much. However, this control method may cause shoot-through of SR MOSFETs when the switching frequency increases fast and switching

transition of the primary-side MOSFETs takes place before the turn-off command of the SR is given. To prevent the shoot-through problem, FAN6208 has gate-shrink functions. Gate shrink takes place in the following three conditions:

1. When an insufficient dead time is detected in the previous switching cycle. When the DETL becomes HIGH within 125ns of the detection window after SR gate is turned off, the SR gate drive signal in the next switching cycle is reduced by $t_{SHRINK-DT}$ (about 1.25µs) to increase the dead time as shown in Figure 14.

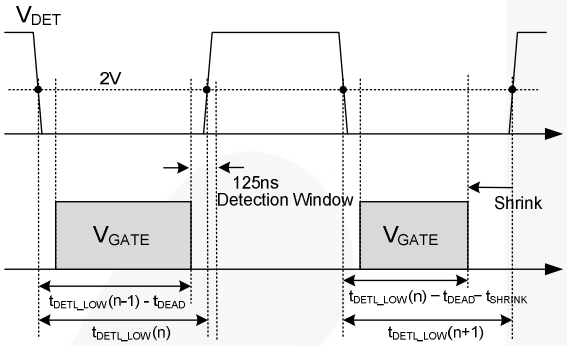

Figure 14. Gate Shrink by Insufficient Dead Time

2. When the feedback information changes fast. FAN6208 monitors the current through the opto-coupler diode by measuring the voltage across the resistor in series with opto-diode, as depicted in Figure 15. If the feedback current through the opto diode increases by more than 20% of the feedback current of the previous switching cycle, SR gate signal is shrunk by $t_{SHRINK-FD}$ (about 1.4µs) for $t_{D-SHRINK-FD}$ (about 90µs), shown in Figure 16.

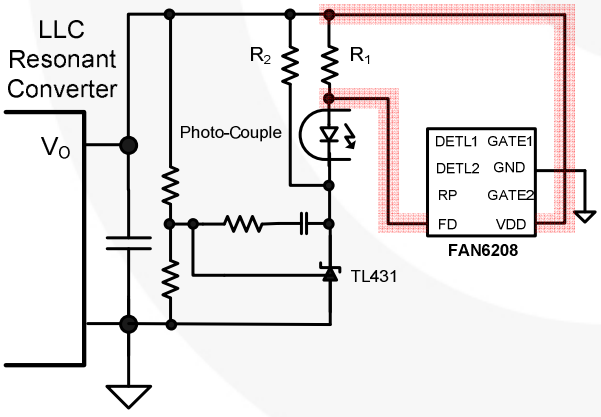

Figure 15. Application Circuit of FD Pin

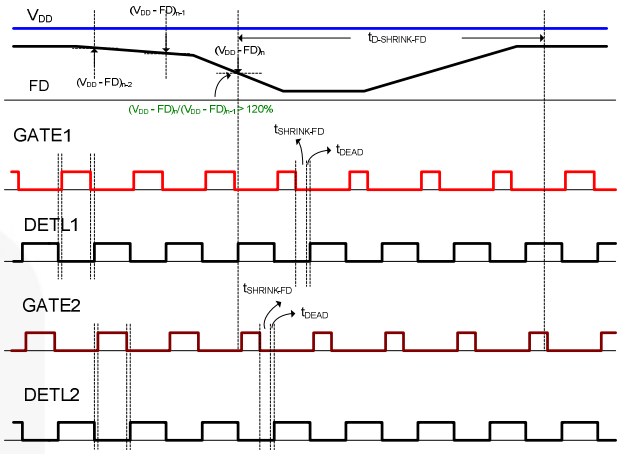

Figure 16. Gate Shrink by Feedback Detection

3. When the DETL voltage has ringing around zero. As depicted in Figure 17, the drain voltage of SR has ringing around zero at light-load condition after the switching transition of primary-side switches. When DETL voltage rises above 2V within 350ns after DETL voltage drops to zero and stays above 2V longer than 150ns, the gate is shrunk by 1.2µs ($t_{SHRINK-RNG}$), as shown in Figure 17.

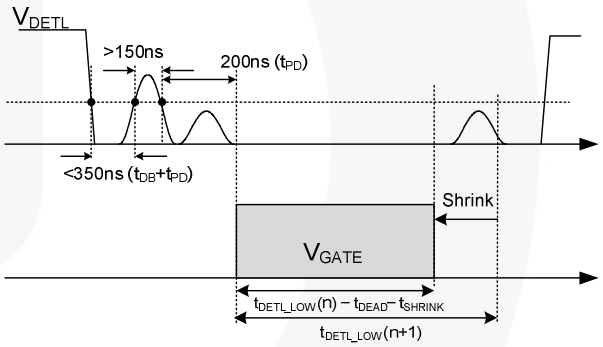

Figure 17. Gate Shrink by the DETL Voltage Ringing

Printed Circuit Board Layout

In Figure 18, the power traces are marked as bold lines. Good PCB layout improves power system efficiency and reliability and minimizes EMI.

Guidelines

- For feedback detection, the FD pin should be connected to the anode of the opto diode. Connecting the FD pin through a resistor can improve surge immunity of the system. Keep trace **1** away from any power trace with high pulsating current.
- The control ground (trace 2) and power ground (trace 7) should meet at a single point to minimize interference. The connecting trace should be as short as possible.
- As indicated by 4, the ground of the feedback loop should be connected to the negative terminal of output capacitor C_O.
- Trace 5 should be long and far from V_o terminal.
- Keep trace **6** as short as possible.
- As indicated by 7, the source terminals of Q_1 and Q_2 are connected to the negative terminal of C_o. Keep trace 10 short, direct, and wide.
- As indicated by 8, the negative terminal of C_o should be connected to the case directly.

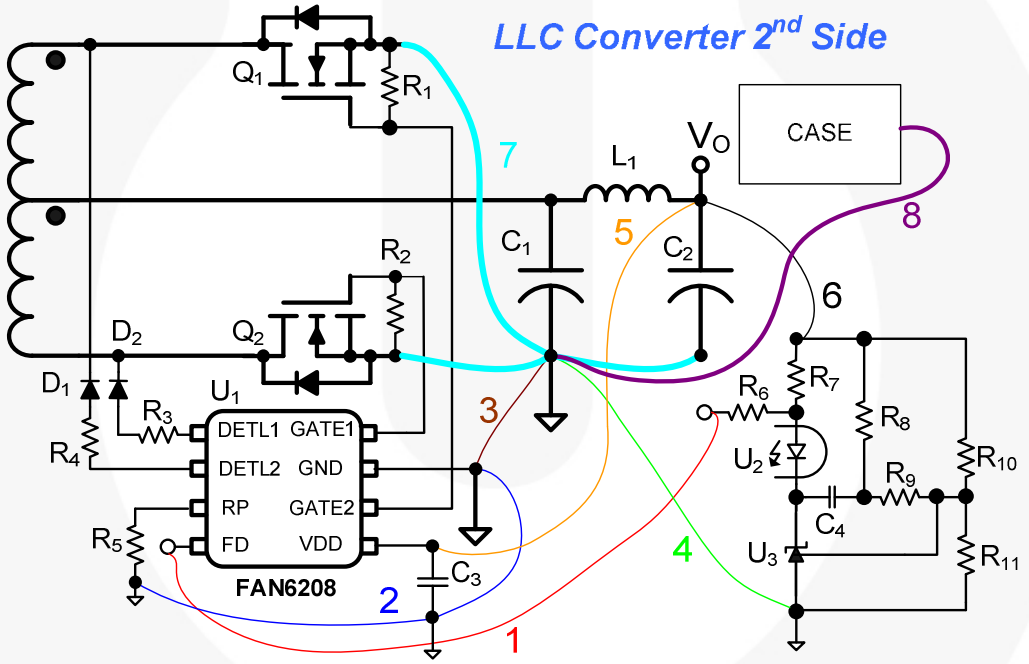

Figure 18. Layout Considerations

Design Example

The following example is a 12V/300W single output power supply with LLC resonant converter topology. As Figure 19 shows, the FAN7621 controller is used for the LLC resonant converter. The integrated CCM PFC controller FAN6982 is used for PFC stage.

The key system parameters are listed in Table 1 and the Bill of Materials (BOM) is summarized in Table 2.

The two-level PFC output voltage function of FAN6982 is used where the typical PFC output voltage is 390V. The PFC output voltage is reduced to 360V for low-line and light-load condition to improve efficiency of the PFC stage. The typical switching frequency (f_s) is 65kHz for PFC stage.

Table 1. System Specification

Input Voltage Range	90~264V_{AC}
PFC Output	360~390V_{DC}
PFC Controller	FAN6982
Main power Controller	FAN7621
Output Voltage (Vo)	12V
Output Power (Po)	300W
PFC Switching Frequency	65kHz
LLC resonant converter Switching Frequency	60~140kHz

The turn ratio n of TX_1 is 13.5, L_m is 1.2mH, L_r is 150µH, and C_r is 47nH. 1N4148 is used for D201 & D202 whose voltage rating is 100V. 27kΩ is used for R204 (R_{RP}) for the Low-Frequency Mode setting.

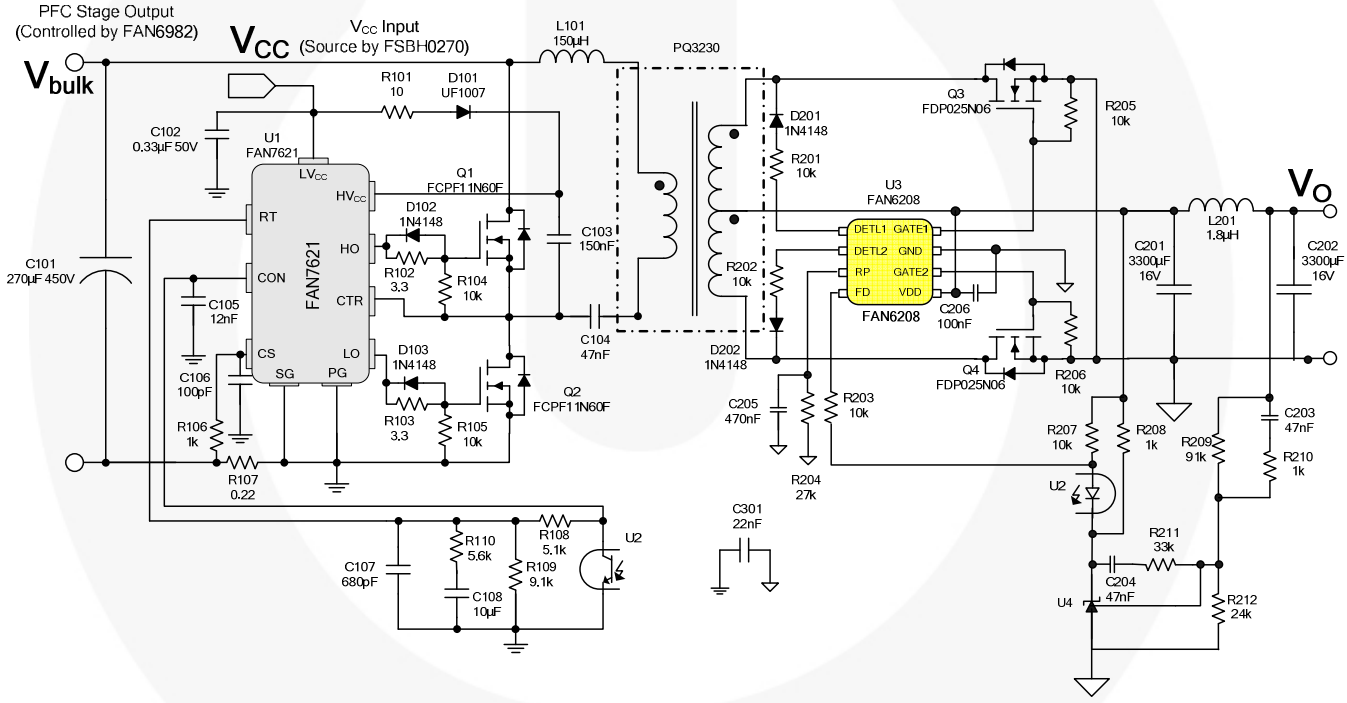

Figure 19. Complete Circuit Diagram

Table 2. Bill of Materials

Part	Value	Note	Part	Value	Note
Resistor			**Capacitor**		
R_{101}	10Ω	1/4W	C_{108}	10μF	25V
R_{102}	3.3Ω	1/4W	C_{201}	3300μF	16V
R_{103}	3.3Ω	1/8W	C_{202}	3300μF	16V
R_{104}	10kΩ	1/8W	C_{203}	47nF	50V
R_{105}	10kΩ	1/8W	C_{204}	47nF	50V
R_{106}	1kΩ	1/8W	C_{205}	470nF	25V
R_{107}	0.2Ω	2W	C_{206}	100nF	50V
R_{108}	5.1kΩ	1/8W	C_{301}	22nF/250V	Y-Capacitor
R_{109}	9.1kΩ	1/8W	**Transformer**		
R_{110}	5.6kΩ	1/8W	TX_1	L_r =10μH/ L_m =1200μH	PQ3230
R_{201}	10kΩ	1/8W	**Diode**		
R_{202}	10kΩ	1/8W	D_{101}	UF1007	1A/1000V
R_{203}	10kΩ	1/8W	D_{102}	1N4148	
R_{204}	27kΩ	1/8W	D_{103}	1N4148	
R_{205}	10kΩ	1/8W	D_{201}	1N4148	
R_{206}	10kΩ	1/8W	D_{202}	1N4148	
R_{207}	10kΩ	1/8W	**Inductor**		
R_{208}	1kΩ	1/8W	L101	L = 150μH	QP2914
R_{209}	91kΩ	1/8W	L201	L = 1.8μH	
R_{210}	1kΩ	1/8W	**MOSFET**		
R_{211}	33kΩ	1/8W	Q_1	FCPF11N60F	
R_{212}	24kΩ	1/8W	Q_2	FCPF11N60F	
Capacitor			Q_3	FDP025N06	
C_{101}	270μF	450V	Q_4	FDP025N06	
C_{102}	0.33μF	50V	**IC**		
C_{103}	150nF	1kV	U_1	FAN7621	LLC Controller
C_{104}	47nF	1kV	U_2	PC817	
C_{105}	12nF	50V	U_3	FAN6208	SR Controller
C_{106}	100pF	50V	U_4	TL431	
C_{107}	680pF	50V			

Figure 20 and Figure 21 show the SR gate drive waveforms for different R_P. As can be seen, the dead time of SR drive can be programmed.

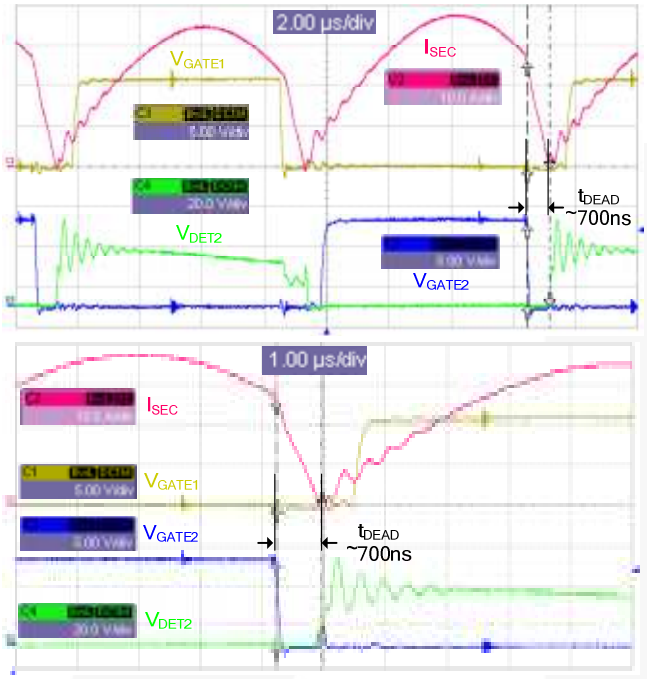

Figure 20. Secondary Side Current and SR Gate Signal by R_{RP}=24kΩ

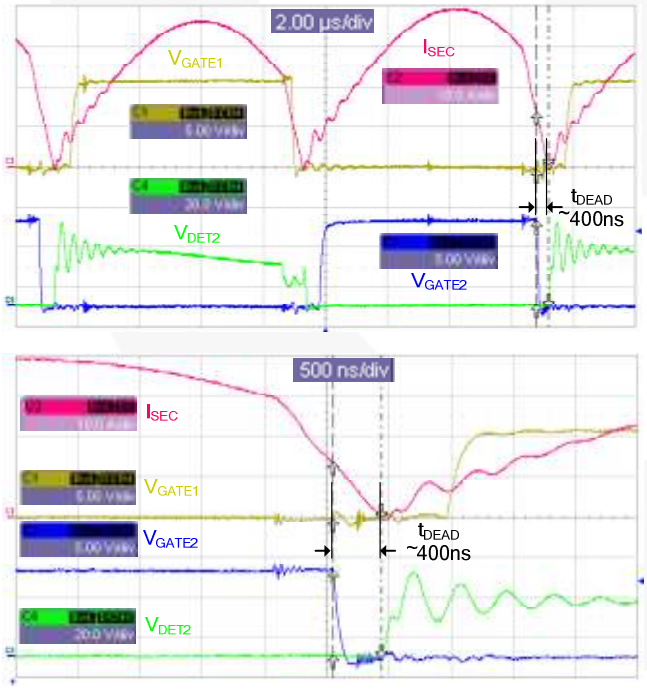

Figure 21. Secondary Side Current and SR Gate Signal by R_{RP}=27kΩ

The efficiency test results of the Schottky diode and synchronous rectification are shown in Table 3 and Table 4. Figure 22 compares the efficiencies of Schottky diode and synchronous rectification. As can be seen, 1~2% efficiency improvement can be obtained using synchronous rectification. Figure 22 also shows how the dead time of SR affects the efficiency. By fine-tuning the dead time, efficiency can be maximized.

Table 3. Efficiency Measurements at V_{AC}=115V on 300W PC Power with Schottky Diodes (MBRP3045)

Load	Input Watts(W)	Output Watts(W)	Efficiency
100%	358.070	307.658	85.920%
50%	176.38	154.91	87.82%
20%	73.30	62.19	84.80%

Table 4. Efficiency Measurements at V_{AC}=115V on 300W PC Power with SRs (FDP025N06 and R_{RP}=30kΩ)

Load	Input Watts (W)	Output Watts (W)	Efficiency	vs. Schottky Diode
100%	347.70	307.62	88.47%	+2.55%
50%	172.81	154.77	89.56%	+1.74%
20%	72.41	62.21	85.91%	+1.11%

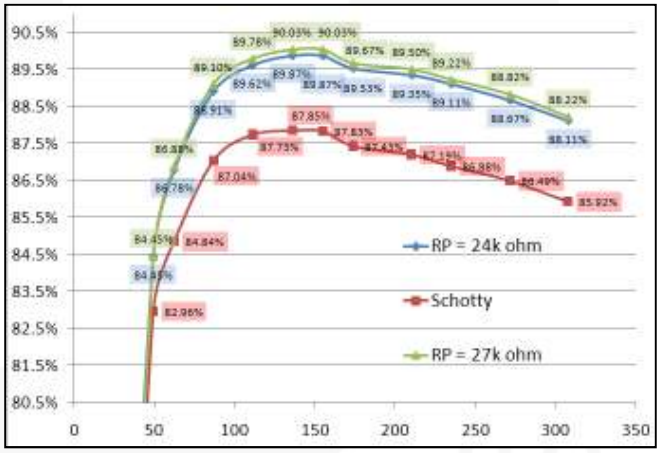

Figure 22. Efficiency Analysis

Related Resources

FAN6208 — Secondary Synchronous Rectifier Controller for LLC Topology
FAN7621 — PFM Controller for Half-Bridge Resonant Converters
FAN6982 — CCM Power Factor Correction Controller
FDP025N06 —FDP025N06 N-Channel PowerTrench® MOSFET 60V,265A, 2.5mΩ
1N/FDLL 914/A/B / 916/A/B / 4148 / 4448 — Small Signal Diode
FSFR2100 — Fairchild Power Switch for Half-Bridge Resonant Converters
AN4137 — Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)
AN-4151 — Half-Bridge LLC Resonant Converter Design Using FSFR-Series Fairchild Power Switch (FPS)

Applying Synchronous Rectification in Resonant Half-Bridge Converters

Technology developed for driving synchronous FETs in flyback topologies can be directly applied in LLC topologies. This technology offers significant gains in efficiency for applications with low output voltages, and high output currents.

Brian King, Applications Engineer, Texas Instruments | *Power Electronics* *Sep 5, 2013*

Resonant half-bridge converters used to drive synchronous FETs in flyback topologies can be directly applied in LLC topologies. Resonant technology provides a cost-effective and efficient solution for offline power supplies in the range of 200 W to 500 W.

Technology developed for driving synchronous FETs in flyback topologies can be directly applied in LLC topologies. This technology offers significant gains in efficiency for applications with low output voltages, and high output currents.

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- LLC Resonant Converters Increase Efficiency in DC-to-DC Applications
- Understanding the Data Sheet Key to Effective Circuit Design
- New Technique for Non-Invasive Testing of Regulator Stability
- Topology Key to Power Density in Isolated DC-DC Converters
- Source Impedance Affects Converter Performance

Resonant half-bridge converters provide a cost-effective and efficient solution for offline power supplies in the range of 200 W to 500 W. This topology is also known as an LLC converter, with the name derived from the fact that the resonant tank comprises two inductors and one capacitor. The transformer's magnetizing inductance accounts for one of the inductors. The other inductor can be either a separate component, or integrated into the power transformer in the form of leakage inductance. This topology benefits from zero voltage switching on the primary switches and as such has been traditionally applied in applications with high input voltages, where switching losses are more dominant. In LLC converters with lower output voltages, losses in the output diodes can be a thermal problem. Replacing them with synchronous rectifiers can reduce losses and increase efficiency, as well as reduce size by eliminating bulky heat sinks.

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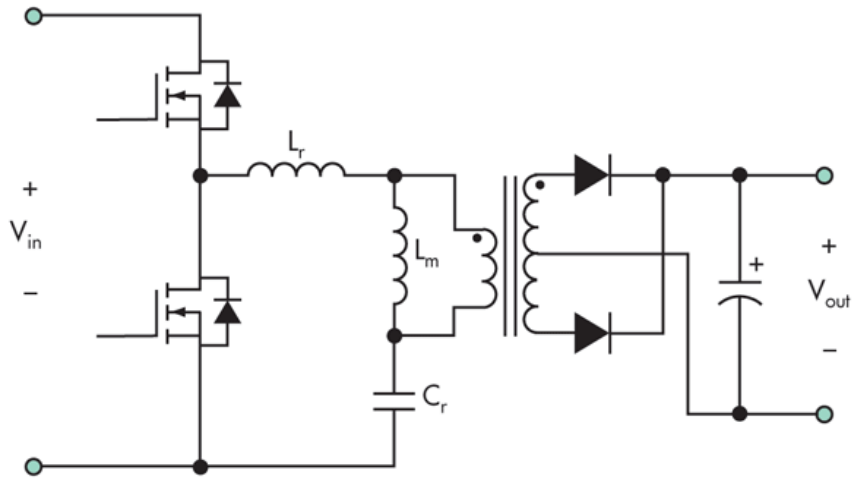

Fig. 1. The secondary winding of an LLC transformer can be configured as a current doubler to make the currents more manageable.

Fig. 1 shows a simplified schematic of an LLC converter. The primary FETs are driven out of phase with each other at a 50% duty cycle. The switching frequency is variable and is controlled to regulate the output voltage. The gain characteristics of the power stage determine the switching frequency at a given input voltage and loading operating point. For proper function, the convert must always operate in the inductive region, to the right of resonance. In high current applications, the secondary of the power transformer is often configured as a current-doubler (*Fig. 1*). Each secondary winding and diode conducts only half of the current that otherwise would flow in a transformer with a single secondary.

A class of synchronous rectifier controller/driver exists that originally was intended for use in discontinuous flyback converters. These devices essentially control a MOSFET in such a manner that it is on when current begins to flow source-to-drain through the body diode, and off when the current drops below a certain level. Since these devices only allow current to flow in one direction, they mimic the action of a diode with low loss and can be referred to as ideal diode emulators. *Fig. 2* shows how this is typically implemented in a flyback converter.

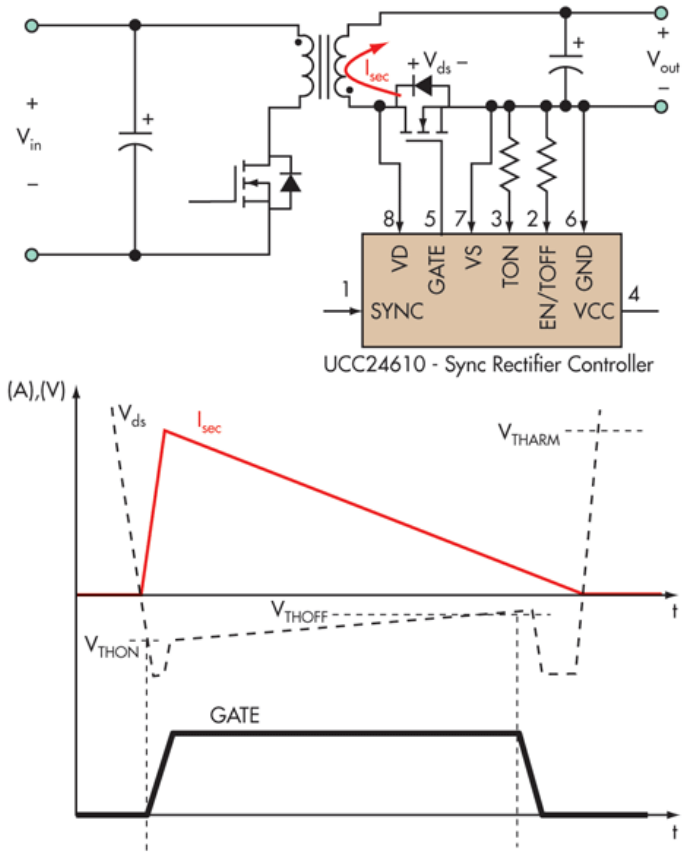

Fig. 2. Ideal diode emulators improve efficiency in flyback converters. A (top) shows the circuit and b (bottom) shows the waveforms.

In *Fig. 2*, the current direction and amplitude is detected by monitoring the voltage on the drain connection of the synchronous rectifier. When the primary FET is turned on, the voltage on the drain of the synchronous rectifier transitions past the V_{THARM} threshold and arms the driver. When the primary FET is turned off, current begins to flow through the body diode of the synchronous rectifier. The driver detects the negative potential (V_{THON}) on the drain, and turns on the synchronous FET. As the secondary current decays, so does the voltage on the drain of the Synchronous FET. When this voltage drops below a threshold (V_{THOFF}),the driver turns off the synchronous FET and waitsto be armed for the next switching cycle. The voltage on the source pin is also sensed through a kelvin connection for a more accurate monitoring of the drain-to-source voltage.

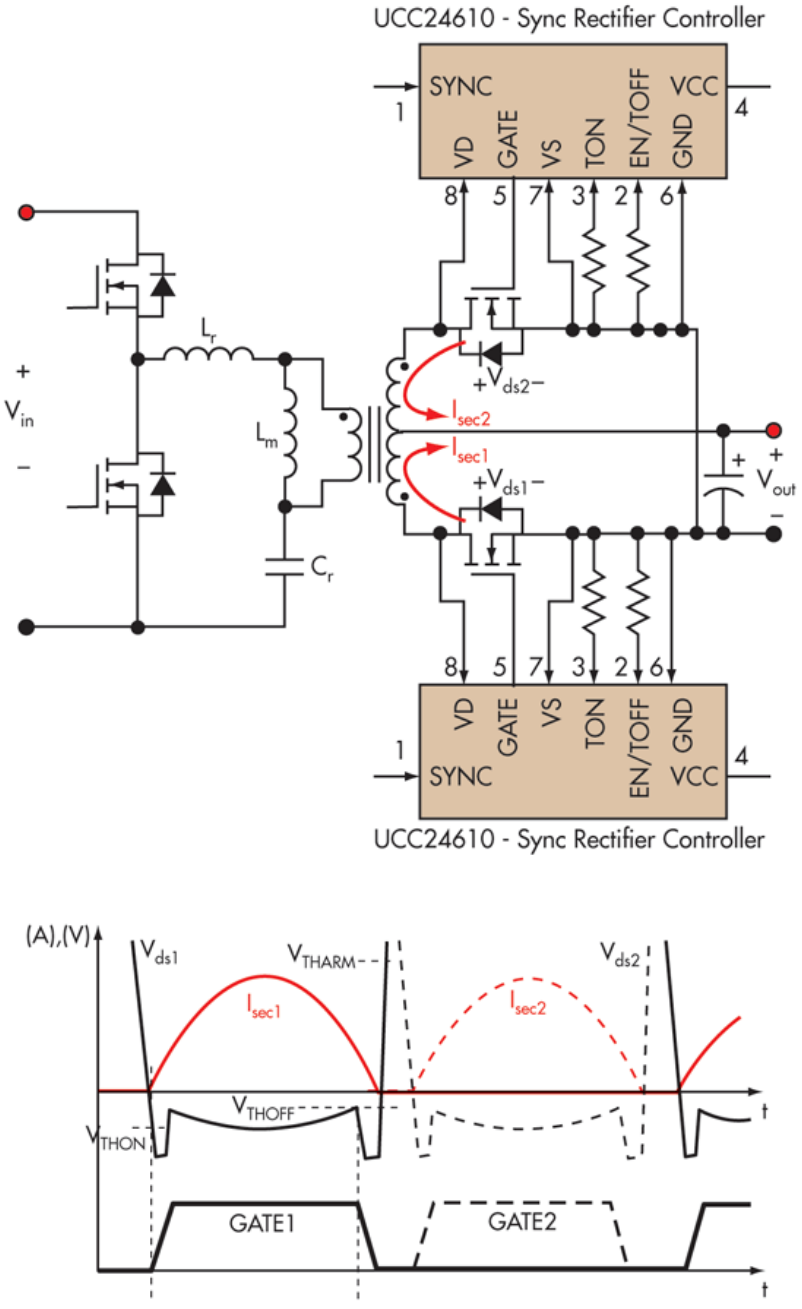

Fig. 3. Ideal diode emulators can be applied in LLC converters. A (top) shows the circuit and b (bottom) shows the waveforms.

Luckily, it turns out that the secondary voltage and current waveforms in LLC convertersare well-suited for ideal diode emulators. The secondary windings act as a current source, forcing the conduction of the output diodes. As shown in *Fig. 3*, two drivers and two synchronous rectifiers are required; one driver and one synchronous rectifier for each secondary winding. The driver is armed when the opposite secondary rectifier is conducting. The current waveform's generally sinusoidal shape provides a gradually decaying slope allowing plenty of time for the synchronous rectifier controller to

detect the V_{THOFF}crossing and turn off the synchronous FET.

The rising edge of the secondary current can pose a potential problem. Because the current begins from zero, the drain to source voltage will be below the turn off threshold at the start of the conduction cycle. Most synchronous rectifier drivers provide a minimum on-time function that masks the turn-off comparator to prevent false triggering due to noise. In LLC applications, it is critical to use a synchronous rectifier driver that provides this function. The minimum on-time should be set long enough to ensure that the drain to source voltage has risen above the turn-off threshold.

As a practical example, consider an application that requires a 12 V, 460 W output to be derived from the output of a PFC pre-regulator. With a 38 A output current, the currents in each of the secondary windings are 19 A (average) and 30 A (rms) per winding. Assuming a forward drop of 0.5 V, Schottky diodes would dissipate around 19 W. This would require significant heat sinking. The advantage offered by synchronous rectification is immediately obvious. With a current doubler configuration, thesynchronous FETs must be rated for at least two times the output voltage plus margin. In this application, 40 V FETs are a good choice. Using three paralleled 3 mΩ FETs limits the dissipation to around 330 mW per FET. There will be some additional loss during the short durations near the zero crossings, when the body diode is conducting. The synchronous rectifiers offera savings of around 17 W compared to using diodes.

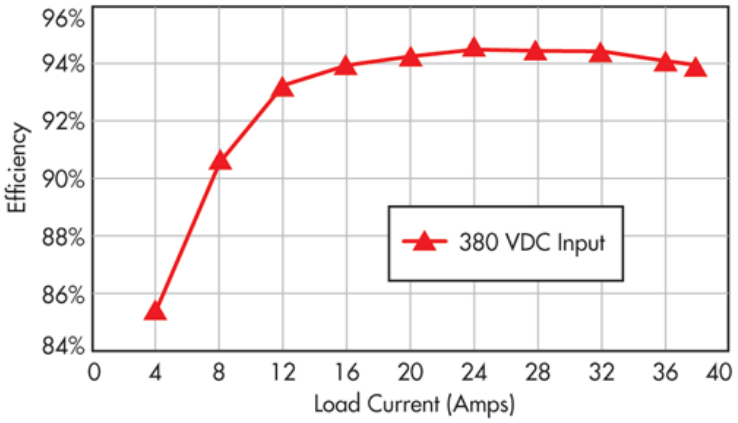

Fig. 4. Synchronous rectifiers provide a 3% increase in efficiency compared to Schottky diodes.

Fig. 4 displays the efficiency measured on a prototype of this 12 V, 460 W design. The synchronous rectifiers provide efficiencies over 94% for much of the load range. By comparison, with Schottky diodes, the efficiency would be around91% at the full 38 A load.

The losses in the synchronous FETs are low enough that surface mount components can be used with some forced air flow, eliminating heat sinks, which reduces the size and simplifies the assembly process. A thermal image of the prototype, *Fig. 5*, shows that the temperature rise of the synchronous FETs is less than 40 °C. In fact, the rectifiers are no longer the hottest components on the circuit board.

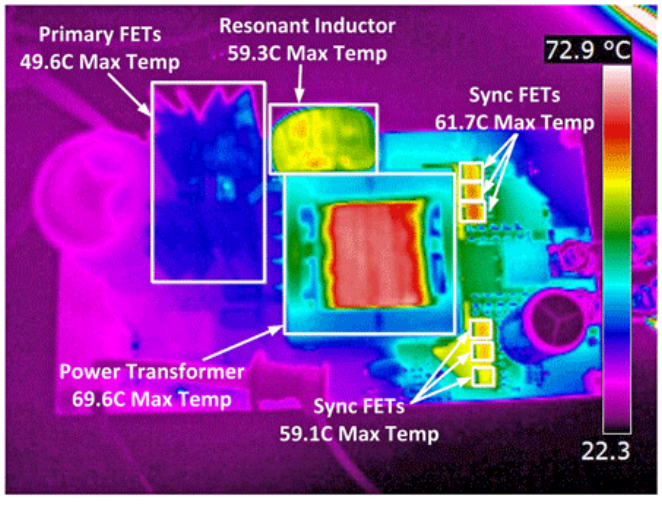

Fig. 5. With some forced air flow, synchronous rectifiers do not require heat sinks to maintain reasonable temperature rises (25ºC ambient).

References

1. PMP 5967 datasheet

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Frequency-Controlled Series-Resonant Converter with Synchronous Rectifier

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This paper presents an analysis and experimental results for a frequency-controlled series-resonant dc-dc converter that consists of a Class-D zero-voltage-switching (ZVS) series-resonant inverter and a center-tapped synchronous rectifier. If the dc output voltage is low, the efficiency of the converter is dominated by the efficiency of the rectifier. Low on-resistance metal-oxide-semiconductor field-effect transistors (MOSFETs) are used in the rectifier instead of diodes because the forward voltage drop across the rectifying device is low, resulting in a high efficiency. The dc output voltage is regulated against variations in the load resistance and the dc input voltage by varying the operating frequency. Experimental results are presented for a converter with a dc input voltage of 150 V, an output voltage of 5 V, and a dc load resistance ranging from 0.5 to 5.5 Ω. The measured efficiency was 86% for a 50 W output and 89% for a 25 W output. The theoretical results were in good agreement with the measured results.

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I. INTRODUCTION

A Class-D dc-ac series resonant inverter can achieve very high efficiency if it is operated above the resonant frequency and if the dc input voltage is high (which is normally the case for step-down converters). The efficiency of the rectifier is very low if the dc output voltage is low, e.g., 5 V or 3.3 V. This is because the forward voltage drop across the rectifying devices (usually, *pn* junction diodes or Schottky diodes) becomes comparable to the dc output voltage. The natural method of improving the rectifier efficiency is to reduce the forward voltage drop of the rectifying devices [1–8]. Unlike diodes, power metal-oxide-semiconductor field-effect transistors (MOSFETs) do not have offset voltages. If the on-resistance of the MOSFET is low, the forward voltage drop is small. Currently, power MOSFETs with on-resistances as low as 10 mΩ are available. Replacing diodes with low on-resistance power MOSFETs significantly reduces the conduction losses. Synchronous rectification, using power MOSFETs rather than diodes in the rectifier, can achieve efficiencies between 85% and 90%. High-frequency resonant converters introduced in recent years offer many advantages: small size and weight, high power density, and low electromagnetic interference (EMI) levels.

The purpose of this work is to present the analysis of an efficient frequency-controlled dc-dc series-resonant converter with a center-tapped synchronous rectifier that is suitable for applications with high-input voltages and low-output voltages. The fundamental-frequency approximation of the current through the resonant circuit is used in the analysis of the inverter. The rectifier is replaced by its input resistance at the fundamental frequency. In Section II, an analysis of the converter is carried out. Section III contains a design procedure of the converter. Experimental results are given in Section IV. Finally, conclusions are presented in Section V.

II. ANALYSIS OF THE CIRCUIT

A. Series-Resonant Inverter

Fig. 1 shows a Class D series-resonant converter. It consists of a series-resonant inverter and a current-driven center-tapped synchronous rectifier. The series-resonant inverter is comprised of two power MOSFETs, a resonant inductor L, and a resonant capacitor C. The shunt capacitor C_2 is used to obtain zero-voltage-switching (ZVS) operation. ZVS operation can be accomplished when the switching frequency is above the resonant frequency $f_0 = 1/(2\pi\sqrt{LC})$ and the MOSFETs are driven with

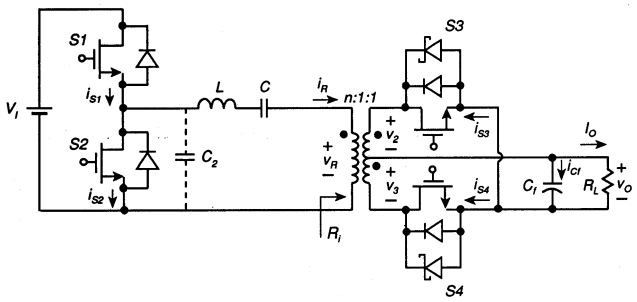

Fig. 1. Class-D series-resonant converter with transformer center-tapped synchronous rectifier.

a sufficient dead time (not shown in Fig. 2(d)). Resistance R_i represents an ac load of the inverter.

Figs. 2(a), (b), and (c) show the equivalent circuits of the Class D series-resonant inverter, including parasitic resistances. In Fig. 2(a), the power MOSFETs are modeled by ideal switches in series with the on-resistances r_{DS1} and r_{DS2} of the MOSFETs. The equivalent series resistance of the resonant inductor is r_L and the equivalent series resistance of the resonant capacitor is r_C. In Fig. 2(b), the dc voltage source V_I and the switches are modeled by a square-wave voltage source v and the averaged parasitic resistance of the MOSFETs $r_{DS} = (r_{DS1} + r_{DS2})/2$. The total parasitic resistance r in Fig. 2(c) is

$$r = r_{DS} + r_L + r_C. \tag{1}$$

Fig. 2(d) shows the waveforms of the gate-source voltage v_{GS2}, the drain-source voltage v_{DS2}, the fundamental component v_{i1} of voltage v_{DS2}, the load current i_R, and the switch currents i_{S1} and i_{S2} of the inverter. In general, the rectifier represents a nonlinear load to the inverter. However, if the loaded quality factor $Q_L = \omega_0 L/(R_i + r)$ is sufficiently high (i.e., $Q_L \geq 2.5$), the current i_R through the series-resonant circuit is nearly sinusoidal, the power of higher harmonics is negligible, and only the power of the fundamental component is transferred from the inverter to the rectifier. The input voltage of the rectifier is a square wave in phase with the quasi-sinusoidal current i_R. Consequently, the rectifier may be modeled by a linear input resistance R_i, which is proportional to the load resistance R_L, as shown in Section IIB. If the input current and voltage were not in phase, a complex input impedance that contains a resistive part and a reactive part would be required to model the input impedance of the rectifier.

The magnitude of the dc-to-ac voltage transfer function of the Class-D inverter is [2]

$$|M_I| = \frac{V_{R1\text{rms}}}{V_I} = \frac{V_{R1\text{rms}}}{V_{\text{rms}}}\frac{V_{\text{rms}}}{V_I} = \frac{\sqrt{2}\eta_I}{\pi\sqrt{1 + Q_L^2\left(\frac{f}{f_0} - \frac{f_0}{f}\right)^2}} \tag{2}$$

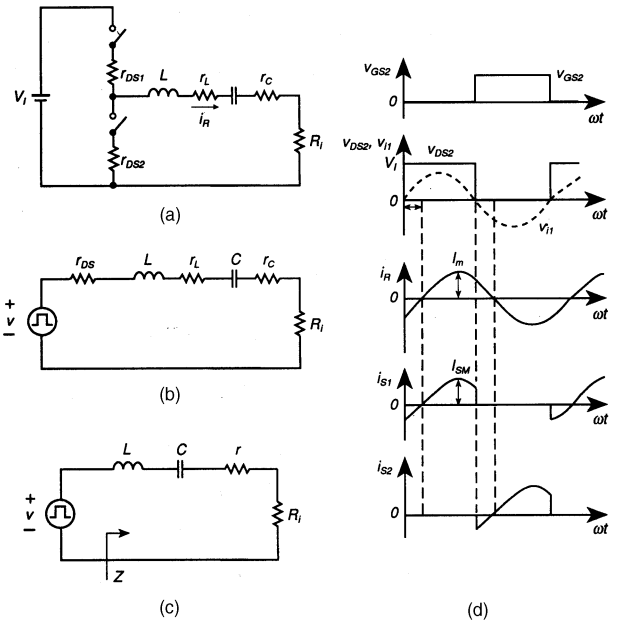

Fig. 2. Class-D series-resonant inverter. (a) Circuit. (b) Equivalent circuit with parasitic resistances. (c) Equivalent circuit showing parasitic resistances combined into equivalent resistance r. (d) Waveforms.

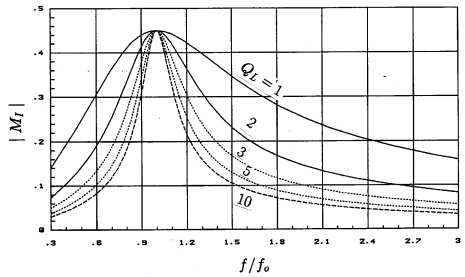

Fig. 3. DC-to-ac transfer function of series-resonant inverter $|M_I|$ as function of f/f_0 at various values of Q_L.

where $V_{R1\text{rms}}$ is the rms value of the fundamental component of the rectifier input voltage, V_{rms} is the rms value of the fundamental component of the voltage v at the input of the resonant circuit, $Q_L = \omega_0 L/(R_i + r) = Z_0/(R_i + r)$ is the loaded quality factor, $Z_0 = \sqrt{L/C}$ is the characteristic impedance of the resonant circuit, and η_I is the inverter efficiency. The magnitude of the dc-to-ac inverter voltage transfer function $|M_I|$ is plotted as a function of f/f_0 at different values of Q_L in Fig. 3.

The conduction power loss in the resonant circuit and both transistors of the inverter is

$$P_r = \frac{I_m^2(r_{DS} + r_L + r_C)}{2} = \frac{I_m^2 r}{2}. \tag{3}$$

The output power of the inverter is

$$P_{Ri} = \frac{I_m^2 R_i}{2}. \tag{4}$$

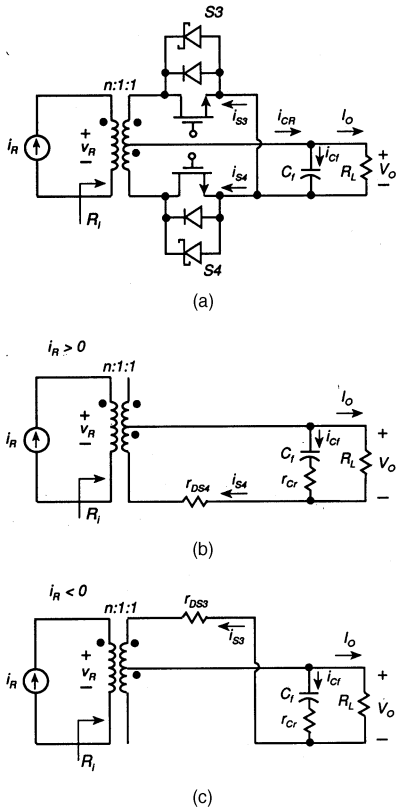

Fig. 4. Class-D current-driven transformer center-tapped synchronous rectifier and its models. (a) Circuit. (b) Equivalent circuit when S_3 is OFF and S_4 is ON. (c) Equivalent circuit when S_4 is OFF and S_3 is ON.

Neglecting switching losses, one obtains the efficiency of the Class-D inverter

$$\eta_I = \frac{P_{Ri}}{P_{Ri} + P_r} = \frac{R_i}{R_i + r} = 1 - \frac{1}{1 + \dfrac{R_i}{r}} = 1 - \frac{Q_L}{Q_0} \tag{5}$$

where $Q_0 = \omega_0 L/r$ is the unloaded quality factor of the resonant circuit. It can be seen that the inverter efficiency η_I depends on r/R_i; it increases with decreasing r/R_i or Q_L/Q_0. As R_L is increased, R_i increases, reducing r/R_i and maintaining high efficiency at light loads.

B. Synchronous Rectifier

Fig. 4 shows a Class-D current-driven transformer center-tapped synchronous rectifier and its models. The synchronous rectifier consists of a center-tapped transformer, two power MOSFETs, two Schottky diodes, and a filter capacitor C_f. Resistance R_L is a dc load. When the power MOSFET is used as a synchronous rectifier, it is configured so that the current normally flows through the channel from source to drain, i.e., in the direction of the body diode. This ensures reverse blocking capability by the body diode (and the Schottky diode), when the transistor is

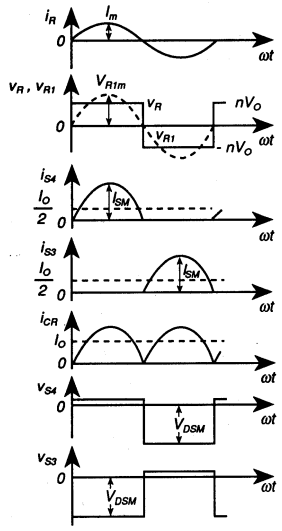

Fig. 5. Waveforms of transformer center-tapped synchronous rectifier.

OFF because there is no current path through the body diode. Notice that the gates of the rectifier MOSFETs are driven with respect to ground.

The waveforms of the rectifier are shown in Fig. 5. The rectifier is driven by a nearly sinusoidal current

$$i_R = I_m \sin \omega t \tag{6}$$

where I_m is the amplitude of i_R. Operation of the synchronous rectifier is similar to that of the basic current-driven center-tapped rectifier with diodes. As a first order approximation, the MOSFETs can be modeled by an equivalent on-resistance r_{DS} when a positive gate voltage is applied and as an open circuit when the gate voltage is zero. For $0 < \omega t \leq \pi$, $i_R > 0$, v_{GS4} is positive and $v_{GS3} = 0$, which turns S_4 ON and S_3 is OFF. Fig. 4(b) shows a model of the rectifier for this time interval. The voltages across the secondaries of the transformer are

$$v_3 = V_0 = v_2 \tag{7}$$

the voltage at the rectifier input is

$$v_R = nv_3 = nV_0 \tag{8}$$

and the voltage across the upper rectifier switch is

$$v_{S3} = -v_2 - v_3 = -V_0 - V_0 = -2V_0 \tag{9}$$

where n is the transformer turns ratio. The current through the upper rectifier switch and the C_f-R_L circuit is

$$i_{S4} = i_{CR} = ni_R = nI_m \sin \omega t. \tag{10}$$

For $\pi < \omega t \leq 2\pi$, $i_R < 0$, v_{GS3} is positive and $v_{GS4} = 0$, which turns S_3 ON and S_4 OFF. A model of the rectifier for this time interval is depicted in Fig. 4(c). From this figure, one obtains the voltages across the secondaries of the transformer

$$v_2 = -V_0 = v_3 \tag{11}$$

the rectifier input voltage

$$v_R = nv_2 = -nV_0 \tag{12}$$

and the voltage across the bottom rectifier MOSFET

$$v_{S4} = v_2 + v_3 = -V_0 - V_0 = -2V_0 \tag{13}$$

the current through the bottom rectifier MOSFET and the C_f-R_L circuit

$$i_{S3} = i_{CR} = -ni_R = nI_m \sin\omega t. \tag{14}$$

The current to the C_f-R_L circuit is

$$i_{CR} = i_{S3} + i_{S4} = n|i_R| = nI_m|\sin\omega t|. \tag{15}$$

The average values of i_{RC} yields the dc component of the output current

$$\begin{aligned} I_0 &= \frac{1}{2\pi}\int_0^{2\pi}(i_{S3} + i_{S4})d(\omega t) \\ &= \frac{1}{\pi}\int_0^{\pi} nI_m \sin\omega t\, d(\omega t) = \frac{2nI_m}{\pi}. \end{aligned} \tag{16}$$

The dc output current I_0 is directly proportional to the amplitude of the input current I_m. The dc component of the output voltage is

$$V_0 = I_0 R_L = \frac{2nI_m R_L}{\pi}. \tag{17}$$

It follows from (17) that the dc output voltage V_0 is directly proportional to I_m and, therefore, can be regulated against load and line variations by varying I_m in such a way that the product of I_m and R_L remains constant.

Using (16), the peak forward current of each rectifier MOSFET is

$$I_{SMr} = nI_m = \frac{\pi I_0}{2} \tag{18}$$

and the peak reverse voltage of each rectifier MOSFET is

$$V_{SMr} = 2V_0. \tag{19}$$

Neglecting the voltage drop across the MOSFETs, the input voltage v_R of the rectifier is a square wave, which can be expressed by

$$v_R = \begin{cases} nV_0, & \text{for} \quad 0 < \omega t \le \pi \\ -nV_0, & \text{for} \quad \pi < \omega t \le 2\pi. \end{cases} \tag{20}$$

Hence, the amplitude of the fundamental component $v_{R1} = V_{R1m}\sin\omega t$ of the rectifier voltage v_R is

$$\begin{aligned} V_{R1m} &= \frac{1}{\pi}\int_0^{2\pi} v_R \sin\omega t\, d(\omega t) \\ &= \frac{2}{\pi}\int_0^{\pi} v_R \sin\omega t\, d(\omega t) = \frac{4nV_0}{\pi} \end{aligned} \tag{21}$$

resulting in its rms value

$$V_{R1\text{rms}} = \frac{V_{R1m}}{\sqrt{2}} = \frac{2\sqrt{2}nV_0}{\pi}. \tag{22}$$

Since the rectifier input current is approximately sinusoidal, the input power contains only the power of the fundamental component. The fundamental component v_{R1} of the input voltage v_R is in phase with the input current i_R. Using (16), the input power of the rectifier can be expressed as

$$P_{Ri} = \frac{I_m^2 R_i}{2} = \frac{\pi^2 I_0^2 R_i}{8n^2}. \tag{23}$$

The rms value of the current through each rectifier MOSFET is

$$I_{S\text{rms}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{S4}^2 d(\omega t)} = \frac{nI_m}{2} = \frac{\pi I_0}{4}. \tag{24}$$

Thus, the power loss in the forward resistance r_{DSr} of each rectifier MOSFET is

$$P_{rDS} = r_{DSr} I_{S\text{rms}}^2 = \frac{\pi^2 I_0^2 r_{DSr}}{16} = \frac{\pi^2 r_{DSr}}{16R_L} P_0 \tag{25}$$

where $P_0 = I_0^2 R_L$ is the dc output power.

From (15), the current through the filter capacitor C_f can be approximated by

$$i_{Cf} \approx i_{CR} - I_0 = nI_m|\sin\omega t| - I_0 = I_0\left(\frac{\pi}{2}|\sin\omega t| - 1\right) \tag{26}$$

which leads to the rms value of the current through the filter capacitor

$$\begin{aligned} I_{Cf(\text{rms})} &= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{Cf}^2 d(\omega t)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_{Cf}^2 d(\omega t)} \\ &= I_0\sqrt{\frac{\pi^2}{8} - 1} \approx 0.4834 I_0 \end{aligned} \tag{27}$$

and the power dissipated in the equivalent series resistance of the filter capacitor r_{Cr}

$$P_{rC} = r_{Cr} I_{Cf(\text{rms})}^2 = r_C I_0^2\left(\frac{\pi^2}{8} - 1\right) = \frac{r_{Cr}}{R_L}\left(\frac{\pi^2}{8} - 1\right) P_0. \tag{28}$$

The total power loss is

$$P_C = 2P_{rDS} + P_{rC} = P_0\left[\frac{\pi^2 I_0^2 r_{DSr}}{8R_L} + \frac{r_{Cr}}{R_L}\left(\frac{\pi^2}{8} - 1\right)\right]. \tag{29}$$

Note that the switching losses in the rectifier MOSFETs have been neglected in (29) because synchronous rectifiers usually have low output voltage and the MOSFETs are turned on and off at zero current, which make the switching losses negligible.

Considering the power loss in the transformer, the input power is found as

$$P_{Ri} = \frac{P_0 + P_C}{\eta_{tr}} \tag{30}$$

where η_{tr} is the efficiency of the transformer. The efficiency of the synchronous rectifier is

$$\eta_R = \frac{P_0}{P_{Ri}} = \left(\frac{V_0}{V_{R1\text{rms}}}\right)^2 \frac{R_i}{R_L} = \frac{\eta_{tr} P_0}{P_0 + P_C} = \frac{\eta_{tr}}{1 + \dfrac{\pi^2 r_{DSr}}{8R_L} + \dfrac{r_{Cr}}{R_L}\left(\dfrac{\pi^2}{8} - 1\right)}. \quad (31)$$

From (23), (30), and (31), one arrives at the input resistance of the rectifier

$$R_i = \frac{8n^2 R_L}{\pi^2 \eta_{tr}}\left[1 + \frac{\pi^2 r_{DSr}}{8R_L} + \frac{r_{Cr}}{R_L}\left(\frac{\pi^2}{8} - 1\right)\right] = \frac{8n^2 R_L}{\pi^2 \eta_R}. \quad (32)$$

Using (31) and (32), one obtains the voltage transfer function of the synchronous rectifier as

$$M_{VR} \equiv \frac{V_0}{V_{R1\text{rms}}} = \sqrt{\frac{\eta_R R_L}{R_i}} = \frac{\pi \eta_{tr}}{2\sqrt{2}n\left[1 + \dfrac{\pi^2 r_{DSr}}{8R_L} + \dfrac{r_{Cr}}{R_L}\left(\dfrac{\pi^2}{8} - 1\right)\right]} = \frac{\pi \eta_R}{2\sqrt{2}n}. \quad (33)$$

III. DESIGN PROCEDURE

Using the design equations developed in Section II, a series-resonant converter with a center-tapped synchronous rectifier was designed and implemented to meet the following specifications: $V_I = 150$ V, $V_0 = 5$ V, $R_{L\text{min}} = 0.5\ \Omega$, and $R_{L\text{max}} = 5.5\ \Omega$. The transformer efficiency is $\eta_{tr} = 0.95$ and $f/f_0 = 1.15$ at full power.

A. Synchronous Rectifier

It is sufficient to design the power stage of the converter for full power. The maximum value of the dc output current is

$$I_{O\text{max}} = \frac{V_0}{R_{L\text{min}}} = \frac{5}{0.5} = 10\ \text{A} \quad (34)$$

and the maximum output power is

$$P_{O\text{max}} = \frac{V_0^2}{R_{L\text{min}}} = \frac{5^2}{0.5} = 50\ \text{W}. \quad (35)$$

The current stress of the rectifier MOSFETs is

$$I_{SMr} = nI_m = \frac{\pi I_{O\text{max}}}{2} = \frac{\pi \times 10}{2} = 15.71\ \text{A} \quad (36)$$

and the voltage stress of the rectifier MOSFETs is

$$V_{SMr} = 2V_0 = 2 \times 5 = 10\ \text{V}. \quad (37)$$

Ultralow on-resistance Motorola MTP75N05HD power MOSFETs were used in the rectifier. The on-resistance of these power MOSFETs is $r_{DSr} = 9.5\ \text{m}\Omega$. Their breakdown voltage is $V_{DSS} = 50$ V and the maximum dc drain current is $I_{DM(\text{max})} = 75$ A. The total typical gate charge is $Q_g = 71$ nC and the total maximum gate charge is $Q_{g\text{max}} = 100$ nC. A 2200 μF capacitor with an equivalent series resistance $r_{Cr} = 53\ \text{m}\Omega$ measured at 100 kHz was used to reduce the output voltage ripple.

Notice that the maximum voltage across each rectifier MOSFET is $v_{DSr(\text{max})} = I_{SMr} r_{DSr} = 15.71 \times 0.0095 \approx 0.1149\ \text{mV} < 0.35$ V. Therefore, the body diode and the Schottky diode are OFF when the rectifier MOSFET is fully ON. The efficiency of the synchronous rectifier at full power is found as

$$\eta_R = \frac{\eta_{tr}}{1 + \dfrac{\pi^2 r_{DSr}}{8R_{L\text{min}}} + \dfrac{r_{Cr}}{R_{L\text{min}}}\left(\dfrac{\pi^2}{8} - 1\right)} = \frac{0.95}{1 + \dfrac{\pi^2 \times 0.0095}{8 \times 0.5} + \dfrac{0.0053}{0.5}\left(\dfrac{\pi^2}{8} - 1\right)} = 0.926. \quad (38)$$

Assuming a transformer turns ratio $n = 8$, the input resistance of the synchronous rectifier can be found as

$$R_i = \frac{8n^2 R_{L\text{min}}}{\pi^2 \eta_R} = \frac{8 \times 8^2 \times 0.5}{\pi^2 \times 0.926} = 28.011\ \Omega \quad (39)$$

and the voltage transfer function of the rectifier becomes

$$M_{VR} = \frac{\pi \eta_R}{2\sqrt{2}n} = \frac{\pi \times 0.926}{2 \times \sqrt{2} \times 8} = 0.1286. \quad (40)$$

The rms value of the fundamental component of the rectifier input voltage is

$$V_{R1\text{rms}} = \frac{V_0}{M_{VR}} = \frac{5}{0.1286} = 38.88\ \text{V}. \quad (41)$$

The ac input power of the rectifier is

$$P_{Ri} = \frac{P_0}{\eta_R} = \frac{50}{0.926} = 53.996\ \text{W}. \quad (42)$$

The resonant frequency of the inverter is chosen to be $f_0 = 100$ kHz. Hence, the operating frequency at full load is $f = 115$ kHz. Assuming the peak gate-to-source voltage $V_{GSp} = 7$ V, the gate drive power of each rectifier MOSFET is

$$P_{Gr} = fQ_{g\text{max}} V_{GSp} = 115 \times 10^3 \times 100 \times 10^{-9} \times 7 = 80.5\ \text{mW}. \quad (43)$$

B. Inverter

From (4), the peak current through the resonant circuit and the MOSFETs of the inverter at $f =$

115 kHz is

$$I_{SMi}(f) = I_m(f) = \sqrt{\frac{2P_{Ri}}{R_i}} = \sqrt{\frac{2 \times 53.996}{28.011}} = 1.9635 \text{ A} \quad (44)$$

and at the resonant frequency $f = f_0$ is

$$I_{SMi}(f_0) = I_m(f_0) = \frac{2V_I}{\pi(R_i + r)} = \frac{2 \times 150}{\pi \times (28.011 + 0.9)} = 3.3 \text{ A}. \quad (45)$$

The voltage stress of the inverter MOSFETs is

$$V_{SMi} = V_I = 150 \text{ V}. \quad (46)$$

Two International Rectifier IRF740 power MOSFETs were used in the inverter. These power MOSFETs have drain-source breakdown voltage $V_{DSS} = 400$ V, the maximum continuous drain current 10 A at the case temperature $T_C = 25°$C and 6 A at $T_C = 100°$C, on-resistance $r_{DSi} = 0.55\ \Omega$, the typical value of the total gate charge $Q_g = 41$ nC, and the maximum value of the gate charge $Q_{g\max} = 60$ nC.

The voltage transfer function of the inverter is

$$|M_I| = \frac{V_{R1\text{rms}}}{V_I} = \frac{38.88}{150} = 0.2592. \quad (47)$$

Let $r = 0.9\ \Omega$. Hence, the efficiency of the inverter at full power is given by

$$\eta_I = \frac{R_i}{R_i + r} = \frac{28.011}{28.011 + 0.9} = 96.89\%. \quad (48)$$

Hence, using (47) and solving (2) for Q_L yields

$$Q_L = \sqrt{\frac{\frac{2\eta_I^2}{\pi^2|M_I|^2} - 1}{\left(\frac{f}{f_0} - \frac{f_0}{f}\right)^2}} = \sqrt{\frac{\frac{2 \times 0.9689^2}{\pi^2 \times 0.2592^2} - 1}{\left(1.15 - \frac{1}{1.15}\right)^2}} = 4.8258. \quad (49)$$

The inductor and capacitor of the series-resonant inverter can be calculated as

$$L = \frac{Q_L(R_i + r)}{2\pi f_0} = \frac{4.8258 \times (28.011 + 0.9)}{2 \times \pi \times 10^5} = 222\ \mu\text{H} \quad (50)$$

and

$$C = \frac{1}{2\pi f_0 Q_L(R_i + r)} = \frac{1}{2 \times \pi \times 10^5 \times 4.8251 \times (28.011 + 0.9)} = 11.41 \text{ nF}. \quad (51)$$

Let $C = 11$ nF. Hence, the characteristic impedance of the resonant circuit is

$$Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{222 \times 10^{-6}}{11 \times 10^{-9}}} = 142.06\ \Omega. \quad (52)$$

The amplitude of the voltage across the resonant capacitor and inductor at the resonant frequency $f = f_0 = 100$ kHz is

$$V_{Cm}(f_0) = V_{Lm}(f_0) = \frac{2V_I Q_{L\max}}{\pi} = \frac{2 \times 150 \times 4.8258}{\pi} = 460.83 \text{ V} \quad (53)$$

and at the resonant frequency $f = f_0 = 115$ kHz is

$$V_{Cm}(f) = V_{Lm}(f_0) = Z_0 I_m = 142.06 \times 1.986 = 282.13 \text{ V}. \quad (54)$$

The ESRs of the resonant capacitor and resonant inductor measured at 100 kHz were $r_L = 0.21\ \Omega$ and $r_C = 0.14\ \Omega$, respectively. The equivalent parasitic resistance r of the inverter is

$$r = r_{DSi} + r_C + r_L = 0.9\ \Omega. \quad (55)$$

The dc input power of the inverter at full load is given by

$$P_I = \frac{P_{Ri}}{\eta_I} = \frac{53.996}{0.9698} = 55.677 \text{ W}. \quad (56)$$

Assuming the peak-to-peak gate-to-source voltage $V_{GSpp} = 14$ V and the total maximum gate charge $Q_{g\max} = 60$ nC, the gate drive power of each inverter MOSFET is

$$P_{Gi} = fQ_{g\max}V_{GSpp} = 115 \times 10^3 \times 60 \times 10^{-9} \times 14 = 96.6 \text{ mW}. \quad (57)$$

The total efficiency of the converter at full load (excluding the drive power of the inverter and rectifier MOSFETs) is given by

$$\eta = \eta_I \times \eta_R = 0.9689 \times 0.926 = 89.7\%. \quad (58)$$

C. Driver

Fig. 6 shows a circuit of a deriver of the MOSFETs. An Unitrode UC2525A IC was used to drive the inverter MOSFETs. It is capable of sourcing and sinking a current in excess of 200 mA. Ferroxcube 1408TS 3C3 ferrite cores were used to make transformers. They were wound with gauge 28 wire at a turns ratio 28 : 28. A 1 μF capacitor was used on the primary side of each transformer to avoid the core saturation due to the dc current flow. The operating frequency was controlled manually by varying the resistance R_T on pin 6. A Unitrode UC3708N dual power driver was used to drive the rectifier MOSFETs. Each output of this buffer can source and sink up to 3 A. The MOSFETs of the synchronous rectifier

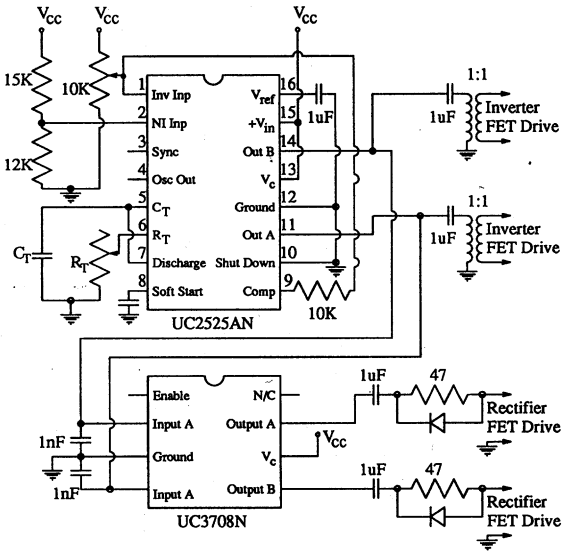

Fig. 6. Driver of MOSFETs in inverter and synchronous rectifier.

should not be allowed to turn on simultaneously because a transformer short circuit will be created. To avoid cross-conduction of the rectifier MOSFETs, a dead time was introduced in the drive gate-to-source voltages. In addition, to avoid a reverse recovery of the MOSFET body diodes, Schottky diodes are connected in parallel with the MOSFETs. Since the Schottky diodes have much lower threshold voltage, the body diodes do not conduct a lot of the current. The dc voltage of both ICs was $V_{CC} = 14$ V and the dc supply current was $I_C = 36$ mA, resulting in a dc power of the driver $P_{CC} = I_C V_{CC} = 0.036 \times 14 = 0.504$ W. Hence, the overall efficiency including the dc power of the driver at full power was

$$\eta_{\text{tot}} = \frac{P_0}{P_I + P_{CC}} = \frac{50}{55.735 + 0.504} = 88.91\%. \quad (59)$$

D. Comparison of Efficiencies of the Diode and Synchronous Rectifiers

Let us consider the efficiency of a rectifier that employs Schottky diodes with the offset voltage $V_F = 0.35$ V and the forward resistance $R_F = 25$ mΩ. All other component values remain the same as in the synchronous rectifier. The efficiency of the diode rectifier is

$$\eta_R = \frac{\eta_{tr}}{1 + \dfrac{V_F}{V_0} + \dfrac{\pi^2 R_F}{8R_{L\min}} + \dfrac{r_{Cr}}{R_{L\min}}\left(\dfrac{\pi^2}{8} - 1\right)}$$

$$= \frac{0.95}{1 + \dfrac{0.35}{5} + \dfrac{\pi^2 \times 0.025}{8 \times 0.5} + \dfrac{0.0053}{0.5}\left(\dfrac{\pi^2}{8} - 1\right)}$$

$$= 0.8376. \quad (60)$$

Thus, the efficiency of the synchronous rectifier is higher than that of the diode rectifier by 8.84%.

IV. EXPERIMENTAL RESULTS

The series-resonant converter designed in Section III was built and tested for a dc input voltage V_I varying from 130 V to 185 V, a dc output voltage of 5 V, and a load resistance ranging from 0.5 to 5.5 Ω. The quality factor of the capacitor was $Q_{Co} = 1/(\omega C r_C) = 1/(2 \times \pi \times 10^5 \times 11 \times 10^{-9} \times 0.14) = 1034$. Ferroxcube A7700 3F3 ferrite pot cores were used for both the inductor (gapped for adjusting inductance) and the transformer (ungapped). In order to reduce the ac resistance due to the skin effect at high-frequencies, gauge 30/30 Litz wire was used to build the resonant inductor whose inductance L was 230 μH. The quality factor of the inductor $Q_{Lo} = \omega L/r_L = 2 \times \pi \times 10^5 \times 230 \times 10^{-6}/0.21 = 688$. The resonant frequency f_0 was 100 kHz. The transformer was wound with AWG 22 solid copper wire on the primary and double strand 20/30 wire on the secondary with a turns ratio of 40 : 5 : 5 = 8 : 1 : 1. The filter capacitor used was a 2200 μF electrolytic capacitor with an equivalent series resistance of $r_{Cr} = 53$ mΩ at $f = 100$ kHz, which kept the output voltage ripple small. Load resistance R_L varied from 0.5 Ω at full load to 5.5 Ω at light load.

The waveforms were observed and the performance characteristics of the converter were measured as functions of the load resistance R_L and the input voltage V_I at $V_0 = 5$ V. The results are shown in Figs. 7–11. Fig. 7(a) shows the waveforms of the drain-to-source voltage and the drain current i_{S2} of the bottom switch S_2 of the inverter and Fig. 7(b) shows the waveforms of the gate-to-source voltage v_{GS4} and the total switch current i_{S4} of switch S_4 in the synchronous rectifier at $V_I = 150$ V, $V_0 = 5$ V, $R_L = 1$ Ω, and $f = 118$ kHz. Note that the duty cycle of the gate-source voltage v_{GS4} of the rectifier MOSFET was less than 50%. Therefore, the conduction angle of the current waveform i_{S4} was less than 180°. The measured and calculated plots of the total efficiency η_{tot} of the converter versus R_L at $V_I = 150$ V and $V_0 = 5$ V are shown in Fig. 8. The measured efficiency increased as the load resistance was increased from $R_{L\min} = 0.5$ Ω to $R_L = 2.5$ Ω and then decreased with increasing load resistance R_L. Discrepancies exist especially at light loads. This can be attributed to the fact that the dc supply power P_{CC} of the MOSFET driver was approximately constant at all loads and was a larger portion of the total power at light loads.

Fig. 9(a) and (b) shows the waveforms of the gate-drive voltage v_{GS4}, the total current of the switch i_{S4}, the MOSFET current i_{DS4}, and the Schottky diode current i_{D4} at full load $R_L = 0.5$ Ω and at light load $R_L = 5.5$ Ω, respectively. It can be seen that the duty

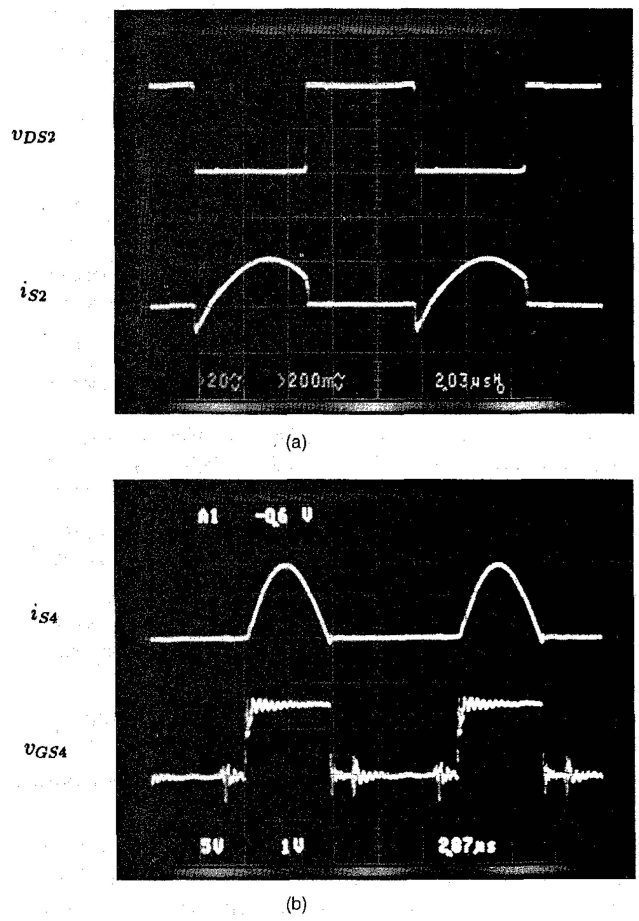

Fig. 7. Current and voltage waveforms of bottom switch S_2 of inverter and switch S_4 of rectifier at $V_I = 150$ V, $V_0 = 5$ V, $R_L = 1\ \Omega$ (50% of full load), and $f = 118$ kHz. (a) Waveforms of v_{DS2} and i_{S2}. Horizontal scale: 20 μs/div. Vertical scale: 75 V/div. and 1 A/div. (b) Waveforms of i_{S4} and v_{GS4}. Horizontal scale: 20 μs/div. Vertical scale: 5 A/div. and 5 V/div.

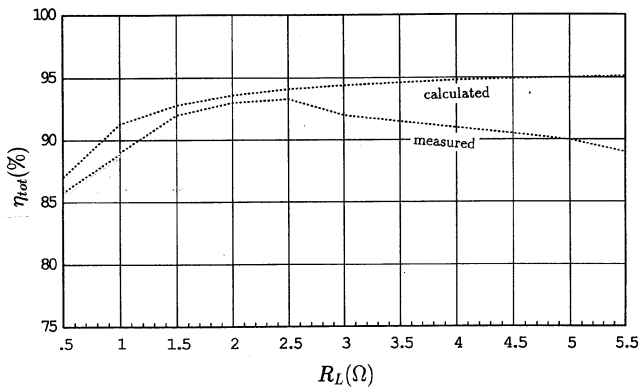

Fig. 8. Total converter efficiency η_{tot} versus load resistance R_L at $V_I = 150$ V and $V_0 = 5$ V.

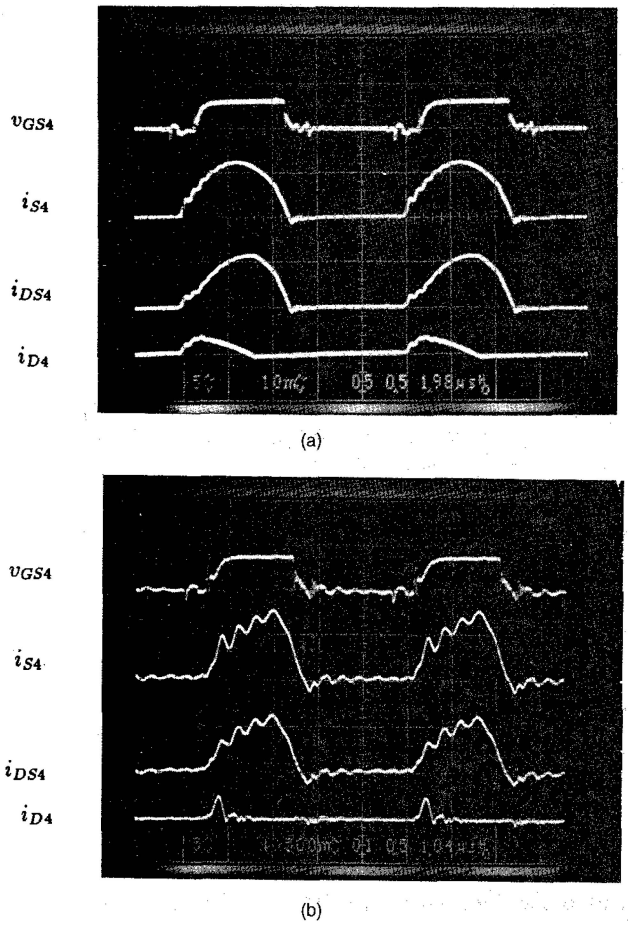

Fig. 9. Waveforms of gate-drive voltage v_{GS4}, total switch current i_{S4}, MOSFET current i_{DS4}, and Schottky diode current i_{D4}. (a) At full load $R_L = 0.5\ \Omega$. Horizontal scale: 20 μs/div. Vertical scale: 10 V/div. and 10 A/div. (b) At light load $R_L = 5.5\ \Omega$. Horizontal scale: 20 μs/div. Vertical scale: 10 V/div. and 1 A/div.

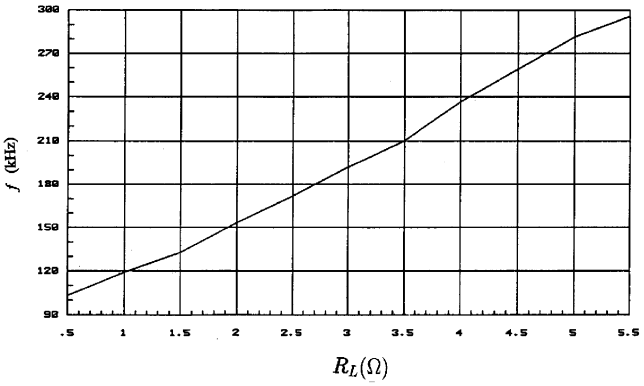

Fig. 10. Switching frequency f versus load resistance R_L at $V_I = 150$ V and $V_0 = 5$ V.

cycle of v_{GS4} was less than 50%, causing the Schottky diode to turn on at the beginning of each half of the cycle. At $R_{L\max} = 5.5\ \Omega$, $Q_{L\min} = 0.464$ and therefore the current i_R through the resonant circuit was not a pure sine wave. The power of both the fundamental component and higher harmonics is transferred from the inverter to the rectifier, resulting in an efficiency that differs from the calculated efficiency.

The measured plot of the switching frequency f versus the load resistance R_L at $V_I = 150$ V and $V_0 = 5$ V is shown in Fig. 10. As the load resistance R_L was increased from 0.5 to 5.5 Ω, the switching frequency was increased from 105 kHz to 291 kHz

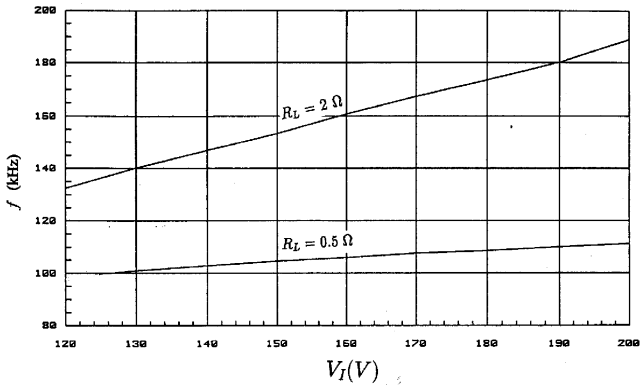

Fig. 11. Switching frequency f versus dc input voltage V_I at $V_0 = 5$ V and $R_L = 0.5$ and 2 Ω.

to maintain a constant output voltage V_0 of 5 V. Fig. 11 shows the plot of the switching frequency f versus the dc input voltage V_I at $V_0 = 5$ V and for $R_L = 0.5$ and 2 Ω. When the dc input voltage V_I was increased from 120 to 200 V, the switching frequency was increased from 98 kHz to 112 kHz at $R_L = 0.5$ Ω, and from 133 to 189 kHz at $R_L = 2$ Ω.

V. CONCLUSIONS

An analysis of the Class-D series-resonant dc-dc converter with a synchronous rectifier was presented. The converter had the following performance characteristics. The efficiency of the synchronous rectifier was 8% higher than that with Schottky diodes. Since the current waveforms of the rectifier MOSFETs are half-sine waves, the rectifier MOSFETs turn on and off at low di/dt, thereby reducing noise. Normally, the converter is designed for full power. The accuracy of the analysis based on the fundamental-frequency component is good at full power. MOSFETs with even lower on-resistance are now available, which will help improve the efficiency of the synchronous rectifiers. For example, Motorola MTP75N03HDL power MOSFETs have a typical on-resistance of 6 mΩ. A full-bridge Class D series-resonant inverter [7] can be used at high power levels.

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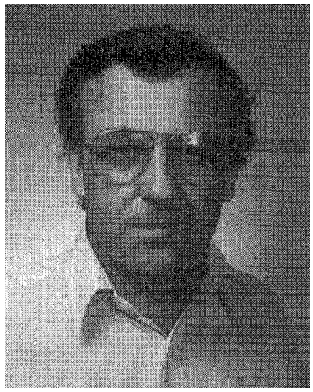

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Chuyun Wu Photograph and biography not available.

LLC synchronous rectification made easy, robust and more efficient

Fan Wang, Systems Engineer, and Brent McDonald, Systems Engineering Manager, Texas Instruments - May 25, 2015

The green energy movement has brought about huge increases in efficiency to commercial AC/DC and DC/DC power supplies. The 80 Plus requirements stipulate that titanium-class power supplies must have a 97% efficiency from input to output. The results are that power supplies run cooler and more reliably, and save significant utility costs. Requirements like these are becoming commonplace. Anyone who has ever attempted to design one of these power supplies knows that synchronous rectification is a must.

This article explores a new synchronous rectification control method that leverages the intelligence present in modern digital controllers. This method has a synchronous rectification technique that seeks to minimize the dead time while constantly on the lookout for dead times that might present a hazard to the system. Since this method is inherently intelligent, it makes the design engineer's job easier. Designers no longer have to perform a worst-case analysis to precisely predict all of the possible dead time conditions and, subsequently, include margin in their dead time settings for those conditions. The end result is faster time-to-market, better robustness and, most importantly, higher efficiency.

Introduction

Nowadays, a resonant converter that uses two inductors (LL) and a capacitor (C), better known as LLC resonant converters are becoming popular for its ability to achieve high efficiency. This topology has been widely used in applications such as enterprise servers and telecom DC/DC converters. For high-efficiency operation, the secondary side rectification diodes are replaced with synchronous MOSFETs to reduce the conduction loss. However, controlling synchronous rectifiers (SR) is non-trivial – both the most optimized turn-on and turn-off edges should be right at the SR current zero crossing point, which moves depending on input voltage and load current. Turning-on/off too early or too late results in efficiency loss, negative current, or high drain-to-source stress. A lot of research and commercial products are focused on providing a good SR control method for LLC converters [1]. **Figure 1** shows a half-bridge LLC resonant converter with SR MOSFETs.

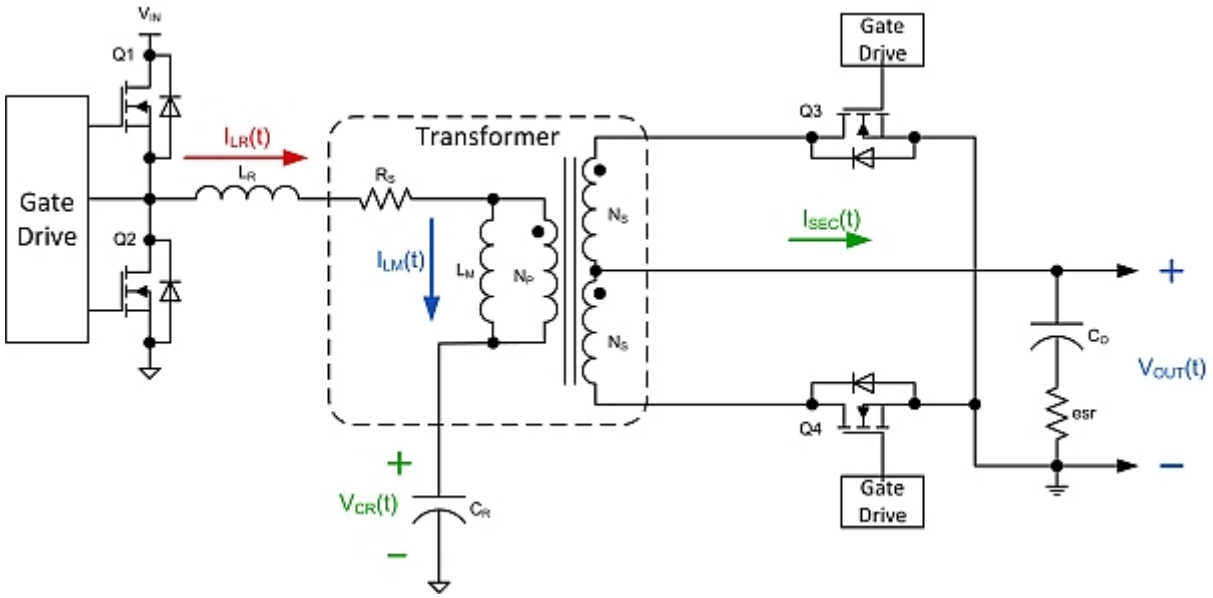

Figure 1: Half-bridge LLC resonant converter with SR MOSFETs

State-of-the-art LLC resonant converter SR driving strategies fall in two categories: 1) MOSFET turn-on resistance (Rdson) voltage drop sensing-based method; and 2) SR pulse width clamp method, which usually is used in digitally-controlled LLC converters.

In the first method, the MOSFET is turned on after a large negative voltage on MOSFET body diode is detected on the MOSFET drain terminal. The MOSFET is turned off when the voltage drop on the MOSFET Rdson goes above a small negative voltage. Some commercial products in this category try to vary the gate drive voltage to enable fast turning off. Turn-on and turn-off blanking times are required in this method. This method doesn't require a gate driver input and works for both analog and digital solutions. One of the drawbacks of this method is that the voltage drop on Rdson is often too small to detect due to low resistance, and varies with layout parasitic and the type of MOSFETs being used. Also, in high current applications where there are several MOSFETs in parallel, the Rdson is so small that the MOSFETs are turned off when the current is still large.

In the second method, the SR gate drive signal comes from the digital controller. The turn-on edge is usually fixed. The turn-off edge changes based on operation modes. At above or equal to resonant frequency, the turn-off edge varies, based on the switching frequency and keeps a fixed dead time relative to the primary side gate drive signal. At below resonant frequency, the SR pulse width is clamped to half of the resonant period minus some dead time. This method is easy to implement with digital power controllers. The drawback is that it requires resonant tank information for programming the pulse width clamp value and, thus, requires calibration. The calibration process often takes a long time in the production line, which makes production costs higher.

Table 1 LLC SR control methods

Table 1 is a summary of the two categories of state-of-the-art LLC SR control methods.

Method	Advantages	Disadvantages
Rdson voltage drop sensing	• Does not require gate drive signal input	• Not suitable for high current applications with several MOSFETs in parallel
		• Layout parasitic concern
SR pulse width clamp	• Digital controller friendly	• Requires calibration in production
	• Simplified system configuration	• No SR turn on edge optimization

Table 1: State-of-the-art LLC SR control methods

A digital adaptive driving scheme for LLC SRs is discussed in reference 1. However, in this work, the SR turn-on edge is fixed and not optimized. It cannot handle the turn-on edge phase-shift at high switching frequencies. To better handle transient response, a clamp is implemented on the SR pulse width. The maximum SR turn-on time is delta T longer than the primary side pulse width, where delta T is a pre-programmed value.

However, this results in a transient problem: the SR turn-on edge is still the same with primary-side gate drive signals, but the turned-off edge is after the primary side. In this way, the SR pulse width will be longer than the primary side gate drive pulse width. This may result in a shoot through or drain-to-source overstress condition. Another issue is that there is no special detection region when transient happens. The SR on-time may adjust toward the wrong direction due to errors in body diode conduction sensing. We will talk about that a little more in a bit.

To overcome the previously mentioned drawbacks of the existing solutions, a novel body diode conduction time (DCT) sensing-based adaptive SR control method is proposed. The drain-to-source voltage on the MOSFET Rdson can vary with package, layout parasitic, and load current. But when the body diode conducts the voltage drop on the body diode it is relatively constant, regardless of parasitic and load conditions. The DCT-sensing method senses the body diode conduction time of the current cycle and adjusts the SR on-time for the next cycle. A configurable body diode conduction detection window is introduced to determine whether the SR on-time is too long or too short. The body diode conduction time can be regulated to a desired length. There is also a negative current prevention mechanism to improve system robustness. Compared with conventional solutions, the benefits of the proposed method are:

- Achieve high efficiency in a wider load range
- Automatically compensate for power stage component parameter variations, no calibration required
- Large signal detection, easy layout, no parasitic concern
- No minimum on/off time or blanking time constraints
- Better noise immunity compared with competitive solutions
- Good performance for both low-current and high-current applications with MOSFETs in parallel

Body diode conduction sensing-based adaptive SR control

Body diode conduction sensing-based adaptive SR control

Desired SR operation

The desired SR operation is different in a variety of LLC operation modes. As shown in **Figure 2a–2b**, at below or equal to resonant frequency, the SR turn-on edge follows closely to the primary side turn-on edge. The SR turn-off edge is then determined by approximately half of the resonant period. At above resonant frequency (**Figure 2c**), the SR turn-on edge is delayed versus the primary side turn-off edge. The SR pulse width is always equal to approximately half of the switching period. Therefore, the turn-off edge of the SR may go past that of the primary side.

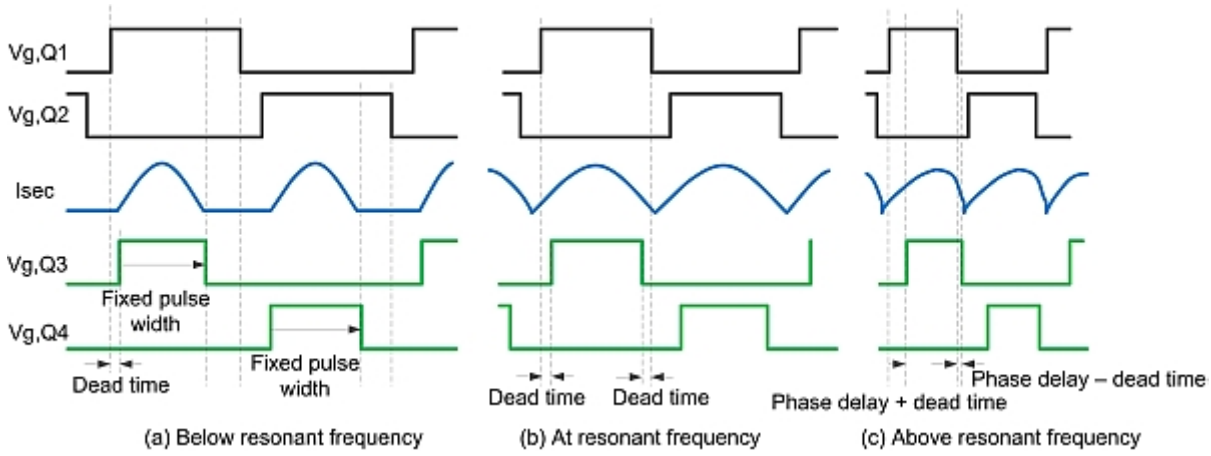

Figure 2: Desired synchronous rectifier operations in a half-bridge LLC converter

Body diode conduction detection

The body diode conduction detector is a comparator with a –150 mV threshold. When body diode conducts, the drain-to-source voltage of the MOSFET, it is usually around -0.7V. This is typically below the threshold, and the comparator outputs are low. Otherwise, the comparator output is high. The body diode cannot be conducting when SR is on. It only happens when SR is off. To avoid any false noise trip on the comparator when SR is on, the comparator output is always pulled high when the SR gate drive signal is high.

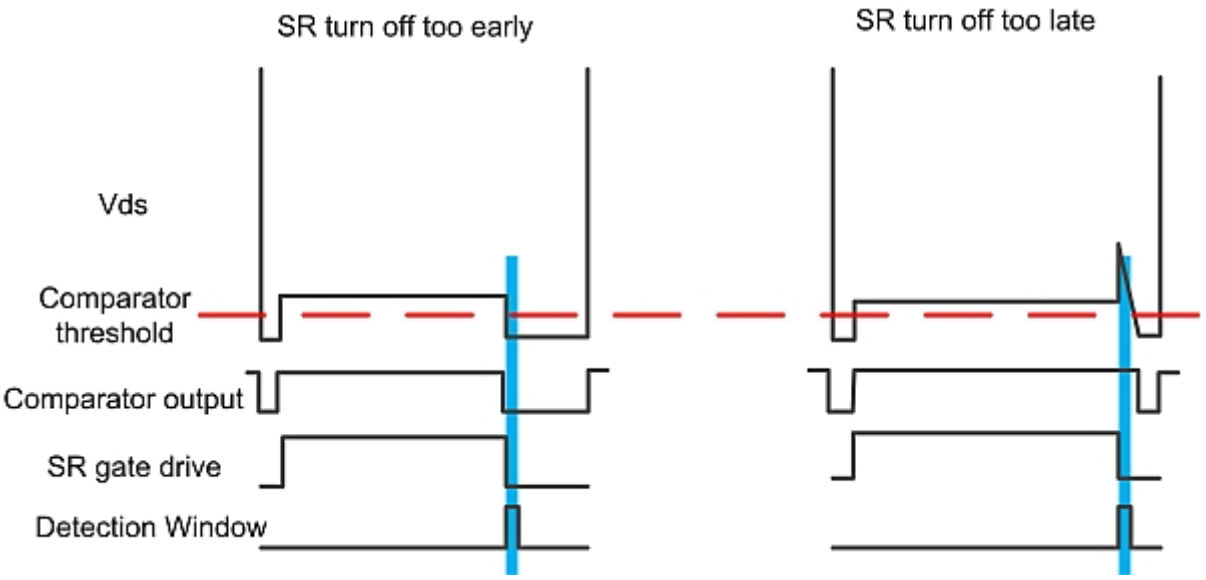

Figure 3: Body diode conduction detection

Figure 3 shows two different cases for how the body diode of the SR MOSFET conducts: a) MOSFET turns off too early, positive current flows; body diode conducts right after SR turns off; b) MOSFET turns off too late, negative current flows; drain-to-source voltage shoots up first, then body diode conducts.

In both cases, the SR on-time should be adjusted in different directions. The digital controller must be able to tell them apart to avoid adjusting in the wrong direction. A detection window is generated for this purpose. The detection window starts right after the SR gate drive turns off. The length of the detection window can be configured based on the delay in the circuit.

If during this window the detected comparator is low, this indicates that SR is turning off too early. If during the detection window no comparator low is detected, this indicates that the SR is turning off too late. Based on this information, the digital controller adjusts the SR on-time of the next switching cycle.

Turn-on and turn-off edge optimization

In the proposed method, the digital controller outputs SR gate drive signals based on the SR clamp method mentioned earlier. This signal, called IN, has a rising edge and a fixed dead time with the primary side gate drive signal. The turn-off edge of IN moves together with the primary side gate drive signal at equal to or above resonant frequency. At lower than resonant frequency, the falling edge of IN is fixed to generate a fixed SR pulse width.

The output of the diode conduction detection comparator is called DCT, which is low when the body

diode conducts.

The actual SR gate signal is called OUT, which can be considered as the SR gate driver IC output.

The rising edge of the OUT signal is determined by both the digital controller output IN, and the DCT comparator output DCT. The OUT signal can only be high when IN is high. If at IN rising edge, DCT is already low, turn on the gate driver output immediately. If at IN rising edge, and DCT is still high, turn on the gate driver output as soon as the DCT falling edge is received.

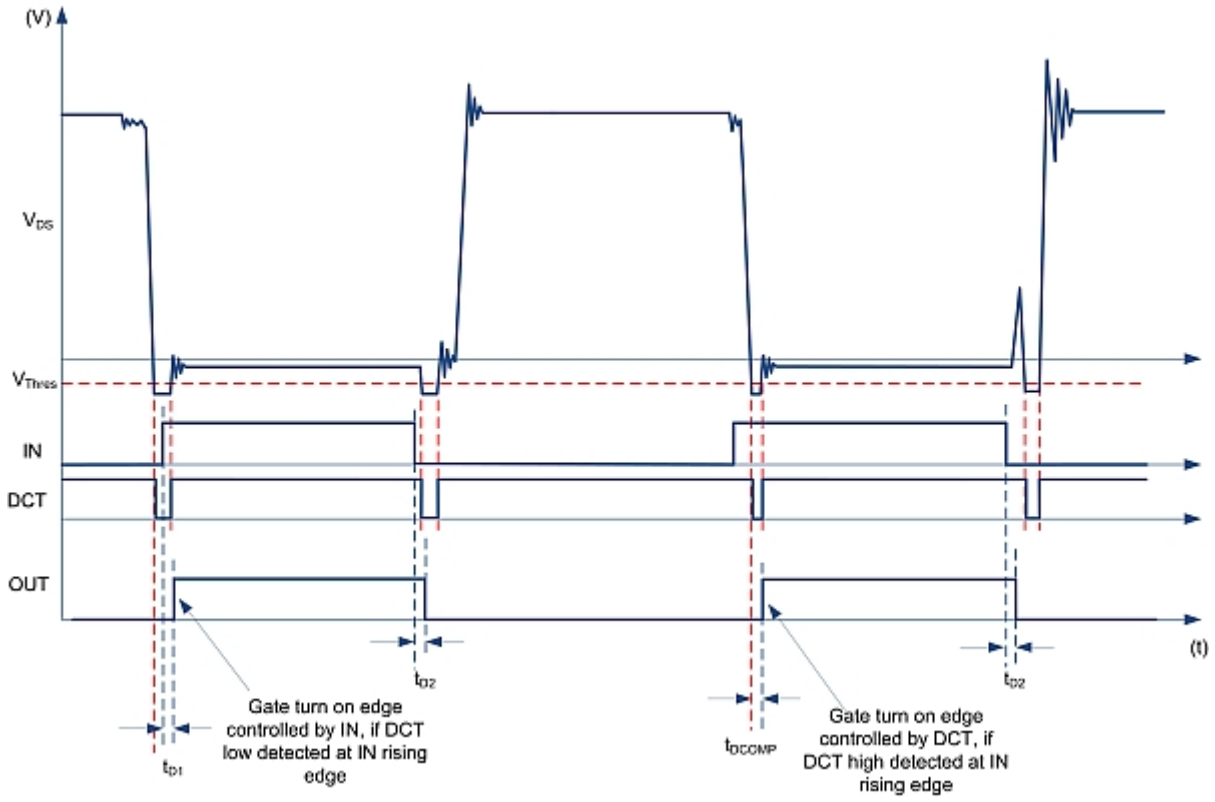

Figure 4: Turn-on edge optimization

On the SR gate driver and DCT detector side, the falling edge of OUT is determined by IN only. The gate is turned off immediately at the IN falling edge. Optimizing the SR turn-off edge is done by the digital controller. The digital controller uses a high-resolution digital counter to determine how long DCT is low during the detection window. If during the detection window, the DCT low time is too short, the falling edge of IN will be moved backward in the next cycle. If during the detection window, DCT low time is too long, the falling edge of IN will be moved forward in the next cycle.

Figure 4 shows the critical signals mentioned in this section.

Negative current prevention

When the SR pulse is on for too long (**Figure 5**), the drain-to-source voltage shoots up. The upper waveform shows the SR current. The lower waveform shows the SR drain-to-source voltage. The black segment is when SR is on, the current keeps dropping and goes negative. The drain-to-source voltage keeps a low voltage close to 0V. The red section shows that when SR is turned off, the negative current has to reset. This causes the capacitance across the drain and source terminal to charge up, and the drain-to-source voltage goes up. The green section shows that when the negative current reset process is completed, the body diode of the MOSFET conducts again briefly.

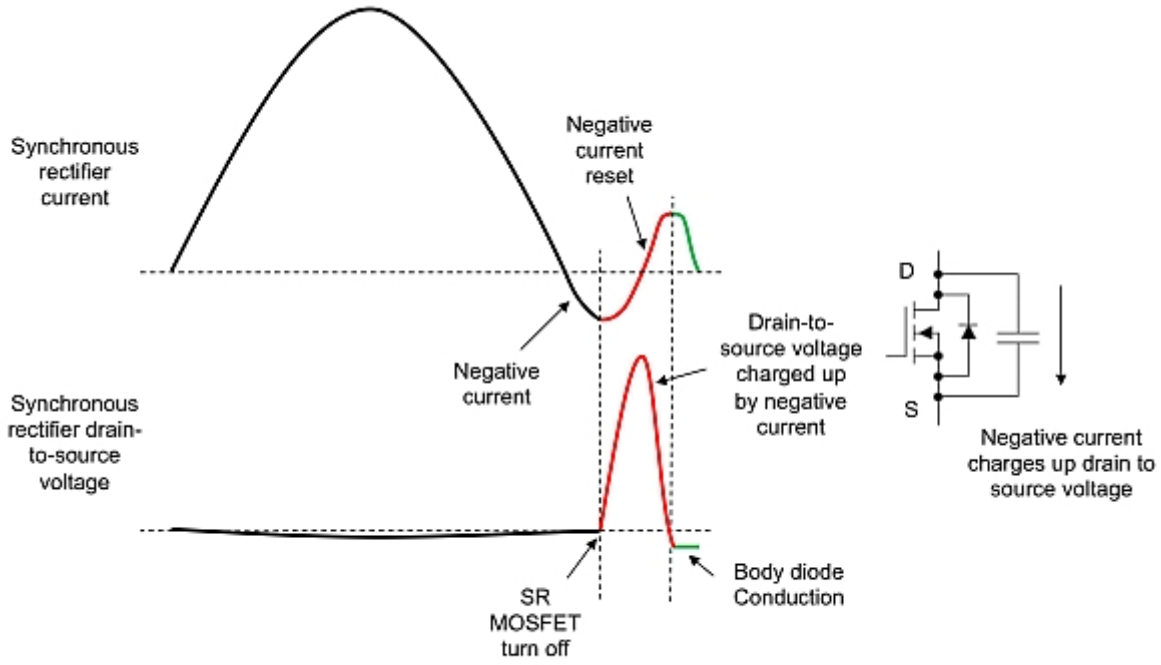

Figure 5: LLC converter SR drain-to-source voltage shoot up when there is negative current flow

To detect negative current, the same detection window and body diode conduction detector described earlier can be used. When there is no body diode conduction during the detection window, negative current may have occurred and the digital controller takes an action to protect the system from damage.

Hardware implementation

Hardware implementation

To prove the proposed method, a digital controller is implemented in silicon to control a 360W LLC resonant converter. A gate driver IC with the DCT detector is developed as well.

Figure 6 shows how the DCT is measured and how the digital controller takes action to adjust the SR on time. This figure shows that a DCT detection window is determined by a DCT blanking time register and a DCT detection window length register.

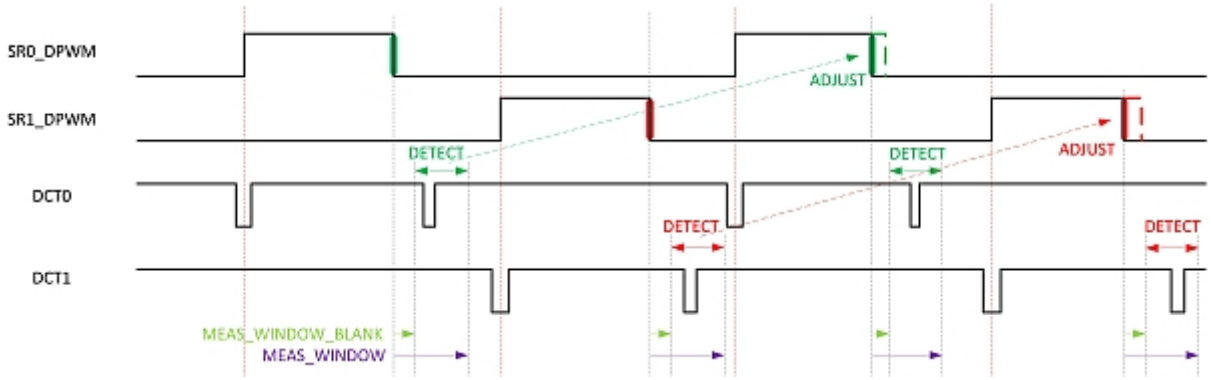

Figure 6: Hardware implementation – digital controller

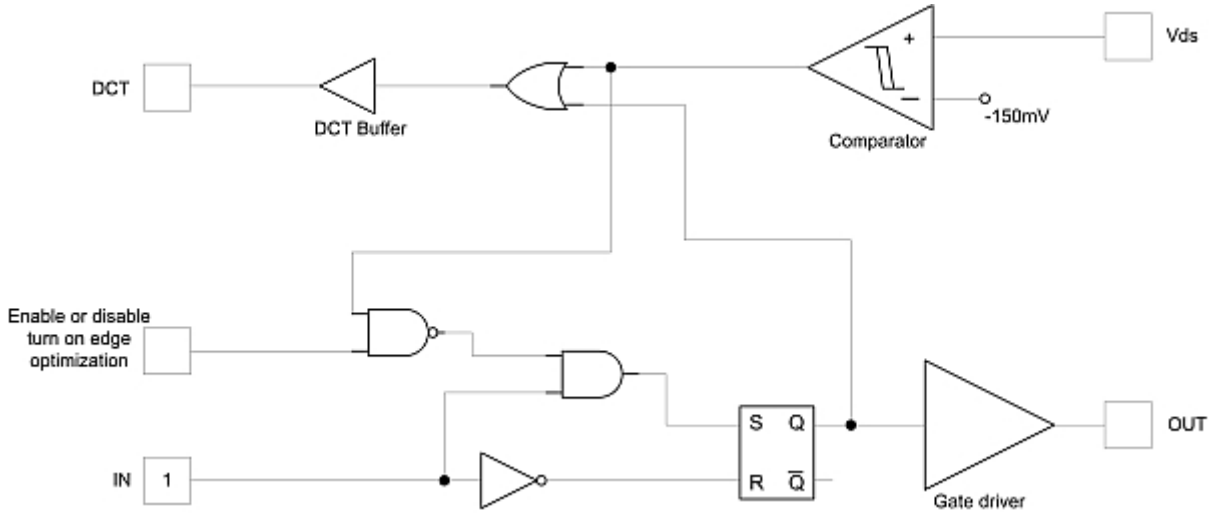

Figure 7: Hardware implementation – SR gate driver and the DCT detector

The DCT signal is only detected during the narrow detection window (**Figure** 7). The signal outside of the detection window is ignored. Therefore, good noise immunity can be achieved comparing with the conventional method mentioned in the first section.

In **Figure 7**, the system block diagram of the SR gate driver together with the DCT detector is illustrated. As can be seen, the turn-on edge optimization can be implemented in a few basic digital building blocks.

Experimental results

Turn-on and turn-off edge optimization

Figure 8 shows the turn-off edge optimization waveforms. The upper left image shows that the SR on-time is too long. The lower left figure shows that the SR on-time is too short. After optimization, both conditions get corrected and a very small body diode conduction time (control target) is maintained.

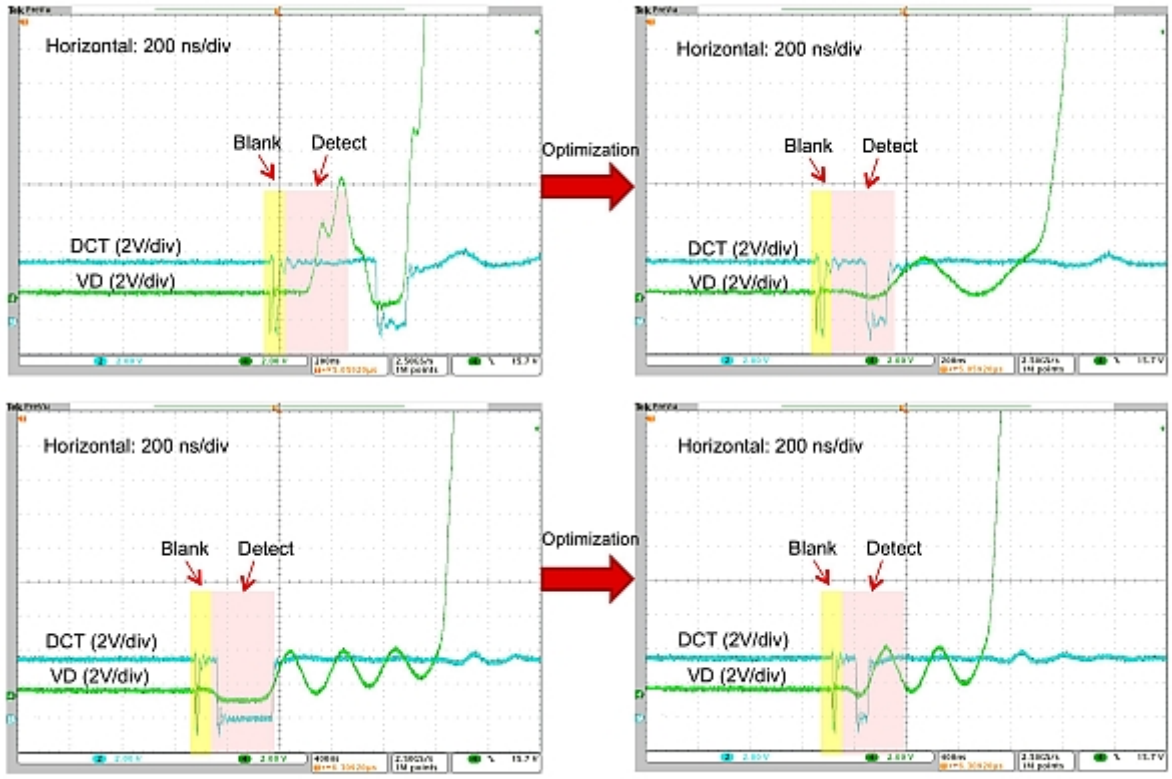

Figure 8: Turn-off edge optimization

Figure 9 shows the turn-on edge optimization waveforms. The upper left figure shows when the SR is turned on too late. The lower left figure shows when the SR is turned on too early. After optimization, both conditions are corrected. A very small dead time can be maintained at the gate driver turn-on edge.

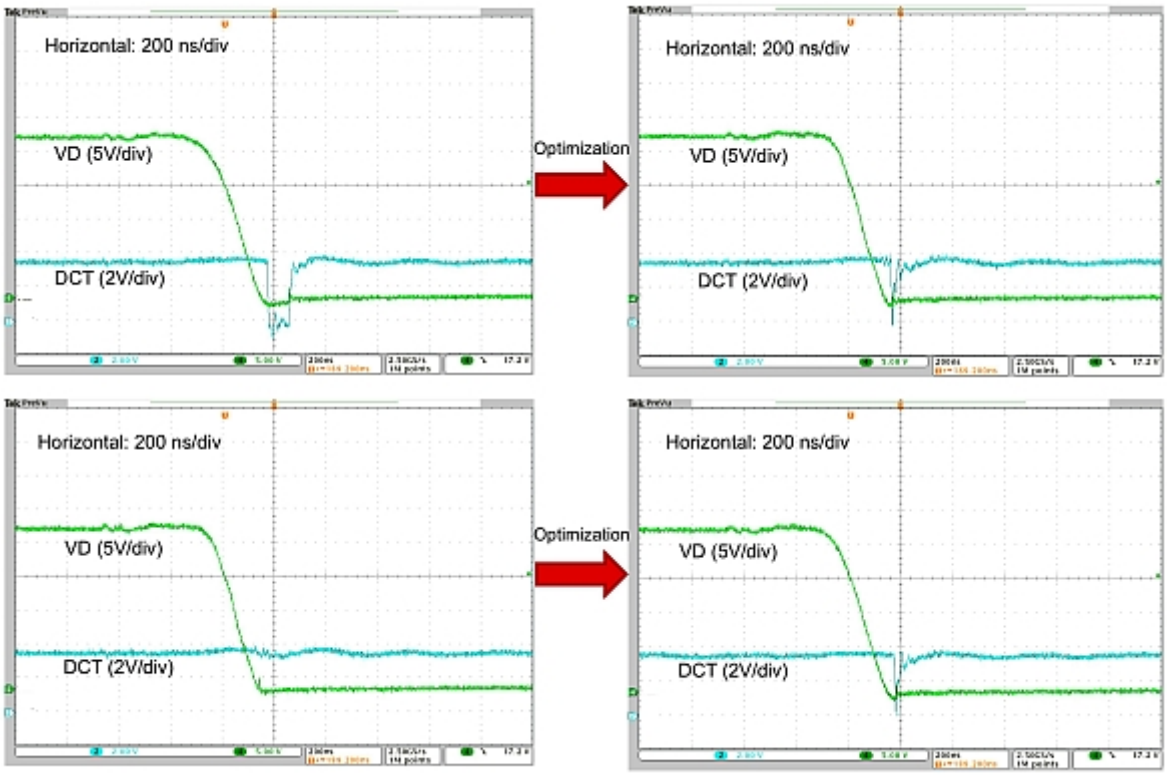

Figure 9: Turn-on edge optimization

Efficiency improvement

Compared with conventional digital control, the proposed method can improve the system efficiency by up to 0.8%. The top diagram in **Figure 10** shows efficiency improvements in different input voltages. At 340V input, the efficiency improvement is the most significant. This is because in 340V, the SR clamp method no longer works well, and large body diode conduction time exists. The proposed auto-tune method benefits the most at these points. The bottom diagram in **Figure 10** shows three test conditions, all with 380V input voltage. This method helps more when the resonant tank error goes bigger.

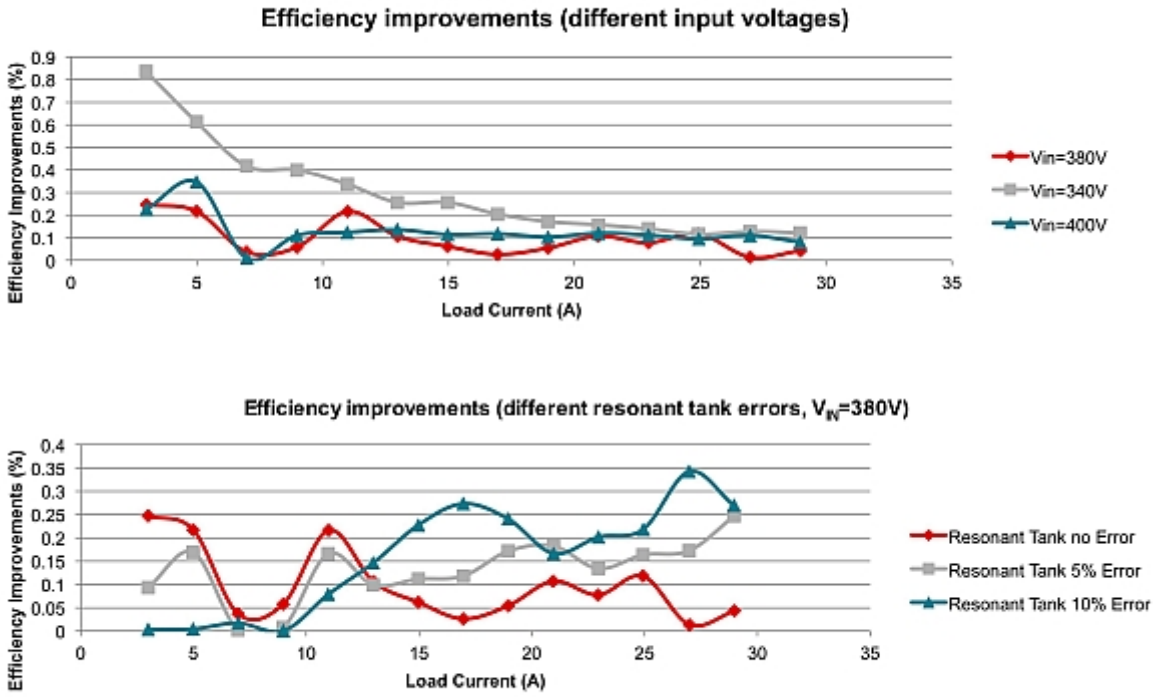

Figure 10: Efficiency improvements

Conclusion

The proposed adaptive synchronous rectification method overcomes the drawbacks of various conventional analog and digital SR control methods, resulting in higher system efficiency and improved robustness. With body diode conduction sensing, both the turn-on edge and turn-off edge of the SRs are optimized. Compared to the Rdson sensing method, the proposed method senses a large signal that doesn't change much with layout and load current. This makes the hardware design much easier. Compared with the SR pulse width clamp method, the proposed method eliminates the need of resonant tank calibration in production. Examples of devices with this silicon implementation method are the digital power controller UCD3138A and the companion SR gate driver UCD7138.

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2. UCD3138A datasheet
3. UCD7138 datasheet

Open Loop Synchronous Rectifier Driver for LLC Resonant Converter

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***Abstract* — Synchronous rectifier (SR) is widely used in LLC resonant converter to reduce the conduction loss. Due to different operation modes, the SR control is complicated and increases system cost. In this paper, based on the observation on LLC diode conduction time, an open-loop fixed-on-time SR driving method is proposed. The optimal on-time is used to control the SR to simplify the implementation in different operation mode and reduce the system cost while maintains large efficiency improvement. The total efficiency of LLC resonant converter with SR driven by the proposed scheme is proved to increase by 2% under different load conditions with minimum system cost.**

***Index Terms* — Synchronous rectifier driver, LLC resonant converter application, efficiency, fixed time, primary side gate drive, low cost, different load conditions.**

I. INTRODUCTION

The pursuit of higher efficiency and power density in DC/DC converters has pushed power electronic devices to their maximum capable switching frequency. Under such circumstances, LLC resonant converter becomes very popular due to its potential in low power loss with high switching frequency [2]. The topology (shown in Figure 1.) has been widely adopted in applications such as digital TV, PC power and server powers. The zero-voltage-switching (ZVS) for primary side switching devices and zero-current-switching (ZCS) for secondary side rectifiers provide the benefits of less switching loss thus improve the converter efficiency and power density in the meantime [1, 2, 3].

Control of the secondary synchronous rectifier (SR) is one of the design challenges for LLC resonant converter. A lot of research efforts have been focused on this area. For example, Figure 2(a) shows the idea of sensing the SR current with current transformer, then initiating the SR gate drive with emergence of diode current signal, is limited by

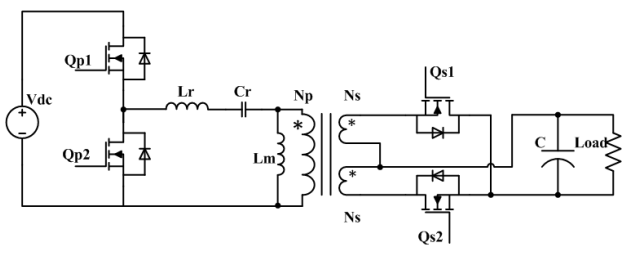


Figure 1. LLC resonant converter with SR on secondary side.

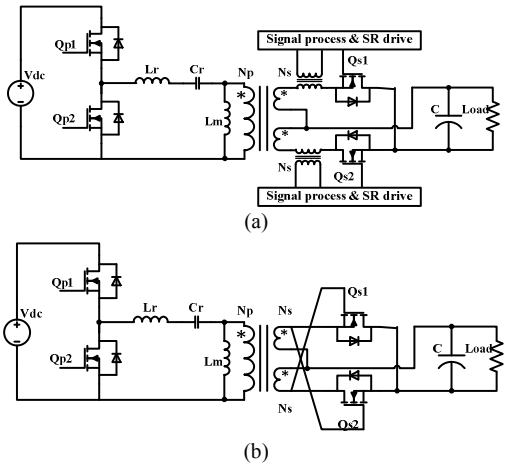


Figure 2. (a) Example of resonant converter with current-driven SR; (b) Example of self-driven series-parallel resonant converter.

the volume of large current transformer for high power applications [3, 7]. While in Figure 2 (b), transformer secondary side voltage is used to drive the SR directly. However, the driving method is not optimal due to sinusoidal voltage waveform induced [3-6]. Currently, the most adopted solution is to measure the SR drain to source voltage and determine the timing for turning ON and OFF the devices.

There are many commercially available chips for secondary SR drive application, such as: Texas Instruments UCC24610, STMicroelectronics SRK2000, Fairchild FAN6208, etc. However, because the signal of V_{ds} reaching negative threshold is used to trigger SR, the control method limits the $R_{ds(on)}$ of SR. Furthermore, this control method is largely affected by the SR parasitic inductors and the system cost is also quite high.

II. PROPOSED FIXED-ON-TIME SR DRIVE

The idea of using primary side gate drive as secondary trigger signal might draw some attention. As could be observed in Figure 3, which shows three cases of different switching frequencies vs. resonant frequencies, primary side gate drive may not always be utilized to drive secondary side SR.

In Figure 3 (a) and (b), when the switching frequency is equal or higher than the resonant frequency, the primary side gate drive could be used since the current on diode is not reaching negative on the primary side gate drive signal edge

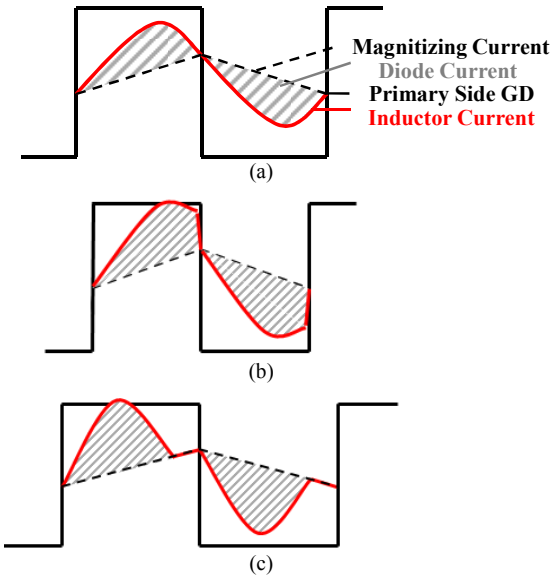


Figure 3. Secondary side diode current waveform vs. primary side gate drive: (a) normal load, (b) light load, (c) heavy load.

and full percentage of diode conduction loss could be saved under such condition.

However, in the case of switching frequency below resonant frequency, the diode current reaches zero before gate drive reverses. If primary side gate drive is applied in this circuit, current on secondary side SR will backflow causing energy transferring backward to primary side. Since the converter is designed to be power unidirectional, this situation might cause overheat in the transformer or even other disastrous situations.

Figure 4 shows diode on-time measurements under different line and load situations with Texas Instruments UCC25600EVM (power rating 300 W, input 390 V, output 12 V) [8]. The diode conduction time varies with different load conditions. In order to develop a feasible, easy, efficient and inexpensive way to drive the SR, the idea of choosing a fixed on-time gate drive for secondary SR under normal to heavy load conditions while directly applying primary side

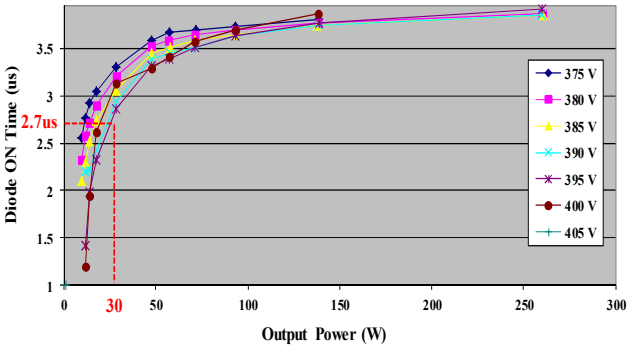


Figure 4. Diode ON time measurement under different input voltages with Texas Instruments UCC25600EVM.

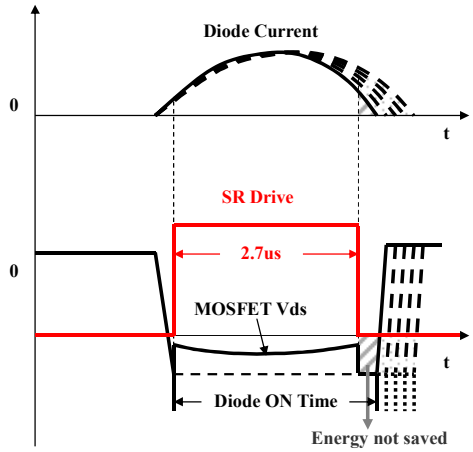


Figure 5. SR drive vs. different current waveform.

gate drive under light load condition was proposed.

The principle could be illustrated in Figure 5. By fixing the SR ON time, certain amount of diode conduction loss would be saved while the rest of conduction loss sacrificed as marked in grey shadow in the figure. Under statistics shown in Figure 4., most of the conduction loss could be saved by choosing the fixed on-time of 2.7 us.

Further conduction loss calculation estimation under different SR on-time with input voltage of 375 V and load of 144 W shown in Figure 6. reveals that the converter's total conduction loss is 5.17 W by using diode. The conduction loss drops to 0.32 W if SR ideally replaces the diodes through conduction period. However, with SR on-time of 2.7 us, the loss reduces to 1.2 W, which is about 80% conduction loss reduction.

Although the SR controller might further reduce the conduction loss by keep SR conduction time longer, there are a few difficulties and actual results might be worse: the SR control adds the system cost; due to the LLC operation mode, before SR turns off, the di/dt generates offset voltage on SR parasitic inductor and cause SR to pre-maturely turn off; the lowest conduction loss SR might not be used because

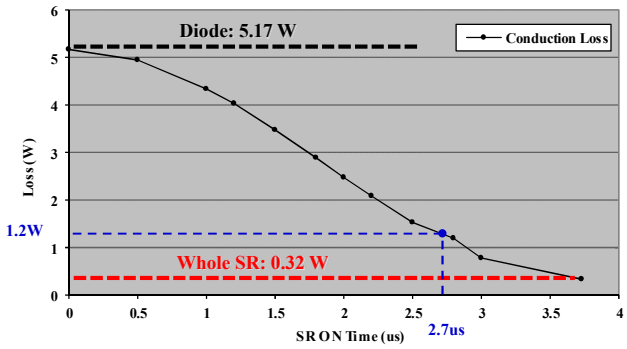


Figure 6. Estimated conduction loss with different SR ON time under input voltage 375V & load 144W.

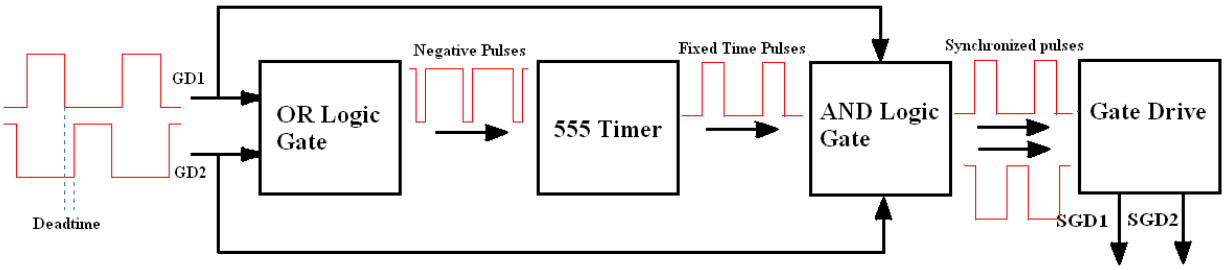


Figure 7. Logic relationship between primary side gate drive and secondary gate drive.

of early turn off at the fixed threshold. For most of the time, the SR controller might not get as much conduction loss reduction as wished.

Based on the proposed control method, the on-time of the SR is fixed for all the line and load conditions when the switching frequency is equal or below the resonant frequency. When the switching frequency is higher than the resonant frequency, the SR on-time is limited by primary side switch on-time. This way, the SR control is completely open loop and operating normally amount different line and load conditions, even during transient.

Figure 7 shows the detailed SR gate drive single generation implementation scheme based on primary side gate signals. By OR logic operation of primary side gate drive, the gate driver turn-on edges are extracted and used to excite the 555 timer.

After the fixed 2.7 us on-time generated, it is processed through AND logic gate to ensure proper operation under different load conditions. The output signals are converted to gate drive signals to control SR. The primary side gate signal automatically limits the maximum on–time of SR, allows proper operation among different line and load conditions.

III. Experimental Result and Efficiency Comparison

The experiment verification setup is implemented on Texas Instruments UCC25600EVM [8]. Hardware picture is shown in Figure 8. Right side on the breadboard is the gate drive circuit, and the left green PCB is the evaluation board with two MOSFETs with small passive heatsinks paralleled to the diode rectifier on the secondary side of LLC resonant converter.

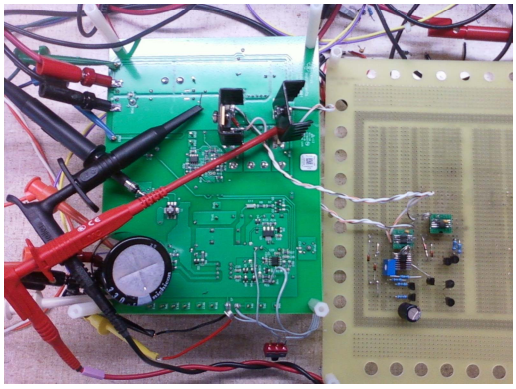


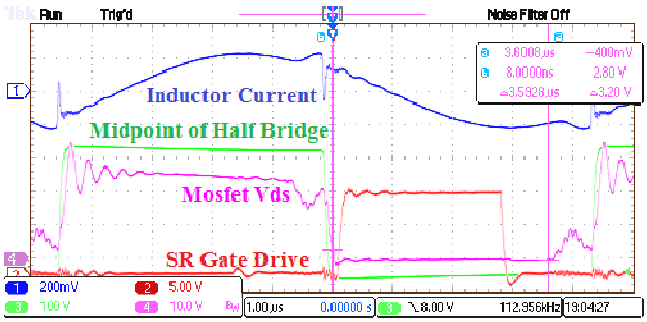
Figure 8. Hardware of proposed control scheme with LLC converter evaluation board.

Figure 9 (a) and (b) show the converter waveforms with SR under heavy and light load conditions.

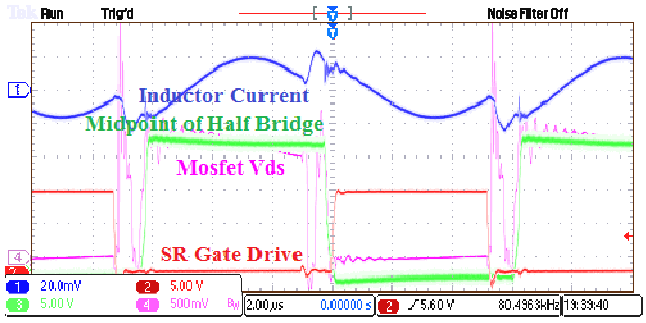
As can be observed in (a), during heavy load condition, SR gate drive covers most of the SR conduction time and raises the efficiency. Though part of the diode conduction time is not covered, that part of conduction loss is ignored.

In (b) light load condition, the diode conduction time is approaching the fixed time of 2.7 us. The transient of SR switching to diode conduction induces large voltage spikes due to parasitic inductance effect.

As revealed in Figure 10, the efficiency is increased by 2% using SR. Further conduction loss improvement can be achieved by using lower conduction loss SRs, because the conduction time won't affected by the MOSFET on resistance.



(a)



(b)

Figure 9. Different load conditions with SR gate drive (a) heavy load, (b) light load.

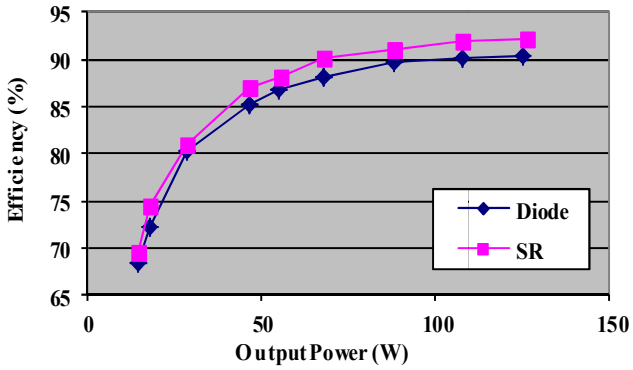


Figure 10. Efficiency comparison under input 375V and various load conditions.

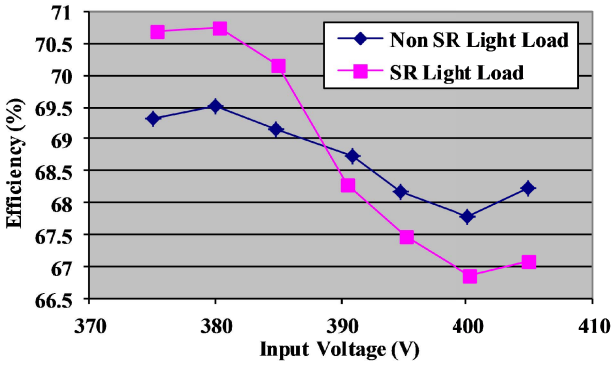


Figure 11. Light load efficiency comparison under 14.4W output.

The statistics result shown in Figure 11 tells that the efficiency of light load with SR could be lower than converter without SR. That is because under light load condition, the switching related loss increases and causes the efficiency to drop dramatically. The SR can be disabled during light load condition and this negative effect can be eliminated.

IV. Conclusion

This paper proposed a fixed on-time SR driver used for LLC resonant converter applications. The design procedure is introduced as: collecting diode conduction time; choose the best SR on time for normal and heavy load; implement the fixed time control scheme and save efficiency.

Instead of "actively" acquiring the diode conduction time used in most adopted applications, the proposed method "passively" sets the SR on time and saves most of the diode conduction loss with extremely low cost and simple control. It works well with different load conditions and especially provides a cost effective solution for cost sensitive applications.

Acknowledgement

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AN-6208

Secondary-Side Synchronous Rectifier (SR) for LLC Resonant Converter Using FAN6208

Introduction

The LLC resonant converter has drawn a lot of attention recently due to its advantages over a conventional series resonant converter and parallel resonant converter: narrow frequency variation over wide load, input variation, and Zero Voltage Switching (ZVS) for the entire load range.

In an LLC resonant converter, rectifier diodes are typically used to obtain DC output voltage from the transformer secondary winding. The conduction loss of diode rectifier contributes significantly to the overall power losses in an LLC resonant converter; especially in low output voltage applications. The conduction loss of a rectifier is proportional to the product of its forward-voltage drop and the forward conduction current. Using synchronous rectification (SR) where the rectifier diode is replaced by MOSFET with a small on resistance (R_{DSON}), the forward-voltage drop of a synchronous rectifier can be lower than that of a diode rectifier and, consequently, the rectifier conduction loss can be reduced.

FAN6208 is a synchronous rectification controller for isolated LLC or LC resonant converters that can drive two individual SR MOSFETs emulating the behavior of rectifier diodes. FAN6208 measures the SR conduction time of each switching cycle by monitoring the drain-to-source voltage of each SR and determines the optimal timing of SR gate drive. FAN6208 also uses the change of opto-coupler diode current to adaptively shrink the duration of SR gate drive signals during load transients to prevent shoot-through. To improve light-load efficiency, Green Mode disables the SR drive signals, minimizing gate drive power consumption at light-load conditions.

This application note describes the design procedure for a SR circuit using FAN6208. The guidelines for printed circuit board (PCB) layout and a design example with experiment results are also presented. Figure 1 shows the typical application circuit of FAN6208.

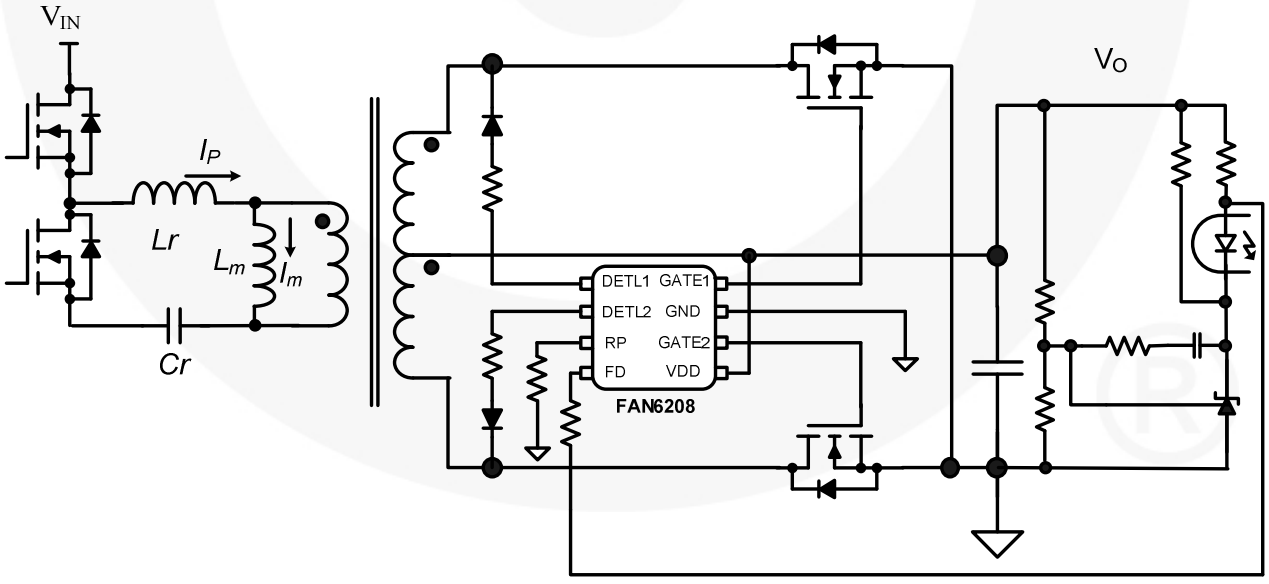


Figure 1. Typical Application

LLC Resonance Converter with SR

Figure 2 shows the simplified schematic of a half-bridge LLC resonant converter, where L_m is the magnetizing inductance that acts as a shunt inductor, L_r is the series resonant inductor, and C_r is the resonant capacitor. Since the magnetizing inductor is relatively small, a considerable amount of magnetizing current (I_m) exists, which freewheels in the primary side without being involved in the power transfer. The primary-side current (I_p) is sum of the magnetizing current and the secondary-side current referred to the primary.

Figure 3 shows the typical gain curve of the half-bridge LLC resonant converter. To allow Zero Voltage Switching (ZVS) for the primary-side switches, gain curves with inductive impedance characteristics should be used, where the gain decreases as frequency increases. The resonant network has a resonant frequency determined by the resonance between L_r and C_r. When the switching frequency is lower than the resonant frequency (below resonance), the half resonance of reflected secondary-side current (diode current) finishes before the primary-side switch is turned off, as shown in Figure 4. When the switching frequency is higher than the resonant frequency (above resonance) the primary-side switch is turned off before the half resonance of reflected secondary-side current (diode current) is completed, as shown in Figure 5.

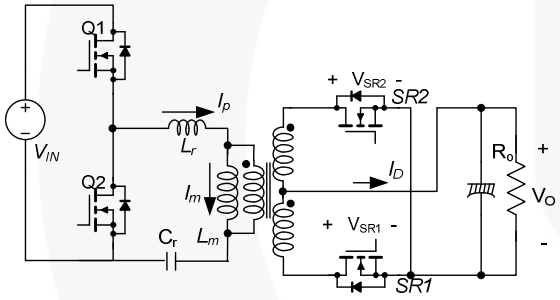


Figure 2. Schematic of LLC Resonant Converter with SR

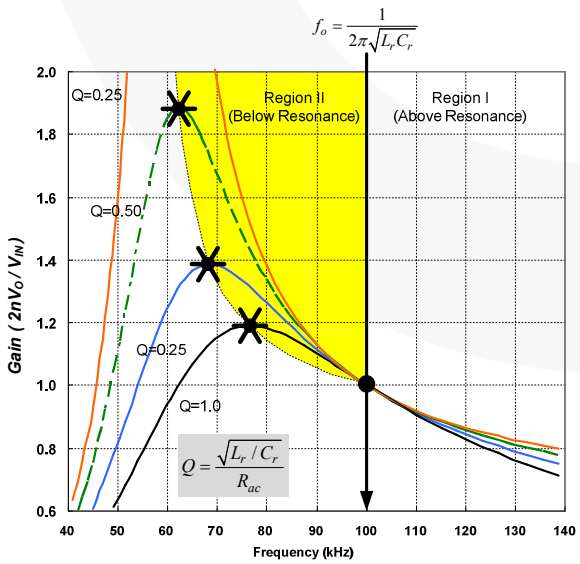


Figure 3. Typical Gain Curves of LLC Resonant Converter

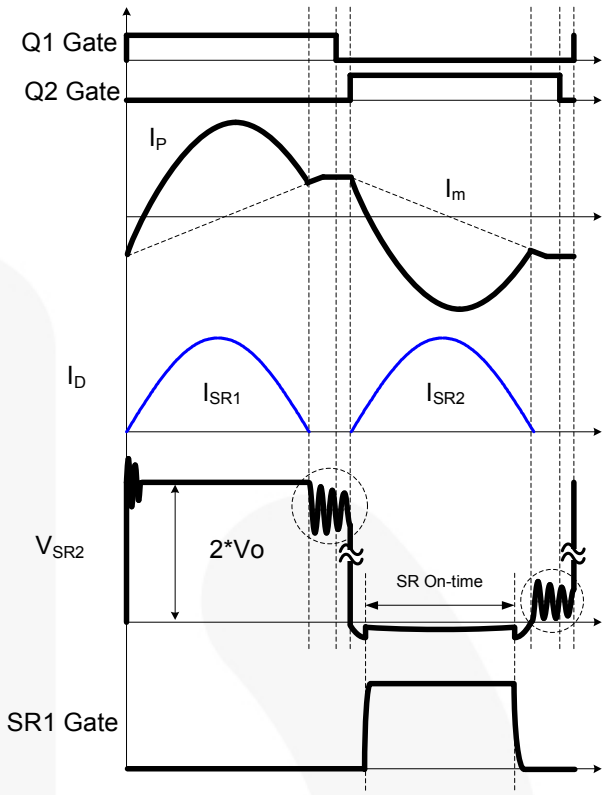


Figure 4. Key Waveforms Below -Resonance Operation

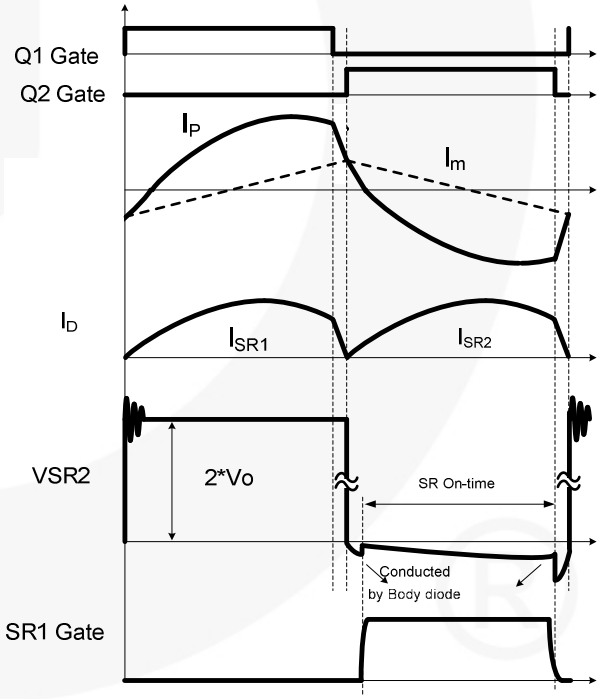


Figure 5. Key Waveforms of Above-Resonance Operation

Application Circuit

Figure 6 shows the typical application circuit of FAN6208 and Figure 7 shows the typical timing diagram of SR gate drive signal. FAN6208 senses the drain-to-source voltage of each SR to determine the gate drive timing. Once the body diode of SR begins conducting, the drain-to-source voltage drops to zero, which causes low detection (DETL) pin voltage to drop to zero. FAN6208 turns on the MOSFET after $t_{ON-ON-DETL}$ (about 350ns), when the voltage on DETL drops below 2V. As depicted in Figure 8, the turn -on delay (after $t_{SR-ON-DETL}$) is a sum of debounce time (150ns) and propagation delay (200ns).

FAN6208 measures the SR conduction duration (t_{DETL}), during which DETL voltage stays lower than 2V, and uses this information to determine the turn-off instant of SR gates of the next switching cycle, as shown in Figure 7. The turn-off instant is obtained by subtracting a dead time (t_{DEAD}) from the measured SR conduction duration of the previous switching cycle.

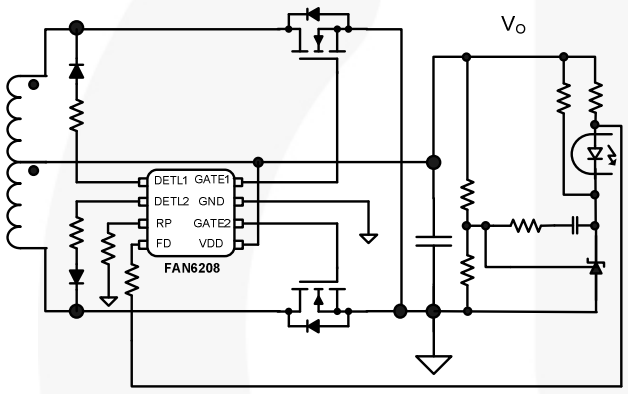


Figure 6. Application Circuit of FAN6208

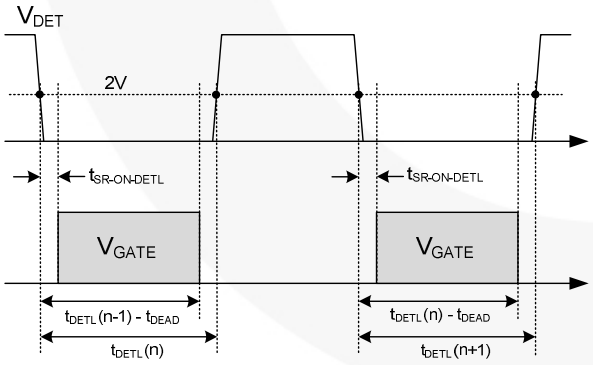


Figure 7. SR Conduction Time Determination

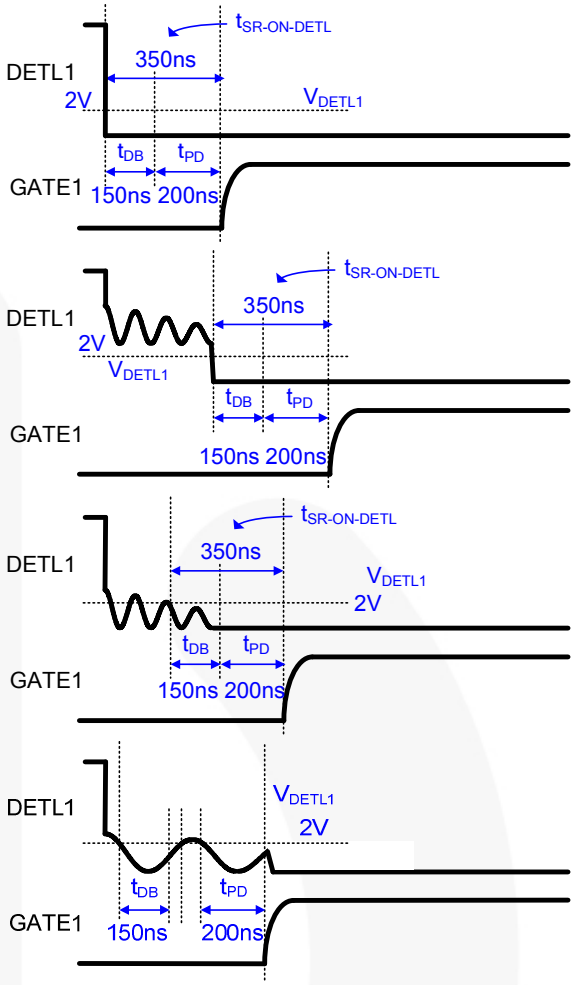


Figure 8. Timing Diagram for Turning On SR

DETL Pin Configuration

Allowable voltage on the DETL pin is from -0.3V to 7V. Since the maximum voltage of the SR drain-to-source voltage is twice that of the output voltage, a diode (D_{DETL}) is required for the DETL pin to prevent high voltage. Diode 1N4148 is typically used for D_{DETL}. Since the DETL internal current source is 50μA, R_{DETL} should be determined such that the DETL voltage is lower than the low detection threshold (2V) with enough margin when the SR conducts. Since the forward-voltage drop of SR can be as low as zero when SR current is small, the DETL resistor should be:

$$R_{DETL} < \frac{(2 - V_{FD})}{50\mu A} \quad (1)$$

where V_{FD} is the forward-voltage drop of DETL diode.

R_{DETL} larger than 20kΩ is not typically recommended for proper low-voltage detection on DETL pin.

R_{DETL} should be determined such that the DETL voltage is higher than -0.3V when the maximum voltage drop occurs across SR, such as:

$$R_{DETL} > \frac{I_{SR}^{max} R_{DS.ON} - V_{FD} - 0.3}{50\mu A} \quad (2)$$

where I_{SR}^{max} is the maximum current of SR and $R_{DS.ON}$ is the maximum on-resistance of the SR MOSFET at high temperature.

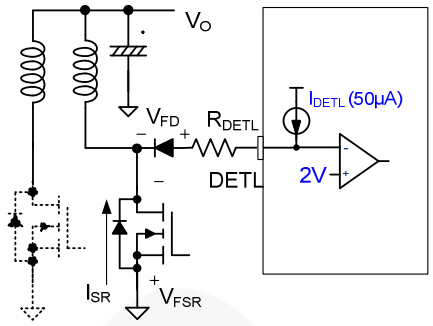


Figure 9. Application Circuit of DETL Pin

RP Pin Configuration

The dead time can be programmed using a resistor on the RP pin. The relationship between the dead time and SR conduction duration (t_{DETL}) for different resistor values on the RP pin are given in Figure 10 and Figure 11. Since the SR conduction time is shrunk by the protection function (gate-shrink function) when t_{DEAD} is smaller than 125ns, R_p should be properly selected such that the gate-shrink function does not operate at maximum switching frequency.

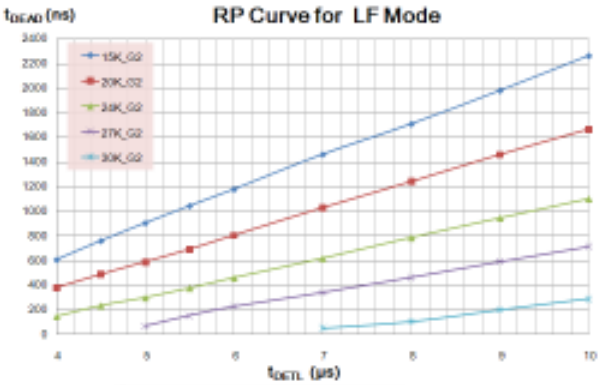


Figure 10. t_{DEAD} vs. t_{DETL} for Different R_P (Low Frequency)

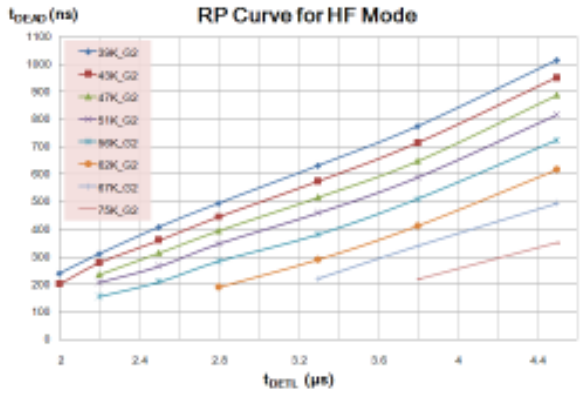


Figure 11. t_{DEAD} vs. t_{DETL} for Different R_P (High Frequency)

The RP pin has an internal constant current source (41.5μA) and the pin voltage is determined by the R_p resistor. Depending on the RP pin voltage, the Green Mode threshold of t_{DETL} is determined as shown in Figure 12. When R_{RP} is less than 36KΩ, FAN6208 operates in Low-Frequency Mode, where Green Mode is enabled when t_{DETL} is smaller than 3.75μs. When R_{RP} is larger than 36KΩ, High-Frequency Mode is selected and Green Mode is enabled for t_{DETL} smaller than 1.90μs.

The RP pin also has two internal thresholds for pin-open / short protection. Using RP pin short protection, remote on / off control can be implemented as shown in Figure 13.

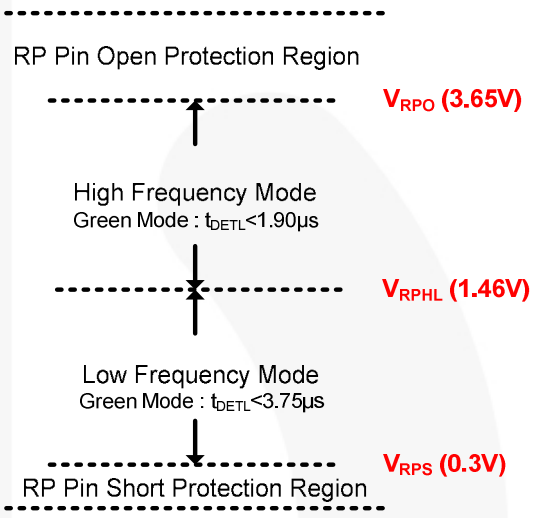


Figure 12. RP Pin Operation

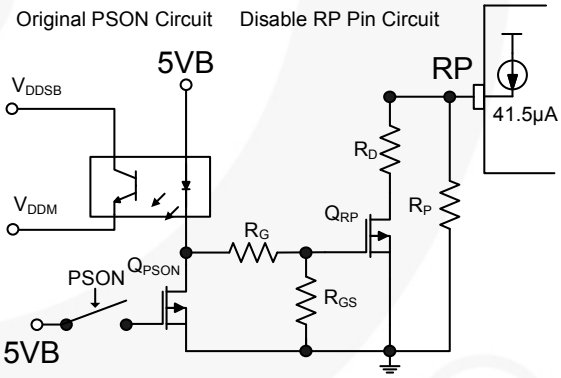


Figure 13. Application Circuit of RP Pin for Remote ON / OFF

Gate-Shrink Functions

In normal operation, the turn-off instant is determined by subtracting a dead time (t_{DEAD}) from the measured SR conduction duration of the previous switching cycle, as shown in Figure 7. This allows proper driving timing for the SR MOSFETS when the converter is in steady state and the switching frequency does not change much. However, this control method may cause shoot-through of SR MOSFETs when the switching frequency increases fast and switching

transition of the primary-side MOSFETs takes place before the turn-off command of the SR is given. To prevent the shoot-through problem, FAN6208 has gate-shrink functions. Gate shrink takes place in the following three conditions:

1. When an insufficient dead time is detected in the previous switching cycle. When the DETL becomes HIGH within 125ns of the detection window after SR gate is turned off, the SR gate drive signal in the next switching cycle is reduced by $t_{SHRINK-DT}$ (about 1.25µs) to increase the dead time as shown in Figure 14.

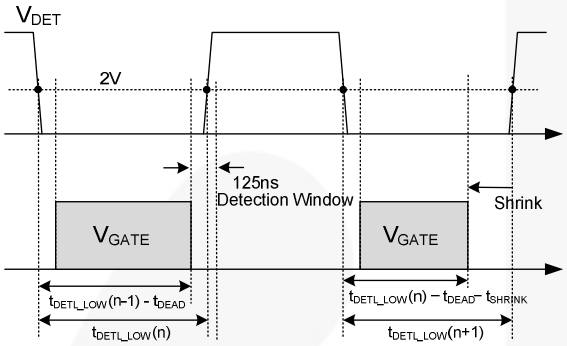


Figure 14. Gate Shrink by Insufficient Dead Time

2. When the feedback information changes fast. FAN6208 monitors the current through the opto-coupler diode by measuring the voltage across the resistor in series with opto-diode, as depicted in Figure 15. If the feedback current through the opto diode increases by more than 20% of the feedback current of the previous switching cycle, SR gate signal is shrunk by $t_{SHRINK-FD}$ (about 1.4µs) for $t_{D-SHRINK-FD}$ (about 90µs), shown in Figure 16.

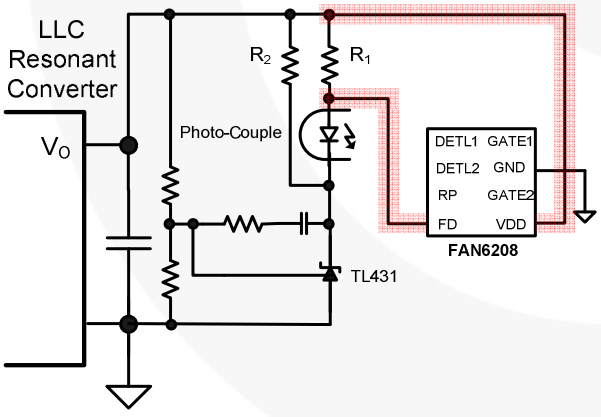


Figure 15. Application Circuit of FD Pin

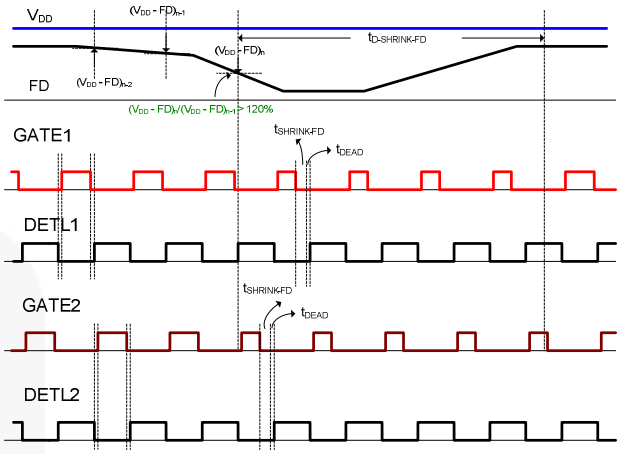


Figure 16. Gate Shrink by Feedback Detection

3. When the DETL voltage has ringing around zero. As depicted in Figure 17, the drain voltage of SR has ringing around zero at light-load condition after the switching transition of primary-side switches. When DETL voltage rises above 2V within 350ns after DETL voltage drops to zero and stays above 2V longer than 150ns, the gate is shrunk by 1.2µs ($t_{SHRINK-RNG}$), as shown in Figure 17.

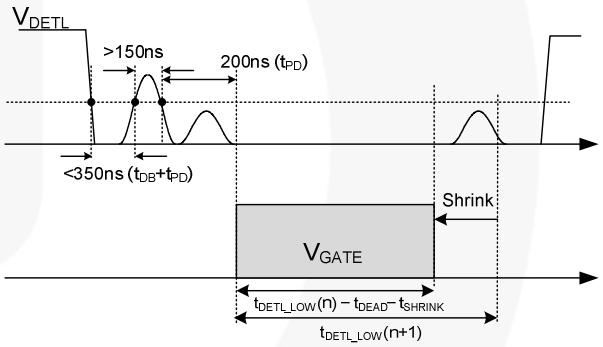


Figure 17. Gate Shrink by the DETL Voltage Ringing

Printed Circuit Board Layout

In Figure 18, the power traces are marked as bold lines. Good PCB layout improves power system efficiency and reliability and minimizes EMI.

Guidelines

- For feedback detection, the FD pin should be connected to the anode of the opto diode. Connecting the FD pin through a resistor can improve surge immunity of the system. Keep trace **1** away from any power trace with high pulsating current.
- The control ground (trace 2) and power ground (trace 7) should meet at a single point to minimize interference. The connecting trace should be as short as possible.
- As indicated by 4, the ground of the feedback loop should be connected to the negative terminal of output capacitor C_O.
- Trace 5 should be long and far from V_o terminal.
- Keep trace **6** as short as possible.
- As indicated by 7, the source terminals of Q_1 and Q_2 are connected to the negative terminal of C_o. Keep trace 10 short, direct, and wide.
- As indicated by 8, the negative terminal of C_o should be connected to the case directly.

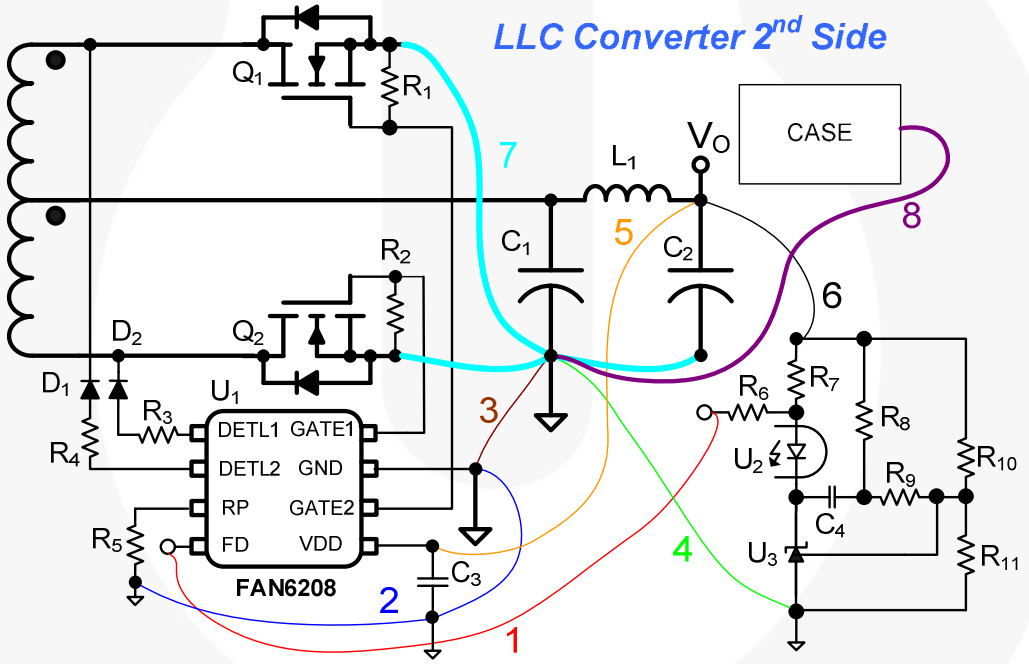


Figure 18. Layout Considerations

Design Example

The following example is a 12V/300W single output power supply with LLC resonant converter topology. As Figure 19 shows, the FAN7621 controller is used for the LLC resonant converter. The integrated CCM PFC controller FAN6982 is used for PFC stage.

The key system parameters are listed in Table 1 and the Bill of Materials (BOM) is summarized in Table 2.

The two-level PFC output voltage function of FAN6982 is used where the typical PFC output voltage is 390V. The PFC output voltage is reduced to 360V for low-line and light-load condition to improve efficiency of the PFC stage. The typical switching frequency (f_s) is 65kHz for PFC stage.

Table 1. System Specification

Input Voltage Range	90~264V_{AC}
PFC Output	360~390V_{DC}
PFC Controller	FAN6982
Main power Controller	FAN7621
Output Voltage (Vo)	12V
Output Power (Po)	300W
PFC Switching Frequency	65kHz
LLC resonant converter Switching Frequency	60~140kHz

The turn ratio n of TX_1 is 13.5, L_m is 1.2mH, L_r is 150µH, and C_r is 47nH. 1N4148 is used for D201 & D202 whose voltage rating is 100V. 27kΩ is used for R204 (R_{RP}) for the Low-Frequency Mode setting.

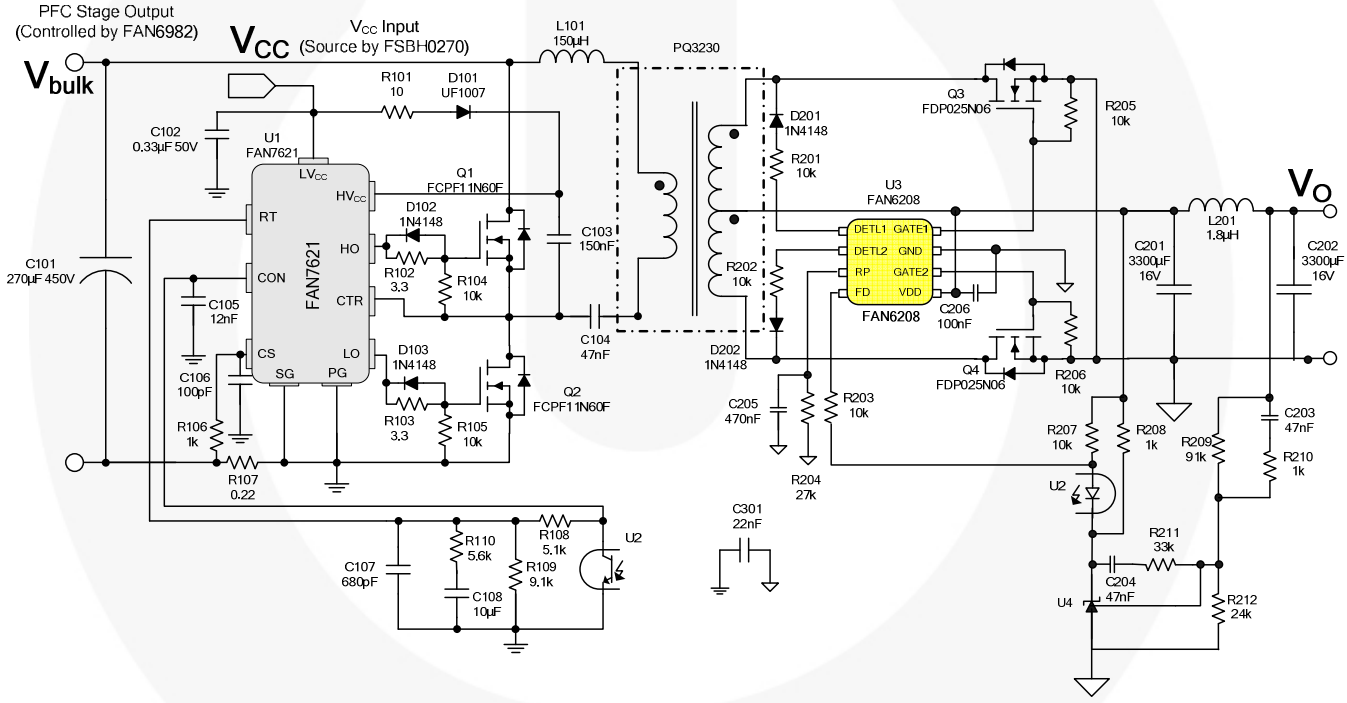


Figure 19. Complete Circuit Diagram

Table 2. Bill of Materials

Part	Value	Note	Part	Value	Note
Resistor			**Capacitor**		
R_{101}	10Ω	1/4W	C_{108}	10μF	25V
R_{102}	3.3Ω	1/4W	C_{201}	3300μF	16V
R_{103}	3.3Ω	1/8W	C_{202}	3300μF	16V
R_{104}	10kΩ	1/8W	C_{203}	47nF	50V
R_{105}	10kΩ	1/8W	C_{204}	47nF	50V
R_{106}	1kΩ	1/8W	C_{205}	470nF	25V
R_{107}	0.2Ω	2W	C_{206}	100nF	50V
R_{108}	5.1kΩ	1/8W	C_{301}	22nF/250V	Y-Capacitor
R_{109}	9.1kΩ	1/8W	**Transformer**		
R_{110}	5.6kΩ	1/8W	TX_1	L_r =10μH/ L_m =1200μH	PQ3230
R_{201}	10kΩ	1/8W	**Diode**		
R_{202}	10kΩ	1/8W	D_{101}	UF1007	1A/1000V
R_{203}	10kΩ	1/8W	D_{102}	1N4148	
R_{204}	27kΩ	1/8W	D_{103}	1N4148	
R_{205}	10kΩ	1/8W	D_{201}	1N4148	
R_{206}	10kΩ	1/8W	D_{202}	1N4148	
R_{207}	10kΩ	1/8W	**Inductor**		
R_{208}	1kΩ	1/8W	L101	L = 150μH	QP2914
R_{209}	91kΩ	1/8W	L201	L = 1.8μH	
R_{210}	1kΩ	1/8W	**MOSFET**		
R_{211}	33kΩ	1/8W	Q_1	FCPF11N60F	
R_{212}	24kΩ	1/8W	Q_2	FCPF11N60F	
Capacitor			Q_3	FDP025N06	
C_{101}	270μF	450V	Q_4	FDP025N06	
C_{102}	0.33μF	50V	**IC**		
C_{103}	150nF	1kV	U_1	FAN7621	LLC Controller
C_{104}	47nF	1kV	U_2	PC817	
C_{105}	12nF	50V	U_3	FAN6208	SR Controller
C_{106}	100pF	50V	U_4	TL431	
C_{107}	680pF	50V			

Figure 20 and Figure 21 show the SR gate drive waveforms for different R_P. As can be seen, the dead time of SR drive can be programmed.

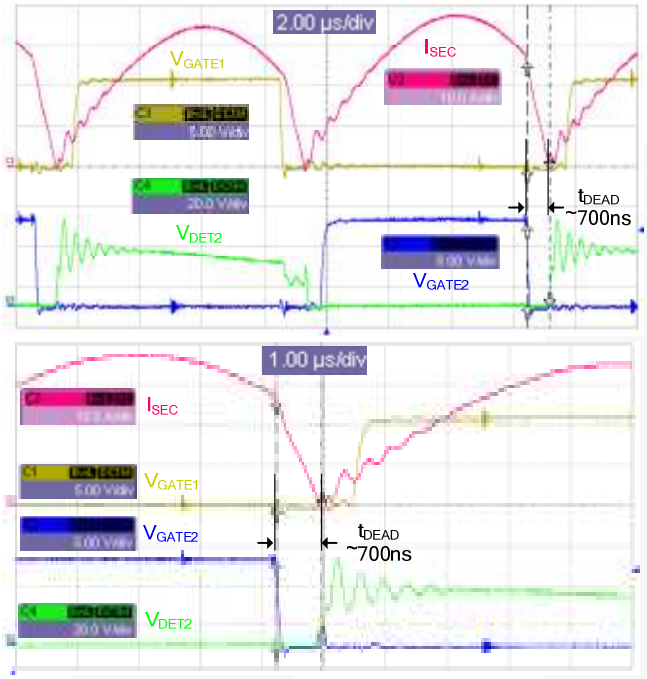


Figure 20. Secondary Side Current and SR Gate Signal by R_{RP}=24kΩ

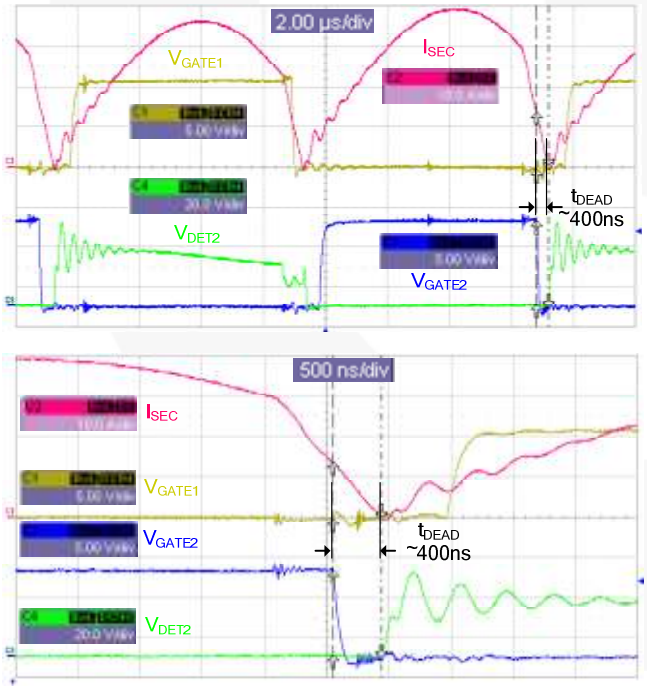


Figure 21. Secondary Side Current and SR Gate Signal by R_{RP}=27kΩ

The efficiency test results of the Schottky diode and synchronous rectification are shown in Table 3 and Table 4. Figure 22 compares the efficiencies of Schottky diode and synchronous rectification. As can be seen, 1~2% efficiency improvement can be obtained using synchronous rectification. Figure 22 also shows how the dead time of SR affects the efficiency. By fine-tuning the dead time, efficiency can be maximized.

Table 3. Efficiency Measurements at V_{AC}=115V on 300W PC Power with Schottky Diodes (MBRP3045)

Load	Input Watts(W)	Output Watts(W)	Efficiency
100%	358.070	307.658	85.920%
50%	176.38	154.91	87.82%
20%	73.30	62.19	84.80%

Table 4. Efficiency Measurements at V_{AC}=115V on 300W PC Power with SRs (FDP025N06 and R_{RP}=30kΩ)

Load	Input Watts (W)	Output Watts (W)	Efficiency	vs. Schottky Diode
100%	347.70	307.62	88.47%	+2.55%
50%	172.81	154.77	89.56%	+1.74%
20%	72.41	62.21	85.91%	+1.11%

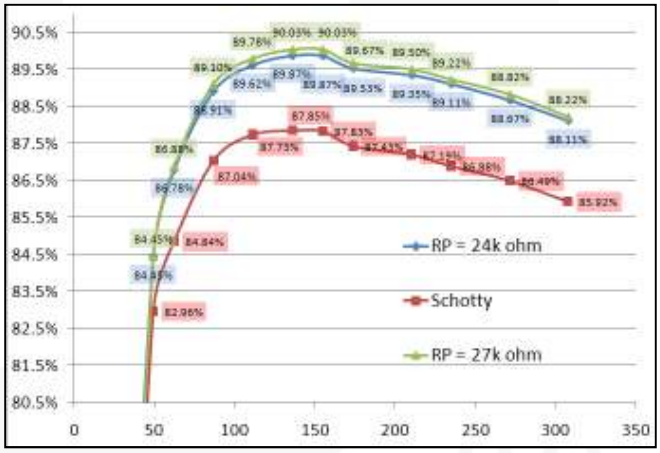


Figure 22. Efficiency Analysis

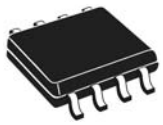
Related Resources

FAN6208 — Secondary Synchronous Rectifier Controller for LLC Topology
FAN7621 — PFM Controller for Half-Bridge Resonant Converters
FAN6982 — CCM Power Factor Correction Controller
FDP025N06 —FDP025N06 N-Channel PowerTrench® MOSFET 60V,265A, 2.5mΩ
1N/FDLL 914/A/B / 916/A/B / 4148 / 4448 — Small Signal Diode
FSFR2100 — Fairchild Power Switch for Half-Bridge Resonant Converters
AN4137 — Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)
AN-4151 — Half-Bridge LLC Resonant Converter Design Using FSFR-Series Fairchild Power Switch (FPS)

SRK2000

Synchronous rectifier smart driver for LLC resonant converters

Datasheet - production data



SO-8

Features

- Secondary-side synchronous rectifier controller optimized for LLC resonant converters
- Protection against current reversal
- Safe management of load transient, light load and startup condition
- Intelligent automatic sleep mode at light load
- Dual gate driver for N-channel MOSFETs with 1 A source and 3.5 A sink drive current
- Operating voltage range 4.5 to 32 V
- Programmable UVLO with hysteresis
- 250 µA quiescent consumption
- Operating frequency up to 500 kHz
- Available in SO-8 package

Applications

- All-in-one PC
- High-power AC-DC adapters
- 80+/85+ compliant ATX SMPS
- 90+/92+ compliant server SMPS
- Industrial SMPS

Description

The SRK2000 smart driver implements a control scheme specific to secondary-side synchronous rectification in LLC resonant converters that use a transformer with center-tap secondary winding for full-wave rectification.

It provides two high current gate drive outputs, each capable of driving one or more N-channel Power MOSFETs. Each gate driver is controlled separately and an interlocking logic circuit prevents the two synchronous rectifier MOSFETs from conducting simultaneously.

The control scheme in this IC allows for each synchronous rectifier to be switched on as the corresponding half-winding starts conducting and switched off as its current goes to zero. A unique feature of this IC is its intelligent automatic sleep mode. It allows the detection of a low-power operating condition for the converter and puts the IC into a low consumption sleep mode where gate driving is stopped and quiescent consumption is reduced. In this way, converter efficiency improves at light load, where synchronous rectification is no longer beneficial. The IC automatically exits sleep mode and restarts switching as it recognizes that the load for the converter has increased.

A noticeable feature is the very low external component count required.

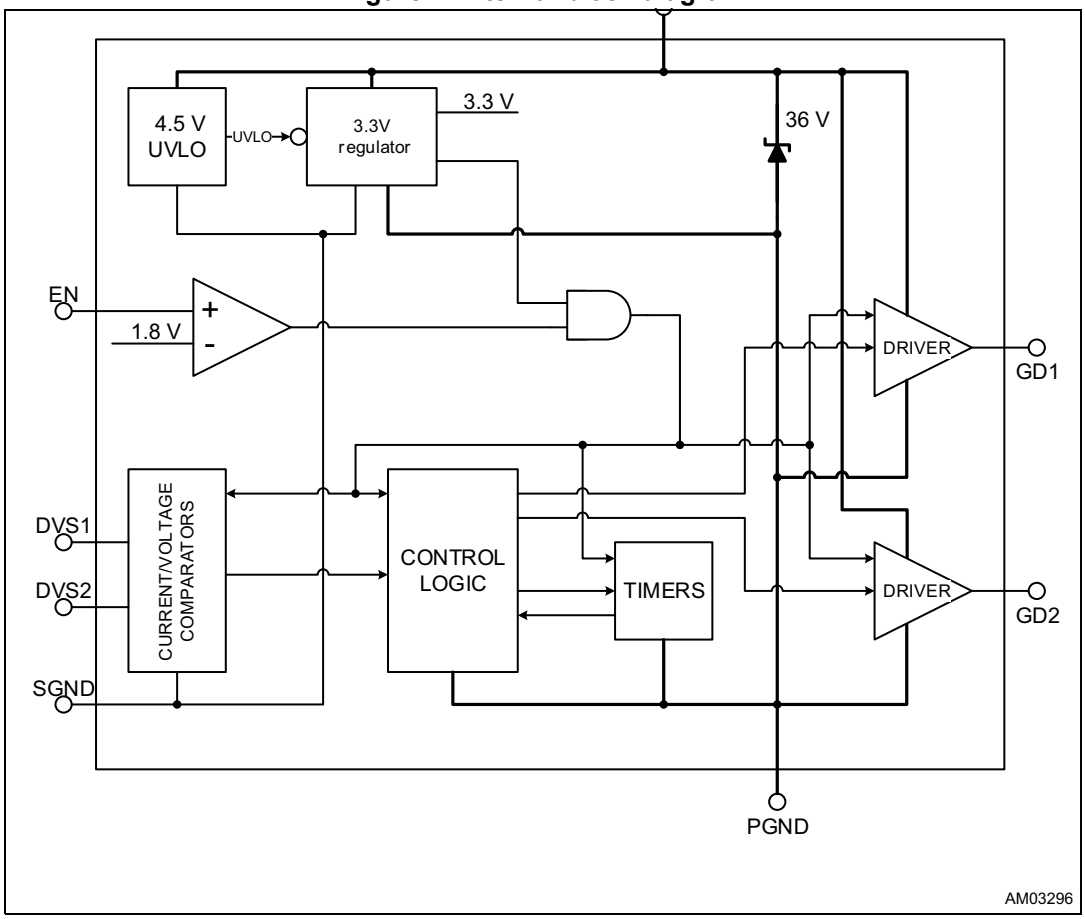
Table 1. Device summary

Order code	Package	Packing
SRK2000D	SO-8	Tube
SRK2000DTR		Tape and reel

Contents

1 Internal block diagram

Figure 1. Internal block diagram



2 Pin description

Figure 2. Pin configuration

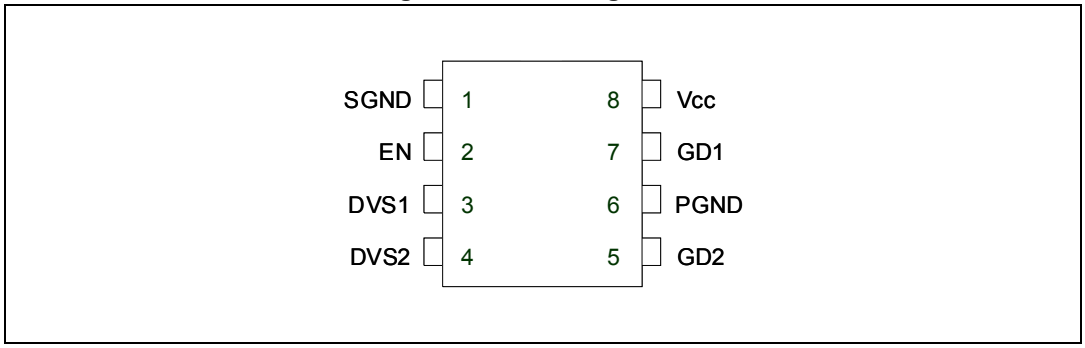
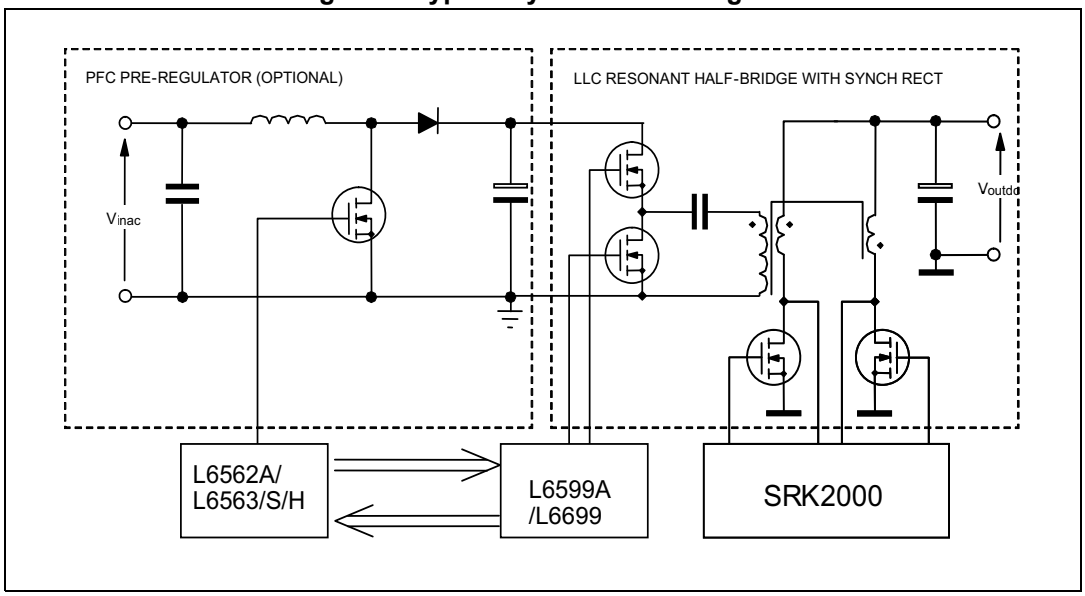


Table 2. Pin description

No.	Name	Function
1	SGND	Signal ground. Return of the bias current of the device and 0 V reference for drain-to-source voltage monitors of both sections. Route this pin directly to PGND.
2	EN	Drain voltage threshold setting for synchronous rectifier MOSFET turn-off. UVLO threshold programming. This pin is typically biased by either a pull-up resistor connected to V_{CC} or by a resistor divider sensing V_{CC}. Pulling the pin to ground disables the gate driver outputs GD1 and GD2 and can therefore be used also as Enable input.
3 4	DVS1 DVS2	Drain voltage sensing for sections 1 and 2. These pins are to be connected to the respective drain terminals of the corresponding synchronous rectifier MOSFET via limiting resistors. When the voltage on either pin goes negative, the corresponding synchronous rectifier MOSFET is switched on; as its (negative) voltage exceeds a threshold defined by the EN pin, the MOSFET is switched off. An internal logic rejects switching noise, however, extreme care in the proper routing of the drain connection is recommended.
5 7	GD2 GD1	Gate driver output for sections 2 and 1. Each totem pole output stage is able to drive the Power MOSFETs with a peak current of 1 A source and 3.5 A sink. The high-level voltage of these pins is clamped at about 12 V to avoid excessive gate voltages in case the device is supplied with a high V_{CC}.
6	PGND	Power ground. Return for gate drive currents. Route this pin to the common point where the source terminals of both synchronous rectifier MOSFETs are connected.
8	V_{CC}	Supply voltage of the device. A small bypass capacitor (0.1 µF typ.) to SGND, located as close to the IC's pins as possible, may be useful to obtain a clean supply voltage for the internal control circuitry. A similar bypass capacitor to PGND, again located as close to the IC's pins as possible, may be an effective energy buffer for the pulsed gate drive currents.

Figure 3. Typical system block diagram



3 Maximum ratings

Table 3. Absolute maximum ratings

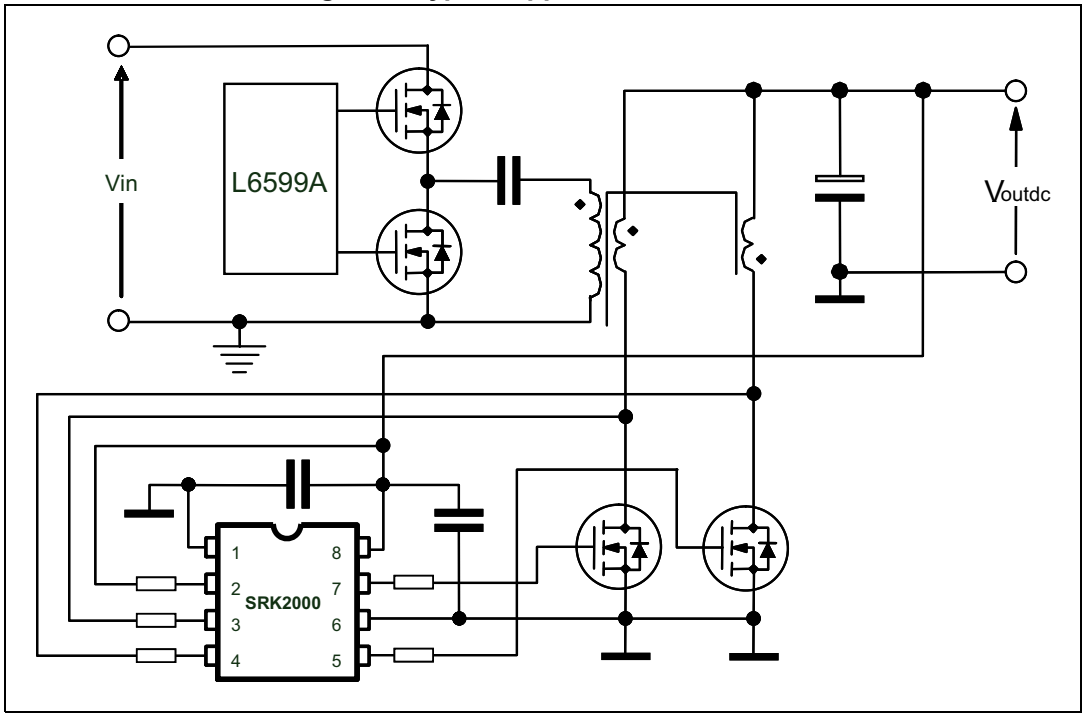
Symbol	Pin	Parameter	Value	Unit
V_{CC}	8	DC supply voltage	-0.3 to V_{CCZ}	V
I_{CCZ}	8	Internal Zener maximum current	25	mA
---	2, 3, 4	Analog inputs voltage rating	-0.3 to V_{CCZ}	V
$I_{DVS1,2\_sk}$	3, 4	Analog inputs max. sink current (single pin)	25	mA
$I_{DVS1,2\_sr}$	3, 4	Analog inputs max. source current (single pin)	-5	mA

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Max. thermal resistance, junction-to-ambient	150	°C/W
Ptot	Power dissipation at T_A = 50 °C	0.65	W
T_J	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

4 Typical application schematic

Figure 4. Typical application schematic



5 Electrical characteristics

T_J = -25 to 125 °C, V_{CC} = 12 V, C_{GD1} = C_{GD2} = 4.7 nF, EN = V_{CC}; unless otherwise specified; typical values refer to T_J = 25 °C.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	4.5		32	V
V_{CCOn}	Turn-on threshold	See(1)	4.25	4.5	4.75	V
V_{CCOff}	Turn-off threshold	See(1)	4	4.25	4.5	V
Hys	Hysteresis			0.25		V
V_{CCZ}	Zener voltage	I_{CCZ} = 20 mA	33	36	39	V
Supply current						
$I_{start-up}$	Startup current	Before turn-on, V_{CC} = 4 V		45	70	µA
Iq	Quiescent current	After turn-on		250	500	µA
I_{CC}	Operating supply current	At 300 kHz		35		mA
Iq	Quiescent current	EN = SGND		150	250	µA
Drain sensing inputs and synch functions						
$V_{DVS1,2\_H}$	Upper clamp voltage	$I_{DVS1,2}$ = 20 mA		V_{CCZ}		V
$I_{DVS1,2\_b}$	Input bias current	$V_{DVS1,2}$ = 0 to V_{CC}(2)	-1		1	µA
$V_{DVS1,2\_A}$	Arming voltage (positive-going edge)			1.4		V
$V_{DVS1,2\_PT}$	Pre-triggering voltage (negative-going edge)			0.7		V
$V_{DVS1,2\_TH}$	Turn-on threshold		-250	-200	-180	mV
$I_{DVS1,2\_On}$	Turn-on source current	$V_{DVS1,2}$ = -250 mV		-50		µA
$V_{DVS1,2\_Off}$	Turn-off threshold (positive-going edge)	R = 680 kΩ from EN to V_{CC}	-18	-25	-32	mV
		R = 270 kΩ from EN to V_{CC}	-9	-12.5	-16	
T_{PD_On}	Turn-on debounce delay	After sourcing $I_{DS1,2\_On}$		250		ns
T_{PD_Off}	Turn-off propagation delay	After crossing $V_{DS1,2\_Off}$			60	ns
T_{ON_min}	Minimum on-time			150		ns
D_{OFF}	Min. operating duty-cycle			40		%
D_{ON}	Restart duty-cycle			60		%
Gate drive enable function						
V_{EN_On}	Enable threshold	Positive-going edge(1)	1.7	1.8	1.9	V
Hyst	Hysteresis	Below V_{EN_On}		45		mV

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{EN}	Bias current	$V_{EN} = V_{EN\_On}$			1	µA
Turn-off threshold selection						
V_{EN-Th}	Selection threshold	$V_{CC} = V_{CCOn}$	0.32	0.36	0.40	V
I_{EN}	Pull-down current	$V_{EN} = V_{EN\_Th}$, $V_{CC} = V_{CCOn}$	7	10	13	µA
Gate drivers						
V_{GDH}	Output high voltage	$I_{GDsource}$ = 5 mA	11.75	11.9		V
		$I_{GDsource}$ = 5 mA, V_{CC} = 5 V	4.75	4.9		
V_{GDL}	Output low voltage	I_{GDsink} = 200 mA		0.2		V
		I_{GDsink} = 200 mA, V_{CC} = 5 V		0.2		
$I_{sourcepk}$	Output source peak current			-1		A
I_{sinkpk}	Output sink peak current			3.5		A
t_f	Fall time			18		ns
t_r	Rise time			40		ns
$V_{GDclamp}$	Output clamp voltage	$I_{GDsource}$ = 5 mA; V_{CC} = 20 V	12	13	15	V
V_{GDL_UVLO}	UVLO saturation	V_{CC} = 0 to V_{CCon} Isink = 5 mA		1	1.3	V

1. Parameters tracking each other.
2. For V_{CC} > 30 V $I_{DVS1,2\_b}$ may be greater than 1 µA because of the possible current contribution of the internal clamp Zener (few tens of µA).

6 Application information

6.1 EN pin - pin function and usage

This pin can perform three different functions: it sets the threshold $V_{DVS1,2\_Off}$ for the drain-to-source voltage of either synchronous rectifier (SR) Power MOSFET to determine their turn-off in each conduction cycle; it allows the user to program the UVLO thresholds of the gate drivers and can be used as Enable (remote on/off control).

6.1.1 Pull-up resistor configuration

At startup, an internal 10 µA current sink (I_{EN}) is active as long as the device supply voltage V_{CC} is below the startup threshold V_{CCOn}. The moment V_{CC} equals V_{CCOn} (4.5 V typ.), the voltage V_{EN} on the EN pin determines the turn-off threshold $V_{DVS1,2\_Off}$ for the drain voltage of both synchronous rectifiers during their cycle-by-cycle operation: if $V_{EN} < V_{EN\_Th}$ (= 0.36 V) the threshold is set at -25 mV, otherwise at -12 mV. Once the decision is made, the setting is frozen as long as V_{CC} is greater than the turn-off level V_{CCOff} (4.25 V typ.).

A simple pull-up resistor R_1 to V_{CC} can be used to set $V_{DVS1,2\_Off}$ turn-off threshold. The voltage on the EN pin as the device turns on is given by:

Equation 1

$$V_{EN} = V_{CCOn} - I_{EN} R1$$

Then, considering worst-case scenarios, we have:

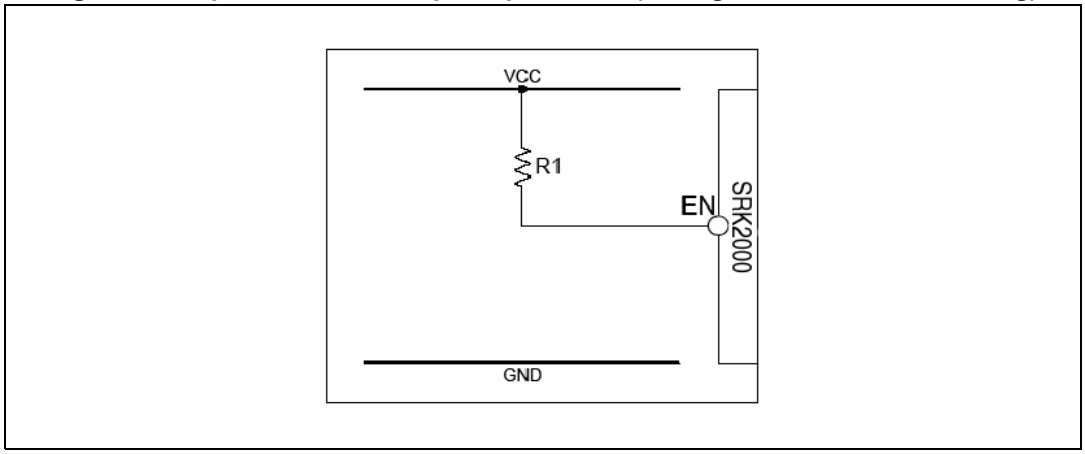
Equation 2

$$R1 > 633\ k\Omega \rightarrow V_{DVS1,2\_Off} = -25\ mV$$

$$R1 < 296\ k\Omega \rightarrow V_{DVS1,2\_Off} = -12\ mV$$

Some additional margin (equal to the resistor's tolerance) needs to be considered; assuming 5% tolerance, the use of the standard values R_1 = 680 kΩ in the first case and R_1 = 270 kΩ in the second case, is suggested.

Figure 5. EN pin biased with a pull-up resistor (for logic level MOSFET driving)



As V_{CC} exceeds V_{CCOn}, the internal current sink I_{EN} is switched off and the enable function is activated. The voltage on the pin is then compared to an internal reference V_{EN_On} set at 1.8 V: if this threshold is exceeded the gate drivers GD1 and GD2 are enabled and the SR MOSFET is operated; otherwise, the device stays in an idle condition and the SR MOSFET in the off state.

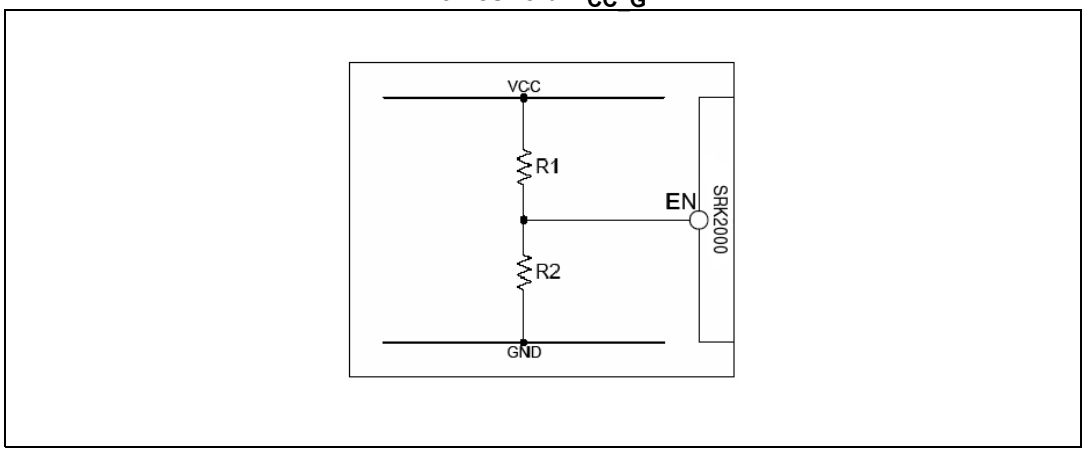
Using the pull-up resistor R_P, the voltage on the EN pin rises as I_{EN} is switched off and tends to V_{CC}, therefore exceeding V_{EN_On} and enabling the operation of both SR MOSFETs. Essentially, this results in enabling the gate-driving as V_{CC} exceeds V_{CCOn} and disabling it as V_{CC} falls below V_{CCOn}. This configuration is thereby recommended when SR MOSFETs are logic level types.

6.1.2 Resistor divider configuration

To enable gate-driving with a V_{CC} voltage higher than a predefined value V_{CC_G}, to properly drive a standard SR MOSFET, the EN pin is biased by a resistor divider (R1 upper resistor, R2 lower resistor) whose value is chosen so as to exceed V_{EN_On} when $V_{CC} = V_{CC\_G}$ and also to set the desired $V_{DVS1,2\_Off}$ level. Note that, with a falling V_{CC}, gate-driving is disabled at a V_{CC} level about 2.5% lower than V_{CC_G}, because of the 45 mV hysteresis of the comparator.

The equations that describe the circuit in the two crucial conditions $V_{CC} = V_{CCOn}$ (when the decision of the $V_{DVS1,2\_Off}$ level is made) and $V_{CC} = V_{CC\_G}$ (when gate-driving is to be enabled) are respectively:

Figure 6. EN pin biased with a resistor divider to program the gate drive UVLO threshold V_{CC_G}



Equation 3

$$\begin{cases} \dfrac{V_{CCOn} - V_{EN}}{R1} = I_{EN} + \dfrac{V_{EN}}{R2} \\ V_{CC\_G}\dfrac{R2}{R1+R2} = V_{EN\_On} \end{cases}$$

Solving these equations for R_1 and R_2 we get:

Equation 4

$$\begin{cases} R1 = \dfrac{V_{CCOn} - V_{EN}\dfrac{V_{CC\_G}}{V_{EN\_On}}}{I_{EN}} \\ R2 = R1\dfrac{V_{EN\_On}}{V_{CC\_G} - V_{EN\_On}} \end{cases}$$

If V_{CC_G} is not too low (< 8 ÷ 9 V), its tolerance is not critical because it is related only to that of V_{EN_On} (± 5.6%) and of the external resistors R1, R2 (± 1% each is recommended). Then, some care needs to be taken only as far as the selection of the -12/-25 mV threshold is concerned: in fact, the large spread of I_{EN} considerably affects the voltage on the EN pin as the device turns on, a value that can be found by solving the first of (1) for V_{EN}:

Equation 5

$$V_{EN} = \frac{V_{CCOn} - I_{EN}R1}{1 + \dfrac{R1}{R2}}$$

A couple of examples clarify the suggested calculation methodology.

Example 1 V_{CC_G} = 10 V, $V_{DVS1,2\_Off}$ = - 25 mV.

In this case, V_{EN} must definitely be lower than the minimum value of V_{EN_Th} (= 0.32 V). From the second of (2), the nominal ratio of R1 to R2 is (10 – 1.8) / 1.8 = 4.555. Substituting the appropriate extreme values in (3) it must be (4.75 - $7 \cdot 10^{-6} \cdot$R1) / (1 + 4.555) < 0.32; solving for R1 yields R1 > 425 kΩ; let us consider an additional 4% margin to take both the tolerance and the granularity of the R1 and R2 values into account, so that:
R1 > 425·1.04 = 442 kΩ. Choose R1 = 442 kΩ (E48 standard value) and, from the second of (2), R2 = 442/4.555 = 97 kΩ; use 97.6 kΩ (E48 standard value).

Example 2 V_{CC_G} = 10 V, $V_{DVS1,2\_Off}$ = - 12 mV.

In this case, V_{EN} must definitely be higher than the maximum value of V_{EN_Th} (= 0.40 V). From the second of (2), the nominal ratio of R1 to R2 is (10 – 1.8) / 1.8 = 4.555. Substituting the appropriate extreme values in (3) it must be (4.25 - $13 \cdot 10^{-6} \cdot$R1) / (1 + 4.555) > 0.4; solving for R1 yields R1 < 156 kΩ; with 4% additional margin R1 < 156/1.04 = 150 kΩ. Choose R1 = 147 kΩ (E48 standard value) and, from the second of (2),
R2 = 147/4.555 = 32.3 kΩ; use 32.4 kΩ (E48 standard value).

Note: In both examples the gate drivers are disabled as V_{CC} falls below 9.75 V (nominal value), as the voltage on the EN pin falls 45 mV below V_{EN_On}.

6.1.3 Remote on/off control

Whichever configuration is used, since a voltage on the EN pin 45 mV below V_{EN_On} disables the gate drivers, any small-signal transistor can be used to pull down the EN pin and force the gate drivers into an off state.

Finally, it should be noted that during power-up, power-down, and under overload or short-circuit conditions, the gate drivers are shut down if the V_{CC} voltage is insufficient: < V_{CCOff} in

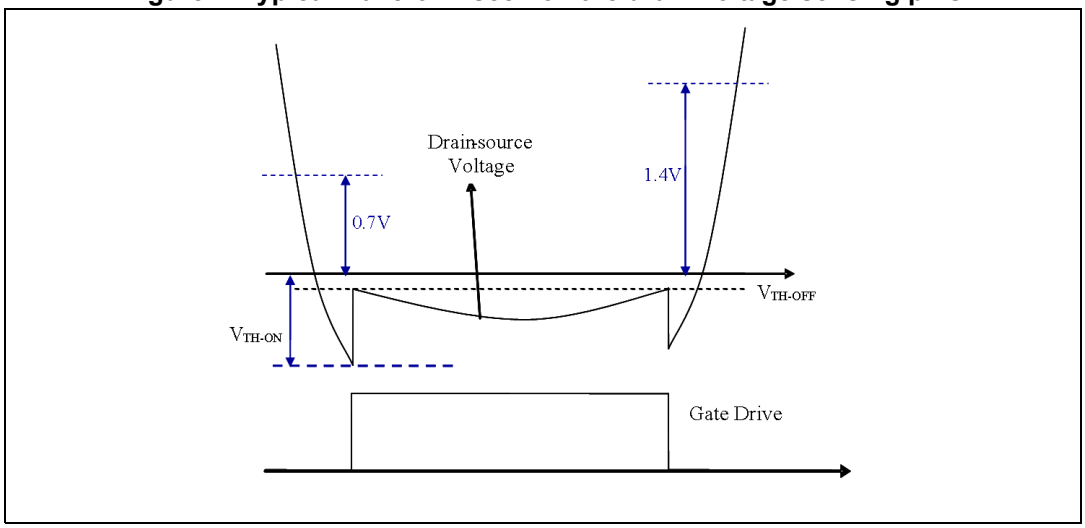
case of pull-up resistor configuration, < 0.975 · V_{CC_G} in case of resistor divider configuration (the coefficient 0.975 depends on the hysteresis on the Enable pin threshold).

6.2 Drain voltage sensing

In the following explanations it is assumed that the reader is familiar with the LLC resonant half bridge topology and its waveforms, especially those on the secondary side with a center-tap transformer winding for full-wave rectification.

To understand the polarity and the level of the current flowing in the SR MOSFETs (or their body diodes, or diodes in parallel to the MOSFETs) the IC is provided with two pins, DVS1-2, able to sense the voltage level of the MOSFET drains.

Figure 7. Typical waveform seen on the drain voltage sensing pins



The logic that controls the driving of the two SR MOSFETs is based on two gate-driver state machines working in parallel in an interlocked way to avoid both gate drivers being switched on at the same time.

There are four significant drain voltage thresholds: the first one, $V_{DVS1,2\_A}$ (= 1.4 V), sensitive to positive-going edges, arms the opposite gate driver (interlock function); the second, $V_{DVS1,2\_PT}$ (= 0.7 V), sensitive to negative-going edges, provides a pre-trigger of the gate driver; the third is the (negative) threshold V_{TH-ON} that triggers the gate driver as the body diode of the SR MOSFET starts conducting; the fourth is the internal (negative) threshold $V_{DVS1,2\_Off}$ where the SR MOSFET is switched off (selectable between -12 mV or -25 mV by properly biasing the EN pin).

The value of the ON threshold V_{TH-ON} is affected by the external resistor in series to each DVS1-2 pin needed essentially to limit the current that might be injected into the pins when one SR MOSFET is off and the other SR MOSFET is conducting. In fact, on the one hand, when one MOSFET is off (and the other one is conducting), its drain-to-source voltage is slightly higher than twice the output voltage; if this exceeds the voltage rating of the internal clamp (V_{CCZ} = 36 V typ.), a series resistor R_D must limit the injected current below an appropriate value, lower than the maximum rating (25 mA) and taking the related power dissipation into account. On the other hand, when current starts flowing into the body diode of one MOSFET (or in the diode in parallel with the MOSFET), the drain-to-source voltage is negative (≅ -0.7 V); when the voltage on pins DVS1,2 reaches the threshold $V_{DVS1,2\_TH}$

(-0.2 V typ.), an internal current source $I_{DVS1,2\_On}$ is activated; as this current exceeds 50 µA, the gate of the MOSFET is turned on. Therefore, the actual triggering threshold can be determined by *Equation 6*.

Equation 6

$$V_{TH-ON} = R_D \cdot I_{DVS1,2On} + V_{DVS1,2\_TH}$$

For instance, with R_D = 2 kΩ, the triggering threshold is located at
- (2 kΩ · 50 µA) - 0.2 V = -0.3 V.

To avoid false triggering of the gate driver, a debounce delay T_{PD_On} (= 250 ns) is used after sourcing $I_{DS1,2\_On}$ (i.e. the current sourced by the pin must exceed 50 µA for more than 250 ns before the gate driver is turned on). This delay is not critical for the converter's efficiency because the initial current is close to zero or anyway much lower than the peak value.

Once the SR MOSFET has been switched on, its drain-to-source voltage drops to a value given by the flowing current times the MOSFET $R_{DS(on)}$. Again, since the initial current is low, the voltage drop across the $R_{DS(on)}$ may exceed the turn-off threshold $V_{DVS1,2\_Off}$, and determine an improper turn-off. To prevent this, the state machine enables the turn-off comparator referenced to $V_{DVS1,2\_Off}$ only in the second half of the conduction cycle, based on the information of the duration of the previous cycle. In the first half of the conduction cycle only an additional comparator, referenced to zero, is active to prevent the current of the SR MOSFET from reversing, which would impair the operation of the LLC converter.

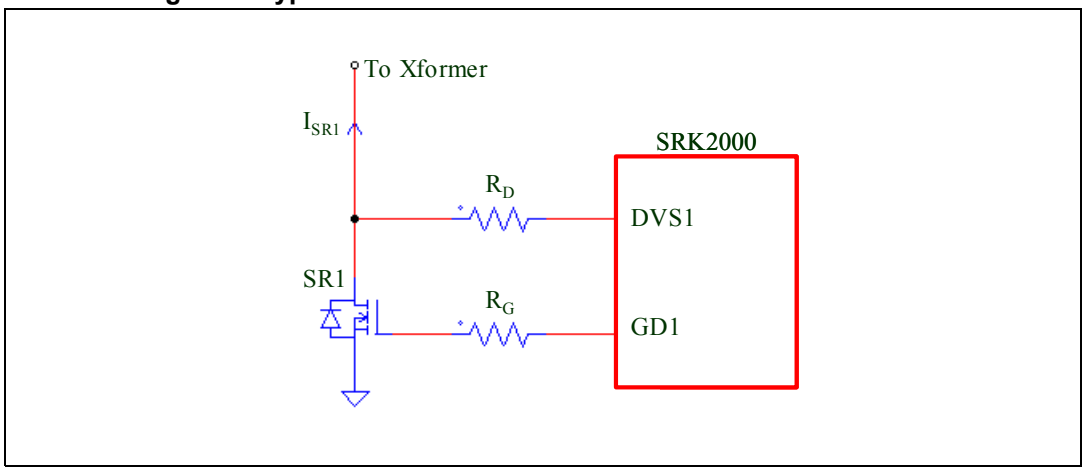
Once the threshold $V_{DVS1,2\_Off}$ is crossed (in the second half of the conduction cycle) and the GATE is turned off, the current again flows through the body diode causing the drain-to-source voltage to have a negative jump, going again below V_{TH-ON}. The interlock logic, however, prevents a false turn-on. It is worth pointing out that, due to the fact that each MOSFET is turned on after its body diode starts conducting, the ON transition happens with the drain-source voltage equal to the body diode forward drop; therefore there is neither a Miller effect nor switching losses at MOSFET turn-on. Also at turn-off the switching losses are not present, in fact, the current is always flowing from source to drain and, when the MOSFET is switched off, it goes on flowing through the body diode (or the external diode in parallel to the MOSFET).

Unlike at turn-on, the turn-off speed is critical to avoid current reversal on the secondary side, especially when the converter operates above the resonance frequency, where the current flowing through the MOSFET exhibits a very steep edge while decreasing down to zero: the turn-off propagation T_{PD_Off} delay has a maximum value of 60 ns.

The interlock logic, in addition to checking for consistent secondary voltage waveforms (one MOSFET can be turned on only if the other one has a positive drain-to-source voltage > $V_{DVS1,2\_A}$) to prevent simultaneous conduction, allows only one switching per cycle: after one gate driver has been turned off, it cannot be turned on again before the other gate drive has had its own on/off cycle.

The IC logic also prevents unbalanced current in the two SR MOSFETs: if one SR MOSFET fails to turn on in one cycle, the other SR MOSFET is also not turned on in the next cycle.

Figure 8. Typical connection of the SRK2000 to the SR MOSFET



6.3 Gate driving

The IC is provided with two high current gate drive outputs (1 A source and 3.5 A sink), each capable of driving one or more N-channel Power MOSFETs. Thanks to the programmable gate drive UVLO, it is possible to drive both - the standard MOSFETs and logic level MOSFETs.

The high-level voltage provided by the driver is clamped at $V_{GDclamp}$ (= 12 V) to avoid excessive voltage levels on the gate in case the device is supplied with a high V_{CC}.

The two gate drivers have a pull-down capability that ensures the SR MOSFETs cannot be spuriously turned on even at low V_{CC}: in fact, the drivers have a 1 V (typ.) UVLO saturation level at V_{CC} below the turn-on threshold.

6.4 Intelligent automatic sleep mode

A unique feature of this IC is its intelligent automatic sleep mode. The logic circuitry is able to detect a light load condition for the converter and stop gate driving, also reducing the IC's quiescent consumption. This improves converter efficiency at light load, where the power losses on the rectification body diodes (or external diodes in parallel to the MOSFETs) go lower than the power losses in the MOSFETs and those related to their driving.

The IC is also able to detect an increase of the converter's load and automatically restart gate driving.

The algorithm used by the intelligent automatic sleep mode is based on a dual time measurement system. The duration of a switching cycle of an SR MOSFET (that is one half of the resonant converter switching period) is measured using a combination of the negative-going edge of the drain-to-source voltage falling below $V_{DVS1,2\_PT}$ and the positive-going edge exceeding $V_{DVS1,2\_A}$; the duration of the SR MOSFET conduction is measured from the moment its body diode starts conducting (drain-to-source voltage falling below V_{TH-ON}) to the moment the gate drive is turned off (in case the device is operating) or the moment the body diode ceases to conduct (drain-to-source voltage going over V_{TH-ON}). While at full load the SR MOSFET conduction time occupies almost 100% of the switching cycle, as the load is reduced, the conduction time is reduced and as it falls below 40% (D_{OFF}) of the SR MOSFET switching cycle the device enters sleep mode. To prevent

erroneous decisions, the sleep mode condition must be confirmed for 16 consecutive switching cycles of the resonant converter (i.e. 16 consecutive cycles for each SR MOSFET of the center-tap).

Once in sleep mode, SR MOSFET gate driving is re-enabled when the conduction time of the body diode (or the external diodes in parallel to the MOSFET) exceeds 60% (D_{ON}) of the switching cycles. Also in this case the decision is made considering the measurement on 8 consecutive switching cycles (i.e. 8 consecutive cycles for each SR MOSFET of the center-tap). Furthermore, after each sleep mode entering/exiting transition, the timing is ignored for a certain number of cycles, to let the resulting transient in the output current fade out; then the time check is enabled. The number of ignored resonant converter switching cycles is 128 after entering sleep mode and 256 after exiting sleep mode.

6.5 Protection against current reversal

The IC provides protection against SR MOSFET current reversal. If a current reversal condition is detected for two consecutive switching cycles, the IC goes into sleep mode, avoiding the turn-on of the SR MOSFETs until a safe condition is restored.

6.6 Layout guidelines

The IC is designed with two grounds, SGND and PGND.

SGND is used as the ground reference for all the internal high-precision analog blocks, while PGND is the ground reference for all the noisy digital blocks, as well as the current return for the gate drivers. In addition, it is also the ground for the ESD protection circuits. SGND is protected by ESD events versus PGND through two anti-parallel diodes.

When laying out the PCB, make sure to keep the source terminals of both SR MOSFETs as close as possible to one another and to route the trace that goes to PGND separately from the load current return path. This trace should be as short as possible and be as close to the physical source terminals as possible. A layout that is as geometrically symmetrical as possible helps the circuit to operate in the most electrically symmetrical way as possible. SGND should be directly connected to PGND using a path as short as possible (under the device body).

Also drain voltage sensing should be performed as physically close to the drain terminals as possible: any stray inductance crossed by the load current that is in the drain-to-source voltage sensing circuit may significantly alter the current reading, leading to a premature turn-off of the SR MOSFET. It is worth mentioning that, especially in higher power applications or at higher operating frequencies, even the stray inductance of the internal wire bonding can be detrimental. In this case, a cautious selection of the SR MOSFET package is required.

The use of bypass capacitors between V_{CC} and both SGND and PGND is recommended. They should be low-ESR, low-ESL types and located as close to the IC pins as possible. Sometimes a series resistor (in the tens) between the converter's output voltage and the V_{CC} pin, forming an RC filter along with the bypass capacitor, is useful in order to get a cleaner V_{CC} voltage.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 9. SO-8 package outline

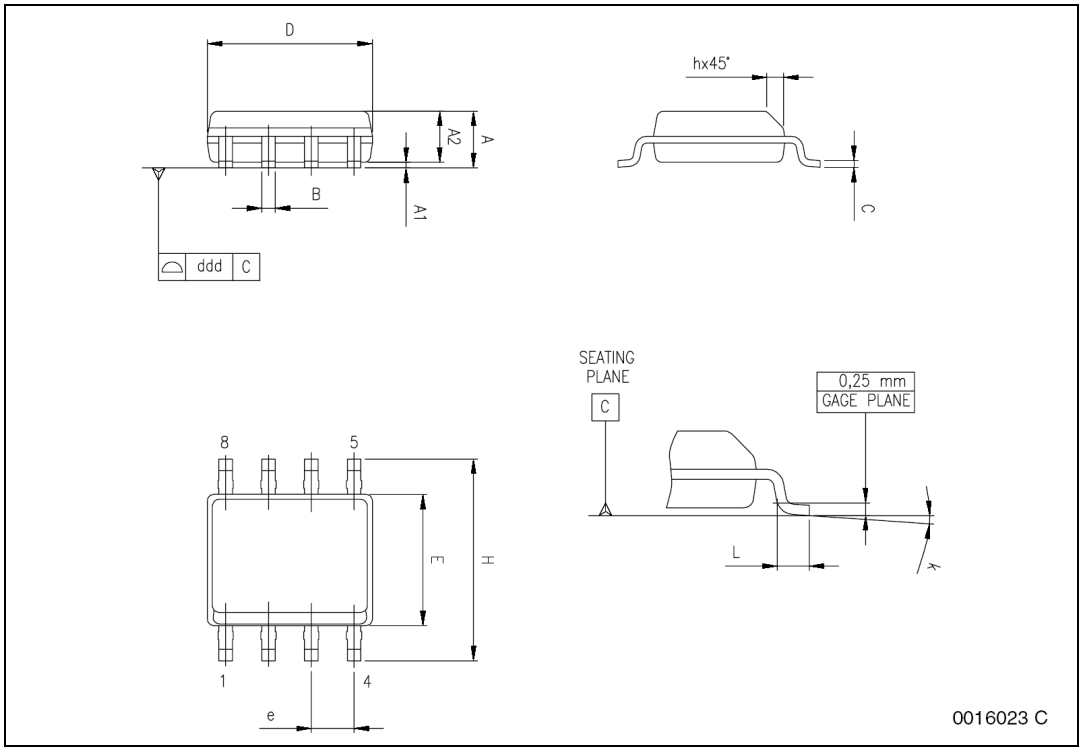


Table 6. SO-8 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. D dimensions do not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs should not exceed 0.15 mm (0.006 inch) in total (both sides).

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
10-Aug-2010	1	Initial release.
08-Feb-2012	2	Minor text changes to improve readability in features, on cover page, and *Chapter 6*. Added *Chapter 6.5: Protection against current reversal*. Document status promoted from preliminary data to datasheet.
01-Aug-2013	3	Updated *Figure 1* and moved to *Section 1: Internal block diagram* (added *Section 1*). Updated *Figure 3* (added L6699 device). Minor corrections throughout document.

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AN69

Synchronous rectifier reduces conduction loss in LLC resonant power supplies

Yong Ang, Snr Applications Engineer, Diodes Incorporated

With increasing drive to shrink electronic solutions, the merits of resonant power converters are now attracting increased attention among power supply engineers. This will especially affect the LCD TV 80PLUS® Silver or the more recent 85PLUS® ATX power supplies segment, where there is more and more pressure to shift towards higher switching frequencies in an attempt to reduce the physical size and cost of key system elements, such as the power transformer, filtering capacitors and heat sinking component. Resonant LLC converters can enable higher frequency through minimization of the primary switches' switching loss. Critically, the rectifier stage can constitute a significant source of conduction loss, since even the Schottky will have a relatively large voltage drop at high current ratings. This article discusses the limitations of using a diode and shows that the ultimate efficiency could be realized by the more elaborate scheme of using synchronous controller in conjunction with low resistance MOSFET as the output rectifier.

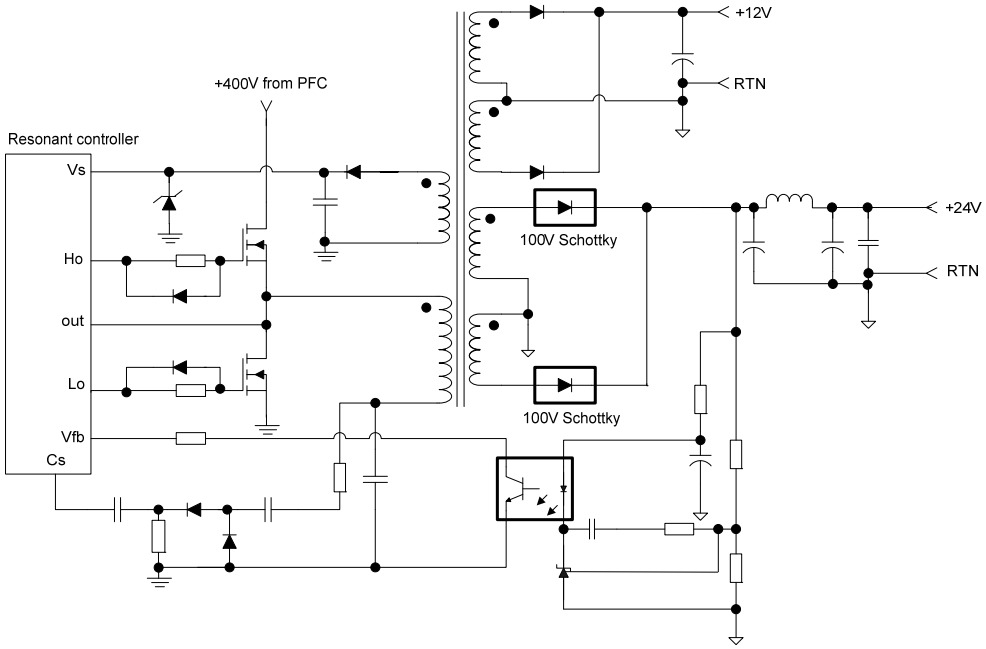


Figure 1 Power supply with LLC resonant downstream DC-DC converter

Resonant converter and limitation of existing rectifier technology

Although migration from the 65kHz typical of both Flyback and Forward PSU to the 100's of kHz allows smaller reactive components to be employed in designs, the resulting supplies are often more susceptible to the effects of parasitic capacitance and leakage inductance. Such effects manifest themselves as high-frequency ringing and large current spikes and switching loss, and unwanted electromagnetic interference. If used in a LCD TV, the EMI pollution could then severely distort the image and sound quality as the panel, the power supply and audio card are in close proximity to each other.

In a resonant converter, the input switching devices as opposed to hard-switched counterparts, can be configured to operate in 'zero voltage' (ZVS) switching modes, thereby greatly reducing levels of edge losses. Another advantage is the reduction of EMI, converters designed to exhibit ZVS do not generate this type of EMI. Furthermore, the sine-wave characteristics of resonant tank voltages and currents reduce the generation of high frequency harmonics.

Figure 2 shows the efficiency curve of a nominal 24V, 4A output LLC resonant DC-DC converter with diode rectification. Generally, the converter will accept its supply from an active power factor correction (PFC) pre-regulator that ensures compliant with the IEC1000-3-2 class D standard. In this design example, the magnetizing L_m and leakage inductance L_{lk} of the integrated magnetic approach transformer─810μH and 180μH respectively, and a 630V 22nF double metalized film pulse resonant capacitor C_s make up the resonant tank. No additional coil is required for resonance. The converter's secondary side is configured in a centre-tapped manner for half wave rectification. 100V 20A rated Schottky diodes are used.

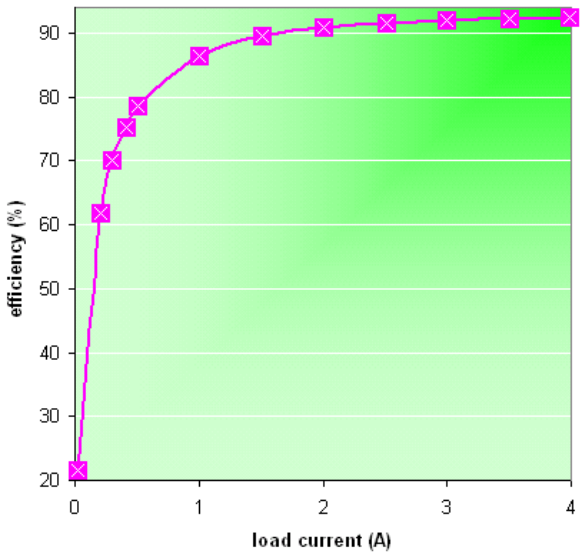


Figure 2 Circuit efficiency versus output current

The Half-Bridge LLC converter is regulated by modulating the switching frequency of the complementary primary switches. Since the PFC output voltage is a regulated 400V with a narrow variation in its normal operation, the LLC resonant converter is optimized to operate close to the load independent frequency at the nominal input voltage as shown in Figure 3. The load independent point which falls on the series resonant frequency is

$$f_r = \frac{1}{2\pi\sqrt{L_{lk}C_s}} = \frac{1}{2\pi\sqrt{180\mu H \times 22nF}} = 80kHz$$

Therefore, the output voltage can be regulated against a wide load variation with relatively narrow switching frequency change. Consequently, the switching frequency of the converter varies from 80kHz at full load up to 95kHz at 5% of peak loading. At zero load, the resonant converter works at its maximum frequency and power consumption of the converter is around 1.8W. Having a low consumption in sleep mode is now a key requirement in display unit. In practice, the resonant circuit could be turned off during standby mode and an auxiliary power supply supplies microcontroller that must remain alive.

The full load efficiency of the resonant LLC converter efficiency is 92.4%. Nevertheless, there is an emerging necessity for low voltage high current output such as those directly supplying microprocessor

or for systems that provide multiple outputs in 80PLUS® power supplies to reduce conduction loss within these rectifiers. In theory, the average currents flowing through each diode are,

$$I_{avg} = 0.5 \times I_{out} = 2A$$

For a typical 20A, 100V Schottky diode, the forward voltage drop at 2A and elevated temperature is about 0.425V. The conduction loss for each of the output diodes is around 850mW. That heat dissipation will raise the junction temperature of a diode in TO-263 on a $1in^2$ to a tolerable 107ºC at 80ºC ambient. In fact in a 10A output converter for LCD TV with display screen size above 32 inches, a total loss of 2.13W will need to be dissipated from the diode and that cannot be removed easily without bulky heat sink. Thereby, in order to achieve the ultimate efficiency and high power density, MOSFETs with low on-state resistance should be considered to replace these diodes.

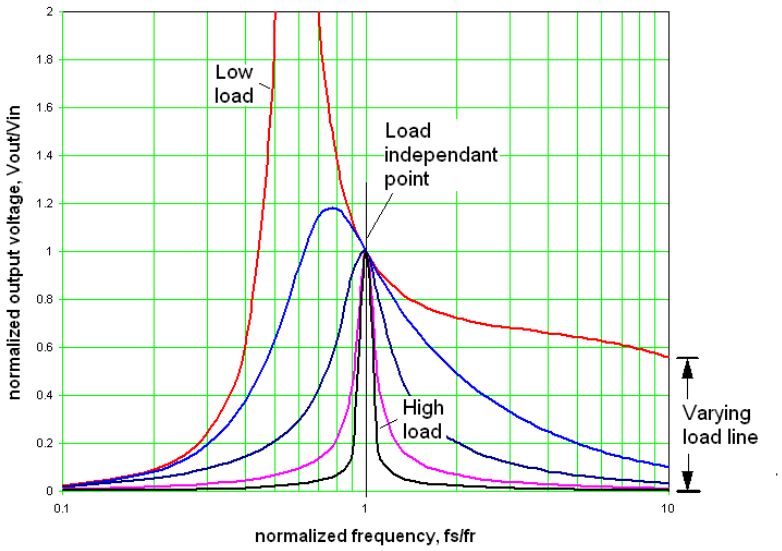


Figure 3 Voltage conversion curve of LLC resonant converter

Drain voltage sensing synchronous controller

The ZXGD3101 synchronous controller provides a solution that avoids the limitations mentioned above, by a scheme utilizing MOSFET voltage sensing, along with an analogue gate drive that is determined by the MOSFET on-state voltage drop.

The configuration in Figure 4 replaces normal diodes on the positive power path with MOSFETs driven by the synchronous controllers. The controller supply voltage is derived through auxiliary windings on the power transformer. Nevertheless, the auxiliary windings only needs to carry a few ten's of mA current. An alternative configuration is to have the synchronous MOSFET on the ground return path. It allows the controller to be powered directly from a low voltage output rail, recommended below 12V, via a drop down transistor at the expense of increasing the risk of ground noise and EMI pollution.

Figure 4 shows the controller monitors the differential voltage across the Drain-Source pin in relation to current flow through the MOSFET and then turns on the MOSFET upon the body diode conduction. The gate drive voltage is then proportional to the Drain-Source reverse voltage, ensuring rapid turn-off as the current decays. Since no timing information needs to be transferred from the primary side and no timing components are needed on the secondary side, the solution is very simple to implement.

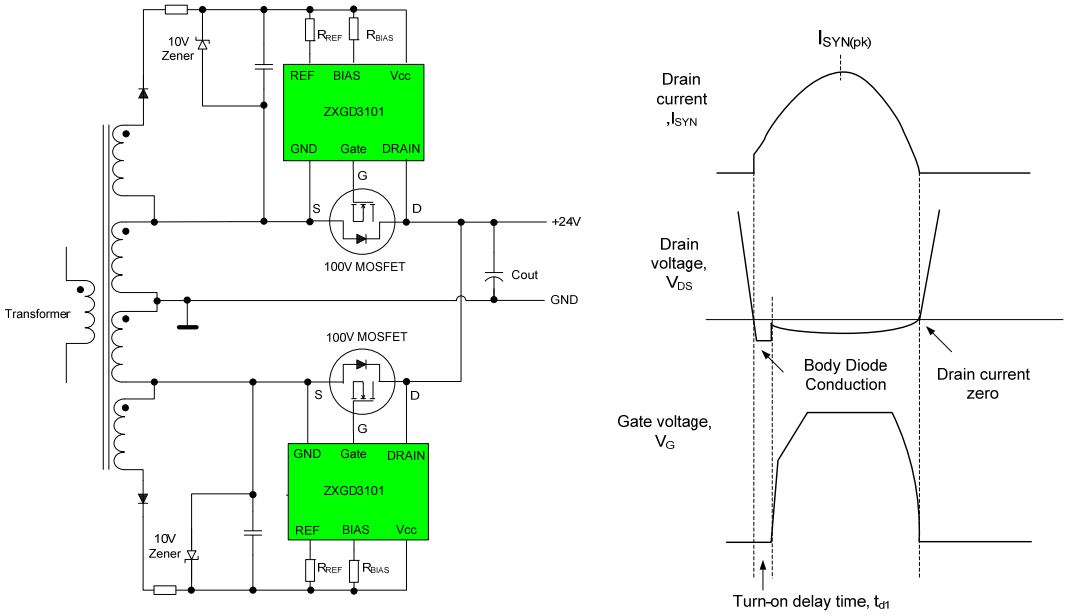


Figure 4 Synchronous rectifications on LLC resonant converter and operating waveforms

It is recommended that the MOSFET on state voltage drop at the peak of the secondary Drain current is equal or less than 100mV. This is to ensure sufficient MOSFET enhancement and to achieve maximum efficiency. Assuming that the LLC resonant tank adequately filters the higher harmonics of the input voltage at full load, the RMS current through the rectifier can be calculated from

$$I_{rms(rect)} = \frac{\pi}{2\sqrt{2}} \times I_{out} = 4.44A$$

From that the I_{rms} through each MOSFET is 2.22A. As the turn on propagation delay t_{d1} of the ZXGD3101 forms a conduction dead band which prevents simultaneous MOSFET conduction, the subsequent body diode conduction loss has been included for loss estimation. The conduction loss in a 100V, $r_{DS(on)@Tj=25ºC}$=16mΩ, Q_g=82nC MOSFET at 100ºC junction temperature is

$$P_{cond} = I_{rms}^{2} \times r_{DS(on)@T_j=100^{\circ}C} + I_{SYN(min)} \times V_{SD(body\_diode)} \times t_{d1} \times f_s$$

$$= 2.22^2 \times 28.8m\Omega + 1A \times 1.2V \times 525ns \times 80kHz = 192mW$$

where $I_{SYN(min)}$ is the MOSFET's current magnitude at the start of the output rectifier conduction cycle. In the example, $I_{SYN(min)}$ is around 1A at full load. Since the body diode turns on prior to the MOSFET conduction and the synchronous MOSFET switches off at zero current, the switching loss can be ignored in the loss estimation. In other words, the MOSFET drastically reduces the power loss in the semiconductor device from 850mW per diode to 192mW per MOSFET. The resulting junction temperature is 95.4ºC at 80ºC ambient in a SO-8 footprint. Taking similar extrapolation, 880mW will need to be dissipated from the synchronous MOSFET in a 10A output converter. The MOSFET if in surface mounted TO-263 footprint could still operate reliably with 37.8ºC junction temperature rise. This reduces the production cost because manufacturing process reduces two-stage to a one-stage assembly as through hole heat sink is not required.

However, the low resistance MOSFET is high on gate charge Qg such that the driving losses could become a critical factor for both light load and full load efficiency at high frequency. The summation of controller operating loss and gate driving loss can be estimated through the equation

$$P_{drv} = I_{op} \times V_{gs} + f_s \times V_{gs} \times Q_g$$

$$= 5.5mA \times 10V + 80kHz \times 10V \times 82nC = 120mW$$

Where I_{op} is the current consumed by the REF and BIAS pin when the controller drives synchronous MOSFET at 50% duty cycle. This loss also reduces the efficiency saving made by the MOSFET low resistance.

Figure 5 compares the efficiency of Schottky diode solution with one that uses 100V 16mΩ MOSFET. The curves show that synchronous rectification improves the conversion efficiency above 25% of the peak loading and the MOSFET solution is more than 1% more efficient at full load. At no load condition, the resonant LLC converter is 4% more efficiency with Schottky rectification.

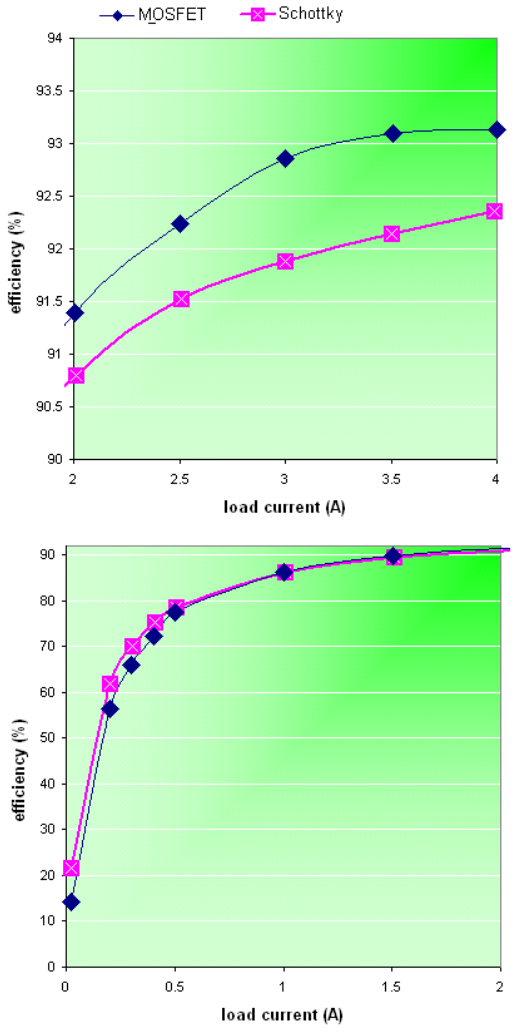
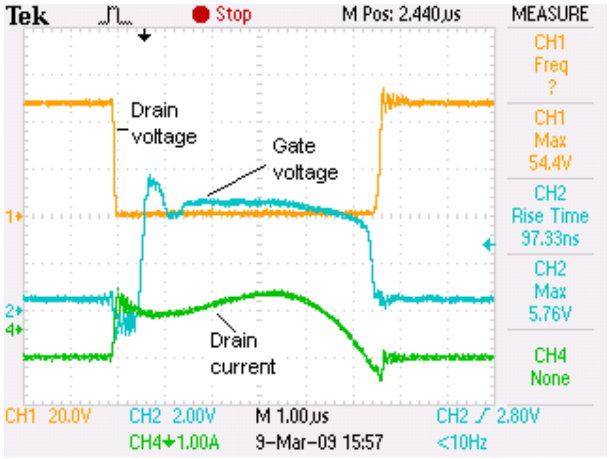


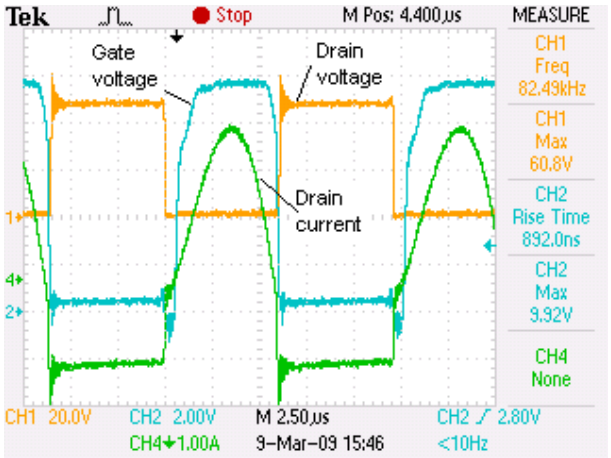
Figure 5 Efficiency comparison between Schottky and MOSFET solution

This is caused by the accumulation of losses associated with the synchronous MOSFET gate charge loss, quiescent power consumption of the ZXGD3101 itself. Although the intrinsic body diode of the MOSFET has to conduct the full rectifier current during the turn on delay, its detrimental effect on the efficiency is low because the rectifier current is normally sinusoidal in shape. The effect will be more prominent at high switching frequency above 200kHz.

Figure 6(a) and (b) shows the actual operating waveforms of the synchronous MOSFET. The Gate voltage was approximately 10V for a sustained period when the MOSFET current was high to achieve low resistance. When the Drain current is low, the Gate voltage then backed off to reduce the effective gate charge so the MOSFET can be turned off quickly at the current zero crossing point.



(a)



(b)

Figure 6 Operating waveforms at (a) 25% load and (b) full load condition

Conclusion

Synchronous MOSFETs will become an essential building block on the secondary side of the high power resonant converter for designing efficient power supplies as motivated by emerging environmental legislation as well as the need for slimmer form factor end product. When used in conjunction with the ZXGD3101 controller, the system offers a higher efficiency than Schottky or standard diodes. This design document describes a built and tested, resonant LLC converter with synchronous rectifier suitable for use in power supply of LCD TV with display screen size below 32 inches. A significant power saving can be achieved with the elaborate scheme especially for high current output converter, MOSFET will generates less heat and surface mounted MOSFET can be used instead of through hole component. This increases power density and reduces assembly cost.

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High Efficiency Optimization of LLC Resonant Converter for Wide Load Range

Ya Liu

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

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in
Electrical Engineering

Dr. Ming Xu, Chairman
Dr. Fred C. Lee
Dr. Fei (Fred) Wang

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High Efficiency Optimization of LLC Resonant Converter for Wide Load Range

Ya Liu

Abstract

As information technology advances, so does the demand for power management of telecom and computing equipment. High efficiency and high power density are still the key technology drivers for power management for these applications. In order to save energy, in 2005, the U.S. Environmental Protection Agency (EPA) announced the first draft of its proposed revision to its ENERGY STAR specification for computers. The draft specification separately addresses efficiency requirements for laptop, desktop, workstation and server computers. The draft specification also proposes a minimum power supply efficiency of 80% for PCs and 75% to 83% for desktop derived servers, depending on loading condition and server type. Furthermore, recently some industry companies came out with a much higher efficiency target for the whole AC/DC front-end converter over a wide load range.

Distributed power systems are widely adopted in the telecom and computing applications for the reason of high performance and high reliability. As one of the key building blocks in distributed power systems, DC/DC converters in the front-end converter are also under the pressure of increasing efficiency and power density. Due to the hold-up time requirement, PWM DC/DC converters cannot achieve high

efficiency for well known reasons when they are designed for wide input voltage range.

As a promising topology for this application, LLC resonant converters can achieve both high efficiency and wide input voltage range capability because of its voltage gain characteristics and small switching loss. However, the efficiency of LLC resonant converter with diode rectifier still cannot meet the recent efficiency target from industry. In order to further improve efficiency of LLC resonant converters, synchronous rectification must be used. The complete solution of synchronous rectification of LLC resonant converters is discussed in this thesis. The driving of the synchronous rectifier can be realized by sensing the voltage V_{ds} of the SR. The turn-on of the SR can be triggered by the body-diode conduction of the SR. With the V_{ds} compensation network, the precise voltage drop on R_{ds_on} can be achieved, thus the SR can be turned off at the right time. Moreover, efficiency optimization at normal operation over wide load range is discussed. It is revealed that power loss at normal operation is solely determined by the magnetizing inductance while the magnetizing inductor is designed according to dead-time t_d selection. The mathematic equations for the relationship between power loss and dead-time are developed. For the first time, the relationship between power loss and dead-time is used as a tool for efficiency optimization. With this tool, the efficiency optimization of the LLC resonant converter can be made according to efficiency requirement over a wide load range. With the expectation to achieve high efficiency at ultra-light load, the green mode operation of LLC resonant converters is addressed. The rationale of the issue with

the conventional control algorithm is revealed and a preliminary solution is proposed.

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Chapter 1 Introduction

1.1 Background and Research Objective

The demands on power supplies for telecom and computer server applications advance with the advancement of information technology. Power-system design for these applications has long been dominated by such issues as efficiency, thermal management, voltage regulation, reliability, power density, and cost. Going forward, these factors will remain critical. A typical breakdown of electricity use and power consumption in data center equipment is shown in Figure 1-1 and Figure 1-2. It can be observed that computer servers consume more than half of the total energy. Unfortunately, while data centers are booming over the world, the power delivery efficiency for data centers as shown in Figure 1-3 is only around 50%.

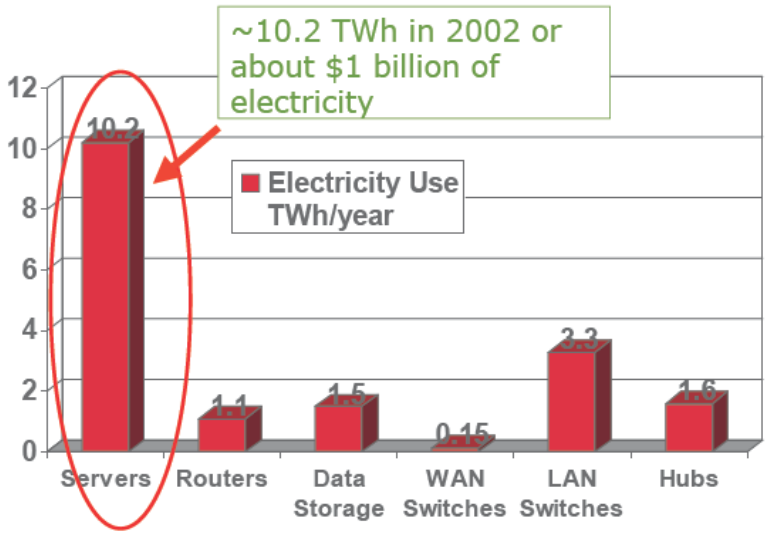


Figure 1.1 Electricity Use in data center equipment

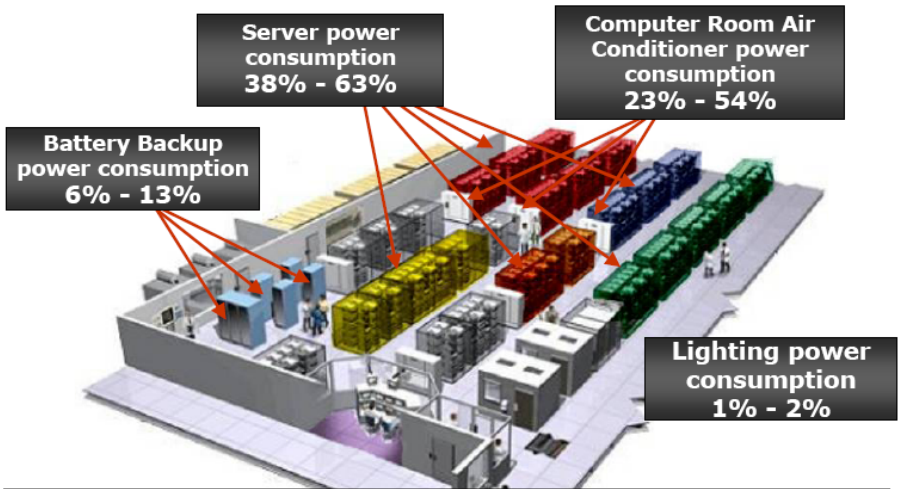


Figure 1.2 Power consumption breakdown in data center

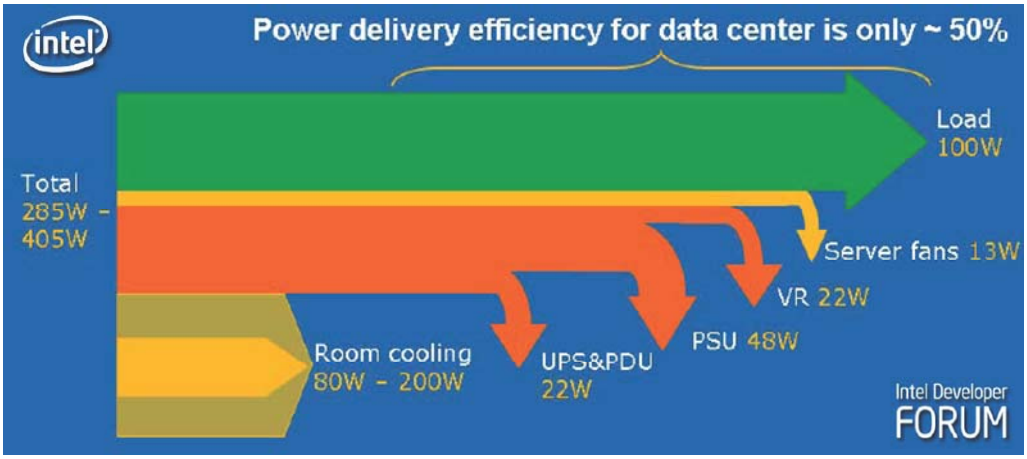


Figure 1.3 Power delivery in data center

In order to save energy consumption in data centers, high efficiency for power management, especially in power supplies for servers, is required. In February 2005, the U.S. Environmental Protection Agency (EPA) announced the first draft of its proposed revision to its ENERGY STAR specification for computers. The draft specification separately addresses efficiency requirements for laptop, desktop, workstation and server computers. It includes provisions for maximum allowable

power consumption in standby mode, sleep mode and idle state. The draft specification also proposes a minimum power supply efficiency of 80% for PCs and 75% to 83% for desktop derived servers, depending on loading condition and server type. Furthermore, with the increasing emphasis of saving energy and extending the battery life, achieving high efficiency, both at full load and light load is required. Recently some industry companies brought out even higher efficiency requirements for front-end AC/DC converters in computer servers as shown in Figure 1-4. Full load is not the only load condition with a high efficiency target any more. High efficiency over a wide load range is now a requirement.

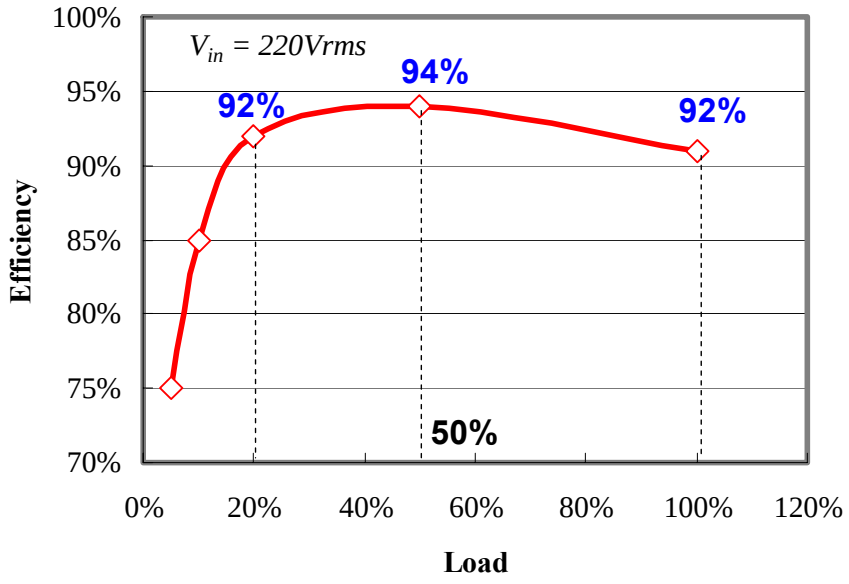


Figure 1.4 Efficiency target from Industry for Front-end AC/DC converter

In the current power management architecture for servers, distributed power systems are widely adopted for the reasons of high performance and high reliability [1.1] [1.2] [1.3]. In a distributed power system, input ac voltage goes through the

front-end converters, which includes PFC and DC/DC converters, then the generated 48V or 12V bus voltage from front-end converters is transferred and converted into voltages by the downstream on-board voltage regulators for final loads. As one of the key building blocks, the DC/DC converter in the front-end converter is also under the pressure of increasing efficiency and power density.

Due to the holdup time requirement, as shown in Figure 1-5, bulk capacitors, also called holdup time capacitors are normally put at the input of DC/DC converter. The holdup time requirement states that when the input ac line is lost, the DC/DC converter can keep its regulated output voltage for 20ms. During the holdup time, the input of DC/DC converter keeps dropping while the output of the DC/DC converter is regulated until the minimum input voltage is reached. After the holdup time, the DC/DC converter can be shut down.

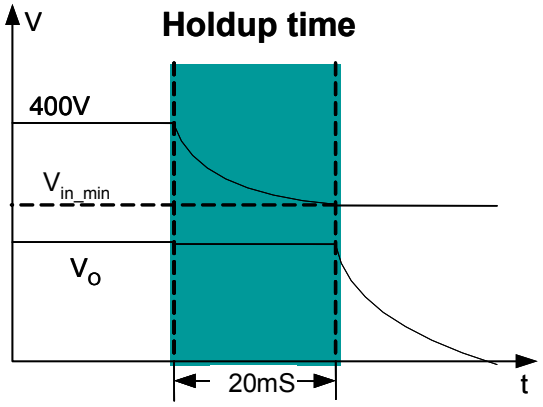


Figure 1-5. Holdup time requirement for front-end DC/DC converter

The relationship between the allowable minimum input voltage for the DC/DC converter and the required holdup time capacitor is determined by the following equation

$$\frac{1}{2}C_h(V_{in}^{\ 2}-V_{in\_\min}^{\ 2})=P_{DC}T_h$$

Here V_{in} is the nominal input of the DC/DC converter, V_{in_min} is the allowable minimum input of the DC/DC converter, C_h is the required holdup time capacitor, P_{DC} is the power of the DC/DC converter and T_h is the holdup time. It can be observed from this equation that the lower the allowable minimum input voltage, the smaller the holdup time capacitor required. Therefore, a DC/DC converter with wide input voltage range capability is preferred.

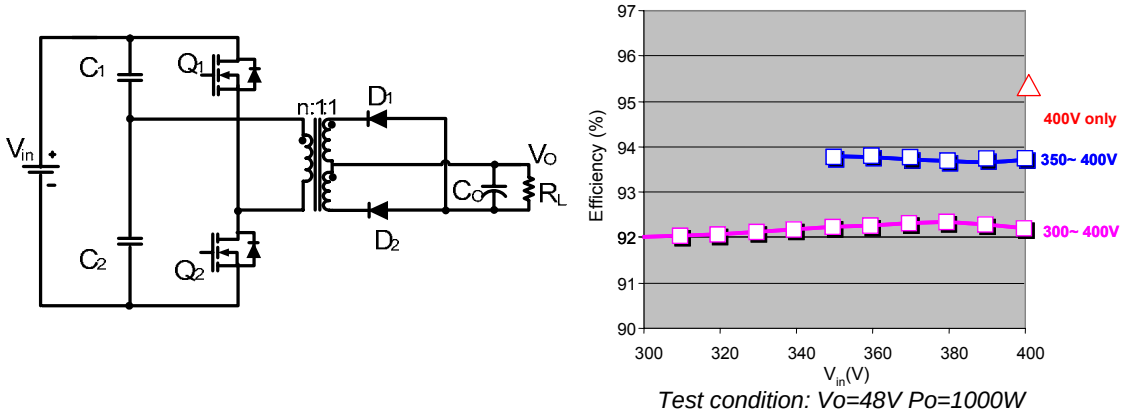


Figure 1-6. Efficiency of asymmetrical half-bridge DC/DC converter

PWM DC/DC converters cannot achieve high efficiency and wide input voltage range at the same time [1-4]. For example, it is desirable for asymmetrical half bridge to operate with 50% duty cycle because maximum efficiency can be achieved [1-5]. However, in order to accommodate a wide input voltage range due to the holdup time requirement, the duty cycle at normal operation has to be less than 50% to regulate output voltage. Efficiency data of a 200 kHz, 1kW 400V to 48V output asymmetrical half bridge is shown in Figure 1-6. 95.4% efficiency can be achieved

when it is optimized only for 400V input. However, when it is designed for 300V to 400V input range, efficiency at 400V drops to only 92.2%.

Great efforts have been spent to achieve both high efficiency and wide input voltage range for PWM converters [1-6] [1.7]. Although these solutions can result in good steady-state performance, they are difficult to adopt in industry because of complex circuit structure and concern on transient performance. As a promising topology for this application, the LLC resonant converter, shown in Figure 1-7, can achieve both high efficiency and wide input voltage range capability.

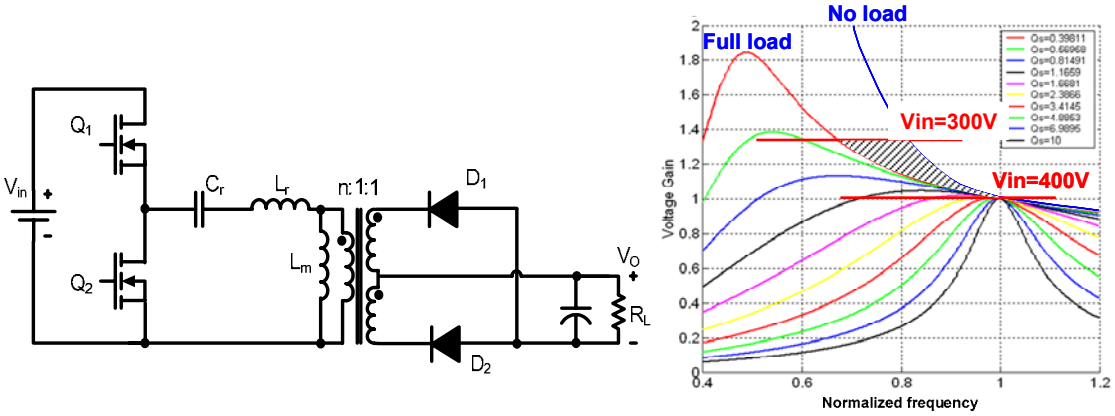


Figure 1-7. LLC resonant converter for Front-end DC/DC converter

The voltage gain characteristic of the LLC resonant converter makes it a very good candidate for a front-end DC/DC converter. LLC is designed to operate at resonant frequency for normal operation. During the holdup time, the output of LLC resonant converter can be regulated by decreasing its switching frequency to achieve higher voltage gain as shown in Figure 1-7. Besides the desirable voltage gain characteristics, small switching loss is another benefit of LLC resonant converters. For primary switches, ZVS turn-on can be achieved for the whole load

range with small turn-off current which is the peak magnetizing current. On the secondary side, rectifiers are turned off with low di/dt, so small switching loss can be achieved. Due to these well-know merits, the LLC resonant converter can achieve high efficiency. Figure 1-8 demonstrates this by showing the efficiency comparison of the LLC resonant converter vs. the asymmetrical half-bridge converter. For the same input voltage range, 300V to 400V, around 3.5% higher efficiency can be achieved with the LLC resonant converter with normal operation at 400V input where the converter is operated most of the time.

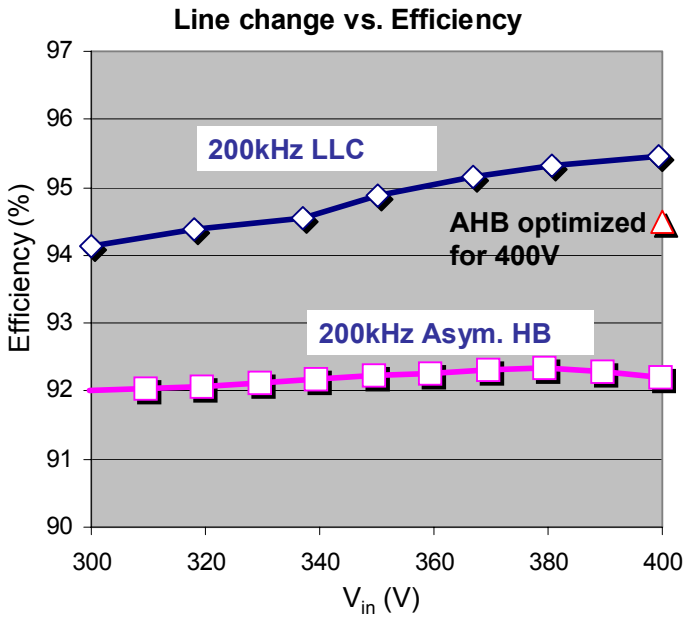


Figure 1-8

Efficiency comparison of LLC resonant cocnverter and asymmetrical half-bridge converter

Because of small switching loss and desirable voltage gain characteristics, high switching frequency can further increase the power density. Figure 1-9 is one example of a 1MHz, 1kW, 400V to 48V LLC resonant converter prototype with diode

rectifier developed by Dr. Lu [1.8]. High power density (76W/in^3) and wide input voltage range (300V to 400V) can be achieved on this prototype.

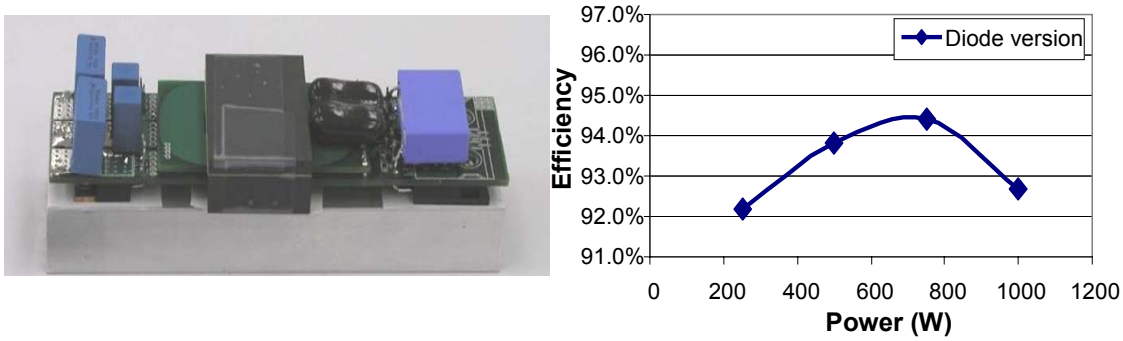


Figure 1-9. 1MHz, 1kW 400V to 48V LLC resonant converter

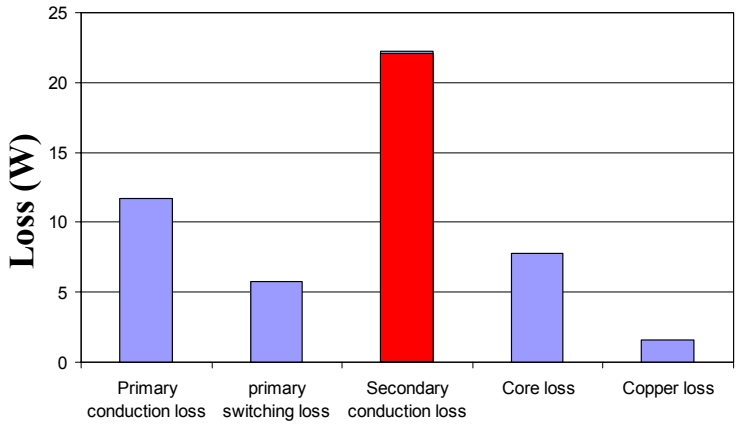


Figure 1-10. Loss breakdown of 1kW LLC DC/DC converter w/ diode rectifier

It can be observed that although high power density and wide input voltage range can be achieved with a high switching frequency LLC resonant converter, efficiency is not good enough as shown in Figure 1-9. For example, with this prototype only 92.6% efficiency can be achieved at full load while the target efficiency for the whole AC/DC converter (PFC+DC/DC) at full load as shown in Figure 1-4, is 92%. From the full load loss breakdown for this 1MHz LLC resonant

converter as shown in Figure 1-10, it is obvious that the secondary conduction loss is the highest loss part. In order to further improve the efficiency of LLC resonant converters, synchronous rectification should be applied. Unfortunately, there are few sources in the literature that address how to drive synchronous rectifiers for LLC resonant converters. Furthermore, efficiency at half load and light load conditions also need to be improved when comparing efficiency of this LLC resonant converter with the target efficiency curve shown in Figure 1-4. There are some papers on how to design LLC resonant converters; however, few papers address how to design LLC resonant converters for high efficiency over a wide load range.

This thesis focuses on the above two issues: driving of the synchronous rectifier in LLC resonant converters, and the design of LLC resonant converter for high efficiency over a wide load range with dead-time optimization and green mode operation.

1.2 Thesis Outline

This thesis contains 5 chapters.

Chapter one gives an introduction to Front-end DC/DC converters in Distributed Power Systems that are widely adopted in telecom and computing equipment. The challenges and problems with state-of-the-art practice are also discussed. LLC resonant converters are a promising candidate to solve these challenges.

Chapter two gives a review of the LLC resonant converter. For application of the LLC resonant converter as Front-end DC/DC converter, it operates at resonant

frequency in normal operation and operates at switching frequency smaller than the resonant frequency during holdup time. The performance of LLC resonant converters in normal operation and holdup time is discussed in this chapter.

In chapter three, the complete solution of synchronous rectification of LLC resonant converter is discussed. The driving of the synchronous rectifier can be realized by sensing the voltage V_{ds} of the SR. The turn-on of the SR can be triggered by the body-diode conduction of the SR. With the V_{ds} compensation network, the precise voltage drop on R_{ds_on} can be achieved, thus the SR can be turned off at the right time. Compared with the diode version, more than 3% efficiency is achieved at full load for LLC resonant converter with synchronous rectification.

In chapter four, efficiency optimization at normal operation over wide load range is discussed. It is revealed that power loss at normal operation is solely determined by magnetizing inductor while magnetizing inductor is designed according to dead-time t_d selection. The relationship between power loss and dead-time provides a tool for efficiency optimization. With this tool, efficiency optimization of the LLC resonant converter can be done according to efficiency requirement for wide load range.

In chapter five, a summary related to this topic is discussed. An approach with digital control is expected to have perfect turn-on and turn-off timing for the synchronous rectifier of the LLC resonant converter. In order to meet the high efficiency requirement at ultra-light load or the minimum power consumption requirement at no load, green mode operation of the LLC resonant converter is

discussed. The rationale of the issue with the state-of-the-art control algorithm is revealed and a preliminary solution is proposed.

Chapter 2 Review of LLC Resonant Converter

2.1 Principles of Operation

Figure 2-1 shows the half-bridge LLC resonant converter, along with the definitions for the resonant frequency f_0, the quality factor Q and the ratio L_n between the magnetizing and resonant inductors, L_m and L_r. The gain characteristics of LLC resonant converter at different loads are shown in Figure 2-2, where the voltage gain is defined as $nV_O/(V_{in}/2)$ due to the half bridge structure, the normalized frequency f_n is defined as f_S/f_0.

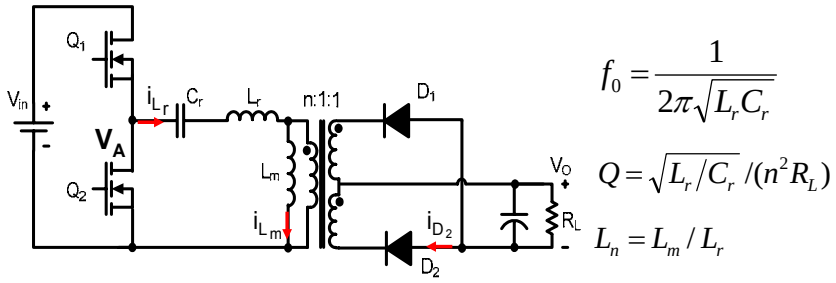


Figure 2-1. LLC resonant converter

It can be seen from Figure 2-2 that the voltage gain is equal to 1 for all load conditions at the resonant frequency. When the switching frequency is higher than the resonant frequency, the gain is always less than 1, and the zero voltage switching (ZVS) for primary switches can be achieved. When the switching frequency is lower than the resonant frequency, either ZVS or the zero current switching (ZCS) for the primary switches can be achieved. For MOSFETs, the ZVS operation is preferred. The gain will be always higher than 1 if the converter works

with ZVS operation when the switching frequency is lower than the resonant frequency.

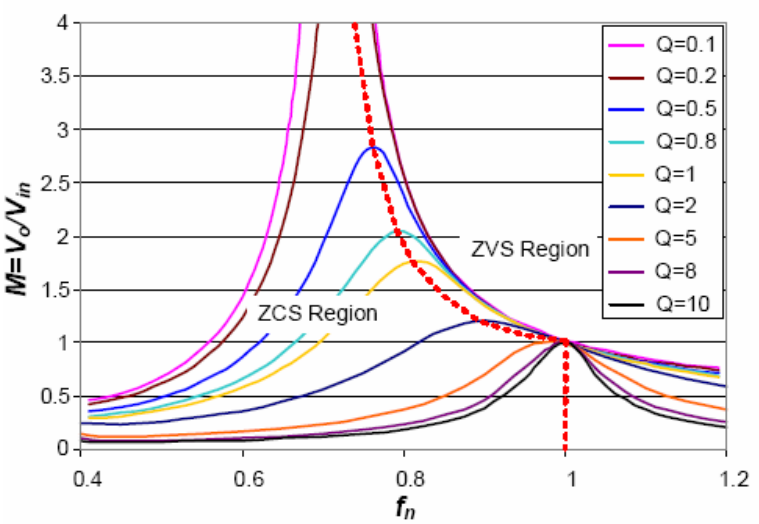


Figure 2-2. Voltage gain characteristics of LLC resonant converter

There are several ZVS operation modes of LLC resonant converter according to the relationship of switching frequency to resonant frequency. Figure 2-3 shows the operation principle of LLC resonant converter at the resonant frequency.

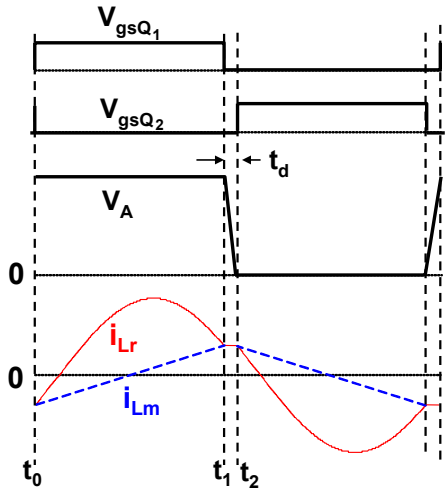


Figure 2-3. Waveforms with $f_S=f_0$

Between time t_0 and t_1, primary switch Q_1 is conducting. On the secondary side, the diode D_2 is conducting according to the polarity of voltage on transformer winding. During this period the energy is transferred from the primary side to the output load. The magnetizing current is linearly increasing with the excitation of the reflected output voltage. At t_1, when the resonant tank current reaches the magnetizing current, the primary switch Q_1 is turned off. During the dead-time in which both primary drive signals are low, the magnetizing current discharges the junction capacitor of primary switches so that at the time t_2, the primary switch Q_2 can be turned on with ZVS. From the time t_2, the other half switching period begins.

When LLC resonant converter operates at the resonant frequency, the timing of turn-off of primary switches is exactly the same as the timing where the resonant tank current reaches magnetizing current. The turn-off current of primary switches is the peak magnetizing current which realizes the ZVS of primary switches.

Operation waveforms for cases $f_S<f_0$ and $f_S>f_0$ are shown in Figure 2-4(a) and 2-4(b) respectively. For the case $f_S<f_0$, the energy is transferred to the output load during the time period of t_0~t_1. The resonant tank current reaches magnetizing current before the turn-off of primary switch. Between time t_1 and t_2, the magnetizing inductor participates in resonance. During this time period, the magnetizing inductor L_m paralleling with the resonant inductor L_r resonates with the resonant capacitor C_r. The turn-off current of primary switches is the peak magnetizing current for this operation mode. When LLC resonant converters operate at $f_S>f_0$, the resonant tank current is higher than the magnetizing current when the primary switch is turned off. The current difference between the resonant tank current and the magnetizing

current at turn-off of primary switch is determined by the load condition and the **distance of** the switching frequency from the resonant frequency. In this operation mode, at the same load condition, the turn-off current in primary switch is higher than that in operation modes $f_S=f_0$ and $f_S<f_0$. The larger turn-off current leads to an excessive turn-off loss in primary switches. Furthermore, secondary side diodes are turned off with a larger di/dt which may causes a higher reverse recovery loss and a higher voltage stress on diodes. Therefore, the operation at $f_S>f_0$ is not preferred.

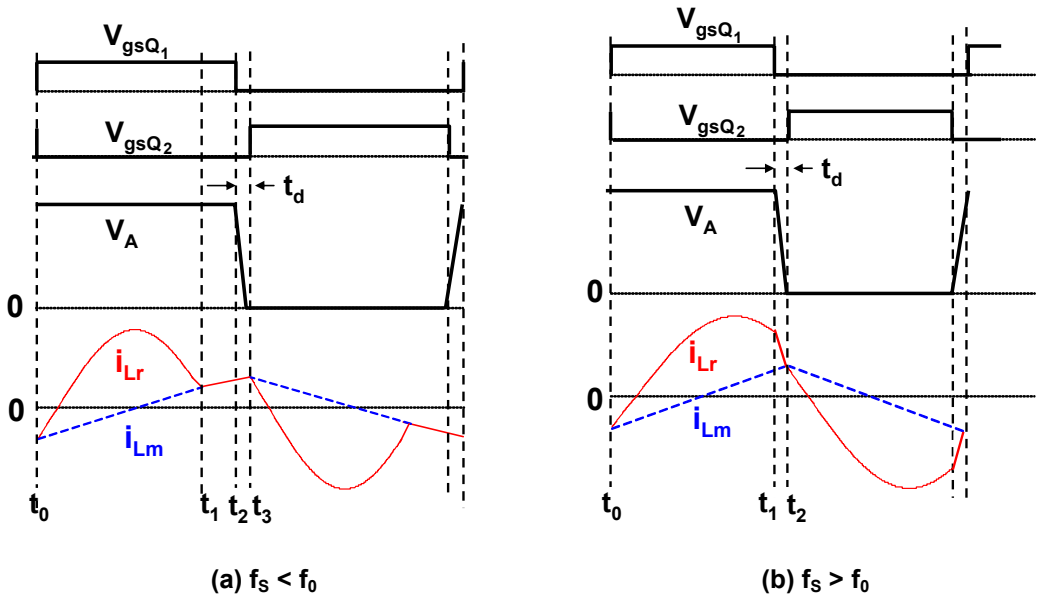


Figure 2-4. Operation waveforms of LLC resonant converter

When LLC resonant converters are designed as DC/DC converters in front-end converters, the converters can be designed to work at the resonant frequency in normal operation to achieve a high efficiency while keeping the output voltage regulated by decreasing switching frequency when the input voltage drops in the hold-up time.

2.2 Performance Analysis of LLC Resonant Converter

Since LLC resonant converters operate at the resonant frequency in the normal operation and operate at $f_S<f_0$ during the holdup time, it is necessary to have an analysis of performance for these two cases. At the resonant frequency, if dead-time is neglected, the resonant tank current will be sinusoidal and the magnetizing current is triangular as shown in Figure 2-5.

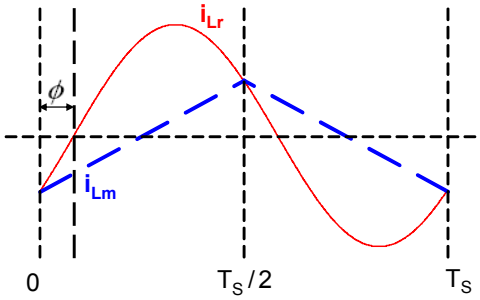


Figure 2-5. Resonant tank current and magnetizing current at resonant frequency

The resonant tank current i_{Lr} can be expressed as

$$i_{Lr}(t)=\sqrt{2}I_{RMS\_P}\sin(\omega_0 t+\Phi)$$

Where I_{RMS_P} is the resonant tank RMS current, ω_0 is the angle frequency of the resonant frequency, and Φ is the initial angle of i_{Lr}. At the resonant frequency, the magnetizing inductor is charged and discharged by the output voltage during half of the resonant period. The magnetizing inductor can be represented as

$$i_{Lm}(t)=-i_{Lm\_m}+\frac{nV_0}{L_m}(t-NT_S) \qquad \text{when } NT_S \le t < \left(N+\frac{1}{2}\right)T_S$$

$$i_{Lm}(t)=i_{Lm\_m}-\frac{nV_0}{L_m}\left[t-(n+\frac{1}{2})T_S\right] \qquad \text{when} \left(N+\frac{1}{2}\right)T_S \le t < (N+1)T_S$$

Where i_{Lm_m} is the peak magnetizing current, n is the transformer turns-ratio, V_0 is the output voltage, L_m is the magnetizing inductance, N is an integer, and T_S is the switching period. The peak magnetizing current is calculated as

$$i_{Lm\_m} = \frac{nV_0}{L_m} \cdot \frac{T_S}{4}$$

Based on the circuit characteristic of LLC resonant converters, at the beginning of each switching cycle, the resonant tank current is equal to the magnetizing current. Therefore, the resonant tank current at the beginning of each cycle is

$$i_{Lr}(t_0) = \sqrt{2} I_{RMS\_P} \sin(\Phi) = -\frac{nV_0}{L_m} \cdot \frac{T_S}{4}$$

The difference between the resonant tank current i_{Lr} and the magnetizing current i_{Lm} is the current that goes through the secondary side. So the following relationship stands,

$$\frac{\int_0^{\frac{T_S}{2}} \left[\sqrt{2} I_{RMS\_P} \sin(w_0 t + \Phi) + \frac{nV_0}{L_m} \cdot \frac{T_S}{4} - \frac{nV_0}{L_m} t \right] dt}{T_S / 2} = \frac{V_0}{nR_L}$$

In this equation, R_L is the load resistance. The RMS current of resonant tank thus can be derived as

$$I_{RMS\_P} = \frac{1}{4\sqrt{2}} \frac{V_0}{nR_L} \sqrt{\frac{n^4 {R_L}^2 {T_S}^2}{{L_m}^2} + 4\pi^2}$$

The resonant tank current continues going through the primary switches, so this RMS current determines the primary side conduction loss.

Besides the primary side conduction loss, the secondary side conduction loss also needs to be investigated especially for low output voltage high output current applications. It is very desirable to minimize the secondary side RMS current. In order to achieve a higher efficiency, synchronous rectification is preferred. The current in synchronous rectifier (SR) is the difference between the resonant tank current and the magnetizing current, then the RMS current in SR can be calculated based on the RMS current definition,

$$I_{RMS\_S} = \sqrt{\frac{\int_0^{\frac{T_S}{2}} \left[i_{Lr}(t) - i_{Lm}(t) \right]^2 dt}{T_S / 2}}$$

The closed-form equation can be expressed as,

$$I_{RMS\_S} = \frac{\sqrt{3}}{24\pi} \frac{V_0}{R_L} \sqrt{\frac{(5\pi^2 - 48) n^4 R_L{}^2 T_S{}^2}{L_m{}^2} + 12\pi^4}$$

From the equations of primary and secondary side RMS current, it can be observed that both primary side and secondary side RMS currents, thus conduction loss, are entirely determined by the magnetizing inductor. Since the magnetizing inductor also determines the turn-off current of primary switches, the turn-off loss can also be minimized by the design of magnetizing inductor. The design of magnetizing inductor is the key for minimum power loss in normal operation.

During the 20ms holdup time, input voltage of LLC resonant converter keeps dropping. In order to regulate output voltage, the switching frequency of LLC resonant converter is reduced to have a higher voltage gain. For the operation at $f_S < f_0$, the effective duty cycle for energy transferring is smaller compared with that at

the resonant frequency. So the efficiency during holdup time operation is lower. However, since this holdup time is only 20ms, the excessive loss will not cause a thermal issue.

The minimum input voltage determines the required peak gain for LLC resonant converters as shown in Figure 2-6. It can be seen that the lower allowable minimum input voltage, the smaller the holdup time capacitor required. Once a minimum input voltage is selected, the required peak gain is determined.

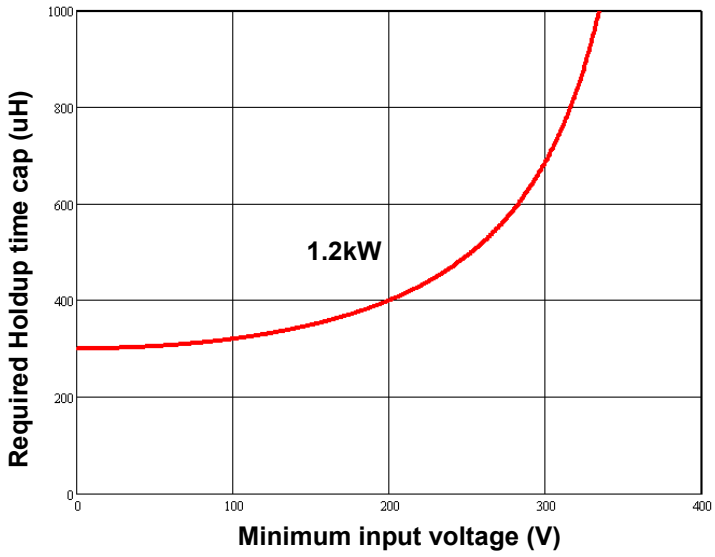
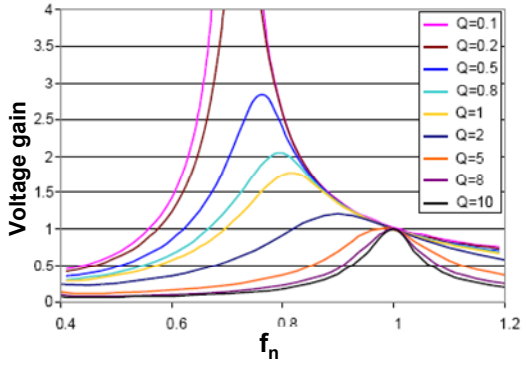


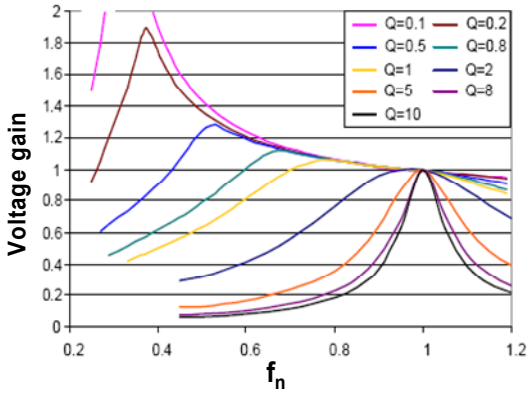
Figure 2-6. Holdup time capacitor vs. minimum input voltage

The voltage gain at resonant frequency is always equal to 1 for any different L_n and Q combinations. However, the gain curve shape and the achievable peak gain for different L_n and Q design are different. Some gain curves are shown in Figure 2-7 for different L_n and Q combinations. It can be observed that the frequency for peak gain is below resonant frequency and it is the boundary of ZCS and ZVS modes. Moreover, with a larger L_n, the distance between the peak-gain frequency and

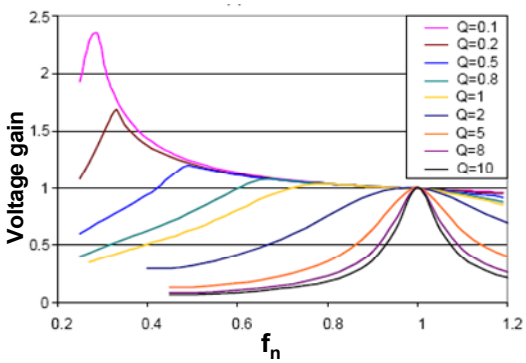
resonant frequency is larger. Each L_n and Q combination gives one peak gain as shown in Figure 2-7. Therefore, a 3D peak gain surface can be drawn as shown in Figure 2-8 by collecting all peak gain values for different L_n and Q combinations.



(a) L_n=4



(b) L_n=10



(c) L_n=15

Figure 2-7. Gain curves with different L_n and Q

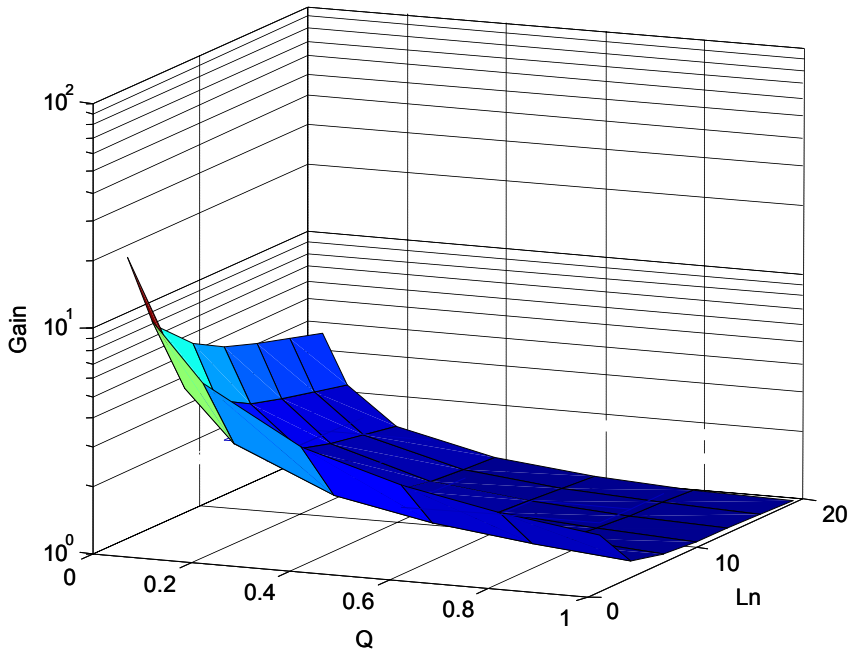


Figure 2-8. Peak gain for different L_n and Q

Chapter 3 Synchronous Rectification of LLC Resonant Converter

3.1 Introduction

With the development of power conversion technology, high efficiency is still the major driver for the front-end DC/DC converter in the computing and telecom equipments. Although LLC resonant converters have been accepted by the industry as a promising topology for the front-end DC/DC converters and lots of efforts have been made to optimize the design of LLC resonant converters [3.1] [3.2] [3.3], very few literatures address the issues and solutions of LLC resonant converters with synchronous rectifier (SR).

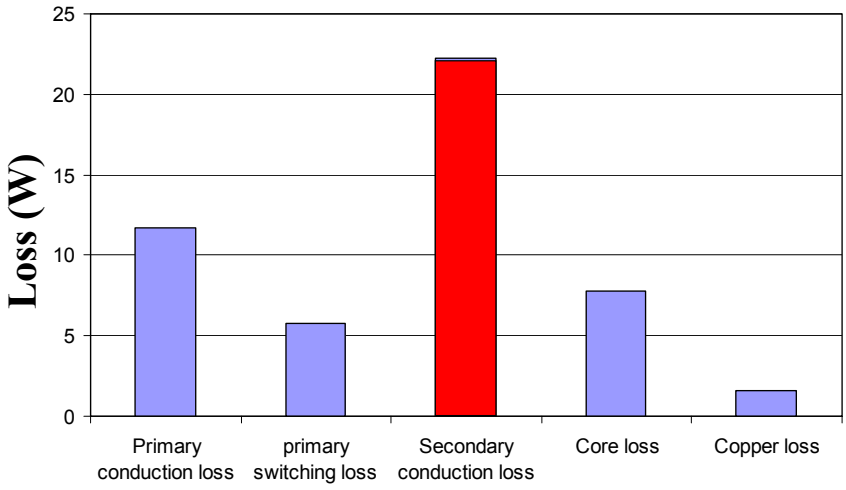


Figure 3-1. Loss breakdown of 1kW LLC DC/DC converter w/ diode rectifiers

Figure 3-1 shows the power loss breakdown at the full load of a 1KW 1MHz LLC resonant DC/DC converter with diode rectifiers. It is easy to observe that the secondary conduction loss is the highest loss part. In order to further improve the

efficiency of LLC resonant converter, the reduction of the secondary conduction loss should be the first target.

In this chapter, firstly, a brief review of SR driving methods for PWM converters is discussed. Then issues of synchronous rectifier driving for LLC resonant converter are discussed. After that, one method to drive synchronous rectifier for LLC resonant converters is developed to achieve high efficiency. Finally, some improvements to the driving method are proposed and experimentally verified by considering the inherent propagation delay of commercial IC and discrete MOSFET drivers.

3.2 Methods of Driving Synchronous Rectifier (SR)

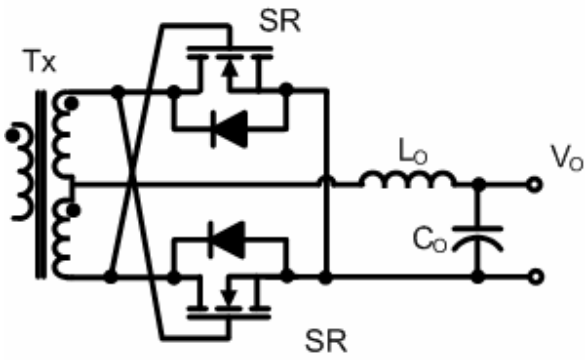
3.2.1 Driving of SR for PWM Converters

Efforts to develop and improve SR performance by improving SR driving schemes never stop since the first day when the synchronous rectification is applied to power conversion. For PWM converters, the technology of SR driving is quite mature after dozens of years' efforts. There are hundreds of papers talking about how to drive SR in PWM topologies. From the driving mechanism point of view, those driving methods can be roughly categorized into self-driven method and externally driven or control-driven method.

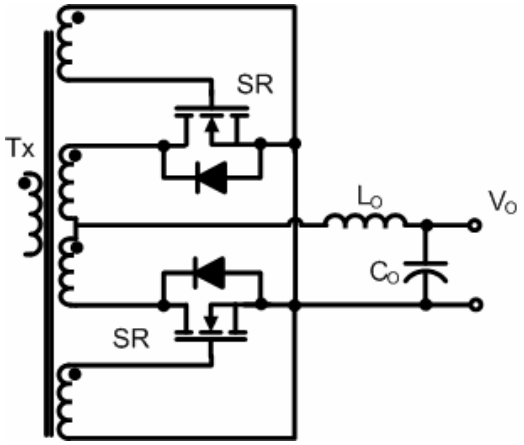
For the self-driven method in PWM converters, there are two sub-categories called voltage self-driven and current self-driven depending on the SR drive signals derived from voltage or current information. Figure 3-2 shows four general voltage self-driven schemes for synchronous rectifier [3.4] ~ [3.10]. The simplest one is gate-

drain cross-coupled connection scheme as shown in Figure 3-2 (a). For the very low or very high output voltage applications, the voltage on secondary winding of power transformer is too low or too high for SR driving. An auxiliary drive winding can be added to drive SR as shown in Figure 3-2 (b). An alternative SR driving way for high output voltage application is to put a capacitor in series in the drive loop of SR as shown in Figure 3-2 (c). Instead of directly deriving SR drive signals from secondary winding of power transformer, the auxiliary drive winding coupled with output filter is another option as shown in Figure 3-2 (d). In some applications, this scheme has some merits compared with the other three schemes. For example, in Forward converter, the drive signal of free-wheeling SR depends on the reset method of the power transformer if SRs are driven with the first three driving schemes shown in Figure 3-2. Only with active-clamp forward, good drive signal can be achieved for the free-wheeling SR. But with the drive scheme in Figure 3-2(d), a good drive signal for free-wheeling SR can always be achieved.

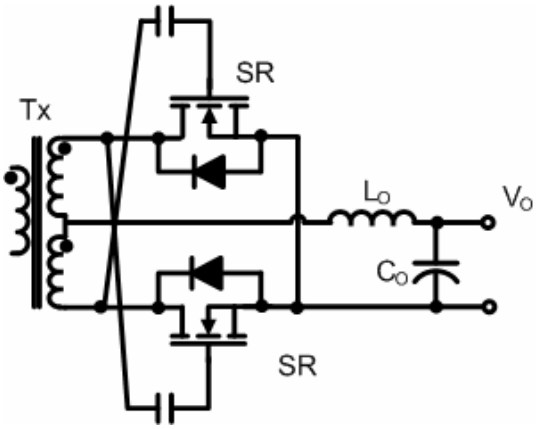
The advantage of voltage self-driven scheme is the simplicity and low cost. But this drive method is limited to topologies. For some topologies such as Flyback (especially in DCM), this drive scheme does not work. Also applicability of voltage self-driven method is limited by the input voltage range of converters.



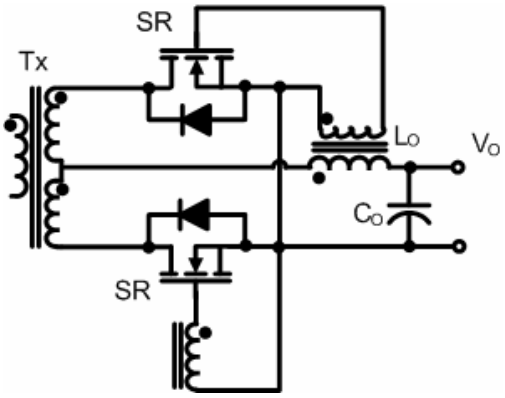
(a)



(b)



(c)



(d)

Figure 3-2. Voltage self-driven synchronous rectifier

Instead of deriving SR drive signals from voltage in power stage, the current self-driven method is to get SR drive signals by sensing the current going through SR [3.11] [3.12]. One typical current self-driven scheme is shown in Figure 3-3. A current-sensing transformer is placed in series with SR to monitor SR current [3.6]. The key advantage of this driving method is that it is not limited to topologies. Theoretically, this method can be applied to any topology because it directly controls the on and off of SR with current information from SR itself. The other advantage is that the drive voltage is constant. However, there are some limitations for this driving method in high switching frequency and high power density applications. The inductance in series with the synchronous rectifier, introduced by the current-sensing transformer, would be detrimental to current commutation in the rectifier.

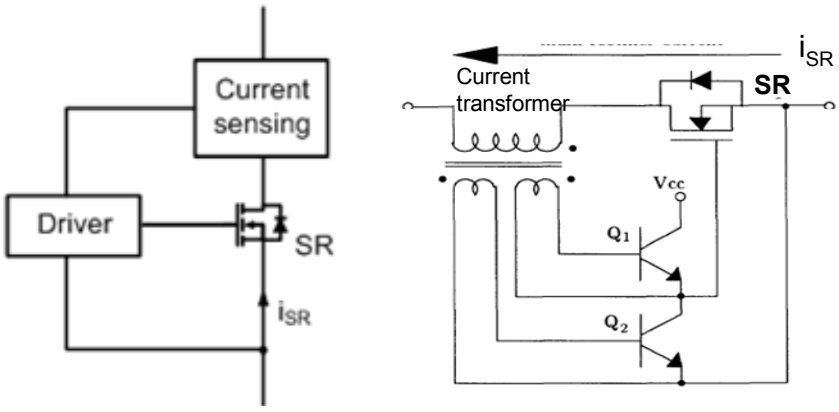
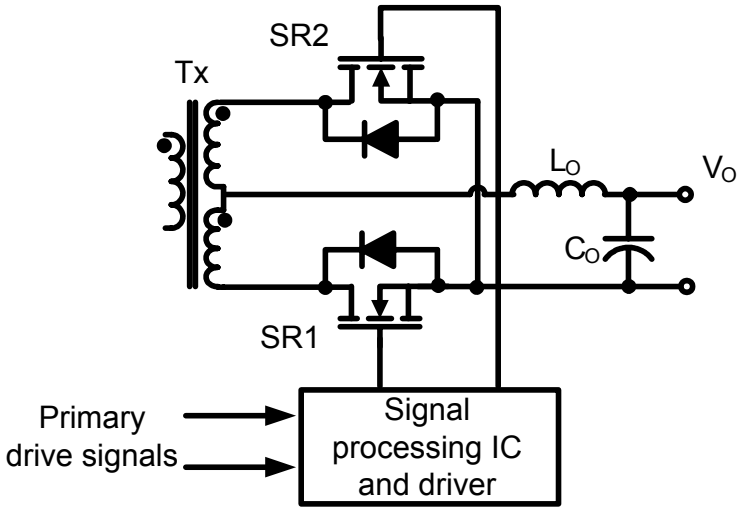


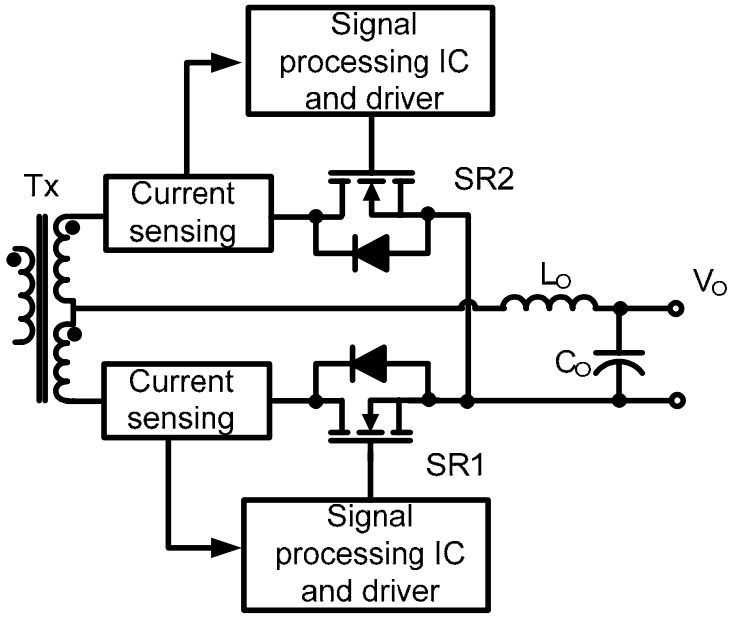
Figure 3-3. Current self-driven synchronous rectifier

Externally driven scheme is the other big category of driving schemes for the SR [3.13]~[3.15]. For this driving method, the voltage or current information firstly is processed by the commercial IC, and then the controlled drive pulse is delivered to the followed driver which finally drives SRs. The externally driven scheme can be realized by processing the dual drive signal of primary switch drive signal for some single-end converters, or directly processing primary drive signals for some double-end converters and bridge type converters as shown in Figure 3-4(a). Similarly, another way to realize the external driven scheme is to sense current information of the SR, and then the sensed current information is processed by commercial IC and thus controlling the switching of the SR. Two options of externally driven schemes by sensing SR current are shown in Figure 3-4(b) and (c). The advantage of the externally driven scheme is the compact size of the drive circuit because of the advanced integration technology. However, this advantage also leads to the high cost. The other drawback for the externally driven scheme is that in order to have

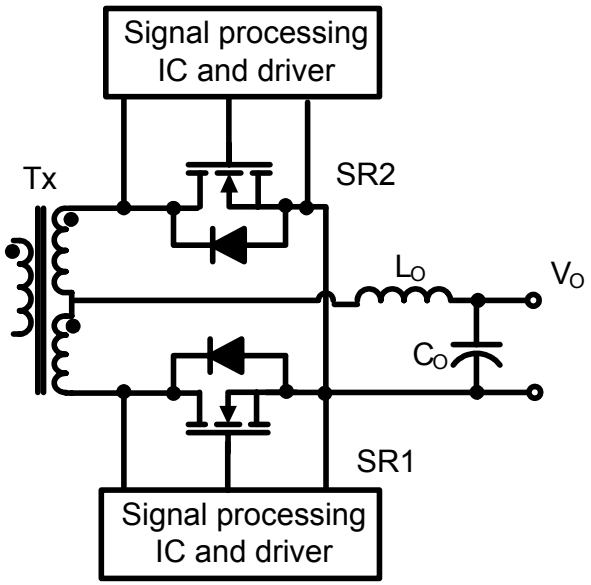
high reliability, a large dead-time is generally inserted between drive signals, which lead to large SR body-diode conduction loss.



(a) Externally driven synchronous rectifier method 1



(b) Externally-driven synchronous rectifier method 2

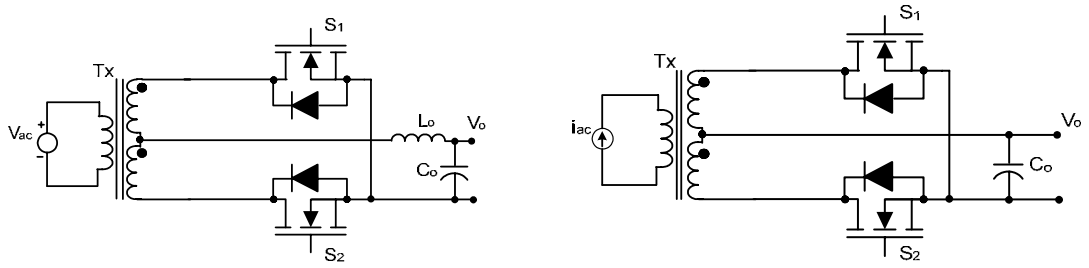


(c) Externally-driven synchronous rectifier method 3

Figure 3-4. Externally-driven synchronous rectifier

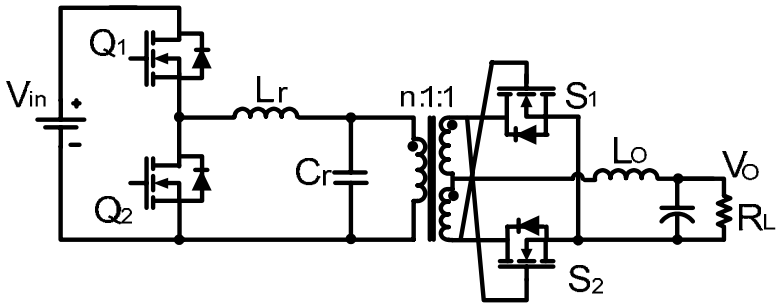
3.2.2 Driving of SR for Resonant Converters

Generally speaking, power conversion topologies of resonant converters can be classified into two types based on the circuit configuration as shown in Figure 3-5: the voltage-fed inductor-loaded configuration and the current-fed capacitor-loaded configuration [3.19] [3.20]. For a topology with a voltage-fed inductor-loaded configuration, such as parallel resonant converters and series-parallel resonant converters, voltage self-driven schemes can be applied for SR driving as shown in Figure 3-6 [3.21]~[3.23]. However, this driving method is not optimal due to the sinusoidal voltage waveform on the secondary winding of the power transformer (in PWM converters, the voltage on the secondary winding of the power transformer is square wave).

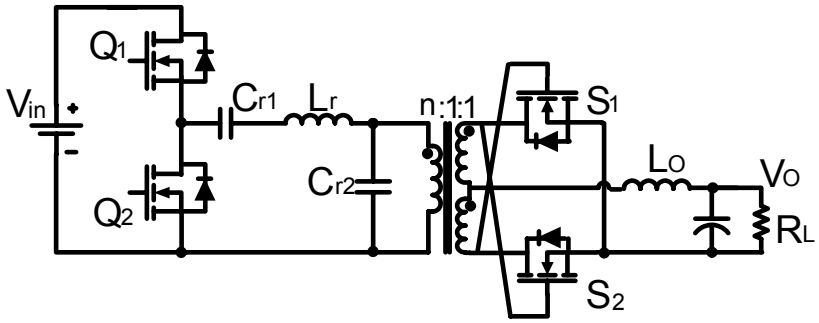


(a) Voltage-fed inductor-loaded structure (b) Current-fed capacitor-loaded structure

Figure 3-5 Circuit structure classification



(a) Parallel resonant converter

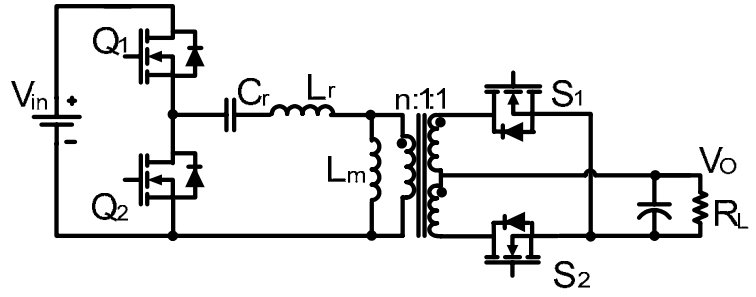


(b) Series-Parallel resonant converter

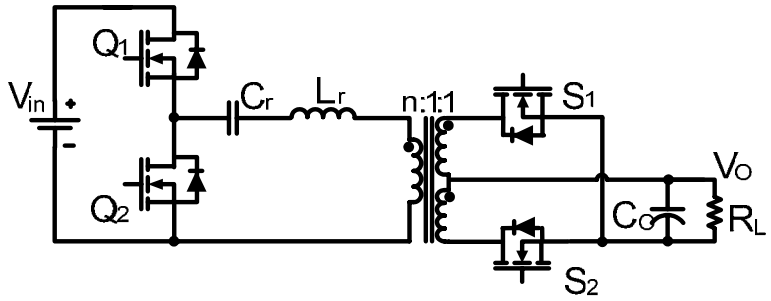
Figure 3-6. Examples of resonant converter w/ voltage self-driven SR

However, an LLC resonant converter shown in Figure 3-6 is a kind of converter with a current-fed capacitor-loaded circuit structure. For this kind of circuit, the polarity of the voltage on the secondary winding can change only after the

synchronous rectifier (SR) is turned off. In other words, when the SR is on, the voltage on the secondary winding is clamped to V_O and lacks the freedom to change polarity before the SR is turned off. So the voltage on the secondary winding cannot be used to achieve self-driven synchronous rectification [3.24].



(a) LLC resonant converter



(b) Series resonant converter

Figure 3-6. Examples of resonant converter with current-fed capacitor-loaded structure

For a converter with current-fed capacitor-loaded structure like LLC resonant converter, the secondary currents need to be used to determine the timing of SR driving signals. One possible SR driving method is the current self-driven scheme as shown in Figure 3-7. However, there are some limitations for this driving method in the high switching frequency and high power density application. The inductance in series with the synchronous rectifier, introduced by the current-sensing transformer, would be detrimental to current commutation in the rectifier. Moreover, operation

with sinusoidal current might result in an excessive dead-time between SR conduction intervals. Furthermore, the large size of the current-sensing transformer is awkward for the high power density requirement.

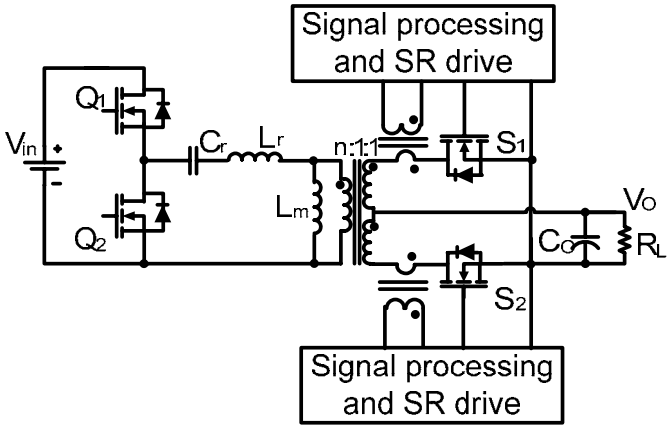


Figure 3-7. Example of resonant converter w/ current self-driven SR

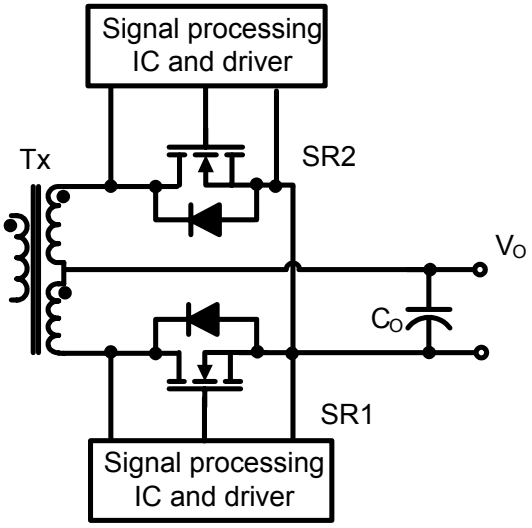


Figure 3-8. Externally driven synchronous rectifier

Another possible driving method for resonant converters with current-fed capacitor-loaded structure is the externally driven scheme by utilizing the drain to source voltage of the SR to qualify the gate driving signals as shown in Figure 3-8.

The sensed V_{ds} of the SR is processed by control circuits to determine the turn-on and turn-off of the SR. The SR can be switched in the close proximity of the zero current transition. With the advanced IC technology and proper noise immunity layout, the precise voltage sensing range can be reached to millivolt level. However, the proper SR drive timing is highly affected by the package of the SR. Due to the inevitable package inductance, the sensed terminal drain to source voltage of the SR is actually the sum of the MOSFET resistive voltage drop and package inductive voltage drop. In Figure 3-9, it is clearly shown that the sensed $V_{d's}$ of SR terminal is far deviated from the real V_{ds} of MOSFET. The SR drive signal is much shorter than the expected value for this reason. The duty cycle of SR is defined as:

$$D_{SR} = \frac{T_{on\_SR}}{T_S / 2}$$

Here T_{on_SR} is the conduction period of the SR and T_S is the switching period. The duty cycle of the SR is calculated as the following with the assumption of sinusoidal current going through the SR:

$$D_{SR} = \frac{\pi - a\tan\left(2\pi f_s \frac{L_{SR}}{R_{ds\_on}}\right) - a\sin\left(\frac{-V_{th1}}{I_o \cdot \frac{\pi}{2} \cdot R_{ds\_on} \cdot \left|1 + j \cdot 2\pi f_s \frac{L_{SR}}{R_{ds\_on}}\right|}\right)}{\pi}$$

Here L_{SR} is the package inductance, R_{ds_on} is the on resistance of SR, f_s is the switching frequency, V_{th1} is the turn off threshold voltage and I_o is the load current.

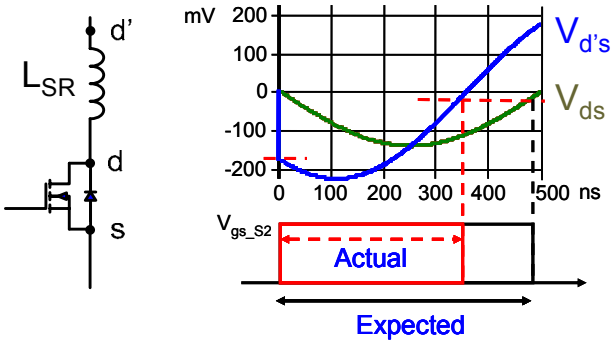


Figure 3-9. Sensing voltage deviation due to SR package inductance

As two examples, Figure 3-10(a) and 3-10(b) show the SR duty cycle at I_o=30A for MOSFET FDP2532 in TO220 package and DirectFET IRF6613 respectively. Here L_{SR} is 8.7nH for FDP2532 from its datasheet, and L_{SR} is 0.5nH for DirectFET IRF6613 as claimed by IR [3.27]. It can be observed that for the package with very small package inductance such as DirectFET, the SR duty cycle loss is still an issue, especially for high switching frequency applications.

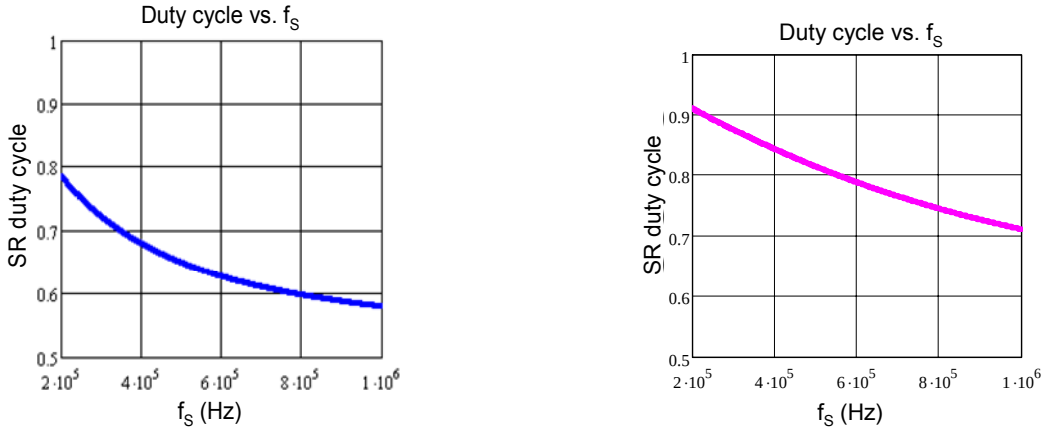


Figure 3-10 (a). SR D_{SR} vs. f_S for FDP2532 (b). SR D_{SR} vs. f_S for IRF6613

3.3 One Method to Drive SR for LLC Resonant Converter

To utilize the voltage drop on R_{ds_on} of the SR to generate SR driving signal is a direct and simple method. The turn-on of the SR can be easily controlled by the

conduction of the body-diode of the SR. The key is how to get the precise voltage drop on R_{ds_on} of the SR to set the right turn-off timing. In order to overcome the issue of phase deviation due to package inductance L_{SR}, the SR driving scheme with phase compensation is developed [3.28]. A block diagram of the driving circuit is shown in Figure 3-11. The main sections are the V_{ds} phase compensation network, the signal processing and gate driver stages for the SR. The input signal to the driving circuit is the voltage across the physical terminal of the power MOSFET SR. This input voltage to the driving circuit is actually $V_{d's}$, the sum of MOSFET resistive voltage drop and package inductive voltage drop, and can not be directly used to qualify SR driving signals. An active phase compensation network is used to provide the true resistive voltage of V_{ds}. Thus, the compensated voltage V_{ds} can be used to exactly determine the turn-off timing of the SR. The phase compensated V_{ds}, as the output signal of the compensation network, is then transferred into the next stage. The post signal processing block consists of a set of window comparators which convert the input signal into control pulses. The driving circuit utilizes these control pulses to ultimately drive the SR using discrete transistors or integrated circuits which may be specifically developed for the purpose.

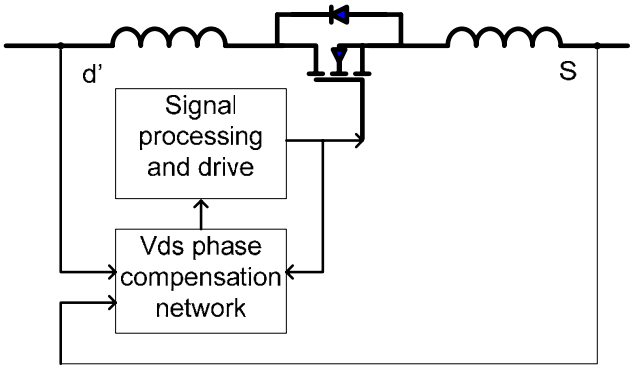


Figure 3-11. Simplified functional diagram for proposed SR driving scheme

The detailed schematic of the phase compensation network is illustrated in Figure 3-12. The passive network composed of R_{cs} and C_{cs} generates the compensated voltage V_{ds}. S_a and S_b are small signal switches to reset the passive phase compensation network in each switching cycle. The operation principle is shown in Figure 3-13. Firstly, the current goes through the body-diode of the SR. When the voltage drop on SR body-diode reaches the threshold V_{th2}, the SR is triggered to turn on. After the SR is turned on, the passive network operates to provide emulated true resistive voltage drop on R_{ds_on} of the SR. The compensated voltage V_{ds} decays with the current going through the SR. Once the pre-set turn-off threshold is reached, the SR can be properly turned off. The equivalent circuits for turn on and turn off periods are illustrated in Figure 3-14.

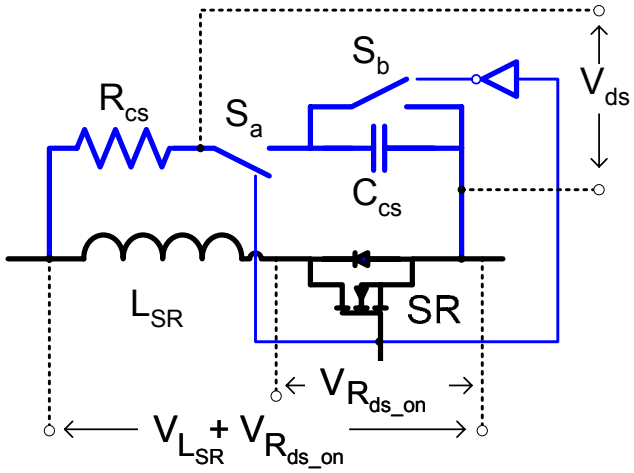


Figure 3-12. Schematic of V_{ds} phase compensation network

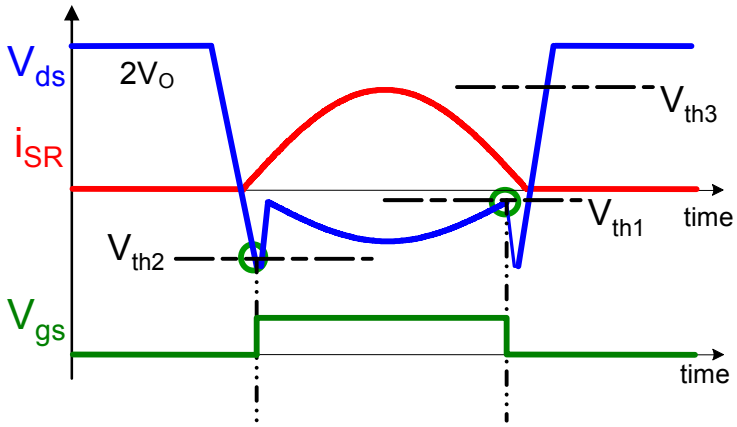
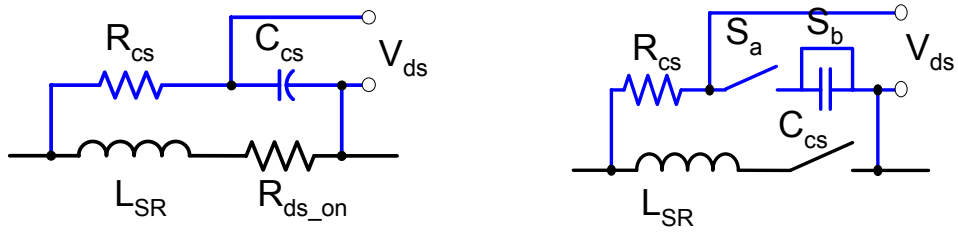


Figure 3-13. Operation Principle of SR driving



(a) Equivalent circuit when SR is on **(b) Equivalent circuit when SR is off**

Figure 3-14. Equivalent circuits for compensation network

To precisely capture the resistive voltage drop on the SR during turn on period, the phase compensation network should be properly designed. Assuming the current goes through SR is $i_{SR}(s)$, the compensated voltage can be expressed as follows:

$$v_{ds}(s) = \frac{i_{SR}(s) \cdot R_{ds\_on} \cdot (1 + s \cdot L_{SR} / R_{ds\_on})}{1 + s \cdot R_{cs} \cdot C_{cs}}$$

If $R_{cs} \cdot C_{cs} = \frac{L_{SR}}{R_{ds\_on}}$

And the initial condition $v_{ds}(t1\_) = v_{Rds\_on}(t1\_)$, then $v_{ds}(s) = i_{SR}(s) \cdot R_{ds\_on} = v_{Rds\_on}(s)$. As a result, the compensation network can precisely represent the voltage of the power MOSFET on R_{ds_on}. The simulation result is shown in Figure 3-15. The SR is modeled as an ideal switch in series with R_{ds_on} and L_{SR}. The V_{ds} is the compensated voltage for the SR driving scheme which is the resistive voltage of SR V_{Rds_on}. It can be seen that V_{ds} follows V_{Rds_on} very well. Theoretically, they are identical in phase and amplitude.

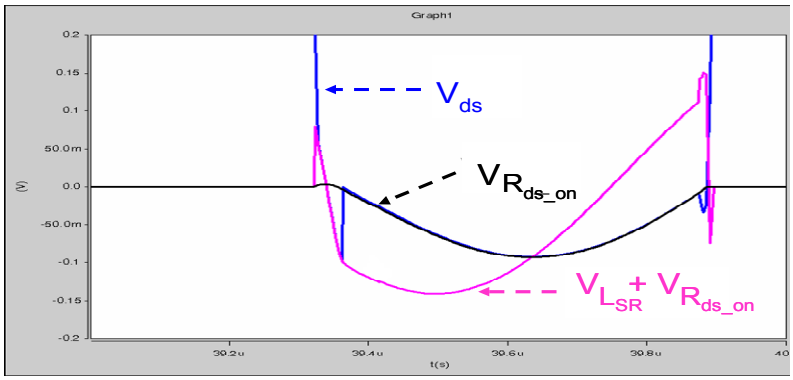


Figure 3-15. Simulation result for V_{Rds_on}, compensated V_{ds} represented in Figure 3-8

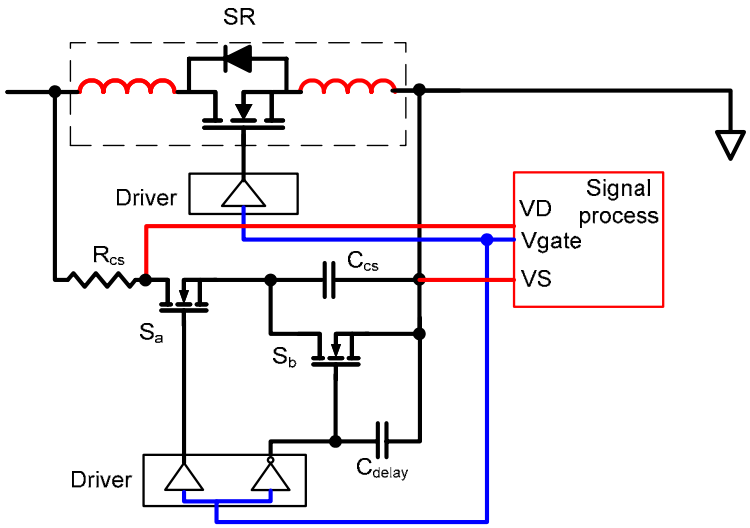


Figure 3-16. Implementation of SR driving scheme w/ V_{ds} phase compensation

The implementation of the driving scheme of SR for LLC resonant converter is illustrated in Figure 3-16. The operating process is described as follows and plotted in Figure 3-17. [t0-t1]: the SR is off. V_{ds} is the voltage drops on the drain to the source of SR. S_a is off and S_b is on. Therefore, the compensation capacitor C_{cs} is shorted. The voltage is zero on C_{cs}. [t1-t2]: The primary side devices switch. Secondary side current begins to go through the body diode of SR. V_{ds} of the SR drops to negative. Once the V_{ds} touches the threshold voltage V_{th2} at t2, the SR can be turned on. [t2-t3]: During this small period, S_a and S_b remains the status as previous stage t1-t2. It guarantees the full turn-on of the SR and also eliminates the adverse effect of the oscillation. [t3-t4]: S_a is turned on and S_b is turned off. The passive compensation network begins to work. The voltage on C_{cs} follows the resistive voltage of the SR. The compensated voltage can be applied to accurately control the SR conduction time. At t4, the current of the SR reduces close to zero. The voltage drop V_{ds} touches the threshold voltage V_{th1}. As a result, the SR can be turned off. Meanwhile, S_a is turned off. [t4-t5]: The current goes through the body-diode of SR. The active network takes the V_{ds} of SR. [t5-t6]: The voltage drop on SR changes from negative to positive potential. The driving circuit is blanked until the V_{ds} touches the V_{th3}. Similarly, this short period is to avoid the adverse effect of turn off ringing. [t6-]: the SR remains off. The passive compensation network remains in the reset mode until the trigger of the next switching cycle.

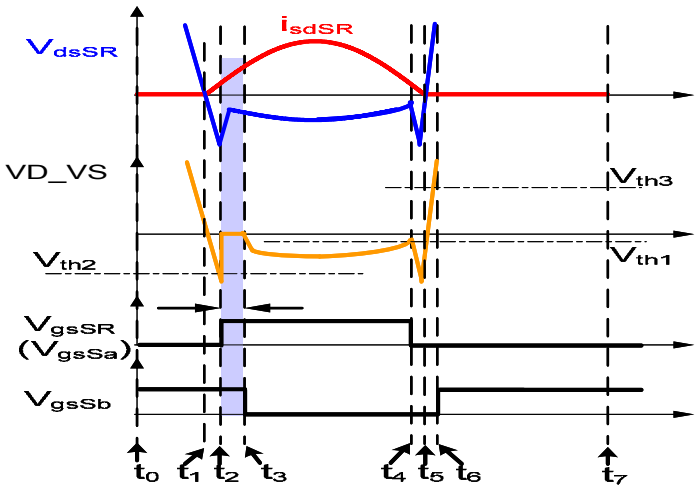


Figure 3-17. Operation modes of SR driving scheme in LLC resonant converter

3.4 Improvements of SR Driving for LLC Resonant Converter

3.4.1 Compensation with Consideration of Driving Circuit's Turn-off Propagation Delay

The design of the phase compensation network for SR V_{ds} sensing in the previous section is based on the ideal case. In the real scenario, several factors have effects to the duty cycle loss of the SR, which makes the net SR duty cycle loss unequal to the calculated result due to the SR package inductance. For instance, the turn-off propagation delay of the driving circuit has the compensation effect to the SR duty cycle loss caused by the SR package inductance as shown in Figure 3-18. For the SR driving implementation scheme in Figure 3-12, though with state-of-the-art integrated circuits technology the propagation delay of a discrete driver can be as small as 10~20ns, the propagation delay of the sensed V_{ds}

processing circuit is still in the range of tens of ns. One reason for the large propagation delay from the V_{ds} processing circuit is the needed large gain for window comparators. Other factors affecting the final net SR duty cycle loss include non-ideal sinusoidal current going through the SR, variation of the R_{ds_on} and the package inductance of the SR.

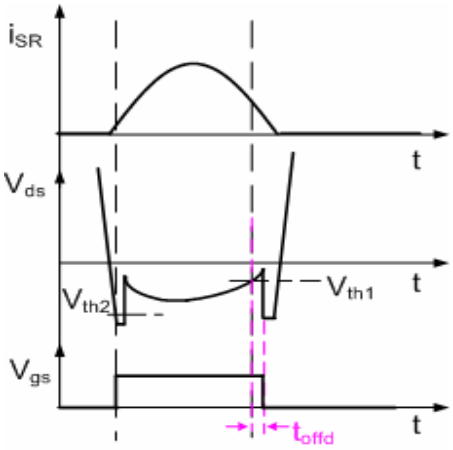


Figure 3-18. Compensation effect of turn-off propagation delay

The SR duty cycle loss in the absolute value with the assumption of sinusoidal current in SR can be calculated as,

$$t_\theta = \frac{a\tan\left(2\pi f_s \frac{L_{SR}}{R_{ds\_on}}\right) + a\sin\left(\frac{-V_{th1}}{I_o \cdot \frac{\pi}{2} \cdot R_{ds\_on} \cdot \left|1 + j \cdot 2\pi f_s \frac{L_{SR}}{R_{ds\_on}}\right|}\right)}{\pi} \cdot \frac{T_S}{2}$$

Here L_{SR} is the package inductance, R_{ds_on} is the SR on resistance, T_s is the switching period, V_{th1} is the turn-off threshold voltage and I_o is the load current.

Figure 3-19 shows the measured waveforms at full load on a 1KW, 1MHz, 400V to 48V LLC prototype. 150V MOSFET FDP2532 in TO220 package is used as the SR on the prototype. The calculated SR duty cycle loss at full load is 210ns with R_{ds_on} at T_j=25C and 8.7nH L_{SR} as indicated in FDP2532 datasheet. However, the measured SR duty cycle loss in the real circuit is 100ns. There is a discrepancy between the calculated result and measured value.

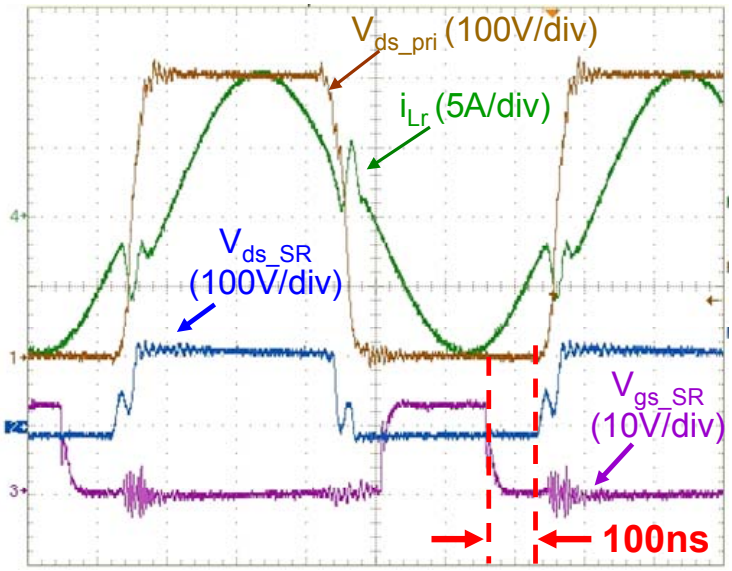


Figure 3-19. Operation waveforms of SR w/o compensation

The breakdown among those factors for the discrepancy is shown in Table 3-1. The total turn-off propagation delay from the driving circuit is 87ns. This means that when considering the compensation effect of the turn-off propagation delay, the SR duty cycle loss due to SR package inductance is 87ns, which is less than the calculated value. In the real LLC circuit, the current in the SR is not ideally sinusoidal. The non-ideal sinusoidal current in the SR gives 5ns less the SR duty cycle loss than the calculated value. Here, T_j of the SR is estimated at 80^{o}C which

gives 1.3 times larger R_{ds_on} as that at T_j=25C. The variation of the R_{ds_on} leads to 10ns less the SR duty cycle loss than the calculated value. Among those factors, the turn-off propagation delay from the driving circuit has the highest weight, which accounts for 80% of the total discrepancy.

Turn-off propagation delay		Non-ideal sinusoidal i_{SR}	R_{ds_on} variation	Other factors
Sensed V_{ds} processing circuit	Discrete driver MAX5056			
65ns	22ns	5ns	10ns	8ns

Table 3-1. Factors for the discrepancy between calculated t_θ and measured t_θ

For the design of the phase compensation network in the driving circuit as described in the previous section, if the turn-off propagation delay of the driving circuit is not considered, the SR will be turned off after zero current crossing. Consequently, the reverse current going through the drain to source of SR will be seen in the SR as shown in Figure 3-20 (When a MOSFET is used as a synchronous rectifier, the channel current goes through the source to drain in proper operation). This reverse current will cause higher conduction loss and switching loss in the SR. Since the SR is not turned off in the vicinity of zero current, the voltage ring will be seen on the SR when it is turned off, thus a higher voltage stress needs to be considered for the selection of MOSFET. Furthermore, during the period where there is a reverse current in the SR due to the delay in turn-off, in the primary side, the resonant tank current i_{Lr} will not follow the magnetizing current i_{Lm} but go in the reverse direction instead. In this case, the current to achieve ZVS operation for primary switches is smaller than the designed value. For the high switching

frequency ~MHz application, this may lead to the loss of primary ZVS operation in LLC resonant converters.

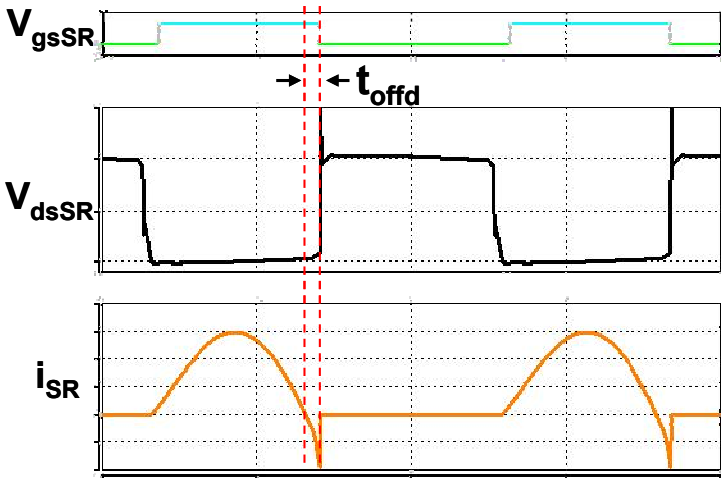


Figure 3-20. Simulation waveforms of SR w/ compensation $R_{cs}C_{cs}=L_{SR}/R_{ds\_on}$

In order to overcome the problem caused by the turn-off propagation delay, the design of V_{ds} phase compensation network R_{cs}, C_{cs} need to be adjusted. A coefficient k is introduced instead of making the time constant of $R_{cs}C_{cs}$ exactly equal to the time constant of L_{SR}/R_{ds_on}. Thus the parameters R_{cs}, C_{cs} can be designed based on:

$$R_{cs} \cdot C_{cs} = \frac{kL_{SR}}{R_{ds\_on}}, \text{ where } k < 1$$

The SR duty cycle loss in absolute value without considering the turn-off propagation delay from the driving circuit is rewritten here:

$$t_\theta = \left[a\tan\left(2\pi f_S \frac{L_{SR}}{R_{ds\_on}}\right) + a\sin\left(\frac{-V_{th1}}{I_o \cdot \frac{\pi}{2} \cdot R_{ds\_on} \cdot \left|1 + j \cdot 2\pi f_S \frac{L_{SR}}{R_{ds\_on}}\right|}\right)\right] \Big/ 2\pi f_S$$

The SR duty cycle loss with considering the turn-off propagation delay t_θ is:

$$t_\theta - t_{offd} = \left[a\tan\left(2\pi f_S \frac{kL_{SR}}{R_{ds\_on}}\right) + a\sin\left(\frac{-V_{th1}}{I_o \cdot \frac{\pi}{2} \cdot R_{ds\_on} \cdot \left|1 + j \cdot 2\pi f_S \frac{kL_{SR}}{R_{ds\_on}}\right|}\right)\right] \Big/ 2\pi f_S$$

Then coefficient k can be expressed as:

$$k = \frac{\frac{\pi}{2} I_o R_{ds\_on} \sin(-2\pi f_S t_\theta + 2\pi f_S t_{offd}) - V_{th1}}{[\sin(-2\pi f_S t_\theta + 2\pi f_S t_{offd})^2 - 1] \cdot L_{SR} 2\pi f_S I_o \pi / 2} \cdot \cos(-2\pi f_S t_\theta + 2\pi f_S t_{offd})$$

Here L_{SR} is the package inductance, R_{ds_on} is the SR on resistance, f_s is the switching frequency, V_{th1} is the turn-off threshold voltage, t_{offd} is the total propagation delay in the driving circuit and I_o is the load current. For a given design, all the parameters in the above equation are achievable.

This compensation scheme is to compensate the adverse effect caused by the MOSFET package inductance, to apply this scheme into practice, the tolerance of MOSFET package inductance and variation of R_{ds_on} should be considered.

Here the tolerance coefficient k_L of MOSFET package inductance is defined as the ratio of real L_{SR} over the nominal value L_{SR},

$$k_L = \frac{L_{SR}}{L_{SR\_N}}$$

Then with the compensation network, the sensed voltage is,

$$v_{ds}(s) = \frac{i_{SR}(s) \cdot R_{ds\_on} \cdot (1 + s \cdot k_L L_{SR\_N} / R_{ds\_on})}{1 + s \cdot R_{CS} C_{CS}}$$

The phase mismatch due to the tolerance of the package inductance can be calculated as,

$$Phase_{mismatch} = \arg\left(\frac{1 + j\frac{2\pi \cdot f_S \cdot k_L \cdot L_{SR\_N}}{R_{ds\_on}}}{1 + j\frac{2\pi \cdot f_S \cdot L_{SR\_N}}{R_{ds\_on}}} \right)$$

To convert this phase mismatch into the SR duty cycle $D_{mismatch}$,

$$D_{mismatch} = \arg\left(\frac{1 + j\frac{2\pi \cdot f_S \cdot k_L \cdot L_{SR\_N}}{R_{ds\_on}}}{1 + j\frac{2\pi \cdot f_S \cdot L_{SR\_N}}{R_{ds\_on}}} \right) \Big/ \pi$$

The physical meaning of $D_{mismatch}$ is the over-compensation and under-compensation of V_{ds}. The 1KW, 1MHz, 400V to 48V LLC design is taken as an example to demonstrate the influence of effect of L_{SR} variation. The SR duty cycle mismatch due to the variation of SR package inductance is plotted in Figure 3-21(a). With the inductance variation from +20% to -20%, the SR duty cycle mismatch is less than 2% (less than 10ns) at 1MHz. Following the same derivation procedure, the effect of R_{ds_on} variation due to the temperature change is plotted in Figure 3-21(b). Due to the junction temperature derating request in practice, for a 150^{o}C T_{jmax} MOSFET, T_j will be limited below 110^{o}C. The SR duty cycle mismatch at T_j up to 110 ^{o}C does not exceed 20ns at 1MHz. This amount of mismatch is tolerable in V_{ds}

compensation practice. With 1% tolerance for R_{cs}, 10% tolerance for C_{cs}, the SR duty cycle mismatch due to variations of R_{cs} and C_{cs} is negligible. Therefore, the compensation method discussed herein is applicable in practice. The design of V_{ds} phase compensation with consideration of turn-off propagation delay provides much better performance for the SR driving which will be shown in section 3.5.

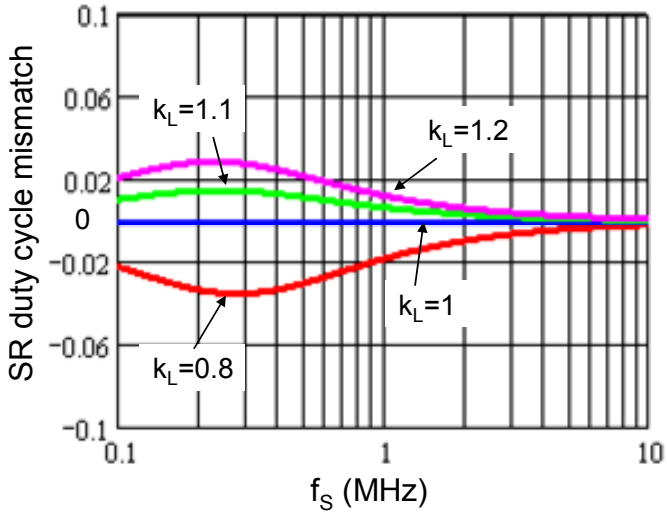


Figure 3-21.(a) SR duty cycle mismatch due to package inductance variation

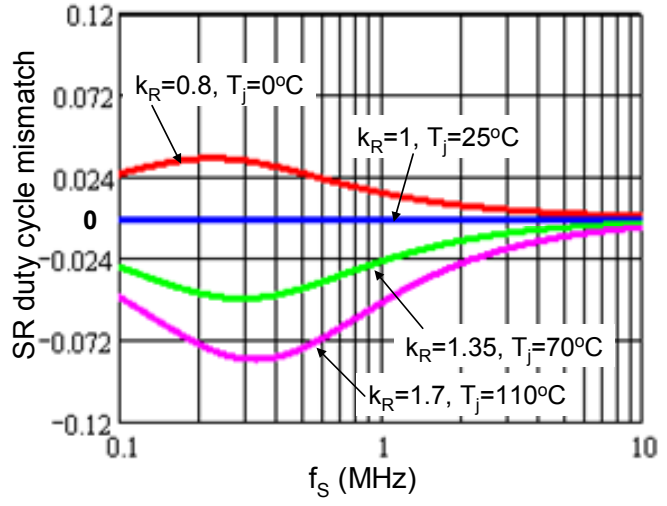
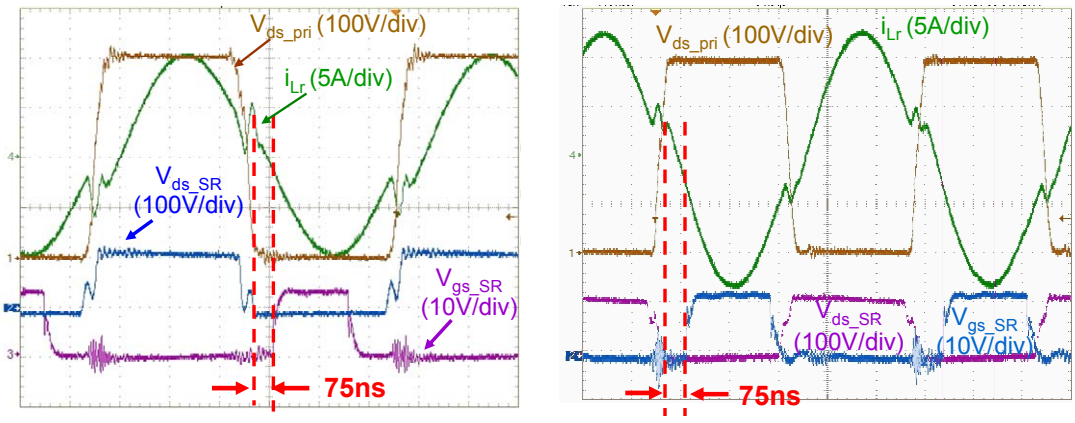


Figure 3-21.(b) SR duty cycle mismatch due to R_{ds_on} variation

3.4.2 Compensation of Driving IC's Turn-on Propagation Delay

For any SR driving circuit, the turn on propagation delay always happens with the turn off propagation delay. The same story happens with the SR driving scheme discussed here. For the same reason as mentioned in section 3.4.1, the turn-on propagation delay in the V_{ds} signal processing circuit is much larger than that comes from the followed discrete driver. For instance, the total SR duty cycle loss at the turn-on on a 1KW, 1MHz, LLC prototype due to the turn-on propagation delay in the driving circuit is 75nS as shown in Figure 3-22. The turn-on propagation delay in the V_{ds} signal processing circuit is 50nS while the turn-on propagation delay in the followed discrete driver MAX5056 is only 25nS. According to the aforementioned discussion, the turn off propagation delay can be compensated and almost ideal SR turn off timing is achievable. However, the compensation network can hardly affect the turn on propagation delay as shown in Figure 3-22. As a result, the SR duty cycle loss due to the turn on propagation delay still exists.



(a) W/O V_{ds} phase compensation (b) W/ V_{ds} phase compensation

Figure 3-22. SR turn-on duty cycle loss due to turn-on propagation delay

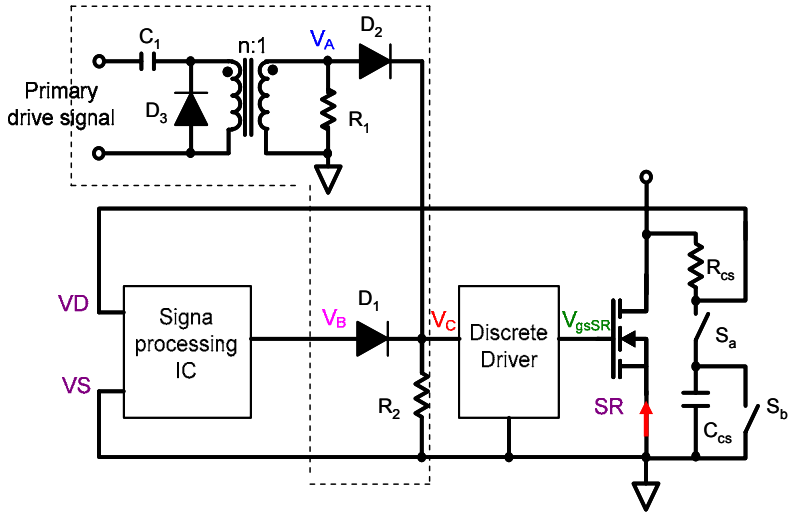


Figure 3-23 Turn on propagation delay compensation circuit

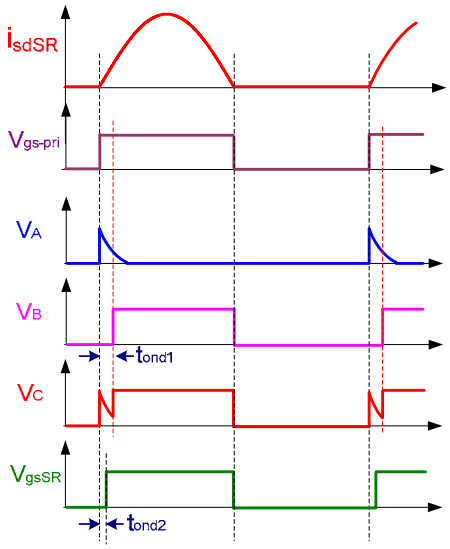


Figure 3-24 Turn on propagation delay compensation circuit analysis

A turn-on propagation delay compensation circuit in the dot-line box, shown in Figure 3-23, is proposed to solve the problem of the duty cycle loss at turn-on edage. Based on the characteristics of LLC resonant converters, the turn on edge of primary side switches is in phase with the SR. Therefore, the primary side turn on signal is utilized to synchronize the SR turn on timing. The detail operation principle

is illustrated in Figure 3-24. When the primary switch is turned on, a narrow pulse signal V_A is generated and delivered to the input of the discrete driver. At this moment, due to the turn-on propagation delay of the discrete driver, the SR is not conducting and the current goes through the body-diode of SR. The conduction of SR body-diode triggers the turn-on threshold of the signal processing IC. But due to the propagation delay in this part, V_B is still low. The input of the discrete driver follows V_A. As long as V_A stays higher than the on-threshold of the discrete driver until high signal V_B comes out, the turn-on propagation delay in the signal processing circuit can be compensated. In the circuit, D_1 and D_2 act as an "OR" logic function. R_2 is for the discharge of the input capacitance of the discrete driver during the off period of the SR.

3.5 Experiment Results and Summary

A 1MHz, 1kW, 400V-48V prototype, shown in Figure 3-25, is built to verify the improved SR driving scheme for the LLC resonant converter. The magnetizing inductance L_m is chosen as 13μH. The resonant inductor L_r is 1μH and the resonant capacitor C_r is chosen as 25nF. The transformer turns ratio is 4. For the primary switch, APT5024BFLL from APT is selected according to 400V input, 1kW power level and high switching frequency 1MHz. 150V Trench MOSFET FDP2532 from Fairchild is selected for the secondary synchronous rectifier for small R_{ds_on}.

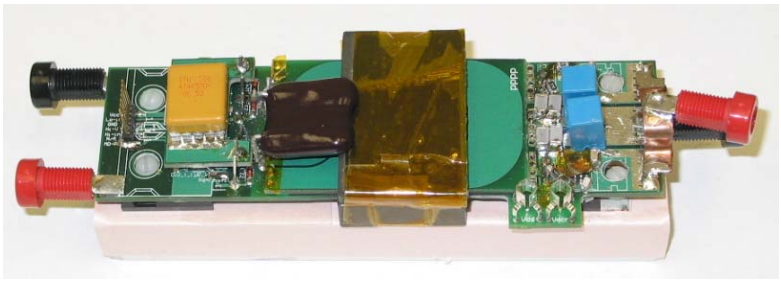
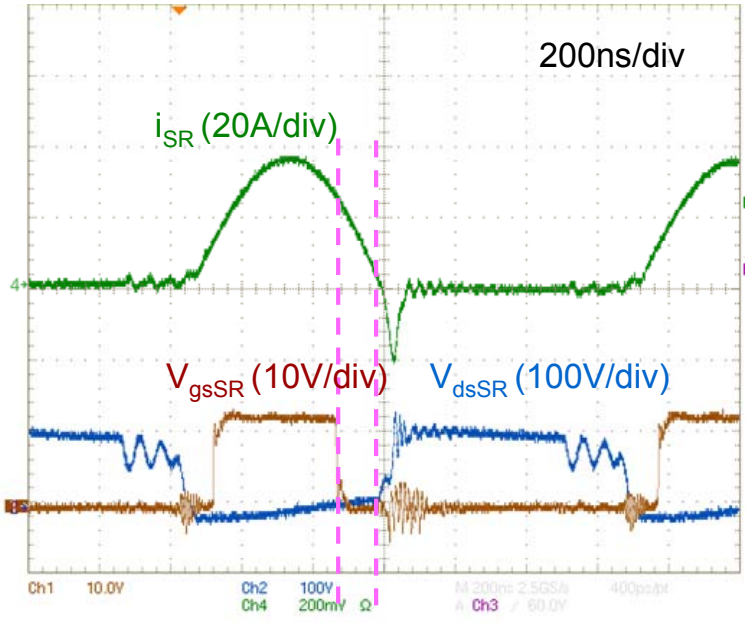
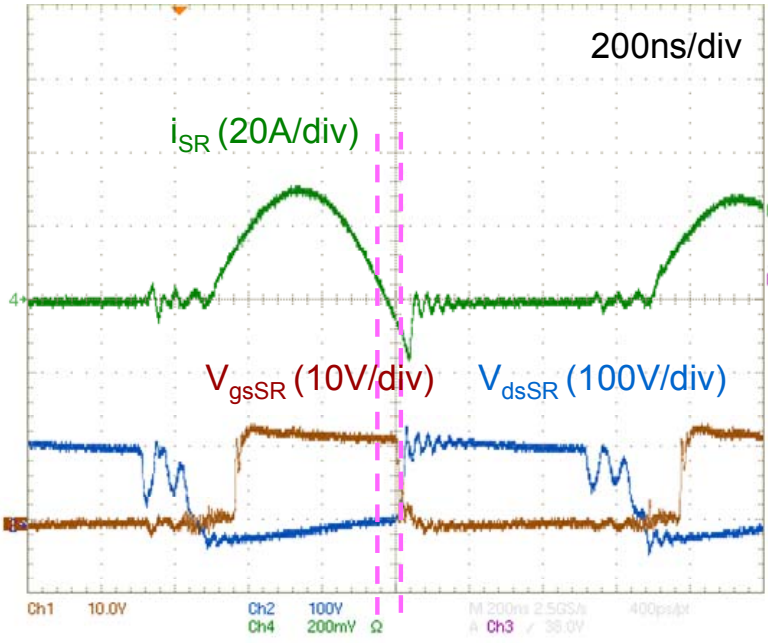


Figure 3-25. 1MHz 1kW 400V-48V LLC resonant converter with SR

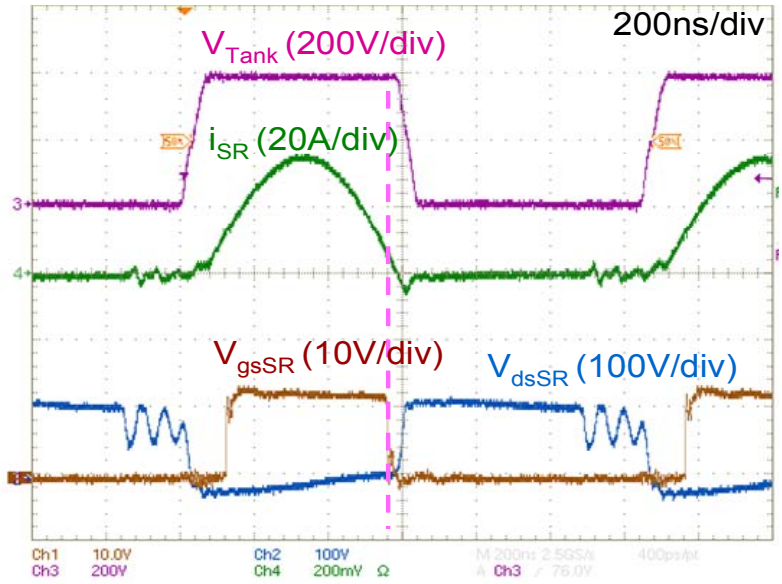
Figure 3-26 shows the measured SR operation waveforms with the driving method discussed aforementioned for different cases. In Figure 3-26 (a), no any V_{ds} phase compensation is applied, the SR duty cycle loss at the turn-off edge due to the package inductance is obvious. In Figure 3-26 (b), the V_{ds} phase compensation network is applied and the parameters R_{cs}, C_{cs} are designed based on $R_{cs}C_{cs}=L_{SR}/R_{ds\_on}$. In this case, it is overcompensated because the turn-off propagation delay in the driving circuit is not considered in the design of compensation. The reverse current in the SR can be observed. This reverse current causes higher conduction loss, switching loss in the SR. Furthermore, it causes voltage ring on the SR at turn-off. In Figure 3-26 (c), the V_{ds} phase compensation network is applied and the parameters R_{cs}, C_{cs} are designed based on $R_{cs}C_{cs}=kL_{SR}/R_{ds\_on}$ with k=0.25. Much better SR performance can be achieved. In all the three figures here, the SR drive timing is a little bit deviated from the expected case, which is caused by the additional introduced inductance in series with SR while measuring SR current waveform.



(a) W/O V_{ds} phase compensation



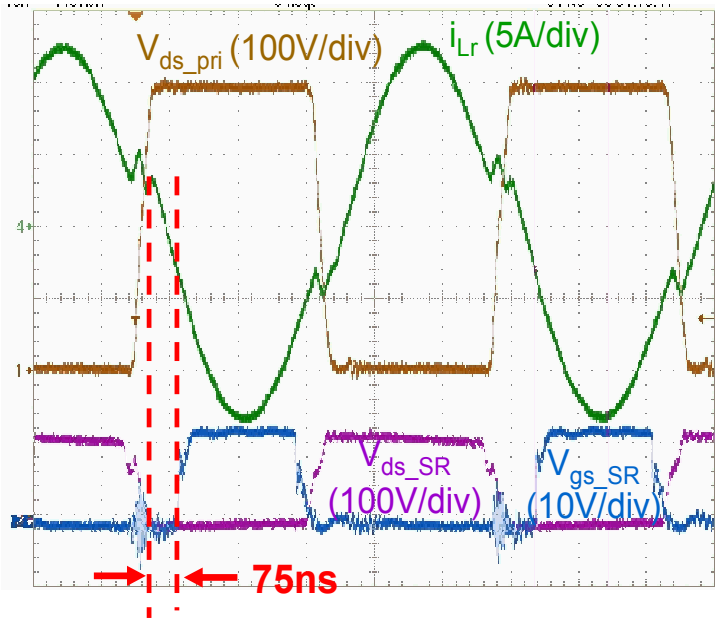
(b) W/ V_{ds} phase compensation based on design $R_{cs}C_{cs}=L_{SR}/R_{ds\_on}$



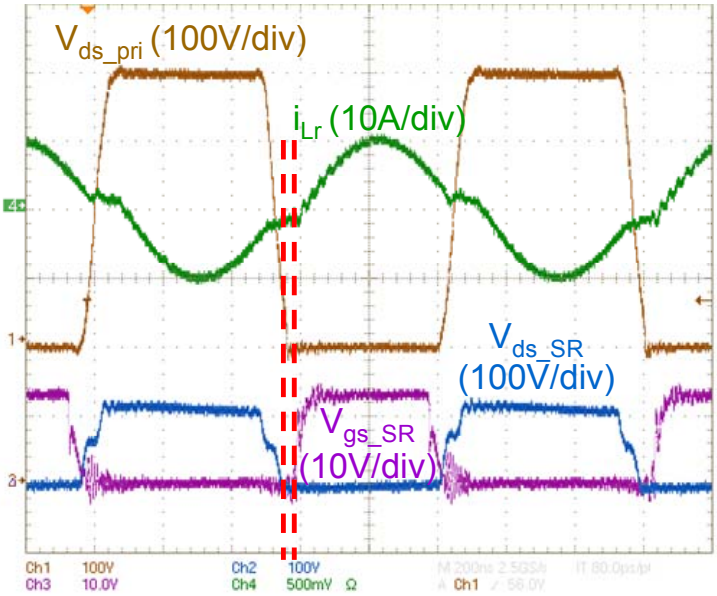
(c) W/ V_{ds} phase compensation based on design $R_{cs}C_{cs}=kL_{SR}/R_{ds\_on}$, k=0.25

Figure 3-26. SR operation waveforms W/O and W/ V_{ds} phase compensation network

The experiment operation waveforms without the SR turn-on compensation circuit and with the turn-on compensation circuit are shown in Figure 3-27(a) and Figure 3-27(b) respectively. In both Figure 3-27(a) and Figure 3-27(b), the V_{ds} phase compensation is applied. Since the V_{ds} phase compensation has no effect to SR duty cycle loss at the turn-on edge, the 75ns duty cycle loss still exists as shown in Figure 3-27(a). After the turn-on compensation circuit is applied, the turn-on propagation delay in the V_{ds} signal processing circuit as shown in Figure 3-27(b) is compensated. With the turn-on compensation circuit, only the turn-on propagation delay in the discrete driver will show up in the driving signal of the SR as shown in Figure 3-27(b), which is almost non-observable.



(a) W/O turn-on compensation



(b) W/ turn-on compensation

Figure 3-27. SR operation waveforms W/O and W/ turn-on compensation circuit

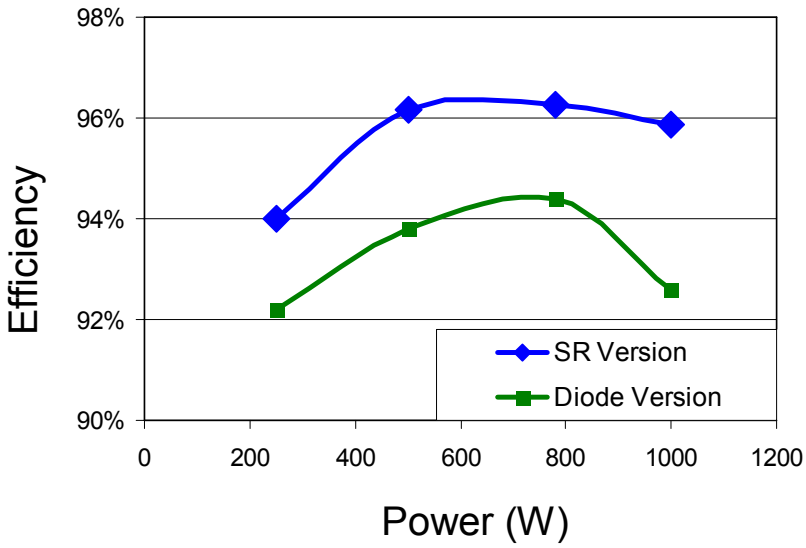


Figure 3-28. Efficiency comparison

In summary, the LLC resonant converter is a promising candidate for the front-end dc/dc converter in computing and telecom equipment. In order to achieve high efficiency, the synchronous rectifier should be used instead of the diode rectifier. The driving of SR in LLC resonant converters can be realized by sensing the voltage drop V_{ds} on the R_{ds_on} of SR. The turn-on of the SR is triggered by the conduction of SR body-diode, and the turn-off of the SR is triggered when the voltage drop on the R_{ds_on} of the SR decays to the pre-set turn-off threshold. The V_{ds} compensation network is designed to overcome the early turn-off issue caused by the unavoidable parasitic package inductance of the SR. To apply the V_{ds} compensation scheme in practical applications, the turn-off propagation delay in the driving circuit needs to considered when designing the compensation network components. By introducing a coefficient k in the design of compensation network, the SR duty cycle loss due to SR package inductance can be well limited. Effects of component tolerance and

temperature variations are discussed. There is also SR duty cycle loss at the turn-on due to the turn-on propagation delay in the driving circuit. With the proposed turn-on compensation scheme, the SR duty cycle loss at the turn-on is well limited. It is demonstrated in a 400V to 48V, 1kW LLC resonant converter hardware that with the complete solution of SR driving scheme discussed herein, the efficiency at full load can be improved by more than 3% as shown in Figure 3-28.

Chapter 4 Dead-time Optimization for High Efficiency over a Wide Load Range

4.1 Introduction

Compared with PWM topologies, the LLC resonant converter can achieve higher efficiency because it can have ZVS turn-on and low turn-off loss for primary side switches over the whole load range which is very important for applications with high input voltage such as the front-end dc/dc converter, and it can also have ZCS turn-off for secondary side rectifiers. However, this statement is based on the assumption that a reasonable resonant tank design is made. It is well-known that the circulating energy, which is not transferred to the output load but adds additional loss in the circuit, is the nature of any kind of resonant topology. For LLC resonant converters, the circulating energy is reflected by the magnetizing current as shown in Figure 4-1. The current in secondary rectifiers is $n(i_{Lr}-i_{Lm})$. In other words, only during the shaded period, the energy is transferred from the input to the output load. The conduction loss in both primary side and secondary side is determined by current i_{Lr} and i_{Lm}. The turn-off loss in primary switches is determined by the current level of i_{Lm} at the turn-off of primary switches. Then how to achieve high efficiency at full load in LLC resonant converter? How to achieve high efficiency over a wide load range in LLC resonant converters? The key is how to design the three-element resonant tank to shape i_{Lr} and i_{Lm} so that the lowest conduction loss and switching loss or the lowest overall power loss can be achieved. Some tradeoffs may need to be played for high

efficiency at heavy load and light load. That is the design optimization of LLC resonant converters.

In this chapter, one existing design procedure of the LLC resonant converter is introduced first. Then the dead-time t_d is considered for the analysis of the design of LLC resonant converters, which is not studied thoroughly in the mentioned existing design methodology and is not paid attention in any other literatures on LLC design either. The dead-time t_d is defined as a time period in which both primary drive signals are low as shown in Figure 4-1. The relationship between the dead-time and the power loss in LLC resonant converters is revealed. Finally the improvement to the LLC design procedure is made by playing some tradeoffs between the conduction loss and switching loss for high efficiency over a wide load range.

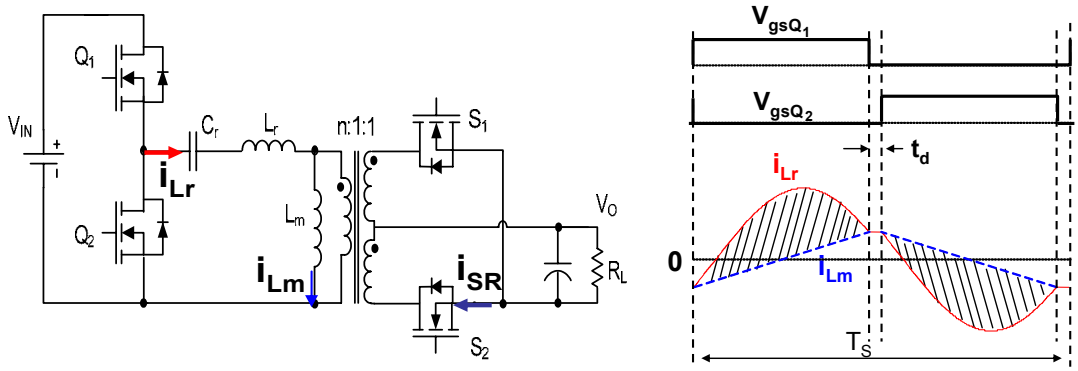


Figure 4-1. LLC resonant converter at resonant frequency

4.2 One Existing Design Procedure of LLC Resonant Converter

The design goals of LLC resonant converters are to achieve minimal loss in normal operation and the required maximum voltage gain to regulate output voltage during the holdup time. According to the analysis by neglecting the dead-time in

Chapter 2, the relationships between design parameters L_m, L_n and Q with the converter performance are revealed. These relationships can be used to develop a design procedure for LLC resonant converters. The keys for this design procedure rely on designing a suitable magnetizing inductor L_m and the inductor ratio L_n ($=L_m/L_r$).

The design procedure can be explained by a flow chart as shown in Figure 4-2. The switching frequency is selected based on the desired converter efficiency and power density requirement. Generally, a higher switching frequency results in smaller passive components size but a lower efficiency. As a result, some tradeoffs are required to be made for the selection of a suitable switching frequency. The resonant frequency f_0 of LLC resonant converters is normally designed as the same as the selected switching frequency.

As discussed in Chapter 2, the LLC resonant converter can achieve maximum efficiency when it operates at the resonant frequency. Therefore, the transformer turns-ratio should be designed so that when the LLC operates with nominal input voltage, the switching frequency is the resonant frequency, which means the voltage gain of the converter is equal to one. Based on this, the transformer turns-ratio can be designed. For a half-bridge LLC resonant converter, the transformer turns-ratio is calculated as:

$$n = \frac{V_{in}}{2V_0}$$

For a full-bridge LLC resonant converter, the transformer turns-ratio is calculated as:

$$n = \frac{V_{in}}{V_0}$$

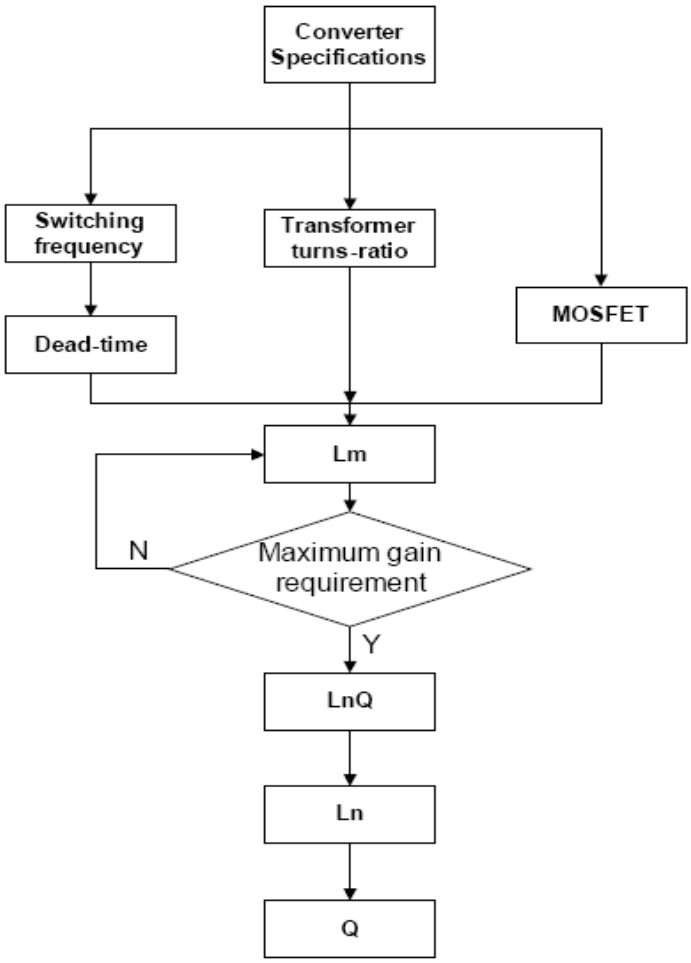


Figure 4-2. Design procedure for LLC resonant converter

After the design of the transformer turns-ratio, the magnetizing inductor L_m is to be designed next. As discussed in Chapter 2, in normal operation condition the conduction loss is purely determined by the magnetizing inductance. A larger magnetizing inductance results in smaller conduction loss if neglecting the effect of dead-time t_d. The equations for the primary side RMS current and secondary side RMS current are rewritten here:

$$I_{RMS\_P} = \frac{1}{4\sqrt{2}} \frac{V_0}{nR_L} \sqrt{\frac{n^4 R_L{}^2 T_S{}^2}{L_m{}^2} + 4\pi^2}$$

$$I_{RMS\_S} = \frac{\sqrt{3}}{24\pi} \frac{V_0}{R_L} \sqrt{\frac{(5\pi^2 - 48) n^4 R_L{}^2 T_S{}^2}{L_m{}^2} + 12\pi^4}$$

It can be seen that a large value of L_m is required to achieve low conduction loss. On the other hand, the switching loss also needs to be minimized. The ZVS turn on condition of the primary switches is determined by the turn-off current of the primary switches. This soft switching transition happens during the dead-time t_d. In normal operation, the switching frequency is at the resonant frequency. During the dead-time, both the primary switches and secondary switches are off. The equivalent circuit during the dead-time is illustrated in Figure 4-3.

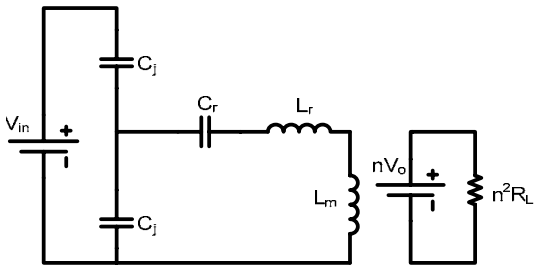


Figure 4-3. Equivalent circuit during dead-time for LLC resonant converter

The turn-off current of the primary switches is the peak magnetizing current as shown in Figure 4-1. Because of the high value of L_m, the transformer magnetizing current during the dead-time can be assumed to be constant. This magnetizing current must be big enough to discharge the junction capacitors of primary switches

during the dead time t_d to ensure the ZVS turn-on. This limitation can be expressed as

$$I_{Lmp} > \frac{2V_{in}C_j}{t_d}$$

Where V_{in} is the input voltage of LLC resonant converters, C_j is the equivalent junction capacitor of primary switch, I_{Lmp} is the peak magnetizing current. C_j is based on the stored charge because of the nonlinearity of the MOSFET junction capacitor. I_{Lmp} can be expressed as

$$I_{Lmp} = \frac{nV_O}{L_m}\frac{T_S}{4}$$

Where n is the transformer turns-ratio, T_S is the switching period. Then to satisfy the ZVS criteria, L_m should be

$$L_m \le \frac{T_S \cdot t_d}{16C_j}$$

To achieve minimum conduction loss, a large L_m is preferred. At the same time, design of L_m also needs to ensure primary switch ZVS turn-on. Therefore, L_m should be designed so that the peak magnetizing current is equal to the current required for ZVS switching. That is,

$$L_m = \frac{T_S \cdot t_d}{16C_j}$$

For a given dead-time t_d, L_m can be optimally designed based on the above equation and the high efficiency at normal operation can be achieved.

After the goal of high efficiency at the normal operation is achieved by design of the magnetizing inductor L_m, the next step is to address the 2nd design goal of having enough maximum voltage gain to regulate output voltage for the holdup time operation.

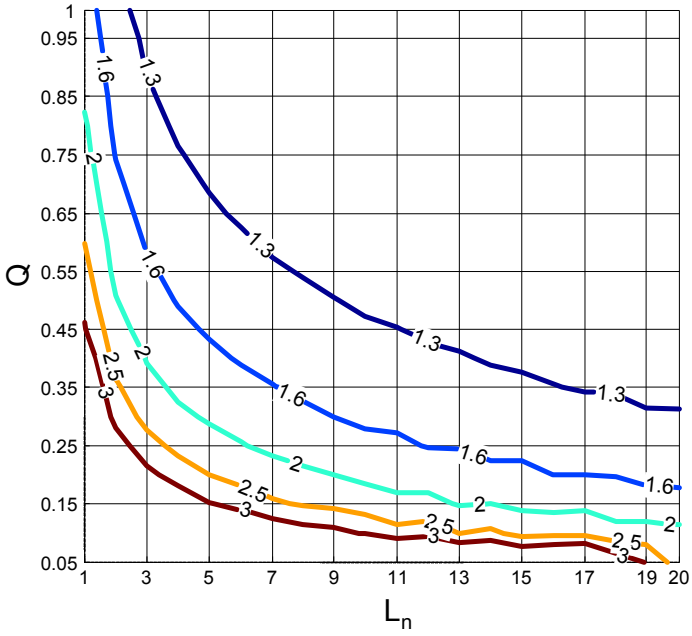


Figure 4-4. Peak gain for different L_n and Q combinations

As analyzed in Chapter 2, the required maximum gain is determined by the selection of the minimum operation voltage for LLC resonant converters. Once the minimum input voltage is selected, the other resonant components can be designed accordingly. With simulation tool Simplis, peak gain for different L_n and Q combinations have been shown in Chapter 2. This peak gain information is redrawn into contour curves here in Figure 4-4 which can be used to locate other design parameters of LLC resonant converters. For example, the nominal input is 400V and the minimum input voltage is selected as 200V. Then the required maximum gain is

2. For this case, any point in Figure 4-5, that is one combination of L_n and Q, on line with mark 2 and below it can satisfy the required peak gain.

In order to narrow the design parameters, L_m is considered. Once L_m is designed for high efficiency in the normal operation, the relationship between L_m and L_nQ is fixed as:

$$L_m = f(L_nQ) = L_nQ \cdot \frac{n^2 R_L}{2\pi f_0}$$

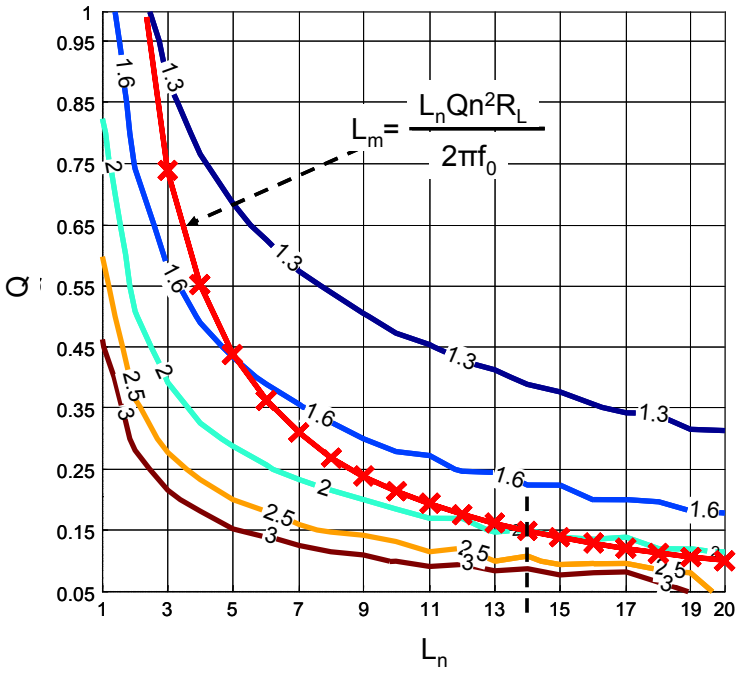


Figure 4-5. One design example of LLC resonant converter

For instance, 1MHz switching frequency and 100ns dead-time are selected for a 1KW LLC resonant converter, the magnetizing inductor is designed as 13uH based on the equivalent junction capacitance (APT5024BFLL is selected as the primary switch). Then with the above equation, L_m can be drawn as shown in Figure 4-5. All

the L_n and Q combinations on this L_m line give the same conduction loss and switching loss in the normal operation. So combining the required maximum gain and L_m line together, L_n needs to be on the L_m line with L_n larger than 14.

After going through these steps, the choice of L_n and Q is narrowed to a portion of L_m line in Figure 4-5. But still infinite choices are there. In order to go further to find a suitable L_n and Q design, the impacts of L_n and Q combination on circuit performance and even components size need to be evaluated. After the L_m is designed, different L_n and Q designs will not influence the efficiency in normal operation. Different L_n and Q combinations could lead to different power loss for the operation during the holdup time. But the time duration for holdup is less than 20ms. So higher power loss during the holdup time will not cause thermal issue. Figure 4-6 shows the voltage stress on the resonant capacitor C_r for different L_n. The x-axis is the voltage gain instead of switching frequency because with same voltage gain different L_n designs that have the same input voltage will give same output, which means a fair comparison. Here the normalized base for the y-axis is the converter output voltage. It can be observed that a larger L_n lead to smaller voltage stress on C_r. On the other hand, a larger L_n means a smaller resonant inductor L_r for a designed L_m, thus a larger C_r value. The voltage rating together with capacitance value determines the capacitor size. So tradeoff needs to be made for L_n design based on state-of-the-art capacitor technology to have a small resonant capacitor size. After L_n is selected, then the L_r is determined. Q and C_r are determined accordingly.

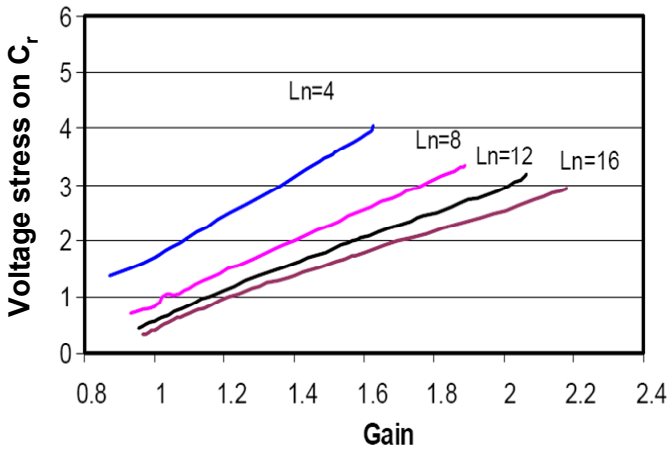


Figure 4-6. Impact of L_n on voltage stress on C_r

To summarize this existing design procedure as follows: According to the input voltage and output voltage for normal operation, the transformer turns-ratio can be designed. By choosing certain switching frequency and dead-time, the magnetizing inductor can be designed for small conduction loss and soft switching. With the required minimum input voltage for the converter, the maximum voltage gain can be checked for the designed L_m. If the required maximum voltage gain cannot be satisfied, L_m can be reduced to meet the gain requirement. After that, L_n can be designed based on the tradeoff of voltage stress and value of resonant capacitor. Finally, Q can be selected accordingly.

4.3 Effect of Dead-time

In the existing design procedure, high efficiency at normal operation and the capability of achieving enough voltage gain to regulate output voltage during the holdup time are the two design goals. It is revealed that the key to achieve high

efficiency is to design a suitable magnetizing inductor L_m. For certain switching frequency and MOSFET junction capacitor of primary switches, the magnetizing inductor is designed based on the equation:

$$L_m = \frac{T_S \cdot t_d}{16 C_j}$$

It is obvious that for a given dead-time t_d, this equation leads to an optimal magnetizing inductor based on the aforementioned design procedure. However, if the dead-time is changed, the magnetizing inductor should be changed accordingly. Now the question is for a given dead-time, the optimal magnetizing inductor can be designed, but the aforementioned design procedure cannot tell what dead-time is the optimal dead-time.

With a larger dead-time, a larger magnetizing inductor can be used while still having ZVS operation. In this case, the magnetizing current is smaller, so turn-off loss in primary switches is smaller. But it is difficult to tell whether the conduction loss is larger or smaller when the dead-time changes from a small value to a large one. In order to keep the converter running at the resonant frequency when changing dead-time, the resonant period should be kept same as shown in Figure 4-7. So with a larger dead-time, the switching period T_S, that equals T_0+2t_d, gets larger. Since the energy is transferred to the load only in the shaded area, the effective duty cycle T_0/T_S for energy transferring is smaller for the larger dead-time case. Therefore, the current difference i_{Lr}-i_{Lm} has to be increased higher to compensate the duty cycle loss caused by the larger dead-time. The RMS current in both primary side and secondary side are determined by the resonant tank current i_{Lr}

together with the magnetizing current i_{Lm} over the whole switching period. Now i_{Lm} is smaller but the current difference i_{Lr}-i_{Lm} is larger during the resonant period. So it is difficult to tell whether the conduction loss is higher or smaller with a larger dead-time before the mathematical equations are derived.

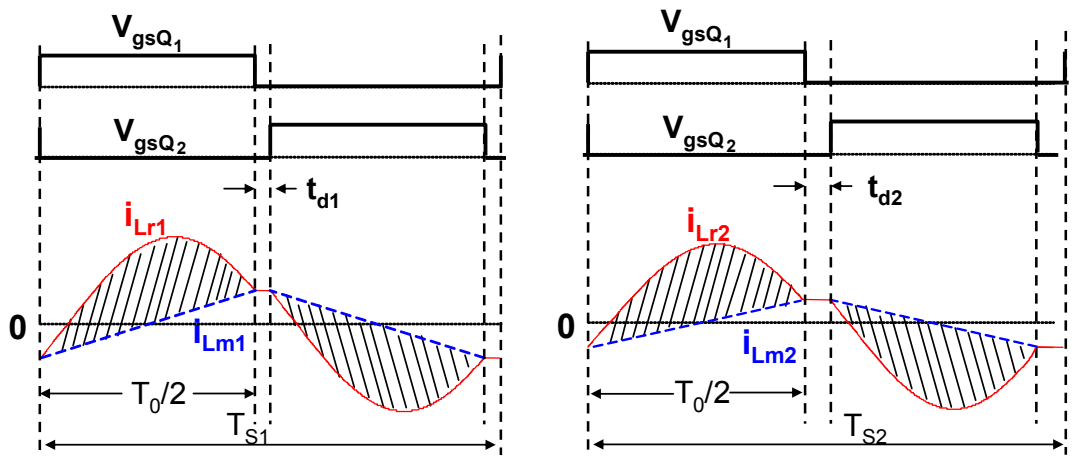


Figure 4-7. Operation waveforms w/ different dead-time t_d (t_{d1}< t_{d2})

When the dead-time is changed from a large value to a small value, the magnetizing inductor is smaller. The turn-off current of primary switch is larger, thus larger turn-off loss. For the conduction loss, the magnetizing current i_{Lm} is higher, but the current difference i_{Lr}-i_{Lm} during the resonant period is smaller. It is still difficult to tell whether the conduction loss is larger or smaller without equations because both primary side and secondary side RMS current is determined by i_{Lr} together with i_{Lm}.

In order to find out what dead-time is optimal for the design LLC resonant converters at normal operation, the equations of RMS current by counting in dead-time for both primary side and secondary side need to be derived. If the dead-time is

not neglected for quantitative analysis, the switching period is equal to T_0+2t_d. The ZVS operation condition for primary switches is

$$I_{Lmp} > \frac{2V_{in}C_j}{t_d}$$

Where V_{in} is the input voltage of LLC resonant converters, C_j is the equivalent junction capacitor of the primary switch, I_{Lmp} is the peak magnetizing current. C_j is based on the stored charge because of the nonlinearity of MOSFET junction capacitor. Assume the magnetizing current is constant during the dead-time, I_{Lmp} can be expressed as

$$I_{Lmp} = \frac{nV_O}{L_m}\frac{T_0}{4}$$

Where n is the transformer turns-ratio, T_0 is the resonant period. Then to satisfy the ZVS criteria, L_m should be

$$L_m \le \frac{T_0 \cdot t_d}{16C_j}$$

To achieve minimum conduction loss, a large L_m is preferred. At the same time, the design of L_m also needs to ensure primary switch ZVS turn-on. Therefore, L_m should be designed so the peak magnetizing current is equal to the current required for ZVS switching. That is,

$$L_m = \frac{T_0 \cdot t_d}{16C_j}$$

This conclusion is same as that in the existing design procedure.

4.3.1 Effect of Dead-time on Conduction Loss

The waveforms with dead-time t_d at the resonant frequency are shown in Figure 4-8. In half of the resonant period the resonant tank current i_{Lr} is a piece of sinusoidal wave, and the magnetizing current i_{Lm} keeps linearly increasing or decreasing. In the dead-time, the resonant tank current i_{Lr} attaches to the magnetizing current i_{Lm} to discharge junction capacitors of primary switches.

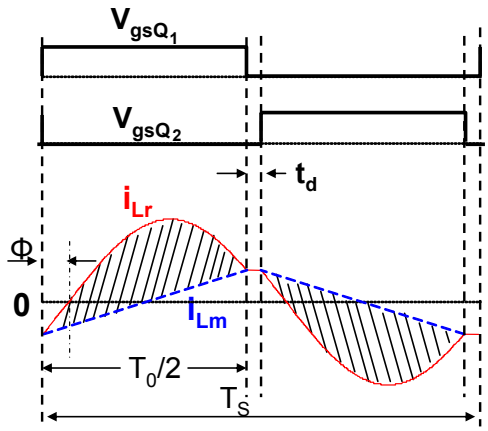


Figure 4-8. Operation waveforms at resonant frequency w/ dead-time t_d

The resonant tank current i_{Lr} during $T_0/2$ can be expressed as

$$i_{Lr}(t) = \sqrt{2} I_{RMS\_P} \sin(\omega_0 t + \Phi)$$

Where I_{RMS_P} is the resonant tank RMS current, ω_0 is the angle frequency of resonant frequency, and Φ is the initial angle of i_{Lr}. At the resonant frequency, the magnetizing inductor is charged and discharged by output voltage during half of the resonant period. The magnetizing current can be represented as

$$i_{Lm}(t) = -i_{Lm\_m} + \frac{nV_0}{L_m}(t - NT_0) \qquad \text{when } NT_0 \le t < \left(N + \frac{1}{2}\right)T_0$$

$$i_{Lm}(t) = i_{Lm\_m} \qquad \text{when } \left(N + \frac{1}{2}\right)T_0 \le t < \left(N + \frac{1}{2}\right)T_S$$

$$i_{Lm}(t) = i_{Lm\_m} - \frac{nV_0}{L_m}\left[t - \left(N + \frac{1}{2}\right)T_0\right] \qquad \text{when } \left(N + \frac{1}{2}\right)T_S \le t < (N+1)T_0$$

$$i_{Lm}(t) = -i_{Lm\_m} \qquad \text{when } (N+1)T_0 \le t < (N+1)T_S$$

Where i_{Lm_m} is the peak magnetizing current, n is the transformer turns-ratio, V_0 is the output voltage, L_m is the magnetizing inductance, N is an integer, T_0 is the resonant period, and T_S is the switching period. The peak magnetizing current is calculated as

$$i_{Lm\_m} = \frac{nV_0}{L_m} \cdot \frac{T_0}{4}$$

Based on the circuit characteristic of LLC resonant converters, at the beginning of each switching cycle, the resonant tank current is equal to the magnetizing current. Therefore, the resonant tank current at the beginning of each cycle is

$$i_{Lr}(t_0) = \sqrt{2} I_{RMS\_P} \sin(\Phi) = -\frac{nV_0}{L_m} \cdot \frac{T_0}{4}$$

The difference between the resonant tank current i_{Lr} and magnetizing current i_{Lm} is the current that goes through secondary side. So the following relationship stands,

$$\frac{\int_0^{\frac{T_0}{2}} \left[\sqrt{2} I_{RMS\_P} \sin(w_0 t + \Phi) + \frac{nV_0}{L_m} \cdot \frac{T_0}{4} - \frac{nV_0}{L_m} t\right] dt}{T_S / 2} = \frac{V_0}{nR_L}$$

In this equation, R_L is the load resistance. The RMS current of the resonant tank thus can be derived as

$$I_{RMS\_P} = \frac{1}{4\sqrt{2}} \frac{V_0}{nR_L} \sqrt{\frac{n^4 R_L{}^2 T_S{}^2}{L_m{}^2} + 4\pi^2 + \frac{16\pi^2 (T_0 t_d + t_d{}^2)}{T_0{}^2}}$$

The resonant tank current continues going through the primary switches, so this RMS current determines the primary side conduction loss. Compared this equation with the resonant tank RMS current without considering dead-time, it can be observed that there is an additional term related to the dead-time. To substitute L_m with $L_m = \frac{T_0 \cdot t_d}{16 C_j}$, the resonant tank RMS current can be expressed as

$$I_{RMS\_P} = \frac{1}{4\sqrt{2}} \frac{V_0}{nR_L} \sqrt{\frac{256 C_j{}^2 n^4 R_L{}^2}{t_d{}^2} + 4\pi^2 + \frac{16\pi^2 (T_0 t_d + t_d{}^2)}{T_0{}^2}}$$

Where V_0 is the output voltage, n is the transformer turns-ratio, R_L is the load resistance, C_j is the junction capacitance of primary switches, T_0 is the resonant period, and t_d is the dead-time. For any specific load, the resonant tank RMS current is only determined by the magnetizing inductance or the dead-time t_d because all other parameters such as transformer turns-ratio and output voltage are predetermined according to the converter specifications. For example, for a 1MHz, 1kW, 400V to 48V LLC resonant converter, if APT5024BFLL from APT is selected as primary switches, n is designed as 4, the relationship between the resonant tank RMS current and the dead-time t_d at full load and 50%I_{omax} is shown in Figure 4-9. Since one dead-time corresponds to one magnetizing inductance, L_m is put in Figure 4-9 as the 2nd x-axis. The resonant tank RMS current is a U-shape curve as a

function of the dead-time. It means that there is an optimal magnetizing inductor determined by an optimal dead-time, which leads to the minimum resonant tank RMS current. Also it can be seen the optimal dead-time for different load is different.

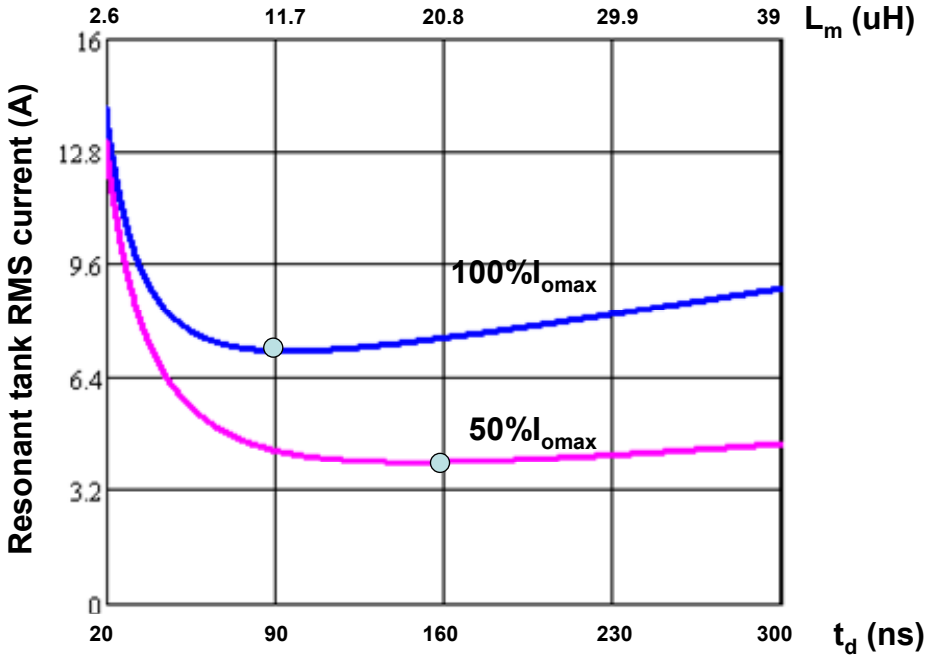


Figure 4-9. Resonant tank RMS current vs. dead-time t_d

Besides the primary side conduction loss, the secondary side conduction loss also needs to be investigated especially for low output voltage and high output current applications. It is very desirable to minimize the secondary side RMS current. In order to achieve higher efficiency, the synchronous rectifier is preferred. The current in the synchronous rectifier is the difference between the resonant tank current and the magnetizing current, then the RMS current in the SR can be calculated based on the RMS current definition,

$$I_{RMS\_S} = \sqrt{\frac{\int_0^{\frac{T_0}{2}} \left[i_{Lr}(t) - i_{Lm}(t) \right]^2 dt}{T_S / 2}}$$

The closed-form equation can be expressed as,

$$I_{RMS\_S} = \frac{\sqrt{3}}{24\pi} \frac{V_0}{R_L} \sqrt{\frac{(5\pi^2 - 48) n^4 R_L{}^2 T_0{}^3}{L_m{}^2 (T_0 + 2t_d)} + \frac{12\pi^4 T_0}{T_0 + 2t_d} + \frac{48\pi^4 (T_0 t_d + t_d{}^2)}{T_0 (T_0 + 2t_d)}}$$

To substitute L_m in this equation, the secondary side RMS current is,

$$I_{RMS\_S} = \frac{\sqrt{3}}{24\pi} \frac{V_0}{R_L} \sqrt{\frac{256 \cdot C_j{}^2 (5\pi^2 - 48) n^4 R_L{}^2 T_0}{t_d{}^2 (T_0 + 2t_d)} + \frac{12\pi^4 T_0}{T_0 + 2t_d} + \frac{48\pi^4 (T_0 t_d + t_d{}^2)}{T_0 (T_0 + 2t_d)}}$$

The secondary side RMS current is also entirely determined by dead-time design. For instance, for a f_0=1MHz, 1kW, 400V to 48V LLC resonant converter, the relationship between the SR RMS current and the dead-time t_d at full load and 50%I_{omax} is shown in Figure 4-10. For the same reason, L_m is put in Figure 4-10 as the 2nd x-axis. The SR RMS current is also a U-shape curve as a function of the dead-time. It means there is an optimal magnetizing inductance determined by an optimal dead-time, which leads to the minimum RMS current in the SR at a specific load condition. The optimal dead-time for different load is different, either.

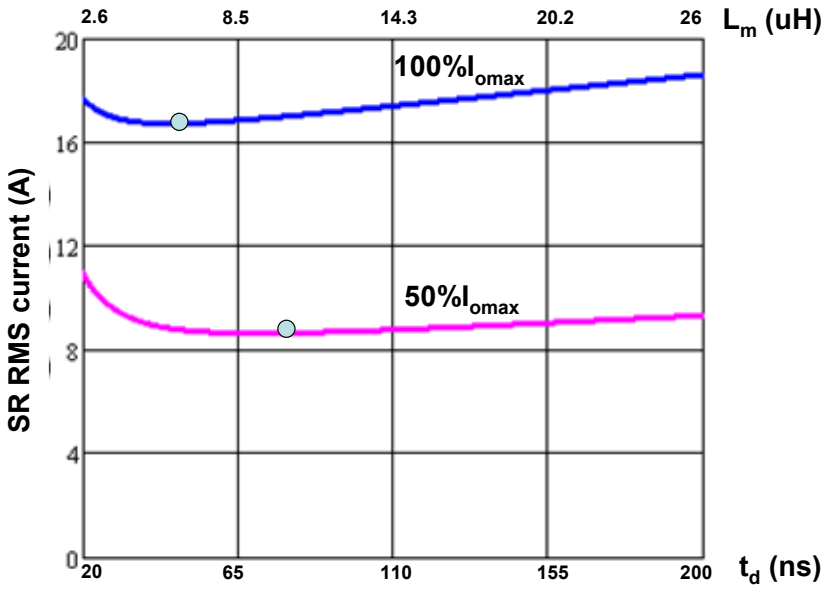


Figure 4-10. SR RMS current vs. dead-time t_d

Through the above analysis, both the primary side and secondary side RMS current is only determined by the magnetizing inductor that is determined by the dead-time design when LLC resonant converters operate at the resonant frequency. Thus both the primary-side and secondary side conduction loss is determined by the dead-time design. It is not true as the conventional wisdom states that the smaller dead-time, the better efficiency. The fact in LLC resonant converters is that conduction loss vs. dead-time curve is a U-shape curve. There is an optimal dead-time that gives minimum conduction loss at a specific load. For different load, the optimal dead-time is different.

4.3.2 Effect of Dead-time on Switching Loss

Because ZVS turn-on can be achieved for primary switches, there is no turn-on loss for primary switches in LLC resonant converters. The switching loss in LLC resonant converters at the resonant frequency is the turn-off loss of primary switches. The turn-off loss is determined by the turn-off current and the length of turn-off transition time. The turn-off current is the peak magnetizing current that is determined by the magnetizing inductor. As discussed aforementioned, one magnetizing inductor corresponds to one dead-time. So it is the dead-time that determines the switching loss in LLC resonant converters.

According to the operation characteristic of LLC resonant converters at the resonant frequency, the turn-off current of primary switches are same over the whole load range. So the switching loss over the whole load range is same. In order to investigate the switching loss, a loss model is needed. Quite lot efforts are spent on developing loss models in the past years. Basically, the loss models can be classified into three types. One is physics-based loss model. The physical parameters of the device, such as geometry, doping density etc., are input into simulation software, e.g. Medici and ISE, to do finite element analysis (FEA). Simulation results are close to reality with this method. However, it takes a long time for simulation. For example, it normally takes one to two days to simulate only two switching cycles of a simple buck converter. The second method is to use device behavior model which has some key parameters to describe the device. Almost every device vendor provides behavior model for its device. The behavior model of

device is put into some simulation software, e.g. Saber, to achieve the switching loss. This method has good tradeoff between accuracy and simulation time. The third one is called analytical loss model or mathematical model. For this method, mathematical equations are derived based on some equivalent circuits. Then the switching loss can be calculated based on the derived equations.

For LLC resonant converters, not like conduction loss which is not same for any different load condition, the switching loss is same over the whole load range, thus the switching loss investigation with both behavior model and analytical model is acceptable from time consumption point of view. The switching loss for a 1MHz, 1kW, 400V to 48V LLC resonant converter at different dead-time is shown in Figure 4-11. For the same reason, the magnetizing inductance is shown as the 2nd x-axis. These data are based on Saber simulation with device model.

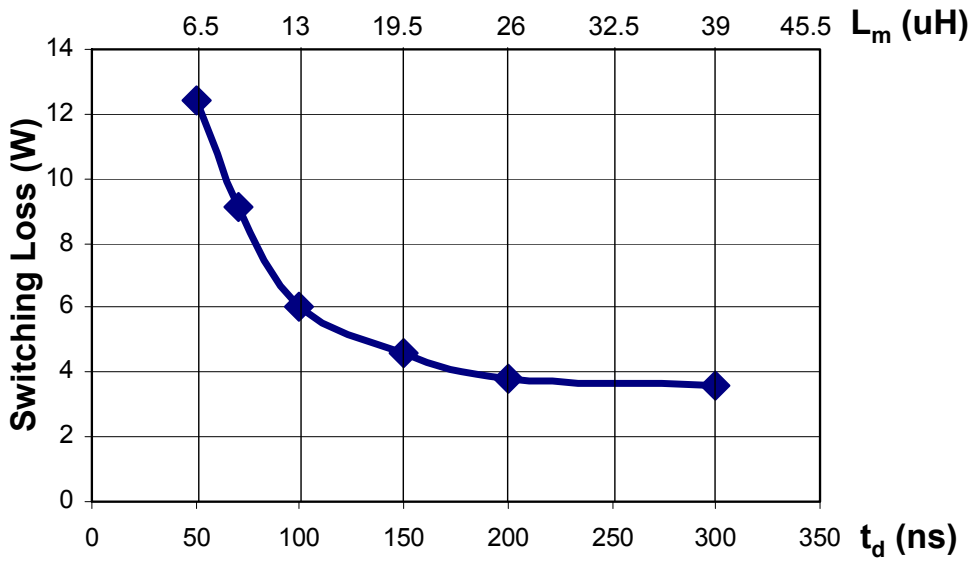


Figure 4-11. Switching loss vs. dead-time t_d

It can be seen that the switching loss keeps decreasing with the increasing of the dead-time. However, the effectiveness of increasing dead-time is limited when it is larger than 200ns for this example. This phenomenon somehow can be explained as the high voltage in the primary side. When the dead-time is larger, the turn-off current of primary switches is smaller. However, the turn-off transition time is longer. Although the current during the turn-off transition period is smaller, the switching loss is not much reduced due to the longer time period of overlapping of switch current and high voltage.

4.4 Dead-time Optimization for High Efficiency

Through the above analysis, both the conduction loss and switching loss for LLC resonant converters operating at the normal condition is only determined by the magnetizing inductance that is determined by the dead-time design. So in order to achieve high efficiency at the normal operation condition, it is to design an optimal dead-time that gives the optimal magnetizing inductance. As shown in the previous two sections, for the conduction loss, the optimal dead-time at different load conditions is different for both primary side and secondary side; for the switching loss, it is same over the whole load range at a specific dead-time. Furthermore, at a specific load condition, the optimal dead-time for primary side conduction loss and secondary side conduction loss is also different. Thus the dead-time optimization should be made based on the total loss of conduction loss and switching loss.

Figure 4-12 shows the relationship between the total power loss and dead-time at the full load on the 1MHz, 1kW LLC resonant converter. APT5024BFLL from APT is selected as primary switch. L_m is designed based on the junction capacitance of APT5024BFLL and different dead-time. Dead-time t_d=100ns is the optimal point for minimum loss at full load.

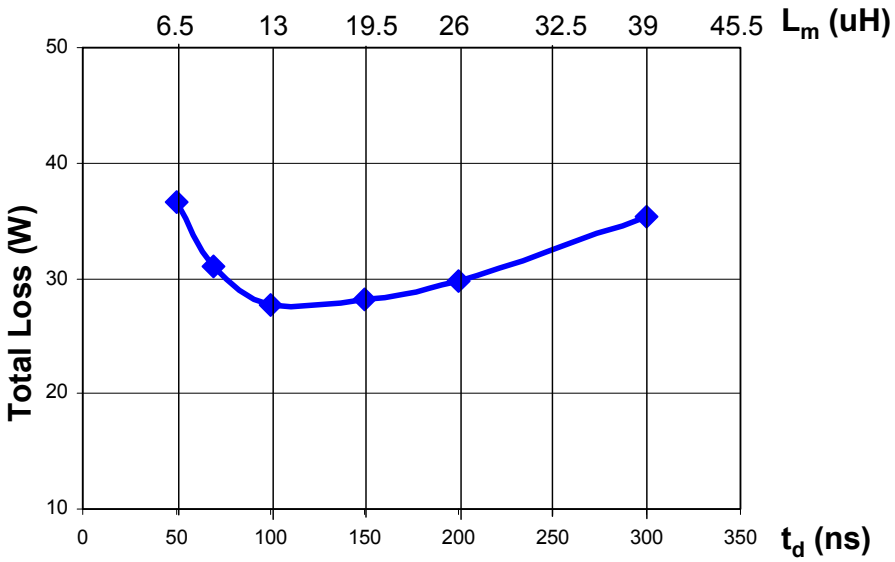


Figure 4-12. Total loss vs. dead-time t_d

However, nowadays the full load is not the only load condition for the high efficiency requirement. In the real world, 70%~80%I_{omax} load condition stands more time than the full load. Furthermore, in order to comply with those energy saving regulations initiated by some international official organizations, industry has raised the efficiency requirement for 50% load, even down to 20% load. High efficiency over a wide load range is the requirement in the real world.

The analysis of dead-time optimization makes high efficiency optimization over a wide load range achievable. Based on the analysis in the previous sections, the

optimal dead-time for a specific load condition can be found. With this method, the total loss over a wide load range at one dead-time can be easily plotted. Then a bunch of total loss curves with different dead-time can be plotted. At what load range, what dead-time can give higher efficiency is obvious on the curves. As an example, Figure 4-13 shows the total loss over 20% load to the full load at several different dead-times for the aforementioned 1MHz, 1kW LLC resonant converter.

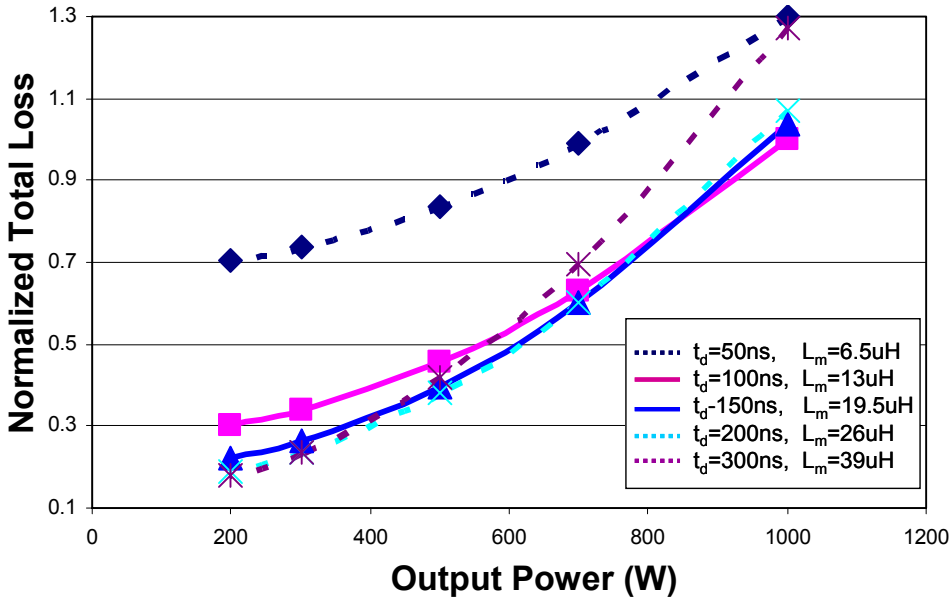


Figure 4-13. Total loss over wide load range w/ different dead-time t_d

It can be observed from Figure 4-13 that the 100ns dead-time can give the best efficiency at the full load while 300ns dead-time can give better performance at less than 50% load conditions. Among these power loss curves, the dead-time 150ns makes a better tradeoff between the heavy load and the light load.

4.5 Experiment Results and Summary

A 1MHz, 1kW, 400V-48V prototype, shown in Figure 4-14, is built to verify the dead-time optimization for the LLC resonant converter at normal operation condition. Synchronous rectification with the driving scheme developed in Chapter 3 is applied. The magnetizing inductance L_m is chosen based on different dead-time. The resonant inductor L_r is kept the same as 1μH and the resonant capacitor C_r is kept the same as 25nF for different L_m which corresponds to different t_d designs. The transformer turns ratio is 4. For the primary switch, APT5024BFLL from APT is selected according to 400V input, 1kW power level and high switching frequency 1MHz. 150V Trench MOSFET FDP2532 from Fairchild is selected for the secondary synchronous rectifier for small R_{ds_on}.

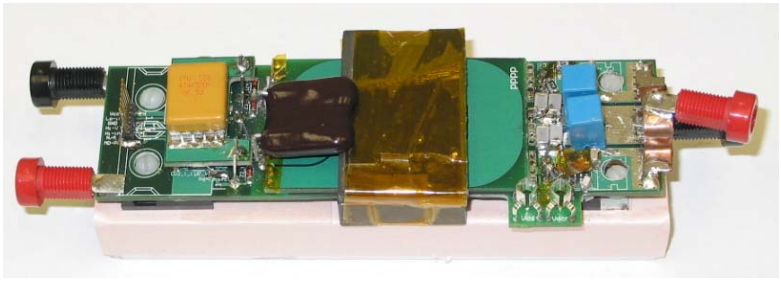


Figure 4-14. 1MHz 1kW 400V-48V LLC resonant converter with SR

The measured efficiency with different dead-time design is shown in Figure 4-15. The measured results match the previous dead-time optimization analysis quite well. The best efficiency at full load is achieved with the design of t_d=100ns. When the load is below 20%I_{omax}, the design with a larger dead-time gives a better performance. Considering the efficiency over a wide load range 20%I_{omax} to full load,

the design with 150ns dead-time can achieve a better overall performance. Because the efficiency of design with t_d=150ns is close to that with t_d=100ns at heavy load while it can achieve 1.5% higher efficiency at 20%I_{omax} and 3% higher efficiency at around 10%I_{omax}. However, it is not to say the design of t_d=150ns is always the best. Actually, which efficiency curve is better depends on the specific efficiency requirement for the wide load range.

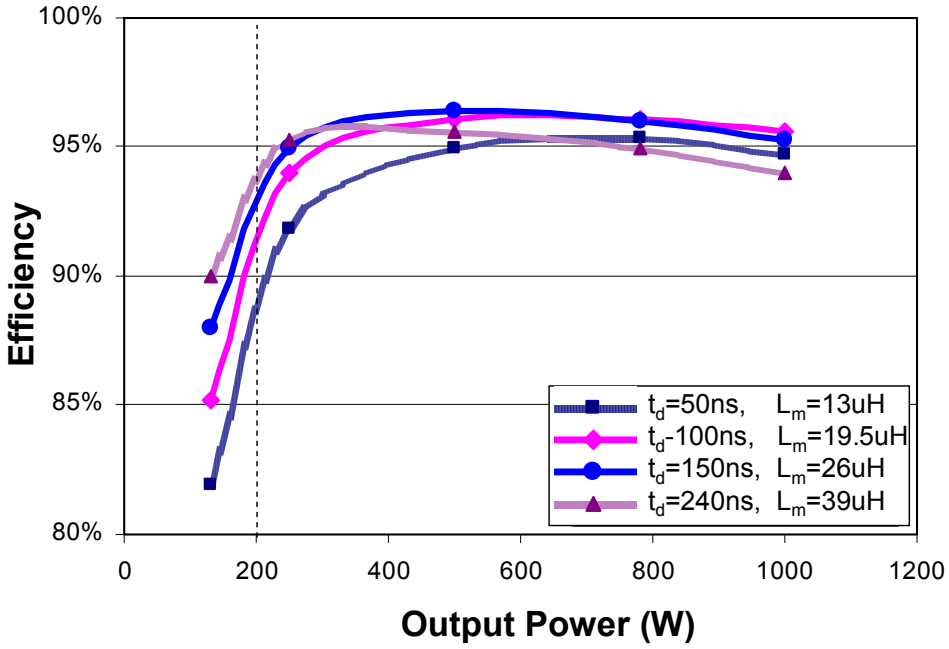


Figure 4-15. Measured efficiency w/ different dead-time design

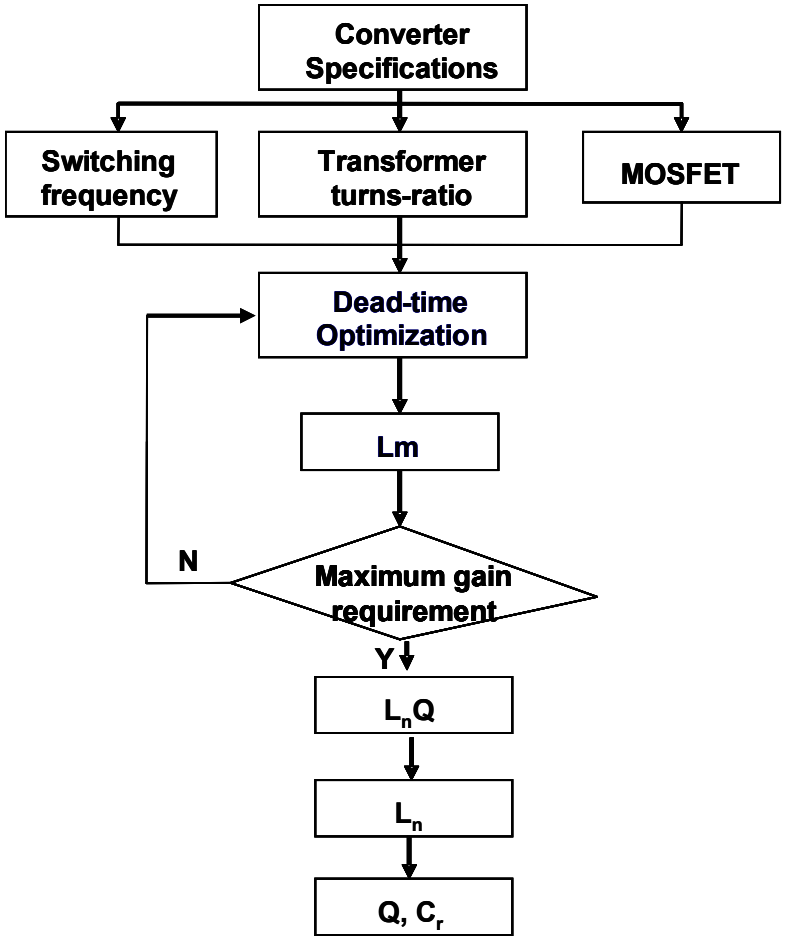


Figure 4-16. Design procedure of LLC resonant converter

This chapter focuses on the design procedure of LLC resonant converters. One existing design procedure is introduced first, and then some improvements to the design procedure on optimization at normal operation are developed. Through the analysis, the performance at normal operation is only determined by the magnetizing inductor design which is determined by the design of dead-time. After mathematical equations derivation for both primary side and secondary side RMS current with consideration of dead-time, it is revealed that both primary side and secondary side RMS current have a U-shape curve vs. dead-time. There is an optimal dead-time

that can achieve the minimum power loss for a specific load. By plotting the total loss over the wide load range with a bunch of different dead-time designs, it is achievable to find the dead-time which can have a better overall performance over a wide load range instead of optimization only at the full load condition. The flowchart representing the whole design procedure of LLC resonant converters is shown in Figure 4-16.

Chapter 5 Summary and Future Work

5.1 Summary

With the development of information technology, the market for power management of telecom and computing equipment keeps increasing. Distributed power systems are widely adopted in the telecom and computing applications for the reason of high performance and high reliability. As one of the key building block in distributed power systems, DC/DC converters in the front-end converters are still under the pressure of increasing efficiency and power density. Furthermore, recently industry brought out aggressively high efficiency requirements for a wide load range for power management in telecom and computing equipment. High efficiency over a wide load range is now a requirement. Due to the hold-up time requirement, bulk capacitors are normally put at the input of DC/DC converters. In order to achieve high power density, DC/DC converters with wide input voltage range capability are preferred. PWM DC/DC converters cannot achieve high efficiency for well known reasons when they are designed for wide input voltage range. As a promising topology for this application, LLC resonant converters can achieve both high efficiency and wide input voltage range capability because of the voltage gain characteristics.

This thesis focuses on how to improve the efficiency of LLC resonant converters. In chapter 3, the complete solution of synchronous rectification of LLC resonant converters is discussed. The driving of synchronous rectifier can be realized by sensing the voltage V_{ds} of the SR. The turn-on of the SR can be triggered by the

body-diode conduction of the SR. With the V_{ds} compensation network, the precise voltage drop on the R_{ds_on} can be achieved, thus the SR can be turned off at the right time. Compared with the diode version, more than 3% higher efficiency is achieved at the full load on a 1MHz, 1KW LLC resonant converter with synchronous rectification.

In chapter 4, the efficiency optimization at normal operation over a wide load range is discussed. It is revealed that the power loss at normal operation is solely determined by the magnetizing inductor while the magnetizing inductor is designed according to the design of dead-time t_d. The relationship between the power loss and the dead-time provides a tool for the efficiency optimization. With this tool, the efficiency optimization of LLC resonant converters can be done according to efficiency requirement over a wide load range.

5.2 Future Work

5.2.1 Digital Control of SR Driving

The complete solution of the SR driving for LLC resonant converters is realized with discrete analog components as discussed in chapter 3. Although the idea for the SR driving is simple, the implementation in the analog way is not simple. Furthermore, due to the parameters variation from component to component, some design margin needs to be left when the analog approach is adopted in production. However, with digital technology, improvements in both above two aspects are

expected. Figure 5-1 shows the drawing of analog approach and the concept drawing of digital approach. With the digital approach, the V_{ds} compensation network is still there, which provides the proper voltage on R_{ds_on} while the SR is on. All calculation and control functions can be left for the digital control. A perfect SR driving is expected with the powerful calculation and self-learning capability of the digital approach.

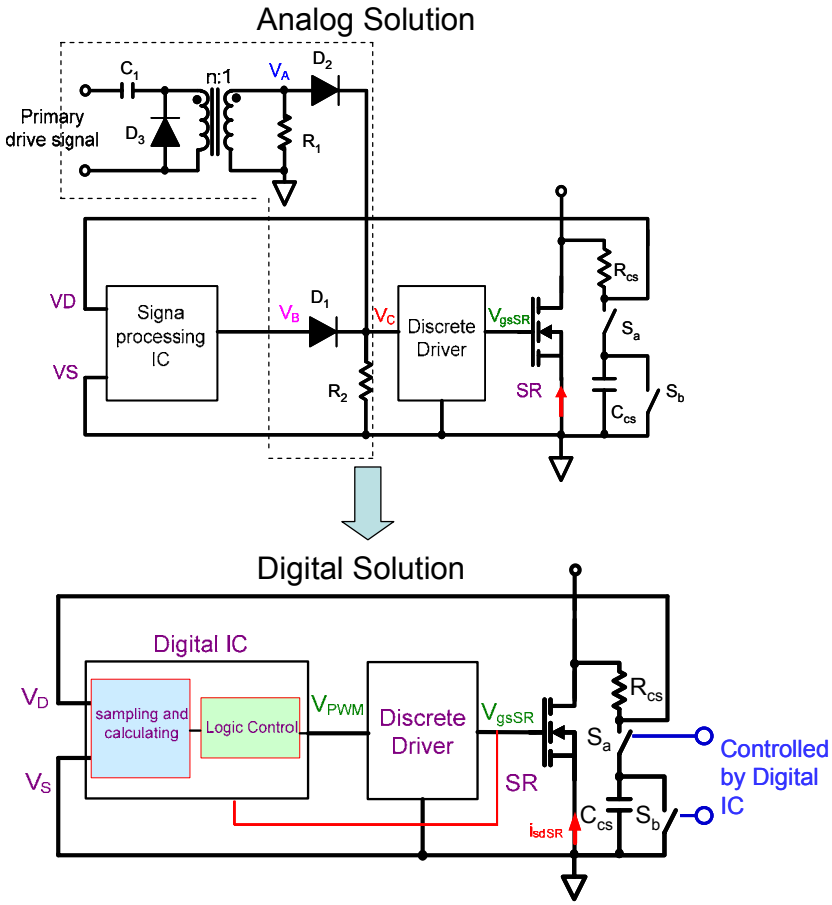


Figure 5-1. Digital solution of SR driving in LLC resonant converter

5.2.2 Green Mode Operation of LLC Resonant Converter

With the pressure of energy saving regulations, high efficiency at very light load, even power consumption at no load will be requirements for power converters in next a few of years. For the LLC resonant converter, this kind of requirements cannot be satisfied if it always operates in the continuous operation mode. The reason is that the switching related loss and core loss of the power transformer are almost same for the whole load range.

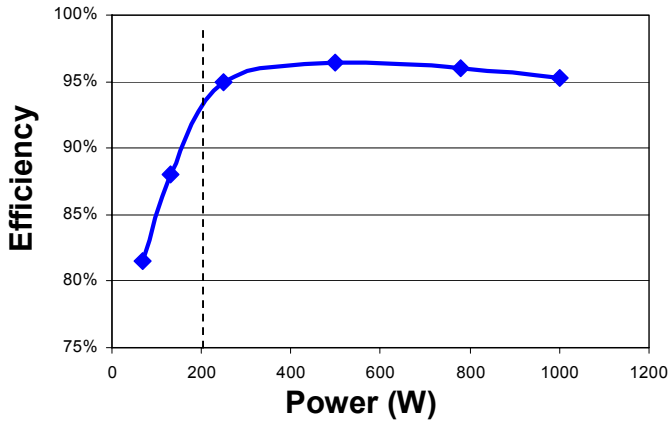


Figure 5-2. Measured efficiency on 1MHz, 1kW LLC converter (SR version)

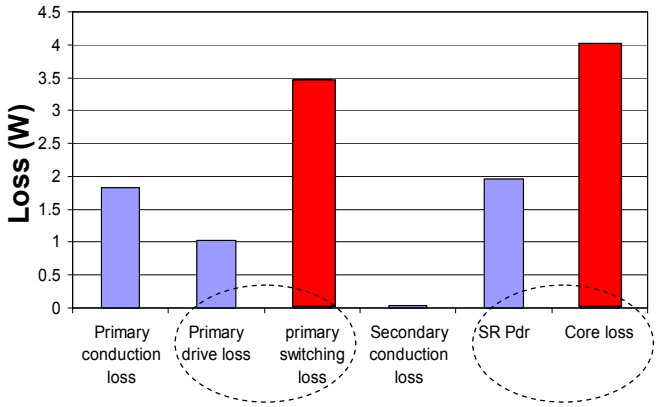


Figure 5-3. Loss breakdown of LLC resonant converter at 5%P_{omax}

The measured efficiency on a 1kW, 400V to 48V LLC resonant converter is shown in Figure 5-2. The efficiency at light load drops very quickly. From the loss breakdown at 5%P_{omax} shown in Figure 5-3, it can be seen that the highest two loss

parts are the core loss of power transformer and switching loss. The primary drive loss and secondary SR drive loss are also switching related loss. This loss-breakdown tells that in order to achieve high efficiency at light load, the approach is to reduce the switching related loss.

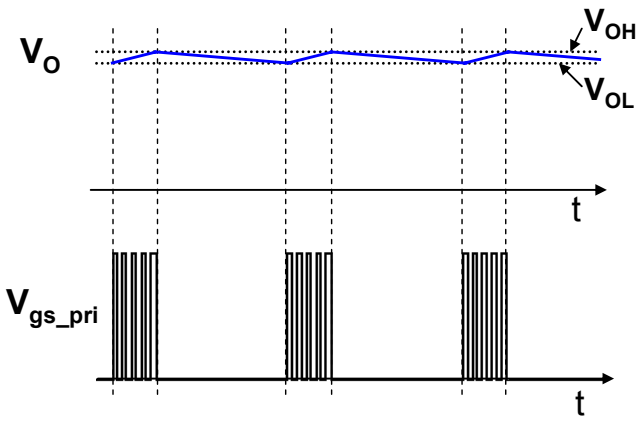


Figure 5-4. Concept of green mode operation

Green mode operation is one effective way to reduce the switching related loss. The concept of the green mode operation is shown in Figure 5-4 in which V_{gs_pri} is drive signal of the primary switch of LLC resonant converters. When the pre-set light load condition is reached, the converter enters the green-mode operation. During the green mode operation, there is a pre-set window for the output voltage. The LLC resonant converter is turned off when its output voltage reaches the up-threshold V_{OH} of the pre-set voltage window. After the converter is turned off, bulk output capacitors of the converter provides energy to the load. The output voltage decreases gradually with the decay of energy stored in the output capacitors. When the output voltage touches the bottom-threshold V_{OL} of the pre-set voltage window, the converter is turned on again.

When the LLC resonant converter operates in the green mode, it operates for some time, and then rests for some time. All switching related loss will be reduced in this operation mode. Core loss will be reduced, too. High efficiency can be expected.

However, there are some challenges with the green mode operation of LLC resonant converters. For PWM converters, during the green mode operation, when converters are turned on when the bottom output voltage threshold V_{OL} is reached, the current in switches can be well limited by the error signal of the closed feedback loop. In other words, it is a kind of soft-start procedure. For LLC resonant converters, the case is quite different. Figure 5-5 shows one control algorithm for LLC resonant converters in the green mode operation [5.3]~[5.7]. When the load changes from the heavy load to the light load, the feedback loop regulates the V_o by increasing the switching frequency. If the pre-set light load condition for the green mode is reached, the converter enters the green mode. The frequency at the pre-set load for the start of the green mode is set as f_{smax}. The converter operates at f_{smax} during the on period in the green mode operation. The design of the 1MHz, 1kW, 400V to 48V LLC resonant converter is again taken as an example to demonstrate the operation of the green mode operation with this kind of conventional control algorithm. The simulated waveforms at $5\%I_{omax}$ in the green mode with this control algorithm are shown in Figure 5-6. It can be seen that there is a high surge current in the circuit, which is even higher than that at the full load in the continuous operation mode as shown in Figure 5-7.

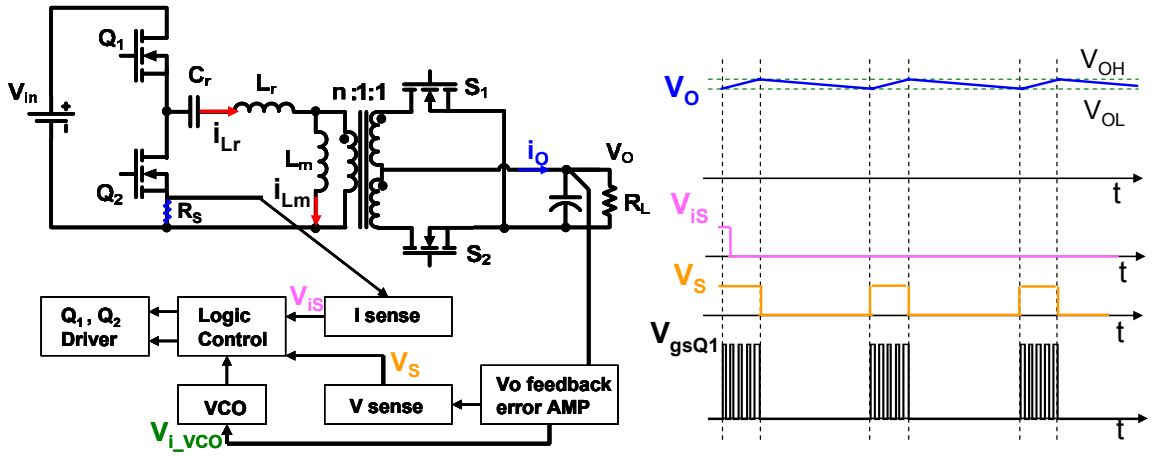
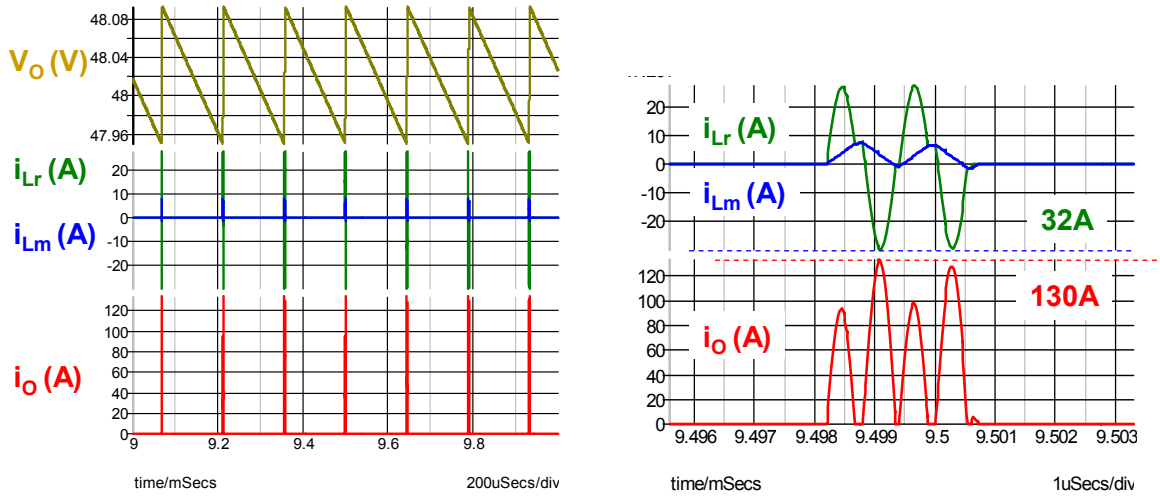


Figure 5-5. One control algorithm of green mode operation in LLC converter



(a) Simulation waveforms at 5%I_{omax} **(b) Zoomed in waveforms of (a)**

Figure 5-6. Simulation waveforms of green mode operation in LLC converter

There are two reasons for this high surge current. The first reason is the voltage gain mismatch as shown in Figure 5-8. According to the control algorithm, when the load reaches the pre-set load condition for the green mode operation, the converter is turned off to enter in the green mode. This pre-set load condition for the start of the green mode corresponds to the switching frequency f_{smax} as shown in Figure 5-8. Then the output voltage of the converter begins to drop. When the output of the

converter touches the pre-set bottom threshold V_{OL} which corresponds to f_{SVOL} in Figure 5-8, the LLC resonant converter is turned on with f_{smax}. The input and output of the resonant tank has a gain mismatch at the turn on as shown in Figure 5-8. This gain mismatch can cause high surge current in the resonant tank.

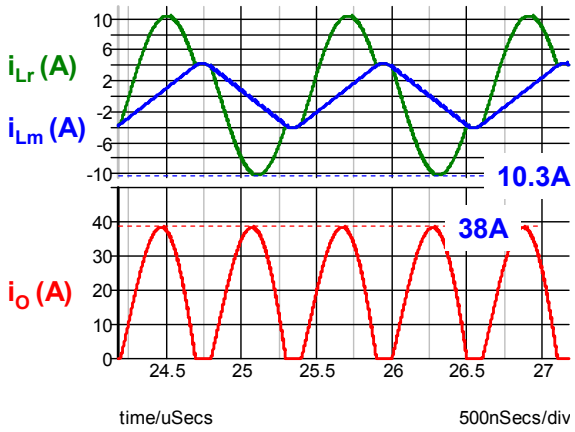


Figure 5-7. Simulation waveforms at full load in continuous operation mode

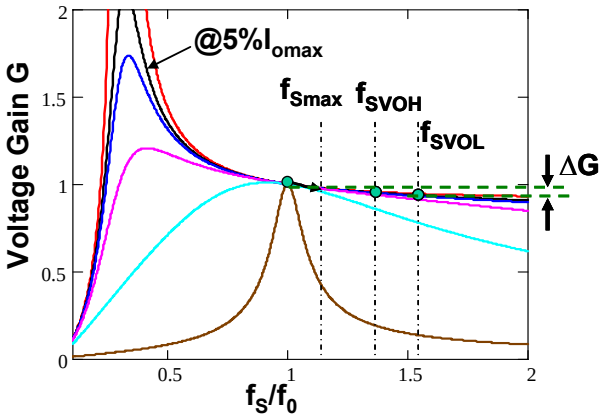
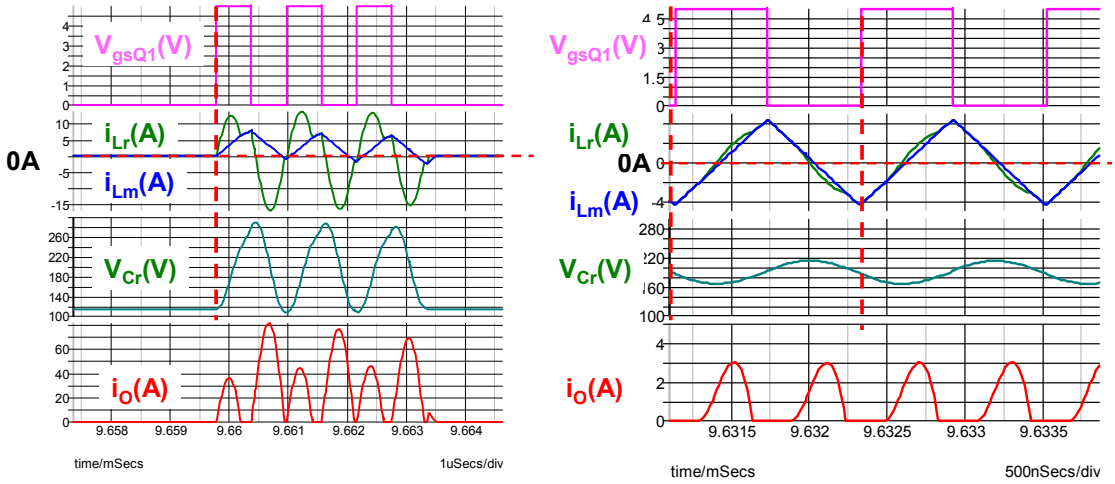


Figure 5-8. Gain mismatch of green mode operation in LLC converter

The other reason for high surge current in the green mode is shown in Figure 5-9. Figure 5-9(a) shows the operation waveforms at 5%I_{omax} in the green mode and Figure 5-9(b) shows the operation waveforms at 5%I_{omax} in the continuous operation mode. It can be observed that in the continuous operation mode, the magnetizing current is always at the peak value at the turn-on edge of primary switches and

crosses 0A at $T_S/4$. However, when the LLC resonant converter is turned on in the green mode as shown in Figure 5-9(a) the magnetizing current starts from 0A, but reaches twice of peak value as that in the steady state. Also the voltage on the resonant capacitor is not same as that in the steady state. The incorrect initial conditions for resonant components cause high surge current in the circuit.



(a) Green mode operation at 5%I_{omax} **(b) Continuous operation at 5%I_{omax}**

Figure 5-9. Simulation waveforms comparison

With the expectation to reduce the high surge current in the green mode operation of LLC resonant converters, a new control algorithm is proposed in Figure 5-10. Since there will be high switching loss when the LLC resonant converter works at the switching frequency higher than the resonant frequency, the converter is designed with switching frequency a little bit smaller than the resonant frequency. Compared with the conventional control algorithm, this control algorithm makes LLC resonant converters work in a totally different way. The regulated V_o is set as the bottom threshold V_{OL} of the output voltage window and the up-threshold V_{OH} of output voltage window is set higher than the regulated V_o. When the load gets

lighter, the converter regulates its output by increasing the switching frequency. When the pre-set load condition for the green mode operation is reached, the switching frequency corresponding to this load condition is remembered as f_{SVOL} as shown in Figure 5-10. Then the voltage gain of the converter is raised up by decreasing the switching frequency so the up-threshold V_{OH} can be reached. The converter is turned off at the time when the up-threshold is touched. Then the output bulk capacitors support the output load. When the bottom threshold V_{OL} is reached after some time, the converter is turned on with the remembered switching frequency f_{SVOL}. In this way, there is no gain mismatch when the converter is turned on. In other words, when the converter is turned on, the resonant tank current i_{Lr} should be the same as the magnetizing current if all resonant components are with correct initial conditions. There is no energy transferring to the output. Then the voltage gain of the converter is raised up by decreasing its switching frequency to touch V_{OH} to repeat the burst cycle. Another novelty of the proposed control algorithm is that the primary top switch is turned on with ¼ of the switching period for the first switching cycle as shown in Figure 5-10. In this way, the magnetizing current will match well with that in the steady state. With this control algorithm, there is no gain mismatch at the turn-on of the LLC resonant converter in the green mode. The magnetizing inductor and the resonant inductor are with correct initial condition at the turn-on of the converter.

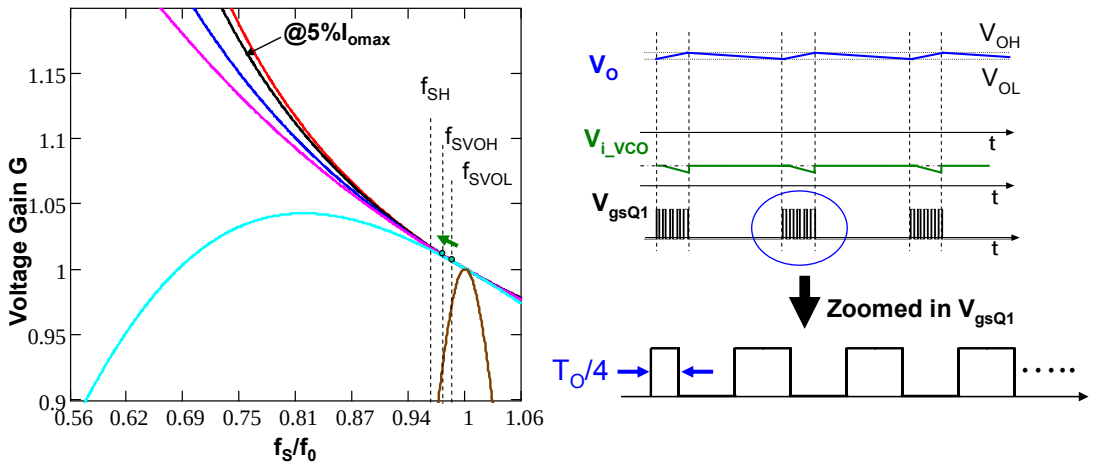
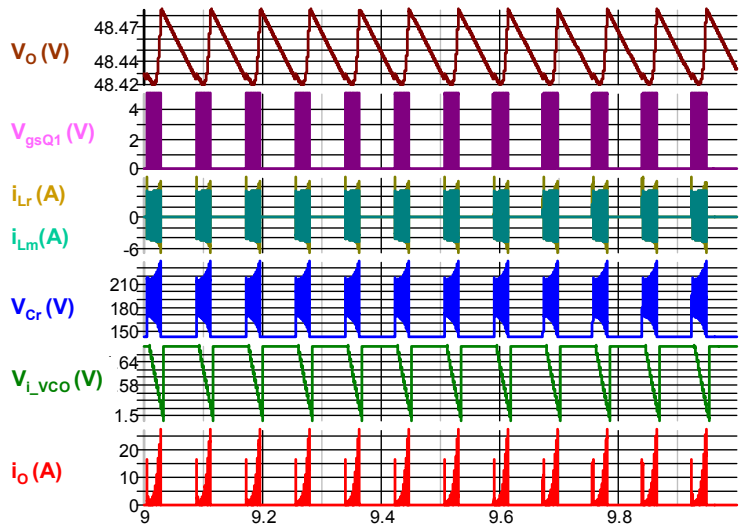


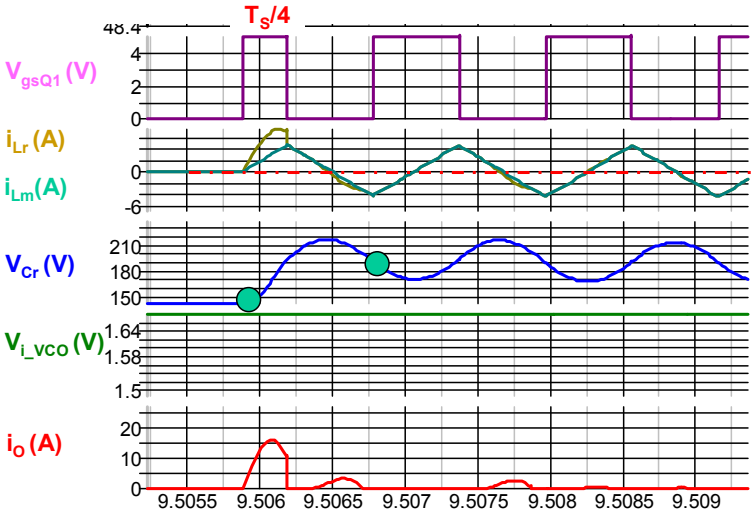
Figure 5-10. Proposed control algorithm for green mode operation of LLC resonant converter

The simulated waveforms at 5%I_{omax} with the proposed control algorithm for the green mode operation of LLC resonant converters is shown in Figure 5-11. It can be clearly seen from the zoomed-in waveforms that the magnetizing inductor is excited from 0A and reaches peak value after ¼ of the switching period in the first switching cycle at the turn-on. However, the resonant tank current is not same as magnetizing current as expected. This is caused by the incorrect initial voltage on the resonant capacitor at the turn-on as shown in Figure 5-11(b). But with this proposed control algorithm, the surge current at turn-on in the green mode can be greatly reduced, which makes the green mode operation of LLC resonant converters possible.

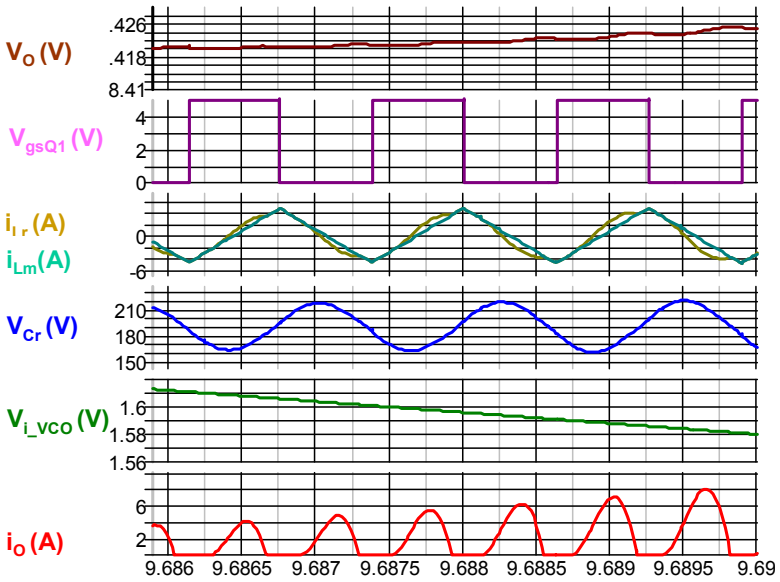
In order to have good performance of LLC resonant converters in the green mode operation, there are a lot of work remained. How to achieve the right initial voltage on the resonant capacitor for the first switching cycle in the green mode is very critical to improve the performance. To implement the control algorithm with the digital control is another interesting aspect of this research topic for future work.



(a) Key simulation waveforms w/ the proposed control algorithm



(b) Zoomed in waveforms at turn-on



(c) Zoomed in waveforms during on period of green mode operation

Figure 5-11. Simulation waveforms w/ the proposed control algorithm for green mode operation of LLC resonant converter

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