ON Semiconductor®

Introduction to LLC resonant converters

Roman Stuler

Agenda

- Introduction
- Switching techniques in SMPS
- Soft switched topologies
- Resonant topologies
- Configurations of the HB LLC converter and a resonant tank
- Operating states of the HB LLC with discrete resonant tank
- HB LLC converter modeling and gain characteristics
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- Secondary rectification design and output cap dimensioning
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- Overcurrent protection sensing
- Design example of 12 V / 20 A output LLC converter with SR

Introduction - Regulatory Agencies Targets

- **Standby (no load) Power Reduction**
  - ~25% of total energy passing through power supplies is in standby mode[13]
  - Concerted effort by worldwide regulatory agencies
- **Active Mode Efficiency Improvement**
  - ~75% of total energy passing through power supplies is in active mode[13]
- **Power Factor Correction (or Harmonic Reduction)**
  - Applicable with IEC61000-3-2[11] (Europe, Japan)
  - Some efficiency specifications also require >0.9 PF.
    → example: computers (ENERGY STAR® rev. 4[12])

=> Energy conversion efficiency significantly affects total power consumption !

China CSC[6] (ex-CECP),

Japan Top Runner[9] program

Japan Eco Mark[10] program

Korea e-Standby program[8]

Australia AGO[7]

California CEC[5]

Europe COC[4]

ENERGY STAR®[3]

Energy Efficiency Regulations

Computing

•**Desktops**:
- ENERGY STAR® 5.0 effective on Jul. 1, 2009
- 80 PLUS & Climate Savers Computing Initiative
- Tiered efficiency levels

•**Laptops** (More information at ENERGY STAR® 2.0 for External Power Supplies)
- Efficiency: ≥ 87%
- Standby (no load) power: ≤ 500 mW
- PF ≥ 0.9

Solid State Lighting Luminaires

•ENERGY STAR® 1.1 effective on Feb. 1, 2009
- Off-state power: 0
- Minimum efficacy (Lumen/Watt) requirements by applications (downlights, outdoor lights, etc…)
- PF ≥ 0.9 for Commercial
  ≥ 0.7 for Residential

•ENERGY STAR® 1.2 effective in 2H2009

•ENERGY STAR® additional requirements LED bulbs
- PF ≥ 0.7
- High system efficacy → high efficiency power supply

Set-Top Boxes (STB)

•ENERGY STAR® 2.0 effective on Jan 1, 2009

•Europe Code of Conduct version 7 effective Jan 1, 2009
- Standard is based on maximum allowable TEC (Total Energy Consumption in kWh/year) or allowance
- Base Allowance depends on the type of STB (Cable, Satellite, etc…)
- Additional functionalities allowance (DVR, etc…)
- Annual Energy Allowance (kWh/year) = Base Functionality Allowance + Additional Functionalities Allowance

For up-to-date information on agencies and regulations, check the PSMA energy efficiency data base at:
www.psma.com

Regulation example - Computing Power Supplies

	Levels	Specification	Efficiency (%) 20% of rated output power	50% of rated output power	100% of rated output power	Effective Date
Single-Output	80 PLUS BRONZE **CSCI Bronze**	• Single-Output • Non-Redundant • PFC 0.9 at 50%	81%	85%	81%	**Start June 2007**
	80 PLUS SILVER **CSCI Silver**	• Single-Output • Non-Redundant • PFC 0.9 at 50%	85%	89%	85%	**Start June 2008**
	80 PLUS GOLD **CSCI Gold**	• Single-Output • Non-Redundant • PFC 0.9 at 50%	88%	92%	88%	**Start June 2010**
	CSCI Platinum	• Single-Output • Non-Redundant • PFC 0.9 at 50%	90%	94%	91%	**Target**

All in 1 PC

Sources:

- 80 PLUS® : http://www.80plus.org/
- Climate Savers® Computing Initiative: http://www.climatesaverscomputing.org/
- ENERGY STAR®: http://www.energystar.gov/index.cfm?c=revisions.computer_spec

Summary

- World consumption of energy increases year-by-year (More and more Computers, LCD and PLASMA TVs, Game consoles)
- Significant portion of energy is lost during power conversion and also during standby mode
- Conversion efficiency has to be increased and no-load consumption has to be minimized to assure that given power networks will be able to supply increased number of electric equipment
- Energy agencies releasing various national programs that define minimum equipment efficiency and maximum no-load consumption in given category

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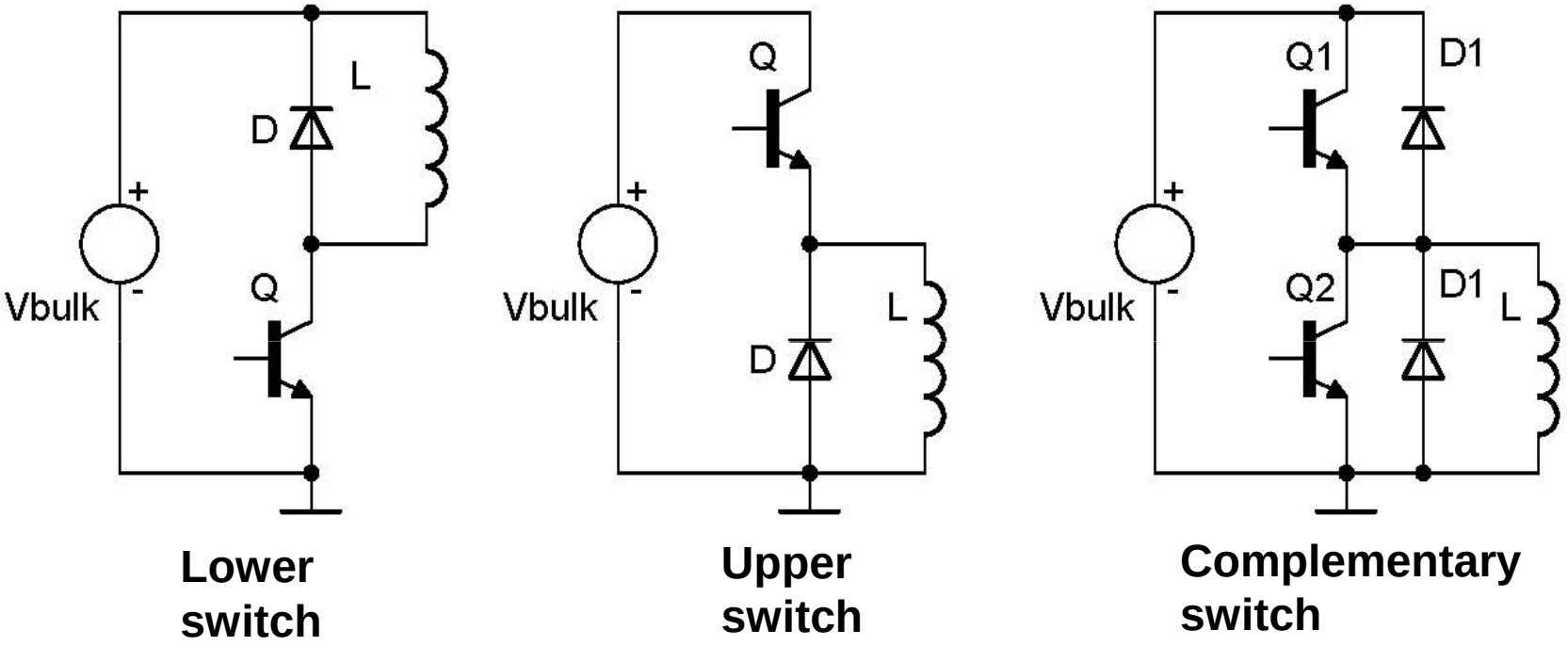
Switch in power electronics



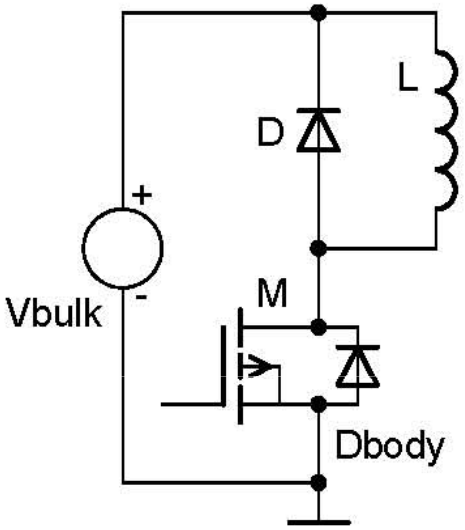
Lower switch

Upper switch

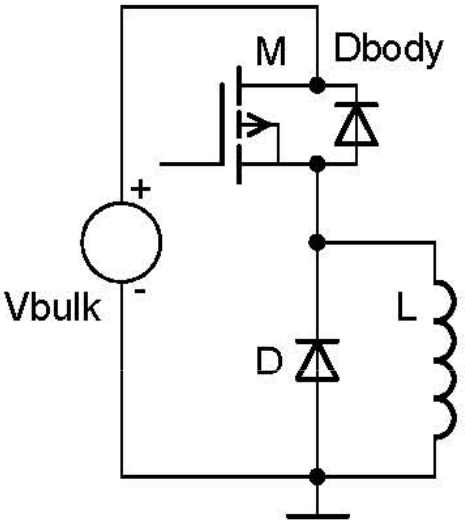
Complementary switch

- Power switch always composes from a switch and freewheeling path (diode or transistor)
- Switch is used to deliver energy to storage element (inductor)
- Freewheeling path is used to close demagnetization current

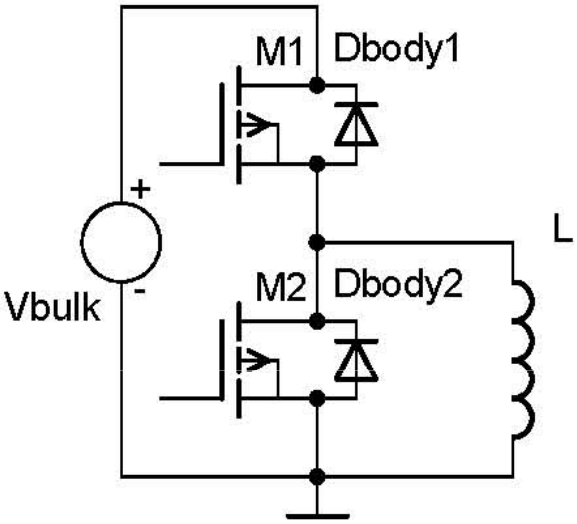
Switch in power electronics using MOSFET



Lower switch



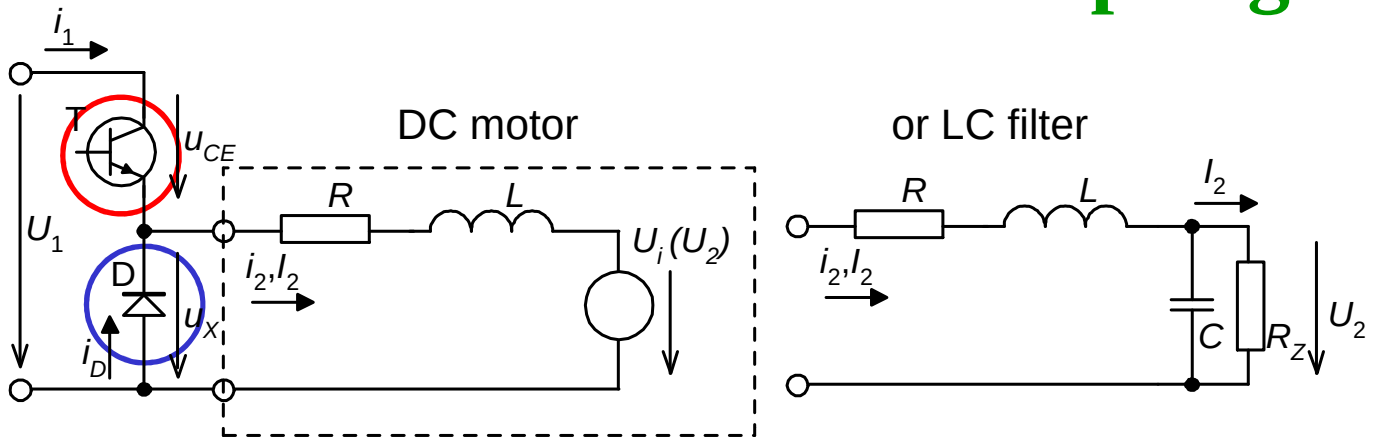
Upper switch



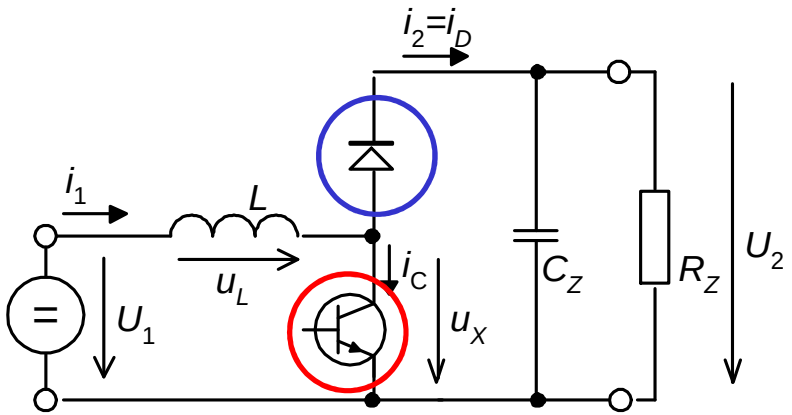
Complementary switch

- Body diode can be used as a freewheeling diode in complementary switch configuration when using MOSFET

Switch in basic non-isolated topologies



Buck converter topology

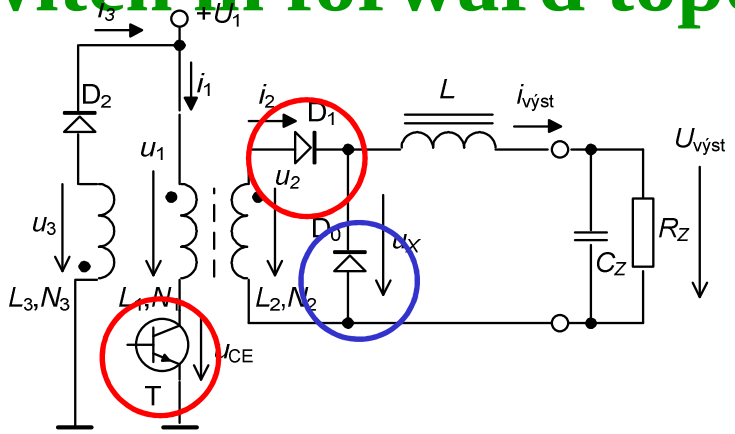


Boost converter topology

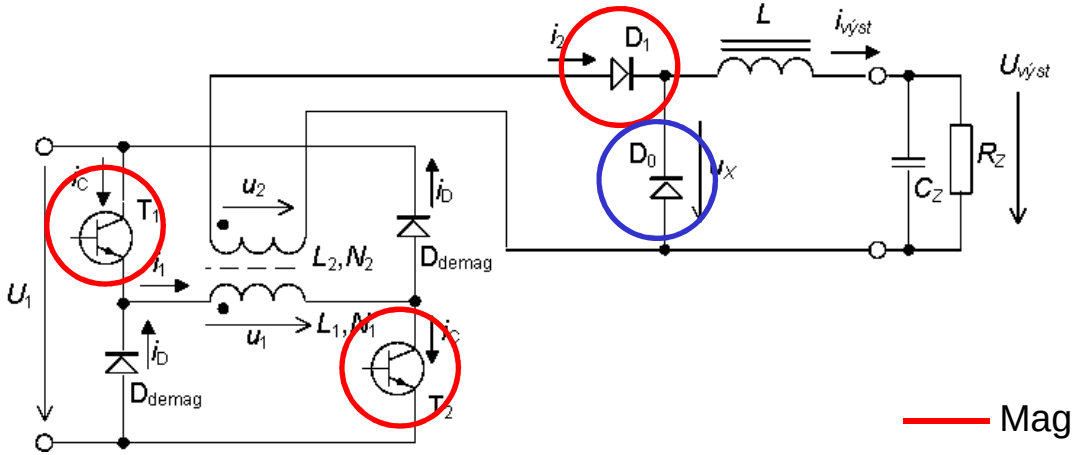
Magnetization phase

Demagnetization phase

Switch in forward topology



Forward topology

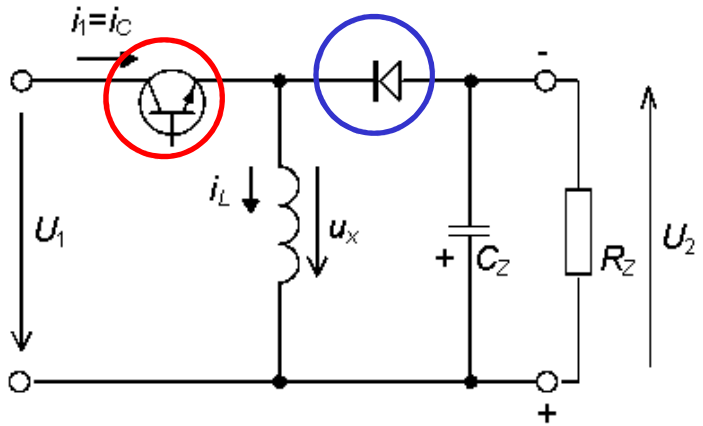


Two switch forward topology

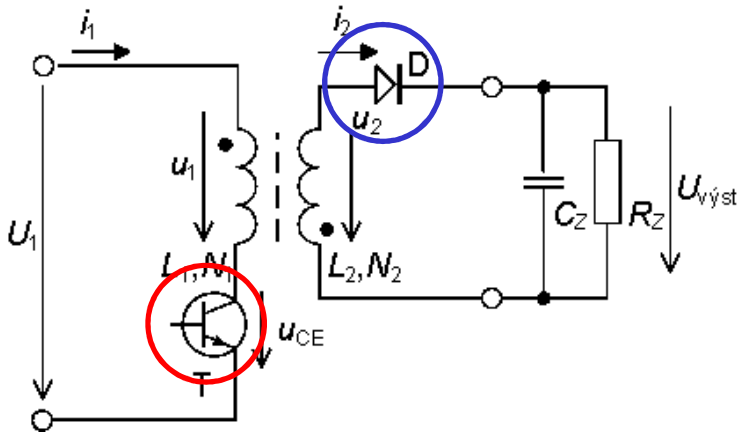
Magnetization phase

Demagnetization phase

Switch in buck-boost topology



Inverting B-B topology

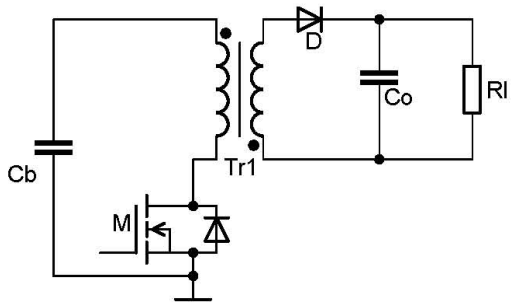


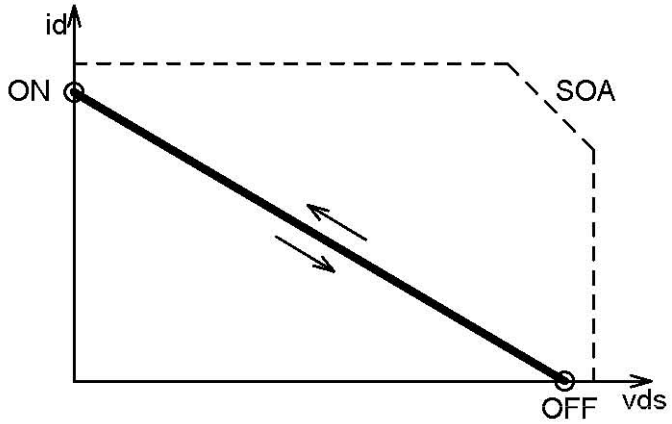
Flyback topology

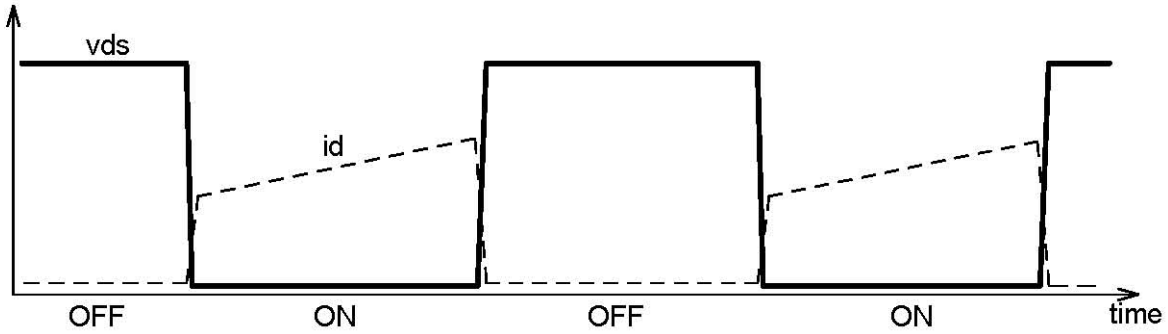
Magnetization phase

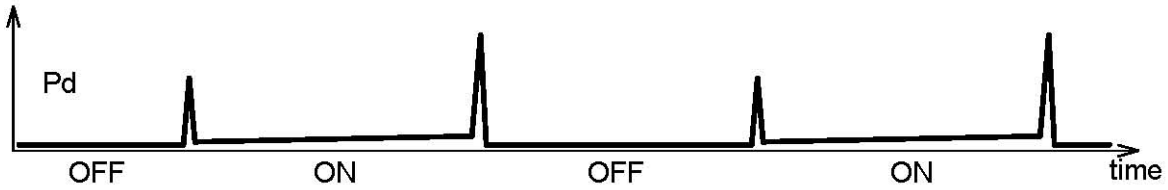
Demagnetization phase

Switch in ideal flyback converter





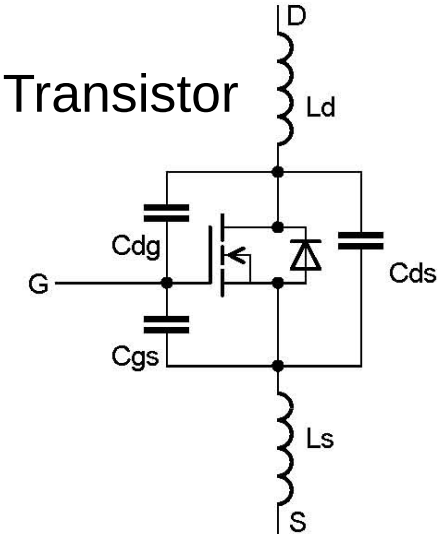




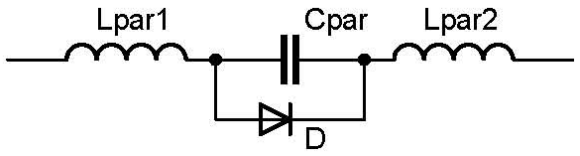
- Minimum current and voltage overlap i.e. negligible switching losses

Real components parasitic elements

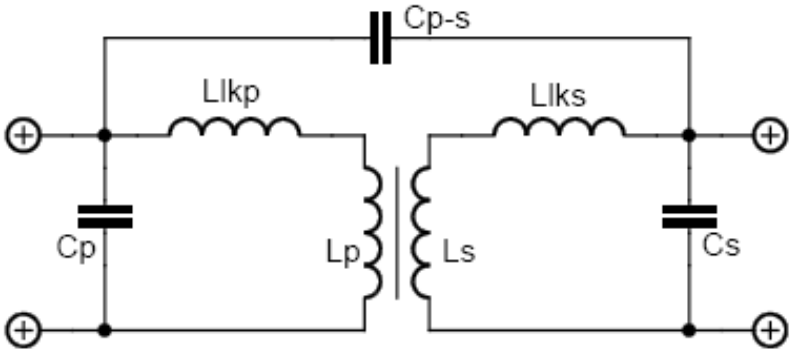
Transistor



Diode

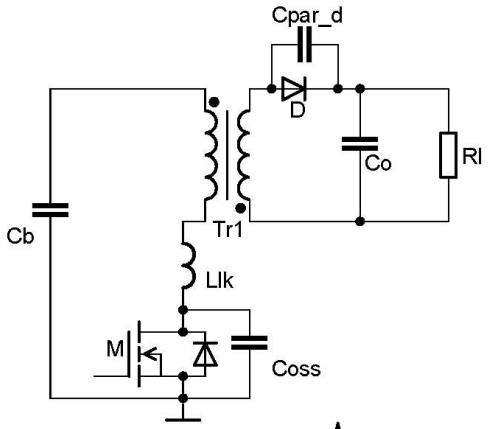


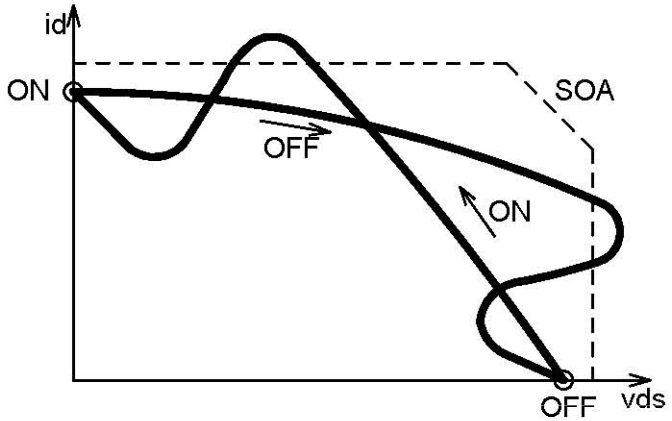
Transformer

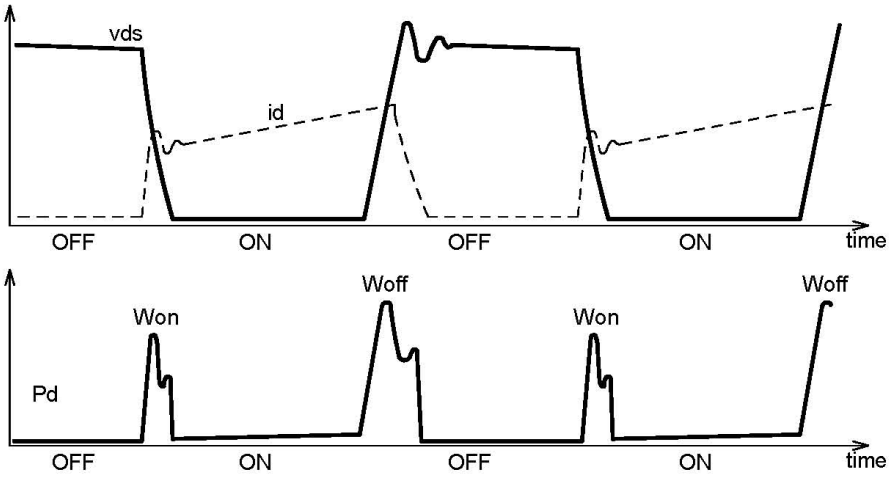


- Parasitic inductances and capacitances causes unwanted resonances
- PCB parasitic inductances and capacitances has to be included as well

Switch in real flyback converter

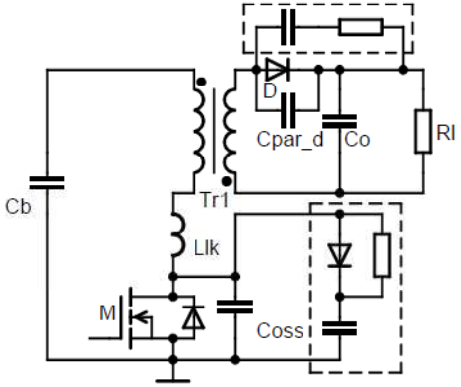


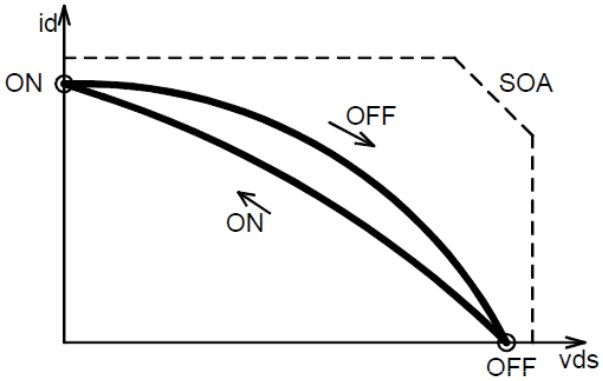


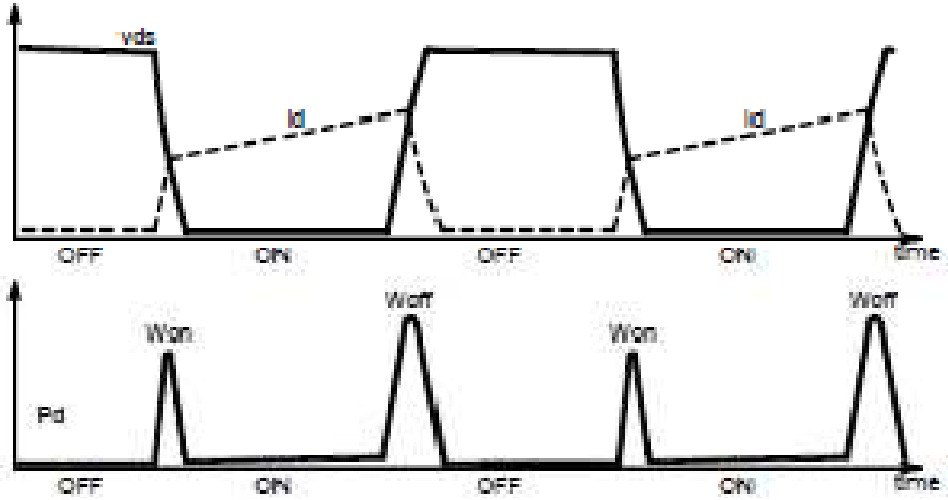


-Ringing and more significant voltage and current overlap occurs in real application just due to parasitic elements

Switch in real flyback converter with snubbers







- Ringing can be damped by snubbers that however uses dissipative elements – the power dissipation is still here

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Need for soft switched topologies

- High turn-on and turn-off losses occur during hard switching
- Coss energy (1/2*Coss*Vds^2) is burnt during each turn-on
- Llk energy (1/2*Llk*Id^2) is burnt during each turn-off
- Diode is commutated under high current => Qrr related losses
- Various parasitic resonances are present causing voltage spikes that may exceed maximum ratings of used components
- Passive and thus dissipative snubber networks are usually needed to damp system
- Application EMI signature is affected by parasitic oscillations and capacitive currents (Coss discharge)

Soft switching basic principles

- Using application parasitic and/or adding some additional energy storage devices (L or C) to implement two basic soft switching principles:

ZVS – Zero Voltage Switching: Switch is turned ON when there is low or ideally zero voltage across its terminals

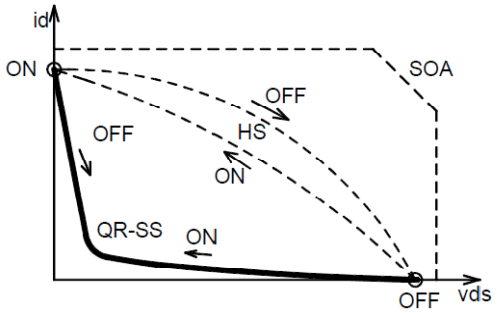
- Ideal switching technique for MOSFETs because it eliminates Coss related losses

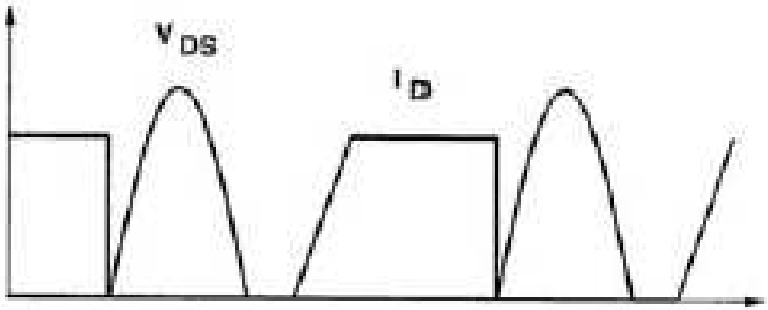
ZCS – Zero Current Switching: Switch is turned OFF when there is low or ideally zero current flowing though its terminals

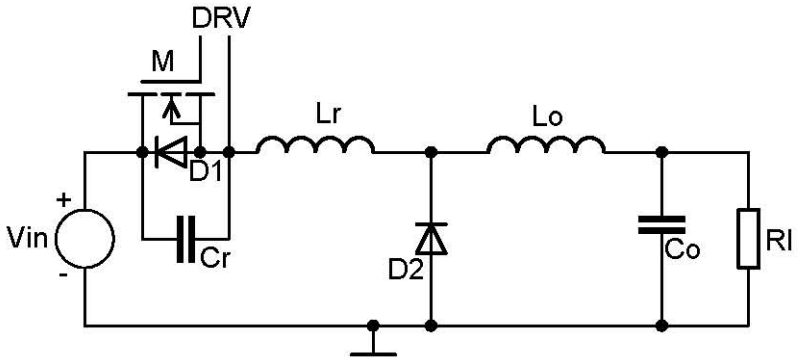
- Ideal switching technique for diodes, BJTs or IGBTs because eliminates trr and storage time related losses

Note: ZVS/ZCS techniques eliminates switching losses however, usually increases conduction losses due to higher RMS current in the switch

Zero voltage switching QR converters

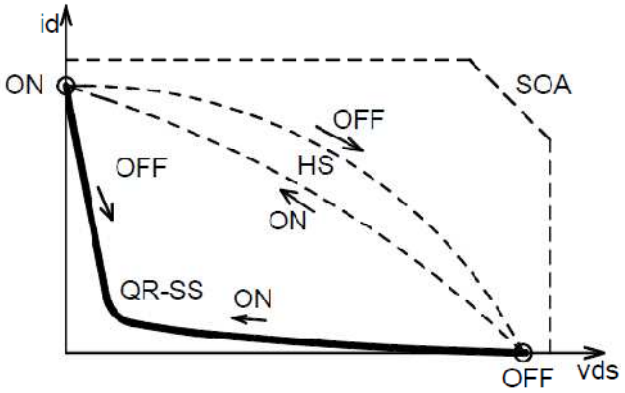


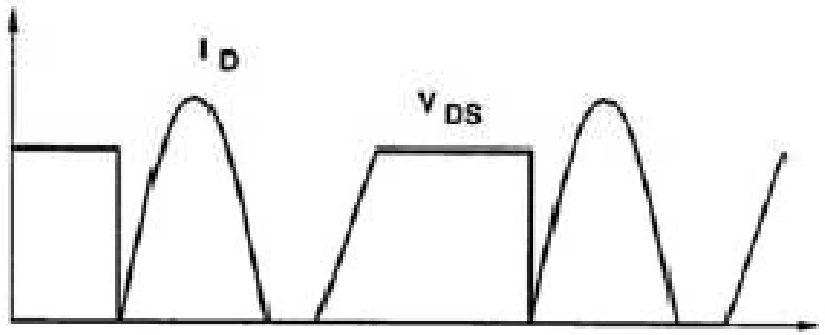


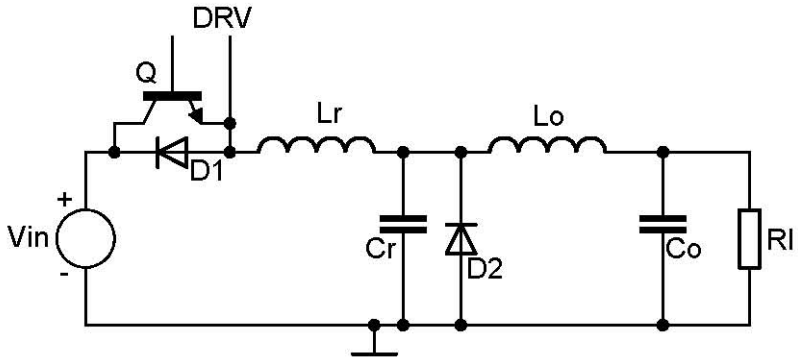


- Example: Half wave mode ZVS QR buck

Zero current switching QR converters



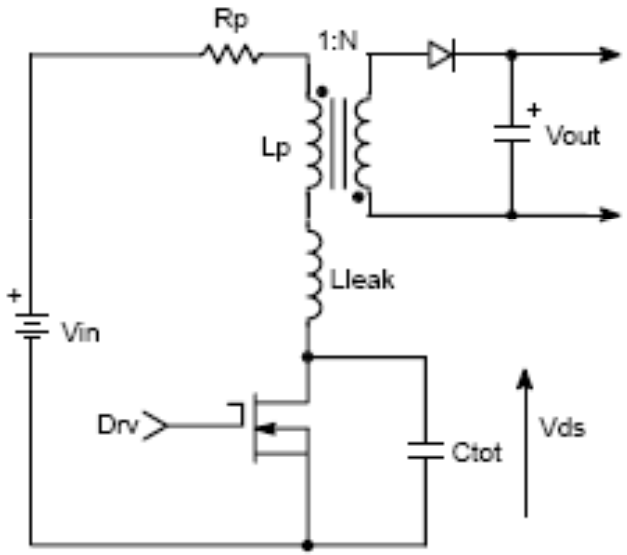


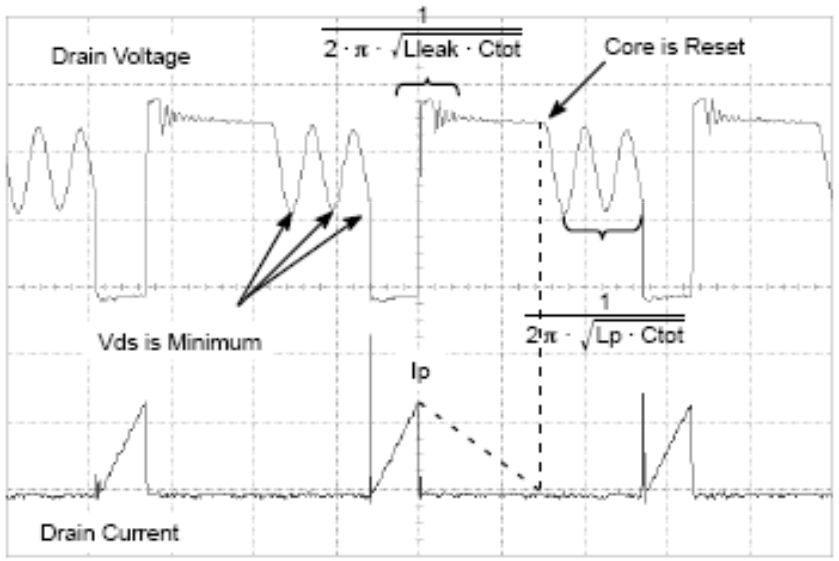


- Example: Full wave mode ZCS QR buck

Quasi resonant AC/DC topologies

- Uses portion of the resonant cycle to prepare nearly ZVS or ZCS condition
- Typical example is flyback quasi resonant topology





- Drawback of DCM operation => high primary and secondary rms current
- Vin and Pout are dependent parameters

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Resonant and Multi-resonant topologies

-The primary current has sinusoidal wave shape for nominal load and line conditions
- ZVS and ZCS conditions are prepared for power semiconductors
-Some resonant converters are called multi resonant because the resonant frequency changes during one switching cycle
- Two main resonant converter topologies can be identified:

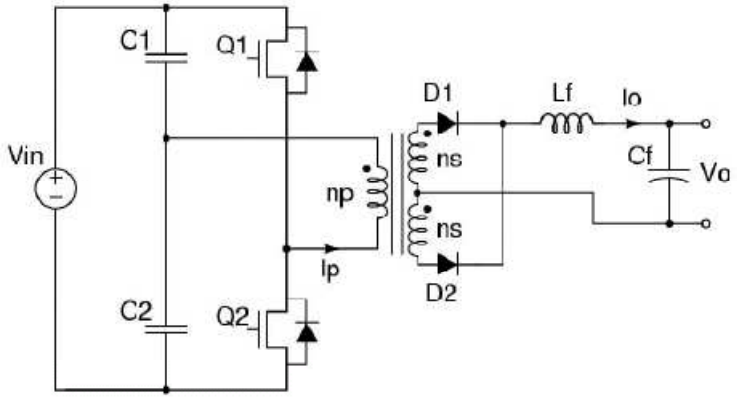
Series resonant converter

Parallel resonant converter

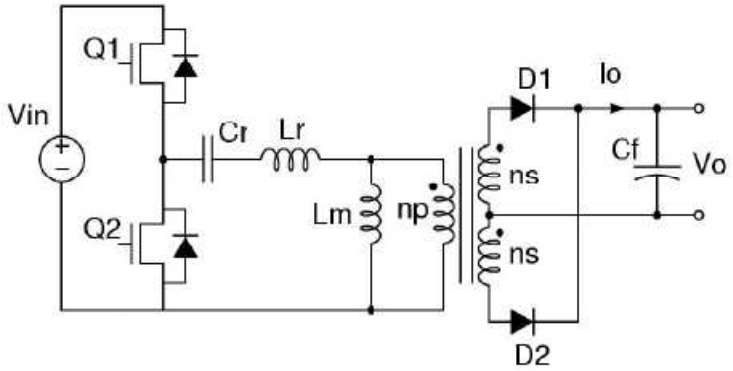
Came out from well known half bridge topology by its power stage modification . Disadvantage of these converters is relatively low regulation range => the line and load changes are limited.

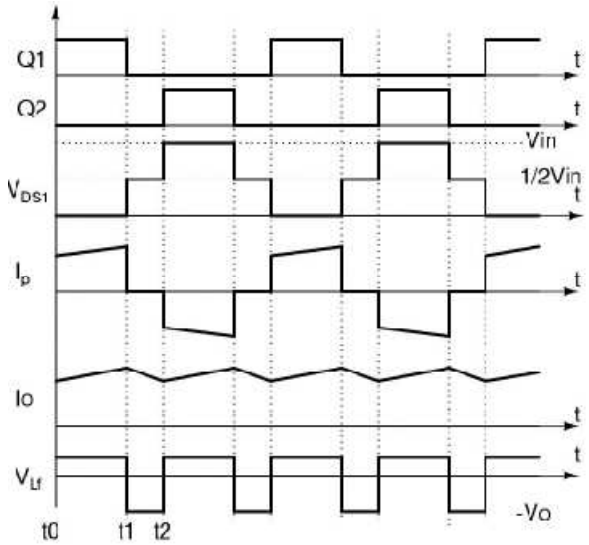
Classical HB to resonant topology transition

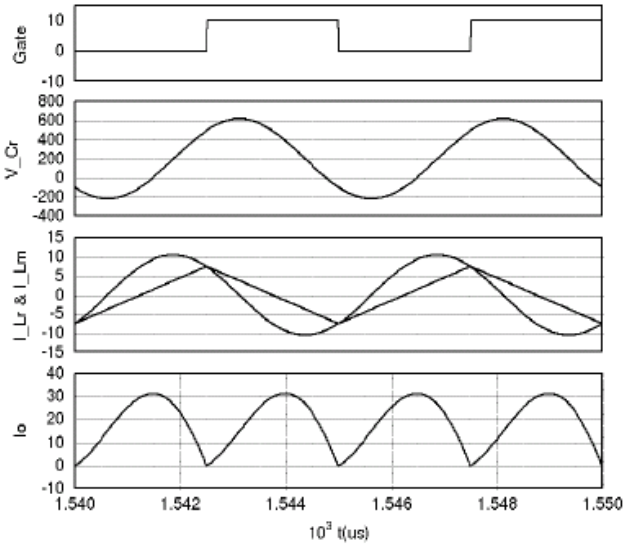
Classical HB topology



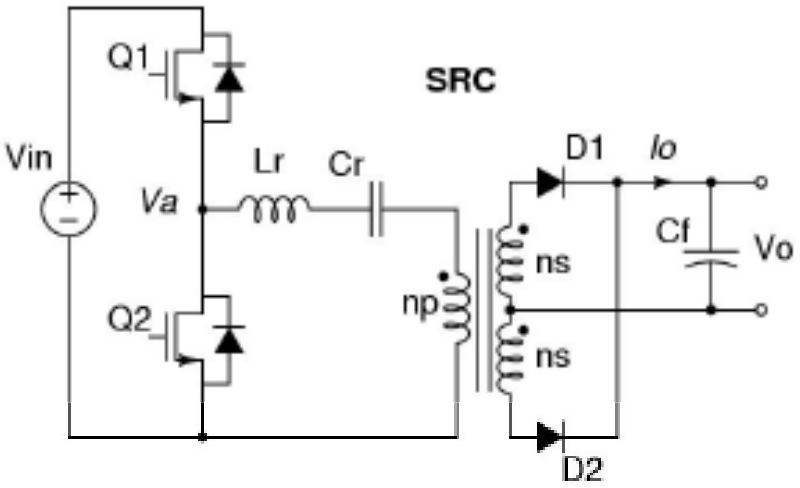
LLC resonant topology

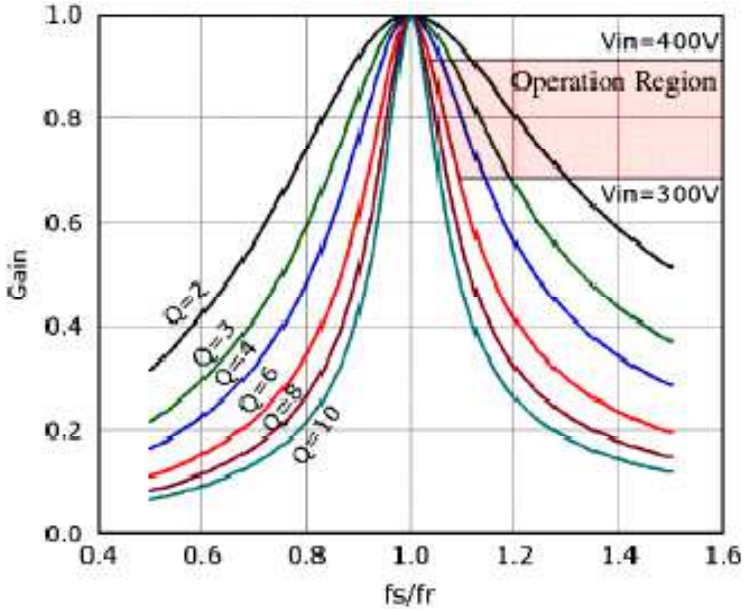






Series resonant converter

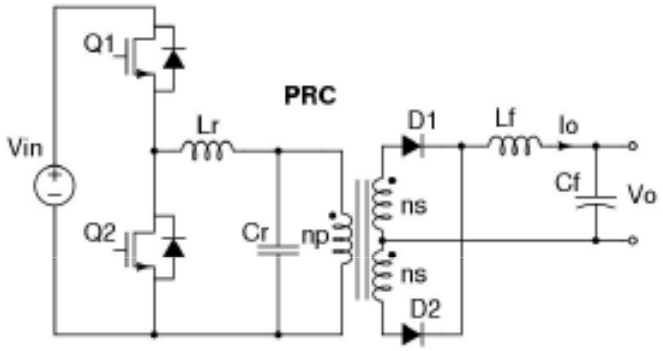


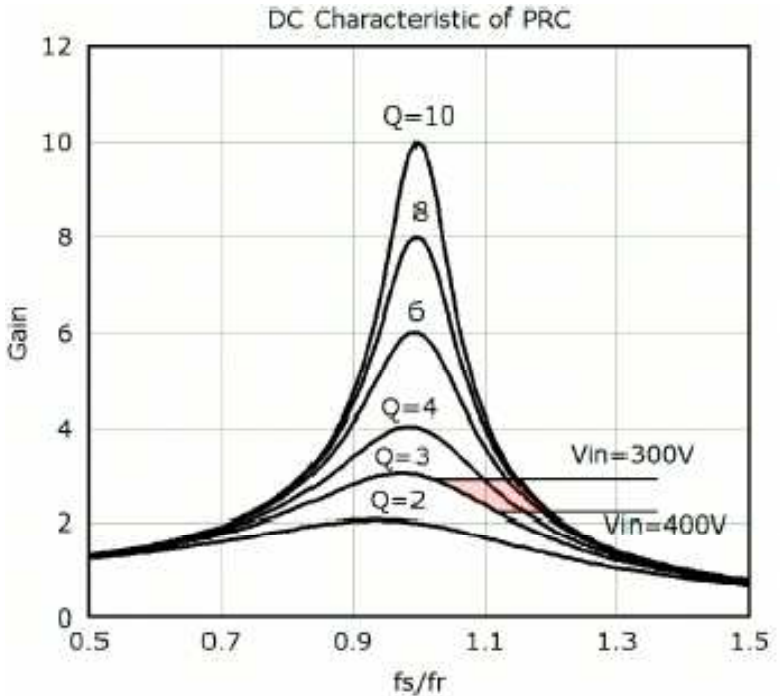


- Lr, Cr and load resistance forms series resonant circuit.
- Resonant tank impedance is frequency dependent
- Regulation can be done by the operating frequency modification
- Maximum gain of this converter is equal to transformer turns ratio for:

$$f_{sw} = f_s = \frac{1}{2 \cdot \pi \cdot \sqrt{L_r \cdot C_r}}$$

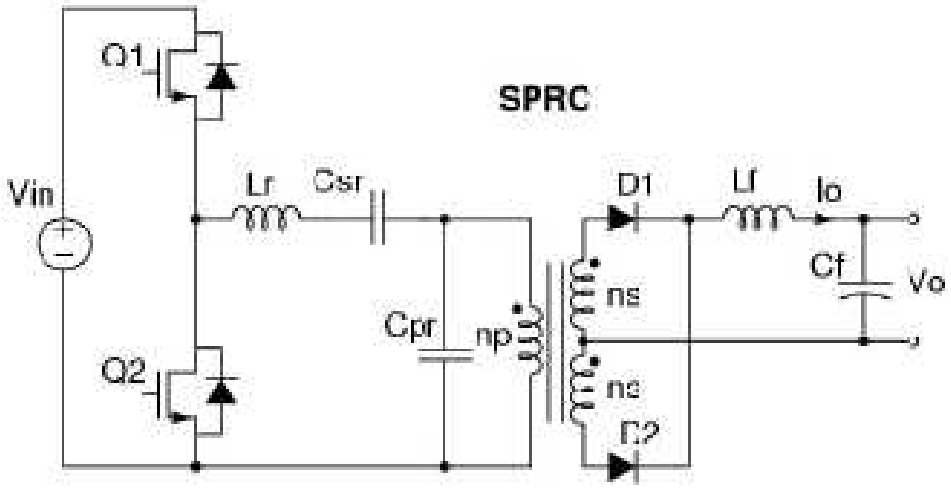
Parallel resonant converter

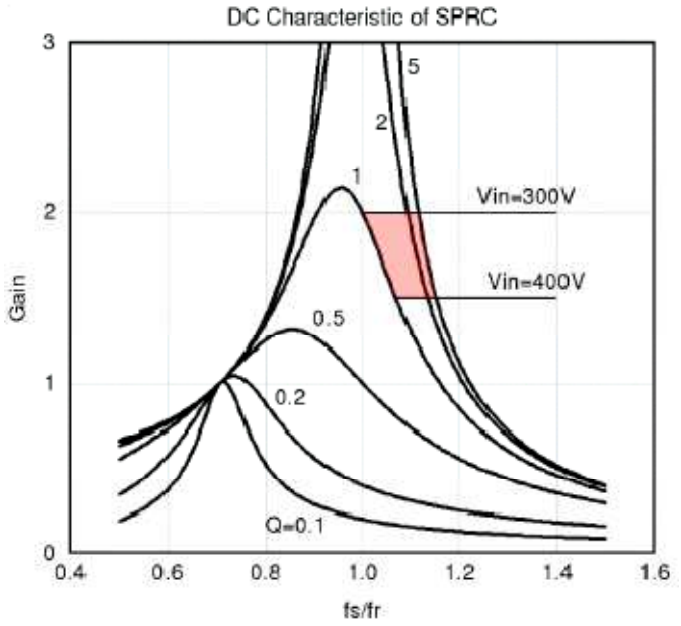




- Lr and Cr forms the series resonant circuit again
- Load resistance is now connected in parallel with resonant capacitor thus called parallel RC.

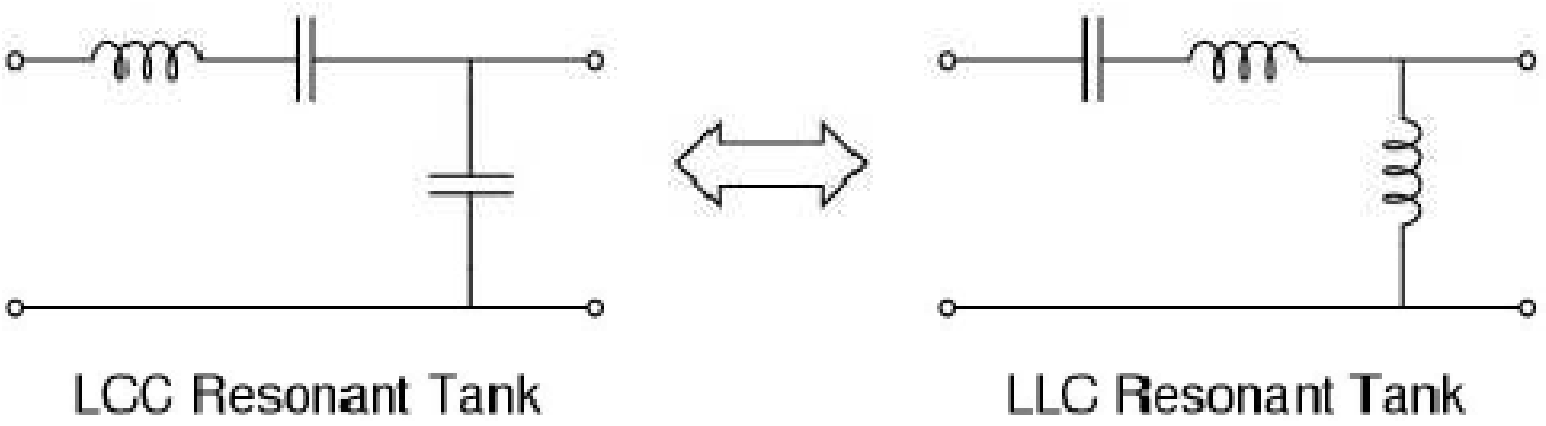
Series parallel resonant converter (LCC)





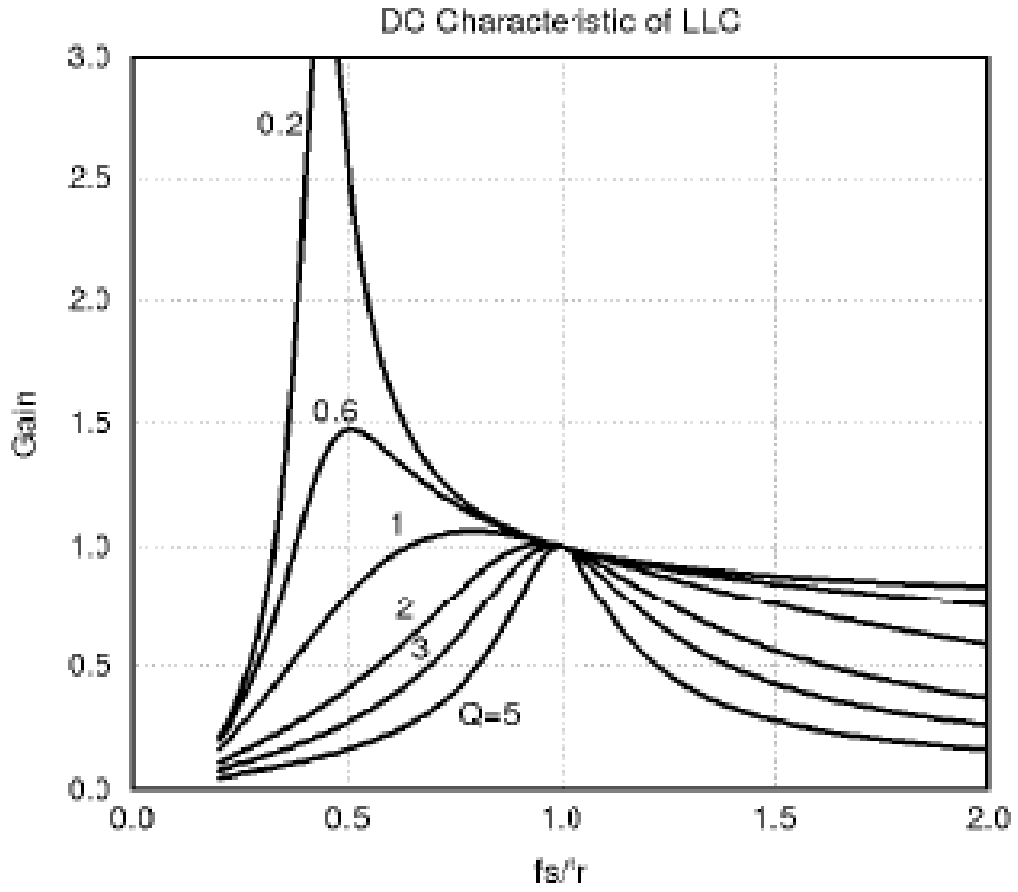
- Contains three resonant components Lr, Csr and Cpr
- Combines advantages of SRC and PRC
- The light or even no load regulation is not problem.

Transition to the LLC resonant converter



-The LCC converter has still many disadvantages => other topology is desirable for high density and efficiency SMPS
- LCC resonant tank can be changed to the LLC resonant tank

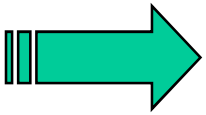
Gain characteristics of the LLC converter



- Operation at fs is possible for nominal load and line conditions

Benefits of an LLC series resonant converter

- Type of serial resonant converter that allows operation in relatively wide input voltage and output load range when compared to the other resonant topologies
- Limited number of components: resonant tank elements can be integrated to a single transformer – only one magnetic component needed
- Zero Voltage Switching (ZVS) condition for the primary switches under all normal load conditions
- Zero Current Switching (ZCS) for secondary diodes, no reverse recovery losses



Cost effective, highly efficient and EMI friendly solution for high and medium output voltage converters

Classical HB and LLC topology differences

Topology	Advantages	Disadvantages
Classical HB	•Low ripple current on the secondary •Wide regulation range •Constant frequency operation	•Switching under high currents (primary and secondary) •ZVS conditions for primary switches can be assured only for limited loads
LLC resonant	•ZVS condition is assured for whole load range •Primary current is harmonic for heavy loads =>EMI •ZCS condition for secondary rectifier for heavy loads	•Higher ripple current on the secondary => lower ESR capacitors needed •Operating frequency isn't constant •Lower regulation range

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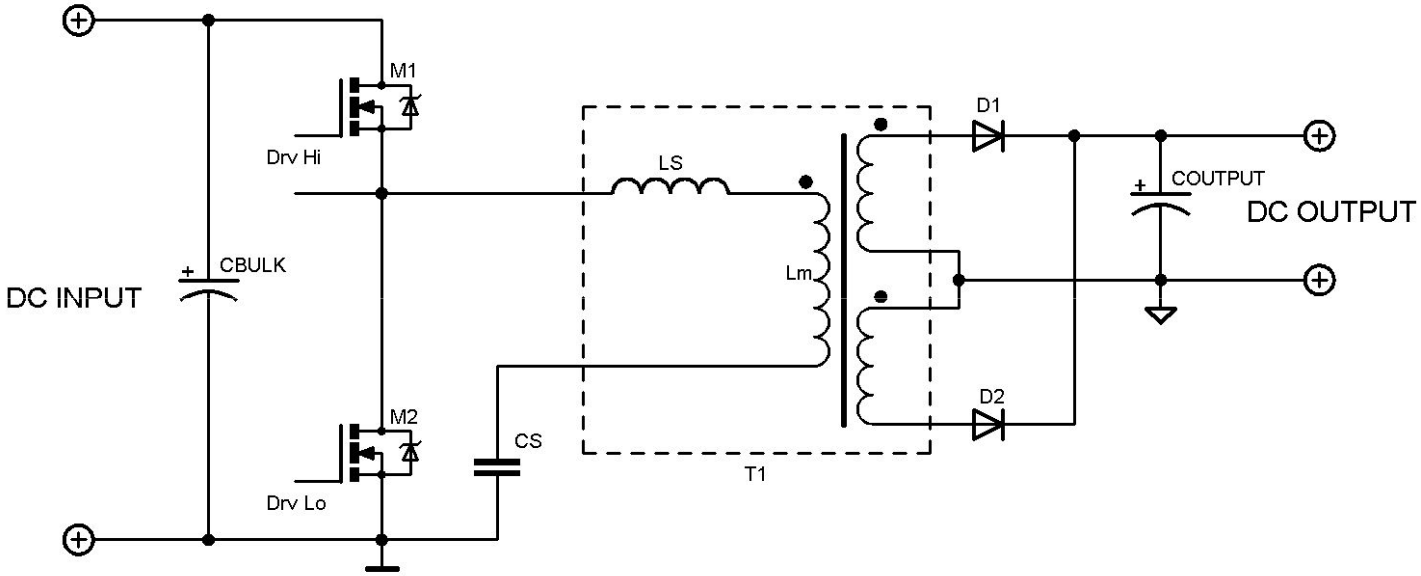
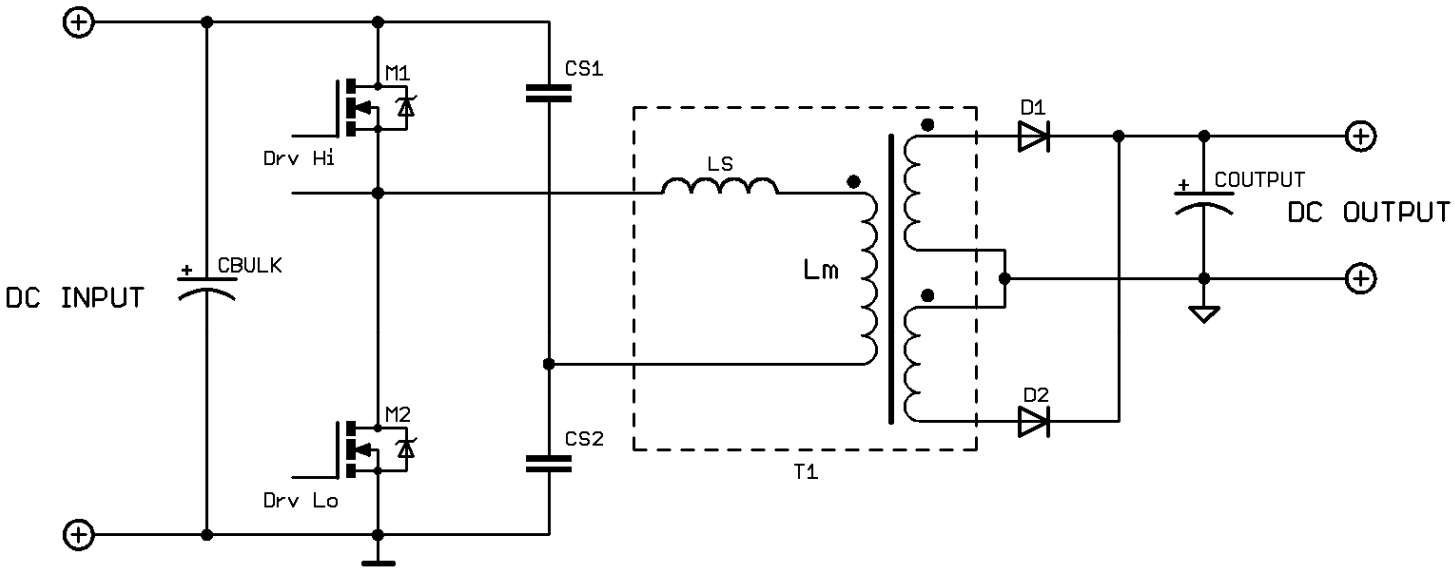
Configurations of an HB LLC – single res. cap



- Higher input current ripple and RMS value
- Higher RMS current through the resonant capacitor
- Lower cost
- Small size / easy layout

Configurations of an HB LLC – split res. cap



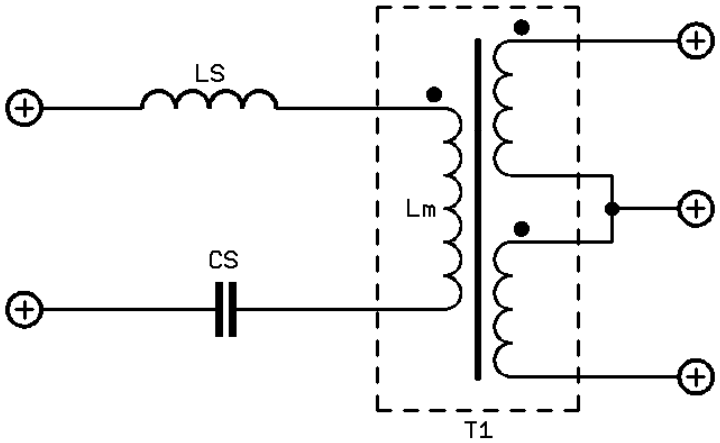
Compared to the single capacitor solution this connection offers:
- Lower input current ripple and RMS value by 30 %
- Resonant capacitors handle half RMS current
- Capacitors with half capacitance are used

Resonant tank configurations – discrete solution

Resonant inductance is located outside of the transformer

Advantages:

- Greater design flexibility (designer can setup any L_s and L_m value)
- Lower radiated EMI emission



Disadvantages of this solution are:

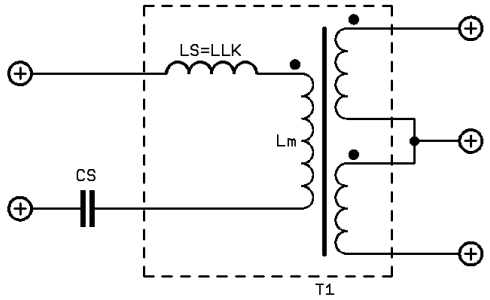
- Complicated insulation between primary and secondary windings
- Worse cooling conditions for the windings
- More components to be assembled

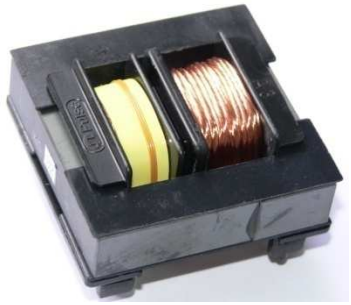
Resonant tank configurations – integrated solution

Leakage inductance of the transformer is used as a resonant inductance.

Advantages:

- Low cost, only one magnetic component is needed
- Usually smaller size of the SMPS
-Insulation between primary and secondary side is easily achieved
- Better cooling conditions for transformer windings





Disadvantages:

- Less flexibility (achievable Ls inductance range is limited)
- Higher radiated EMI emission
- LLC with integrated resonant tank operates in a slightly different way than the solution with discrete L_s, different modeling has to be used
- Strong proximity effect in the primary and secondary windings

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Operating states of the LLC converter

Discrete resonant tank solution

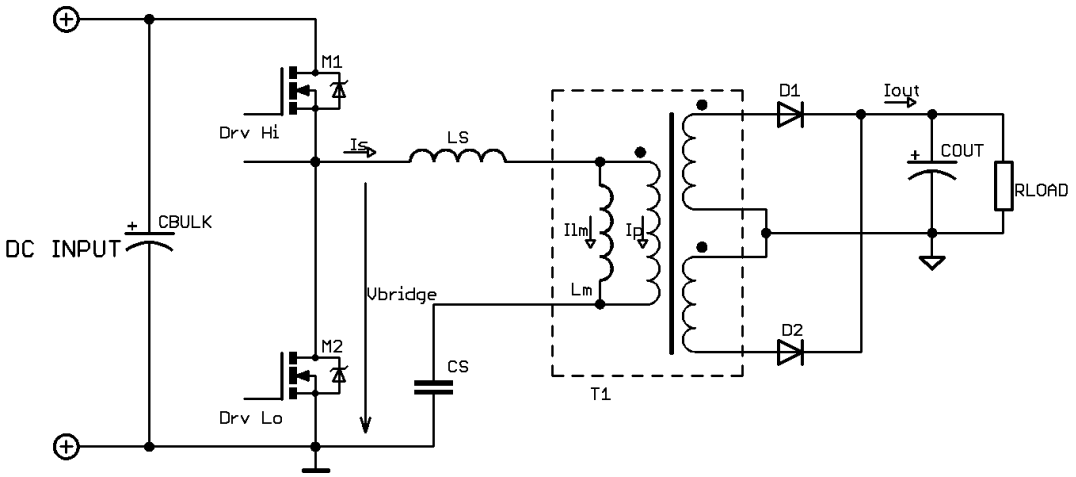
Two resonant frequencies can be defined:

$$F_s = \frac{1}{2 \cdot \pi \cdot \sqrt{C_s \cdot L_s}}$$

$$F_{min} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_s \cdot (L_s + L_m)}}$$

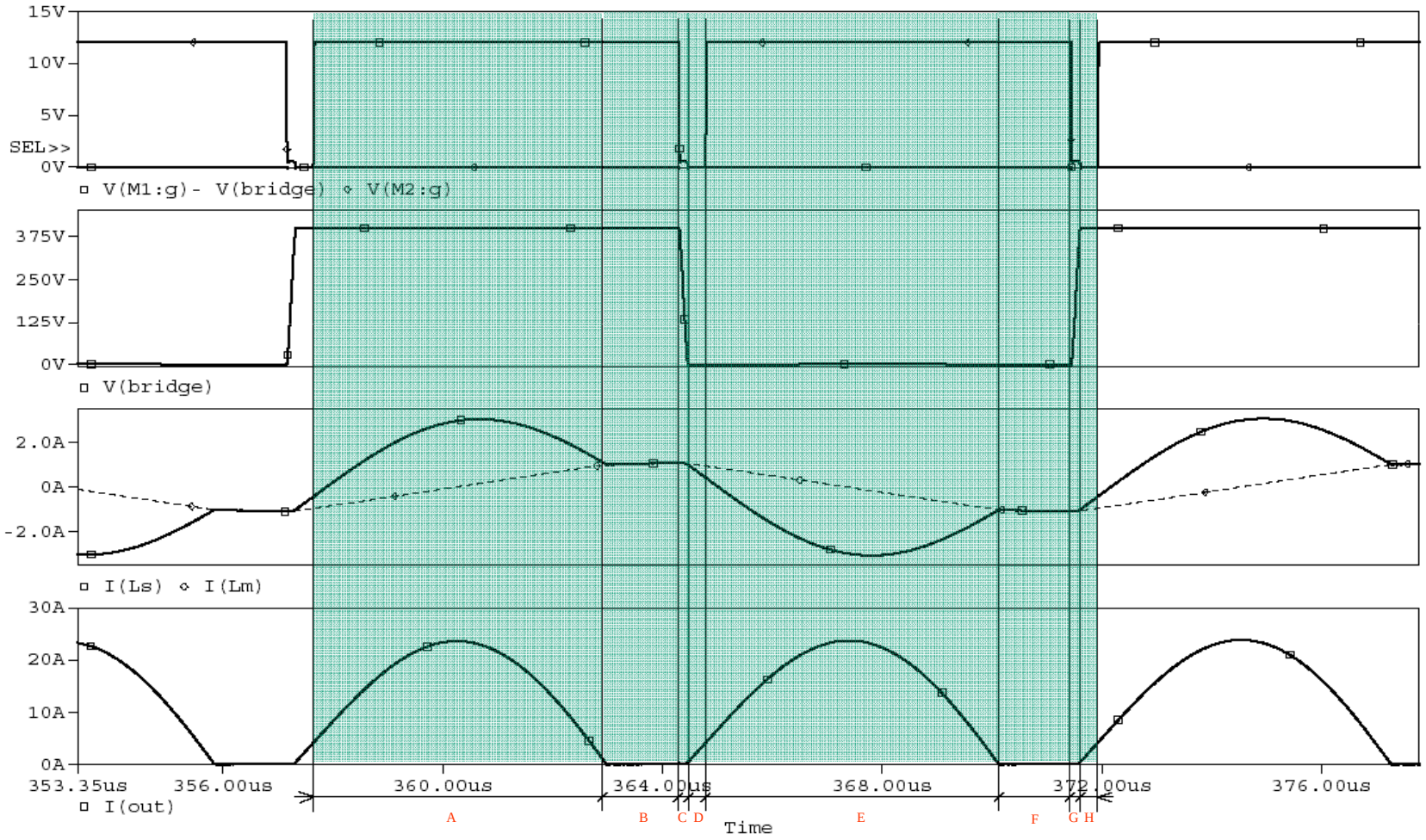
LLC converter can operate:

a) between F_{min} and F_s
b) direct in F_s
c) above F_s
d) between F_{min} and F_s - overload
e) below F_{min}



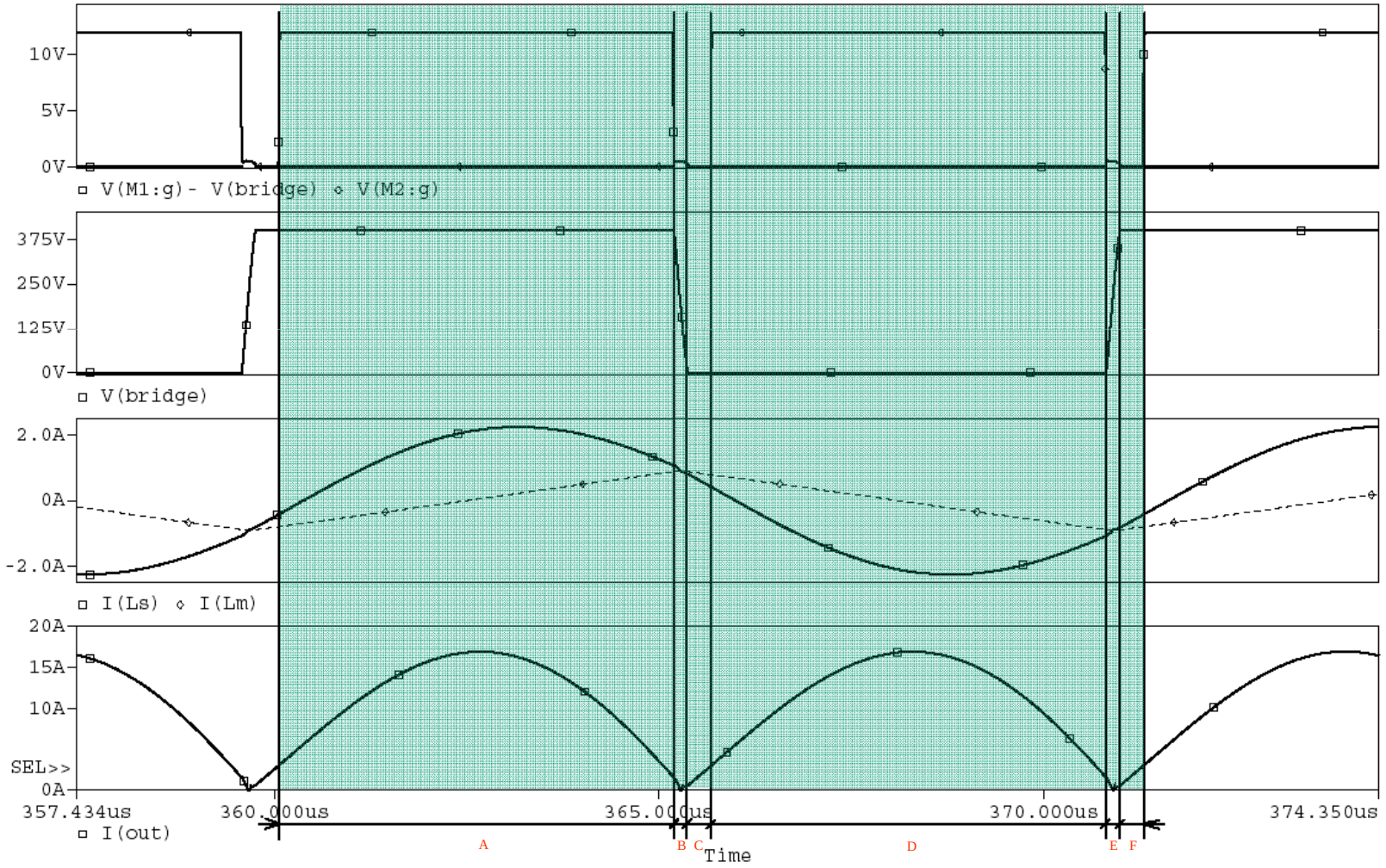
Operating states of the LLC converter

a) Operating waveforms for $f_{min} < f_{op} < f_s$



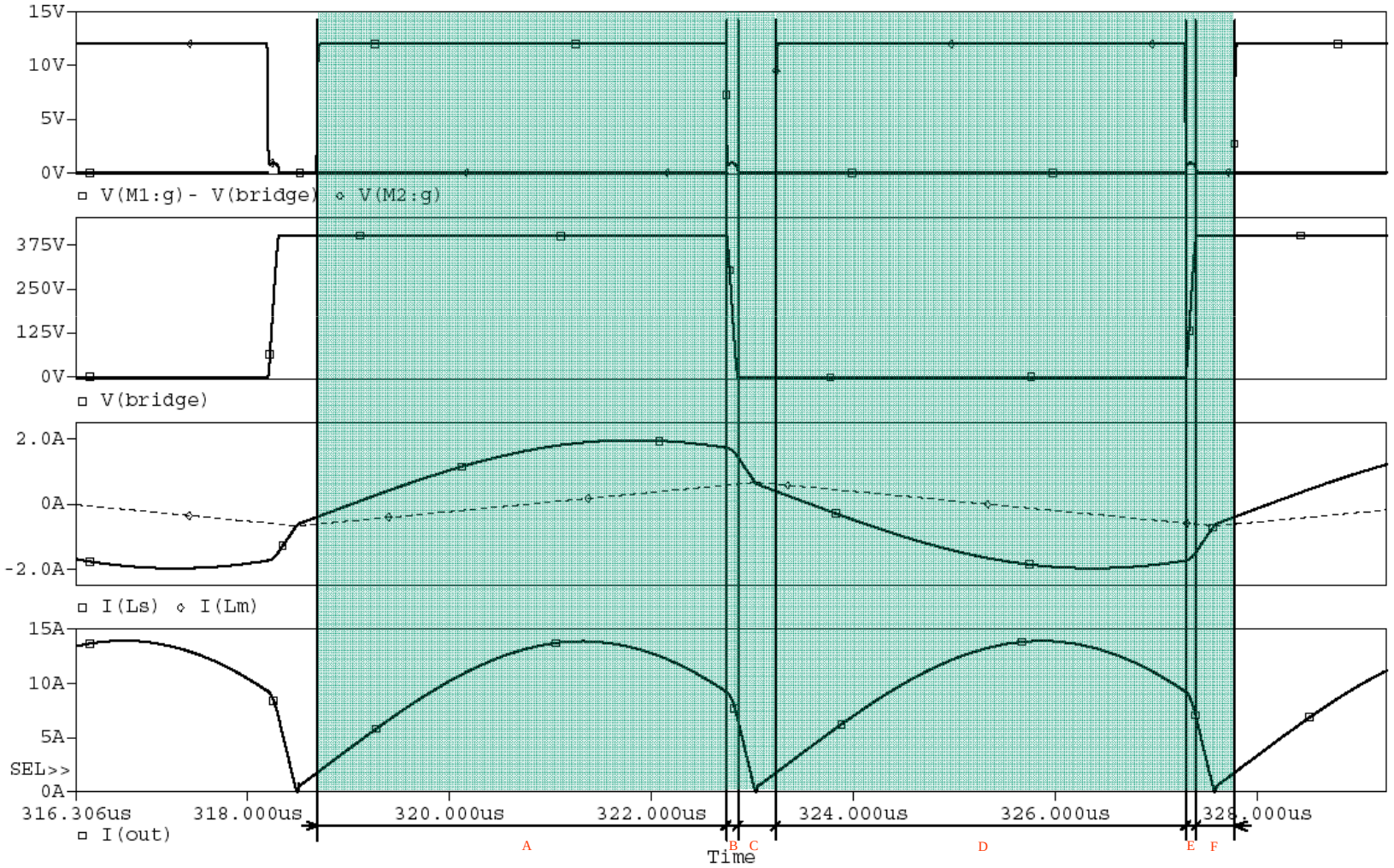
Operating states of the LLC converter

b) Operating waveforms for $f_{op} = f_s$



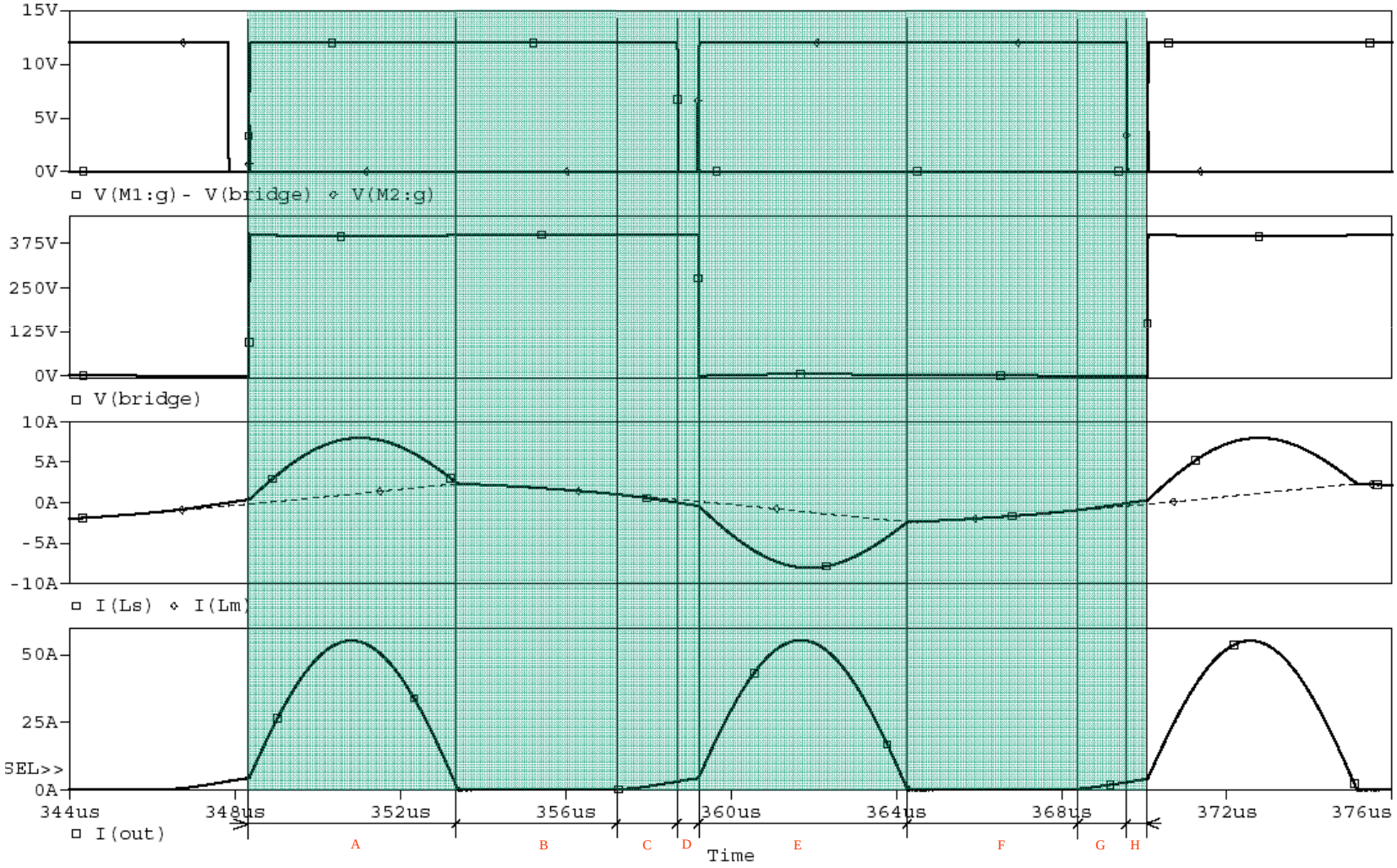
Operating states of the LLC converter

c) Operating waveforms for $F_{op} > F_s$ Discrete resonant tank solution



Operating states of the LLC converter

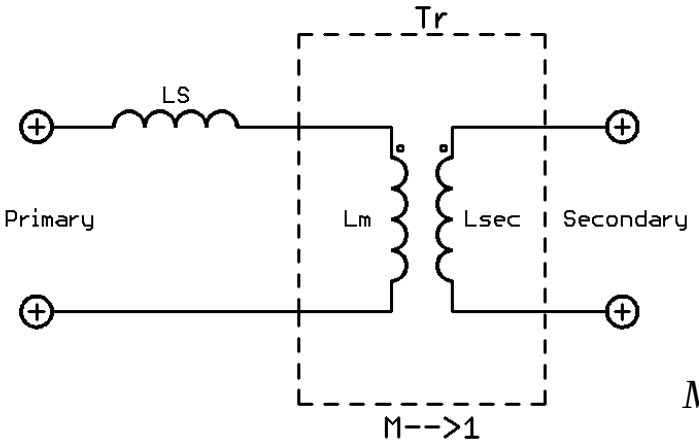
d) Operating waveforms for fmin < fop < fs – strong overload



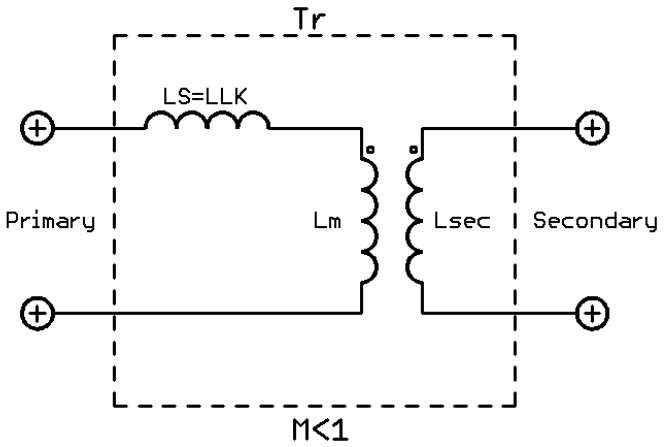
Operating states of the LLC converter

Integrated resonant tank solution

- Integrated resonant tank behaves differently than the discrete resonant tank
- leakage inductance is given by the transformer coupling
- L_{lk} participates only if there is a energy transfer between primary and secondary
- Once the secondary diodes are closed under ZCS, L_{lk} has no energy



$$M = \sqrt{1 - \frac{L_{lk}}{L_m}}$$



Secondary diodes are always turned OFF under ZCS condition in HB LLC.
The resonant inductance L_s and magnetizing inductance L_m do not participate in the resonance together as for discrete resonant tank solution when secondary diodes are closed!

Operating states of the LLC converter

Integrated resonant tank solution

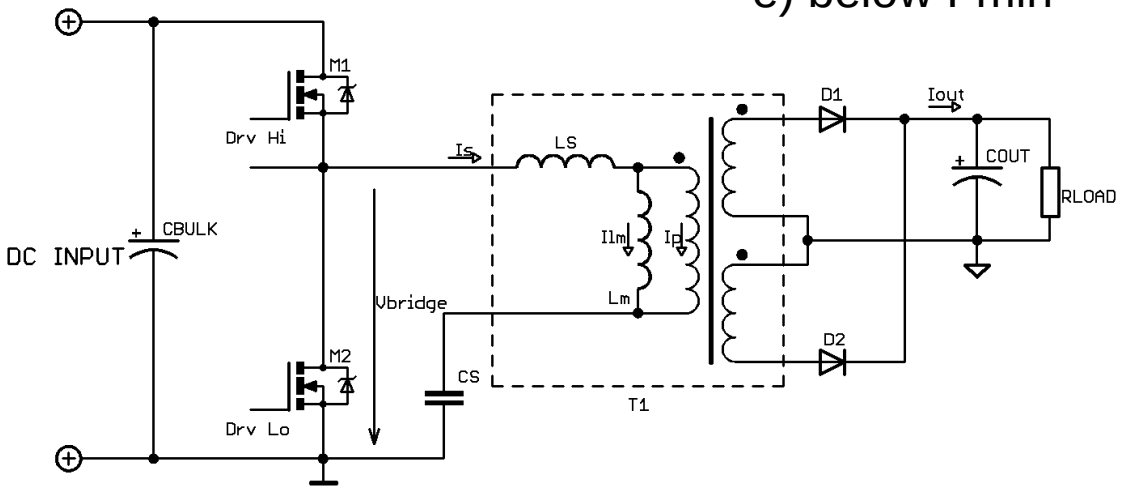
Two resonant frequencies can be defined:

$$F_s = \frac{1}{2 \cdot \pi \cdot \sqrt{C_s \cdot L_s}}$$

$$F_{min} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_s \cdot L_m}}$$

LLC converter can again operate:

a) between Fmin and Fs
b) direct in Fs
c) above Fs
d) between Fmin and Fs – overload
e) below Fmin



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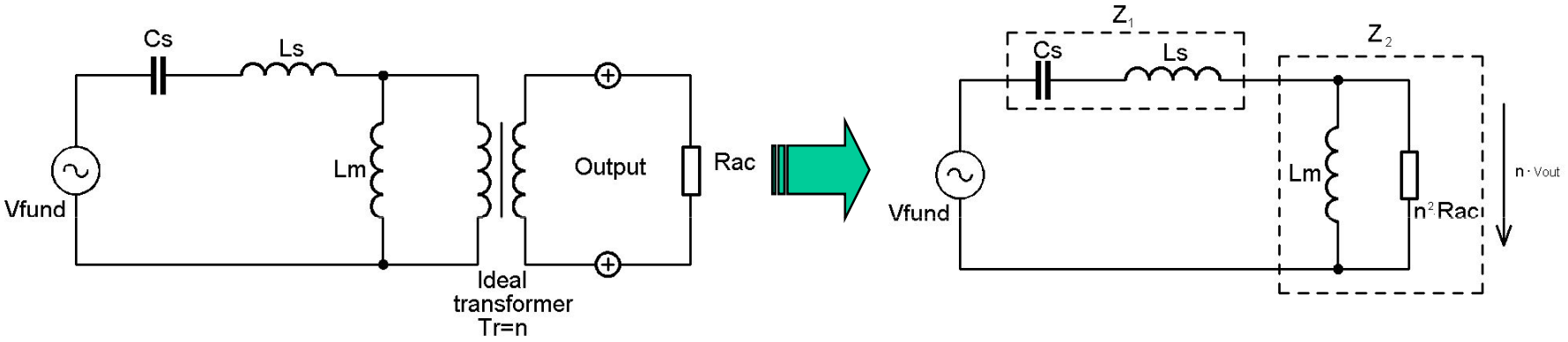
LLC converter modeling – equivalent circuit

LLC converter can be described using firs fundamental approximation. Only approximation – accuracy is limited!! Best accuracy is reached around F_s.



Transfer function of equivalent circuit:

$$G_{ac} = \frac{n \cdot V_{out}}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}$$

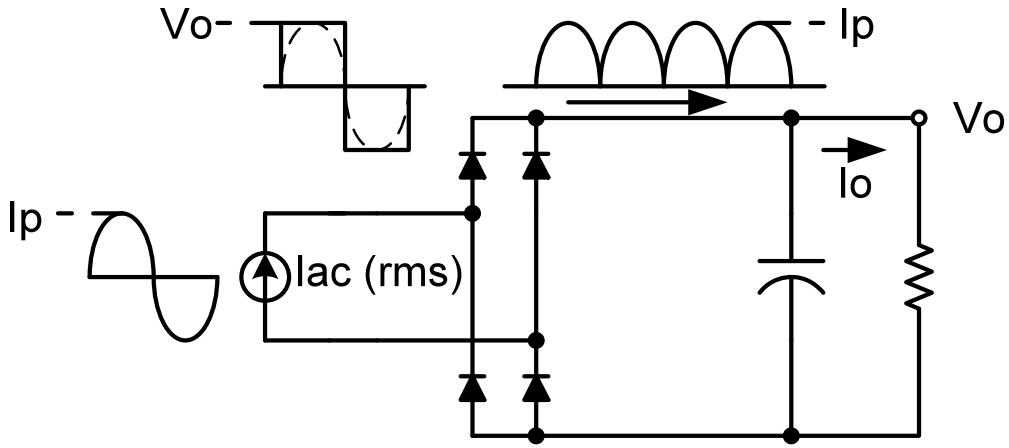
Z_1, Z_2 are frequency dependent => LLC converter behaves like frequency dependent divider. The higher load, the L_m gets to be more clamped by R_{ac}. Resonant frequency of LLC resonant tank thus changes between F_s and F_{min}.

LLC converter modeling – equivalent circuit

Real load resistance has to be modified when using fundamental approximation to convert non linear circuitry to linear model.

In a full-wave bridge circuit the RMS current is:

$$I_{ac\_RMS} = \frac{\pi}{2\sqrt{2}} I_O$$



Considering the fundamental component of the square wave, the RMS voltage is:

$$V_{ac\_RMS} = \frac{2\sqrt{2}}{\pi} V_O$$

The AC resistance R_{ac} ca be expressed as:

$$R_{ac} = \frac{V_{ac\_RMS}}{I_{ac\_RMS}} = \frac{8}{\pi^2}\frac{E_O}{I_O} = \frac{8}{\pi^2} R_L$$

Resonant tank equations

Quality factor:

$$Q = \frac{n^2 \cdot R_L}{Z_0}$$

Load dependent !

Characteristic impedance:

$$Z_0 = \sqrt{\frac{L_s}{C_s}}$$

Lm/Ls ratio:

$$m = \frac{L_m}{L_s}$$

Gain of the converter:

$$G = \frac{2 \cdot (V_{out} + V_f)}{V_{in}}$$

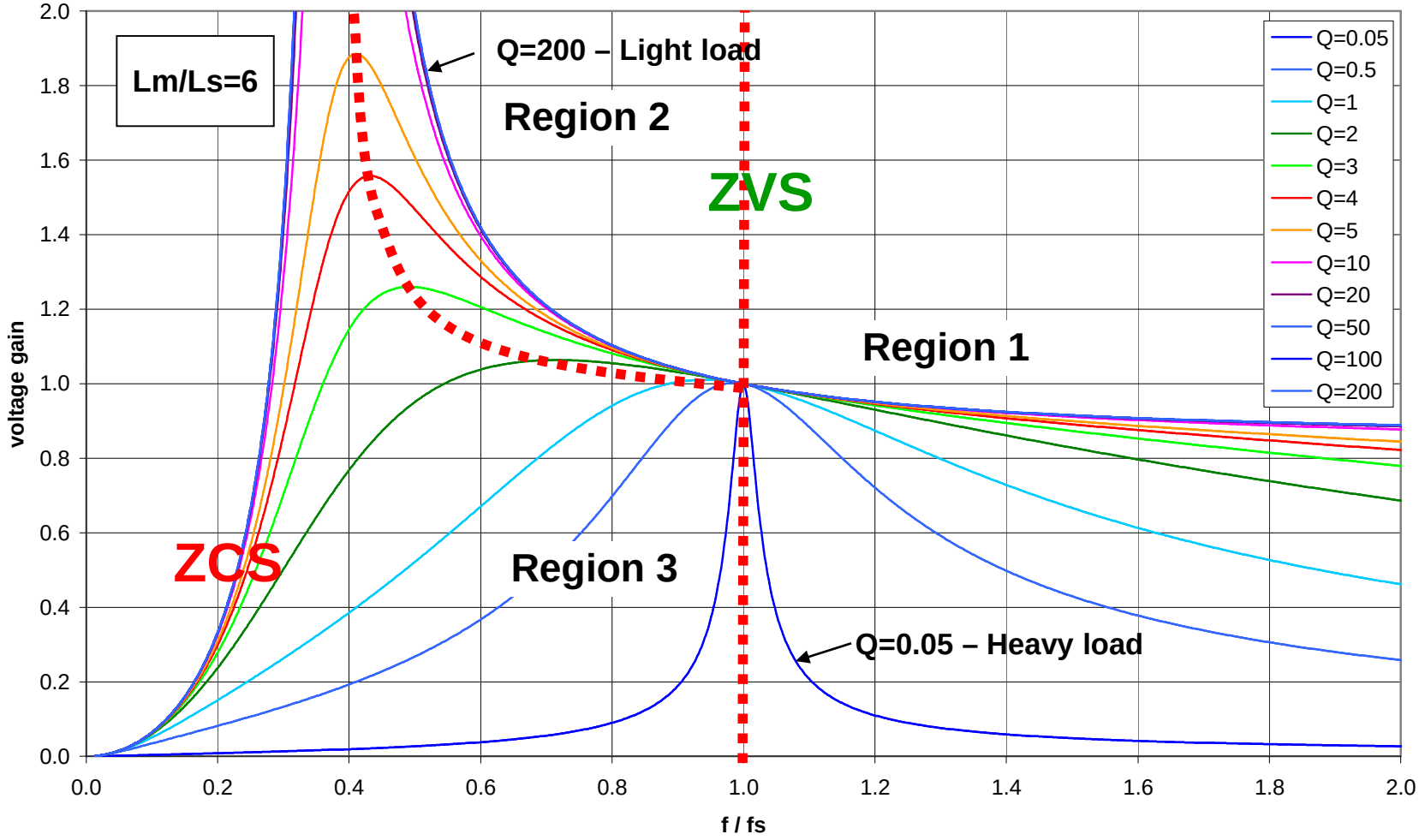
Series resonant frequency:

$$F_s = \frac{1}{2 \cdot \pi \cdot \sqrt{C_s \cdot L_s}}$$

Minimum resonant frequency:

$$F_{\min} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_s \cdot (L_s + L_m)}}$$

Normalized gain characteristic



Region3: ZCS region

Region 1 and 2: ZVS operating regions

Gain characteristic discussion

- The desired operating region is on the right side of the gain characteristic (negative slope means – ZVS mode for primary MOSFETs).

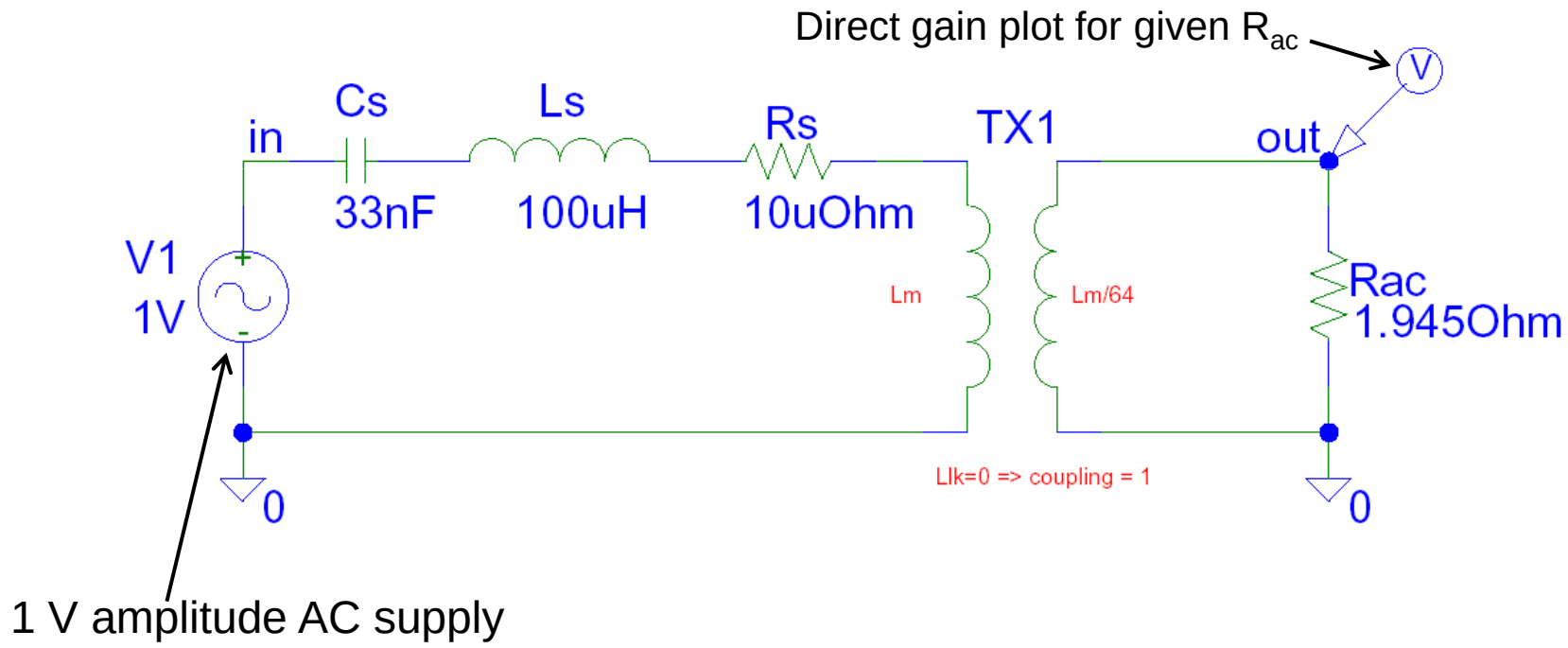
-Gain of the LLC converter, which operates in the f_s is 1 (for discrete resonant tank solution) - i.e. is given by the transformer turns ratio. This operating point is the most attractive from the efficiency and EMI point of view – sinusoidal primary current, MOSFETs and secondary diodes optimally used. This operating point can be reached only for specific input voltage and load (usually full load and nominal V_{bulk}).

Gain characteristics shape and also needed operating frequency range is given by these parameters:

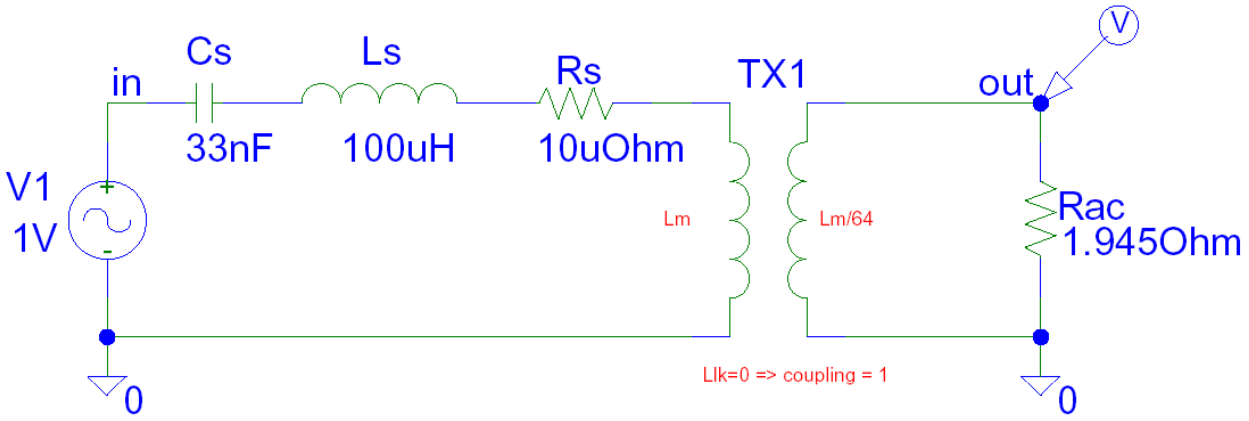
- L_m/L_s ratio
- Characteristic impedance of the resonant tank
- Load value

How to obtain gain characteristics?

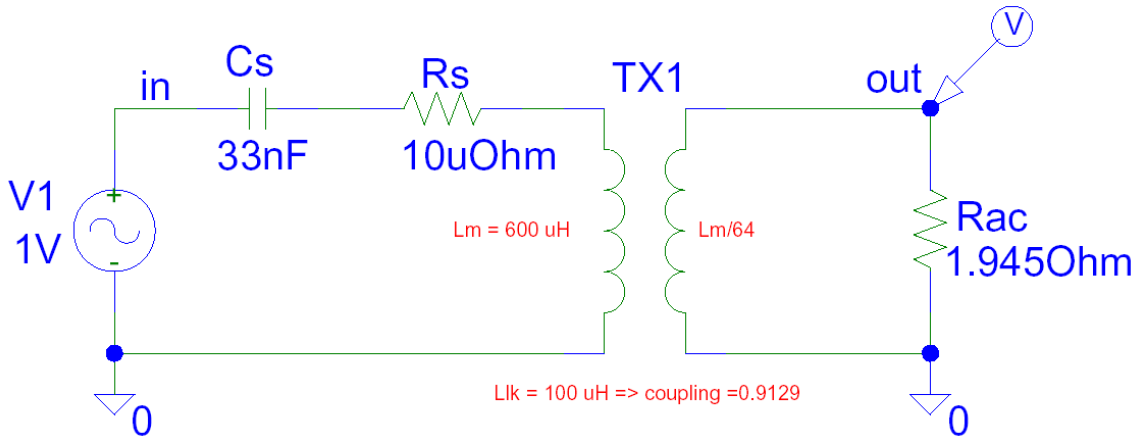
Use fundamental approximation and AC simulation in any simulation software like PSpice, Icap4 etc..



Discrete and integrated tank gain differences



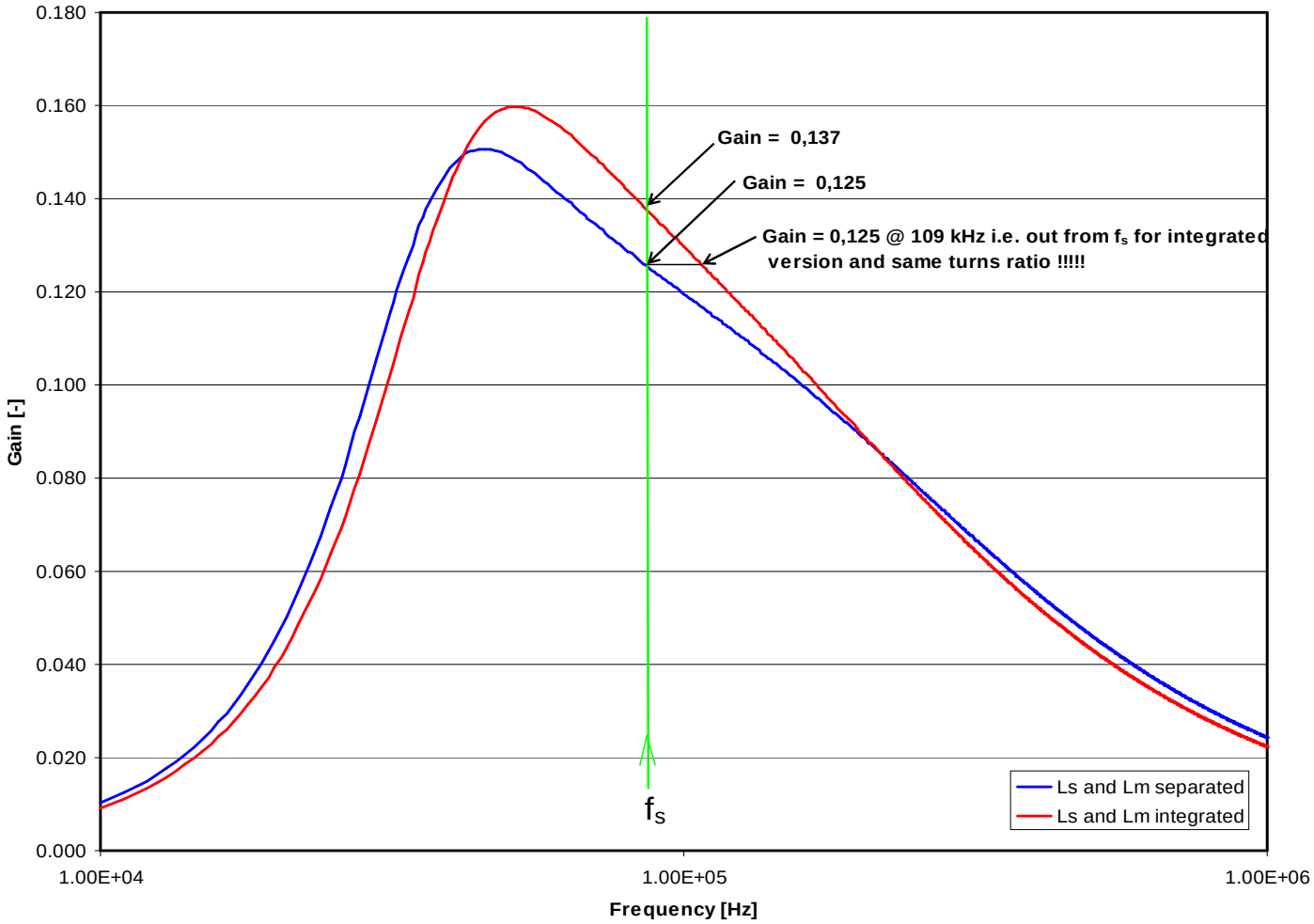
Simulation schematic for discrete solution



Simulation schematic for integrated solution

Discrete and integrated tank gain differences

(the same Ls, Lm values and transformer turn ratio)



Discrete and integrated tank gain differences

- Integrated solution provides higher gain in comparison to the discrete solution and the same transformer turn ratio!
- The leakage inductance “boost” the transformer gain
- Gain difference increases with L_s/L_m ratio i.e. higher L_s causes higher gain difference as the L_m gets to be less clamped by the secondary load
- Turns ratio correction has to be done when designing integrated solution based on the discrete solution model.

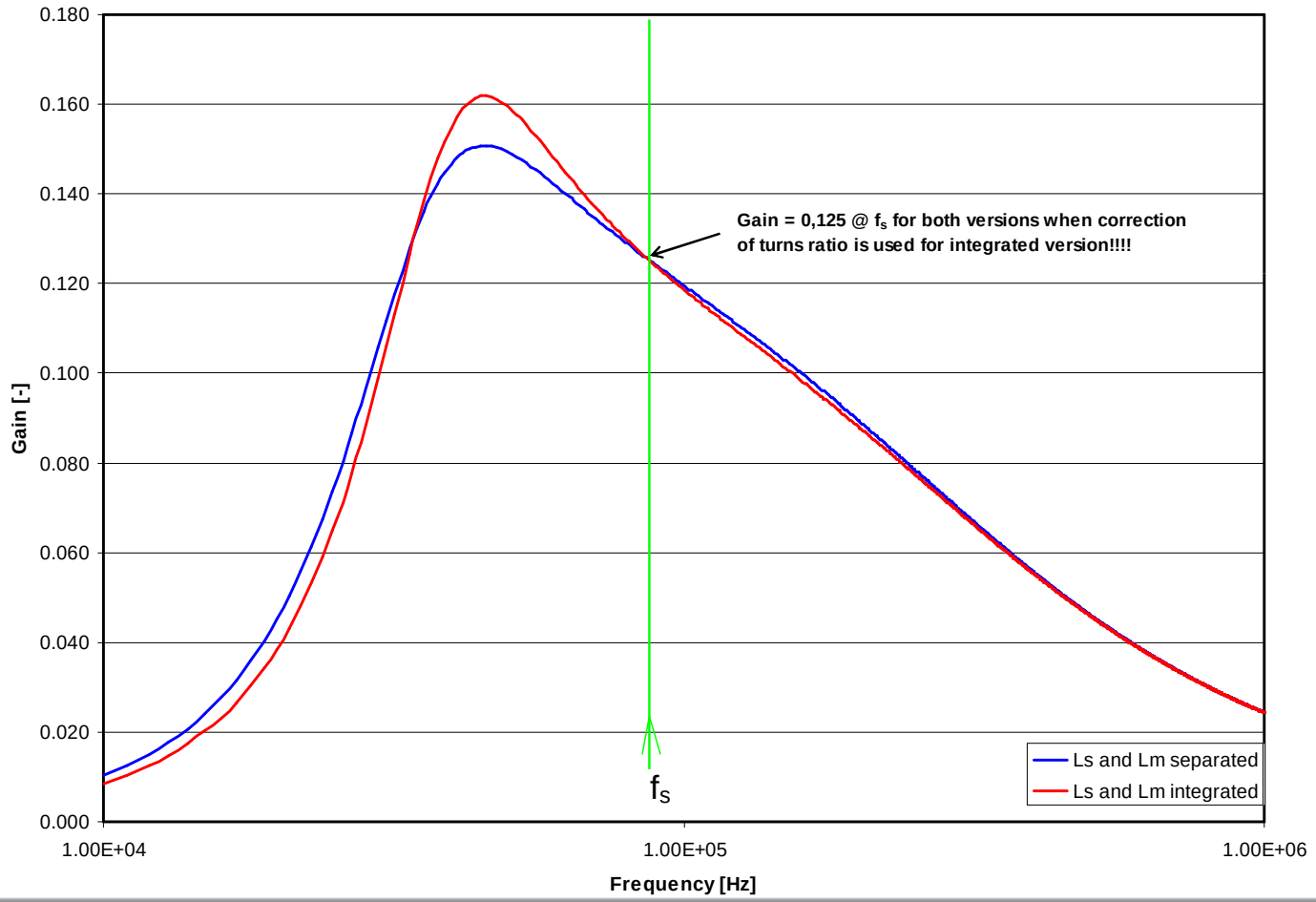
$$n_{\text{int}} = \frac{n_{disc}}{k} = \frac{n_{disc}}{\sqrt{1 - \frac{L_{lk}}{L_m}}}$$

Where: n_{int} is turns ratio of the integrated solution
n_{disc} is turns ratio of the discrete solution
k is transformer coupling coefficient

Note: Leakage inductance is usually very small in comparison to the magnetizing inductance for discrete solution => its impact to the gain characteristic can be neglected but in fact the discrete solution is always combination of both solutions as ideal transformer doesn’t exist.

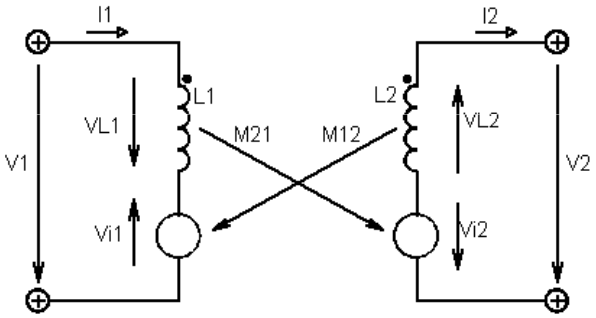
Discrete and integrated tank gain differences

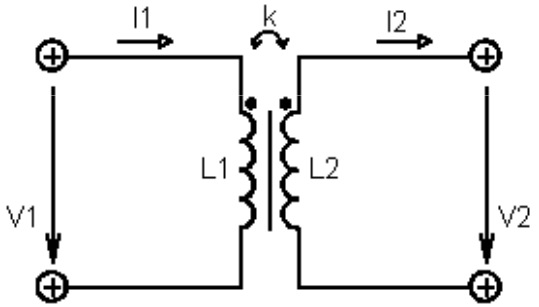
(the same Ls, Lm values after turn ratio correction)



Basic transformer model

As mentioned in previous slides, there exist differences in gain characteristic and power stage operation when comparing discrete and integrated resonant tank solutions. These differences are related to the leakage inductance existence. Generic transformer model reflects the reality and can be used without any problems:





Thanks to the transformer reciprocity the $M_{12}=M_{21}=M$ one can then derive:

$$u_1(t) = L_1 \cdot \frac{di_1(t)}{dt} - M \cdot \frac{di_2(t)}{dt}$$

$$u_2(t) = M \cdot \frac{di_1(t)}{dt} - L_2 \cdot \frac{di_2(t)}{dt}$$

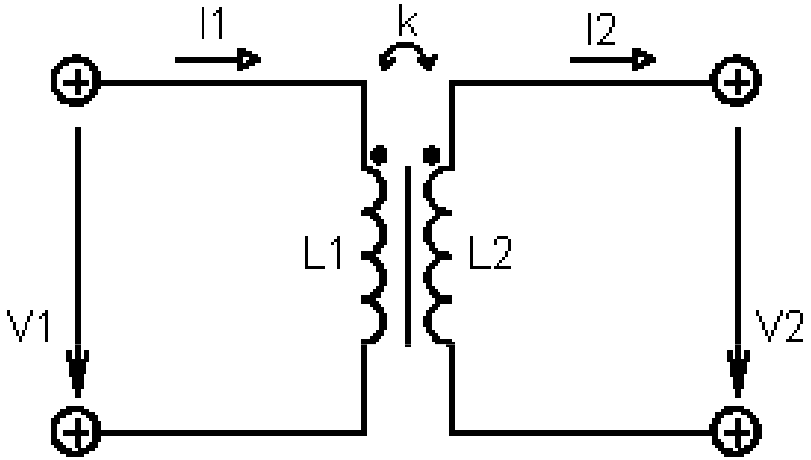
$$k = \frac{M}{\sqrt{L_1 \cdot L_2}}$$

How to get coupling coefficient k ?:

$$k = \sqrt{1 - \frac{L_{1s}}{L_1}} = \sqrt{1 - \frac{L_{2s}}{L_2}}$$

Where: L_{1s} is primary inductance when secondary is shorted
L_1 is primary inductance when secondary is opened
L_{2s} is secondary inductance when primary is shorted
L_2 is secondary inductance when primary is opened

Impedance transformer model parameters derivation from Ls and k and Gnom



Inputs from res. tank deign:

L_s - required resonant inductance

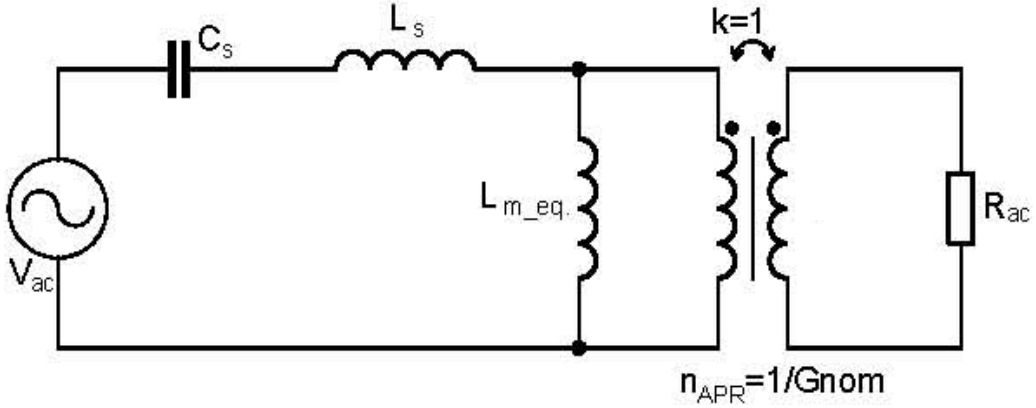
G_{nom} - nominal gain at f_s

$m = \frac{L_m}{L_s}$ - Inductance ratio

$$L_1 = L_m = m \cdot L_s \qquad k = \sqrt{1 - \frac{1}{m}} \qquad L_2 = L_s (m-1) \cdot G_{nom}{}^2$$

Basic model parameters can be easily derived from resonant inductance, required nominal gain and primary to resonant inductances ratio

APR transformer model



Inputs from real transformer:

L_1, L_2, k

$$L_s = L_{lk1} \qquad L_{m\_eq} = L_1 - L_{lk1}$$

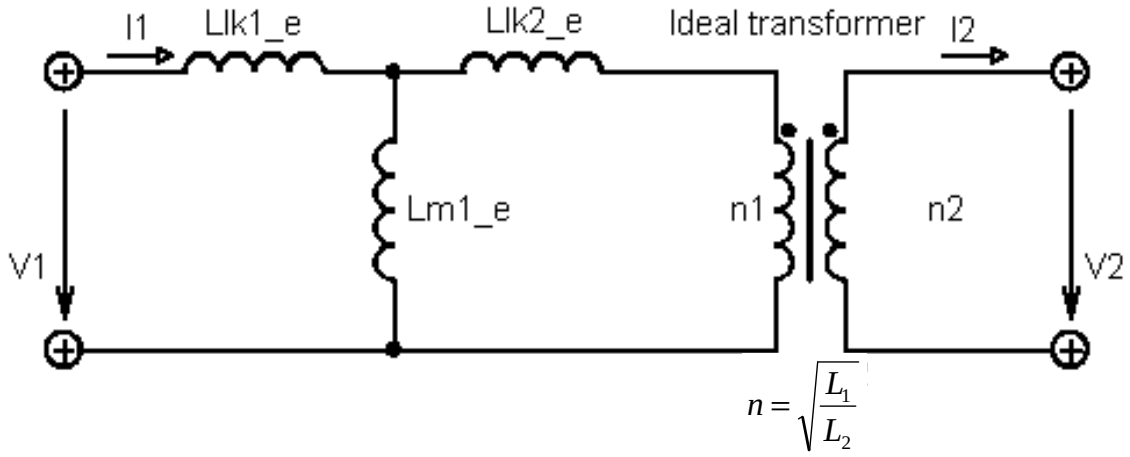
$$n_{APR} = \frac{1}{G_{nom}} = k \cdot n = k \cdot \sqrt{\frac{L_1}{L_2}}$$

Where:
Gnom – nominal gain at fs
n – primary and secondary transformer ratio

- FHA can be easily applied to APR model => suitable for analysis
- Ideal trf. in APR model transfers sec. impedance to primary by $1/G_{nom}$
- Real transformer inductance ratio n is affected by coupling coefficient

Integrated LLC stage can be also modeled using T or Π transf. model

T model of the transformer

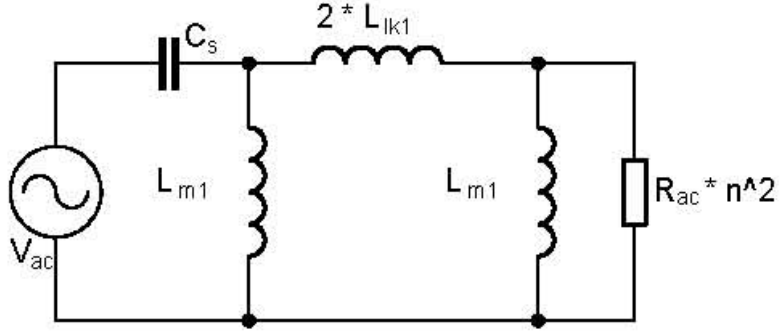


Inputs from real transformer:
L_1, L_2, k, n

$$L_{lk1\_e} = (1-k) \cdot L_1 \qquad L_{m1\_e} = k \cdot L_1 \qquad L_{lk2\_e} = L_{lk1\_e}$$

- The equivalent magnetizing inductance cannot be clamped by output load
- Model components values cannot be measured physically
- This model uses ideal transformer with turns ratio that is equal to inductance turns ratio

Π model of the transformer



Inputs from real transformer:

L_1, L_2, k

$$n = \sqrt{\frac{L_1}{L_2}}$$

$$Lll = \frac{1}{2}\frac{\sqrt{Lp\_s^2\,Lp\_o^2 - Lp\_s^3\,Lp\_o}}{Lp\_o - Lp\_s}$$

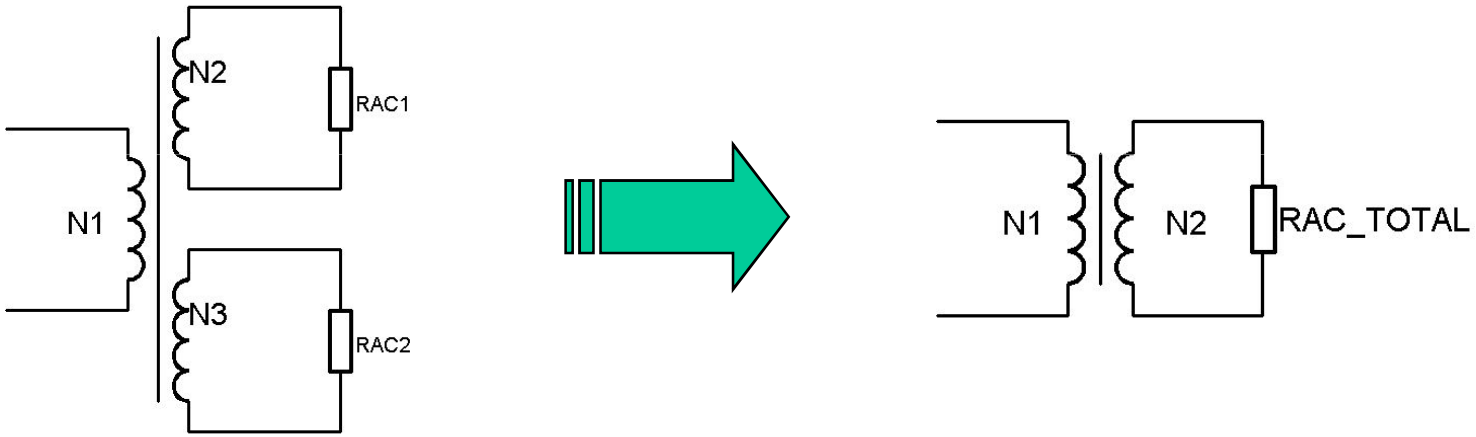
$$Lm1 = Lp\_o - \frac{1}{2}\frac{\sqrt{Lp\_s^2\,Lp\_o^2 \quad Lp\_s^3\,Lp\_o}}{Lp\_o - Lp\_s} + \frac{1}{2}\sqrt{4Lp\_o^2 + \frac{Lp\_s^2\,Lp\_o^2 \quad Lp\_s^3\,Lp\_o}{(Lp\ o - Lp\ s)^2}}$$

- The left equivalent magnetizing inductance cannot be clamped by load
- Model components values cannot be measured physically
- This model uses ideal transformer with turns ratio that is equal to inductance turns ratio

→ - Magnetizing inductance is not fully clamped by load in integrated res. tank designs due to leakage inductance

Gain characteristics - multiple output design

Use fundamental approximation with AC simulation and recalculate AC resistances to only one output i.e. parallel combination of recalculated AC resistances.



$$R_{ac\_total} = \frac{Rac_1 \cdot Rac_2 \cdot \left(\frac{n_2}{n_3}\right)^2}{Rac_1 + Rac_2 \cdot \left(\frac{n_2}{n_3}\right)^2}$$

Full load Q and m factors optimization

Proper selection of these two factors is the key point for the LLC resonant converter design! Their selection will impact these converter characteristics:

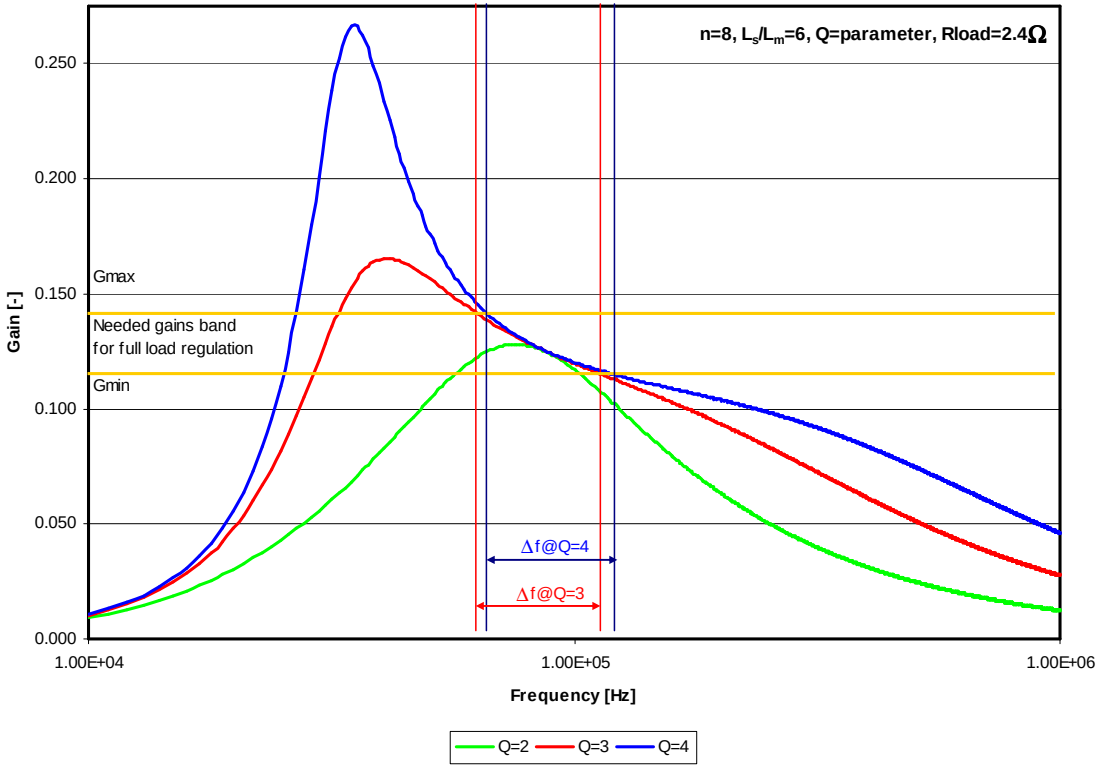
- Needed operating frequency range for output voltage regulation
- Line and load regulation ranges
- Value of circulating energy in the resonant tank
- Efficiency of the converter

The efficiency, line and load regulation ranges are usually the most important criteria for optimization.

Quality factor Q directly depends on the load. It is given by the L_s and C_s components values for full load conditions:

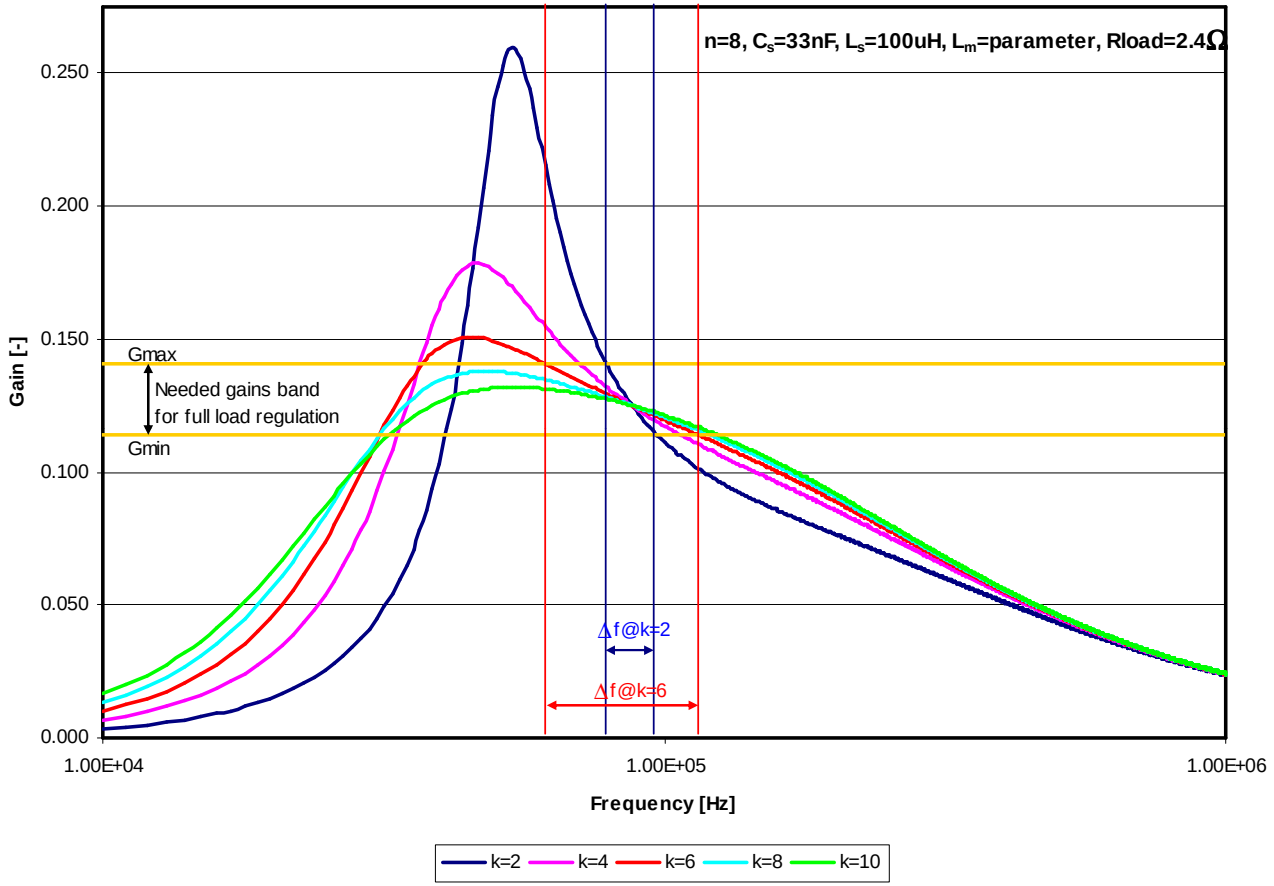
$$Q = \frac{n^2 \cdot R_L}{\sqrt{\frac{L_s}{C_s}}}$$

Full load Q and m factors optimization



- Higher **Q factor** results in larger F_{op} range
- Characteristic impedance has to be lower for higher Q and given load => higher C_s
- Low Q factor can cause the loss of regulation capability!
- LLC gain characteristics are degraded to the SRC for very low Q values.

Full load Q and m factors optimization



- The $m=L_m/L_s$ ratio dictates how much energy is stored in the L_m.
- Higher **m** will result in the lover magnetizing current and gain of the converter.
- Needed regulation frequency range is higher for larger m factor.

Full load Q and k factors optimization

Practically, the $\mathbf{L_s}$ (i.e. leakage inductance of the integrated transformer version) has only limited range of values and is given by the transformer construction (for needed power level) and turns ratio.

The **Q** factor calculation is then given by the wanted nominal operating frequency f_s.

The **m** factor has to be calculated to assure gains needed for the output voltage regulation (with line and load changes).

The **m** factor can be set in such a way that converter wont be able to maintain regulation at light loads – skip mode can be easily implemented to lover no load consumption.

The higher $\mathbf{Z_0}$ i.e. L_s/C_s ratio is used the lower freq range is needed to maintain Regulation. If to low C_s is used the voltage grows to excessive values and gain doesn't have to be high enough for regulation.

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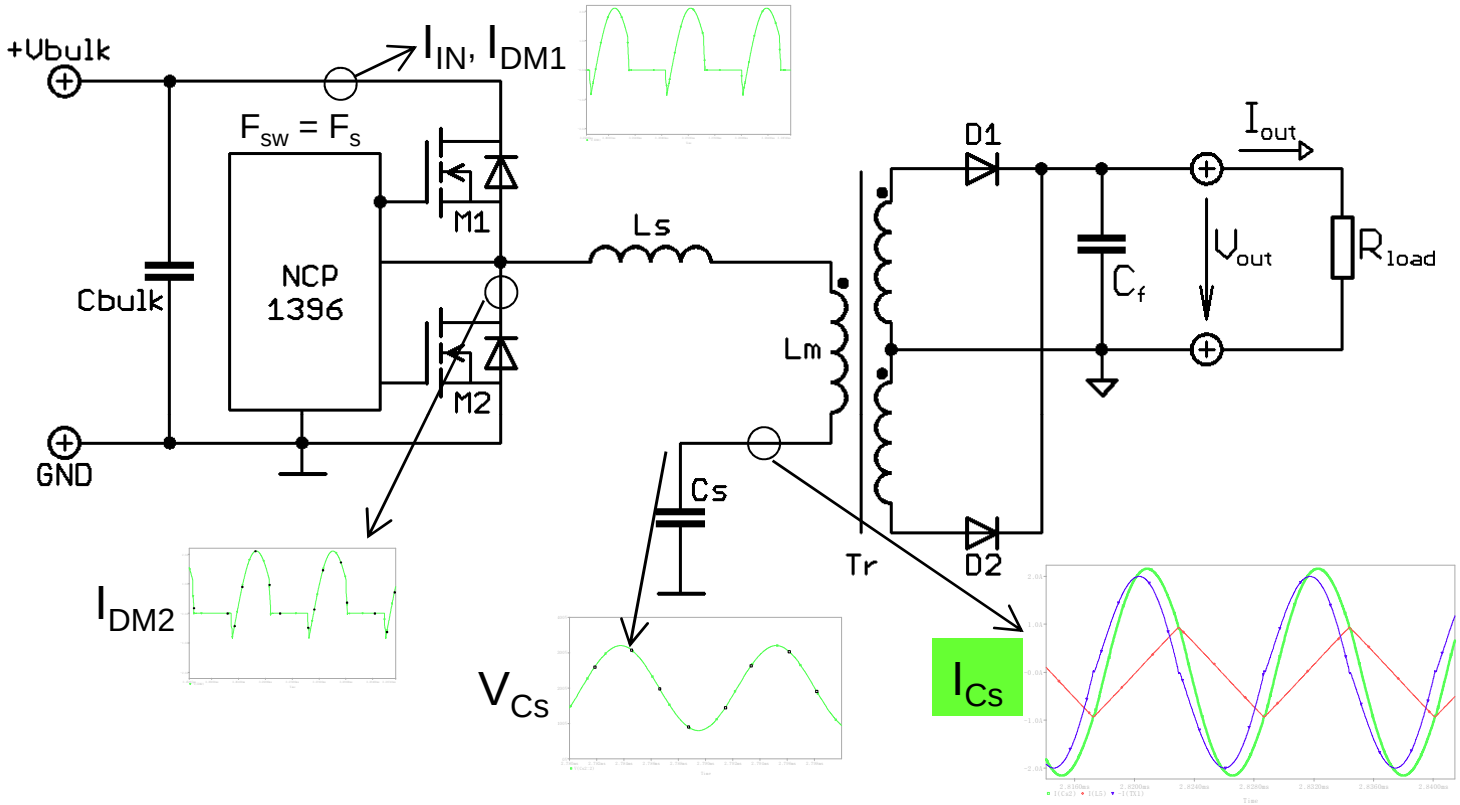
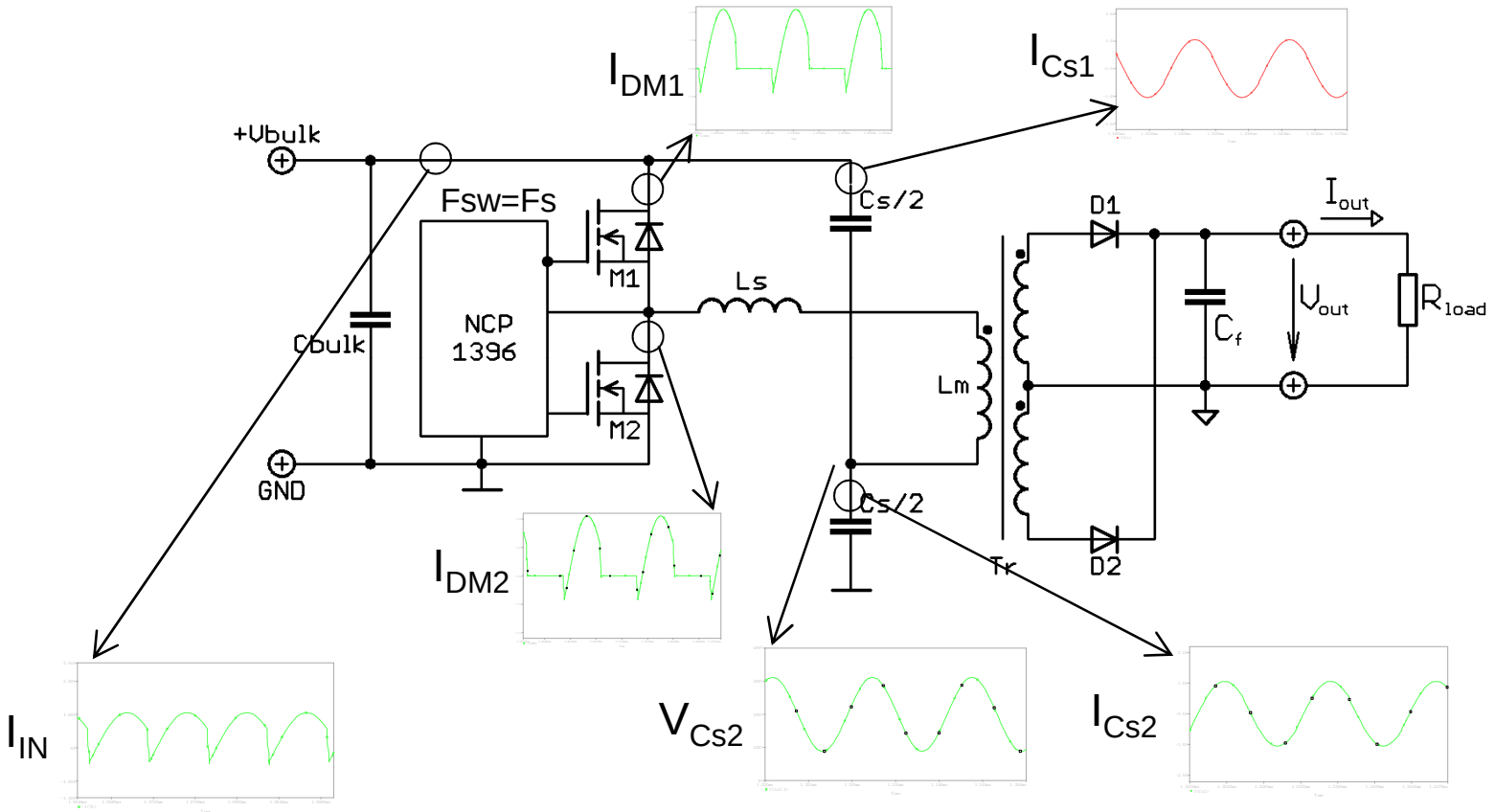
Primary currents – single resonant cap



$$I_{C_s} = I_{primary} = \frac{I_{sec}}{n} + I_{L_m} \quad \Rightarrow \quad I_{C_s\_RMS} \approx \sqrt{\frac{1}{8} \cdot \left(\frac{{I_{out}}^2 \cdot \pi^2}{n^2} + \frac{{V_{bulk}}^2}{24 \cdot {L_m}^2 \cdot {f_{sw}}^2} \right)}$$

Primary currents – split resonant cap



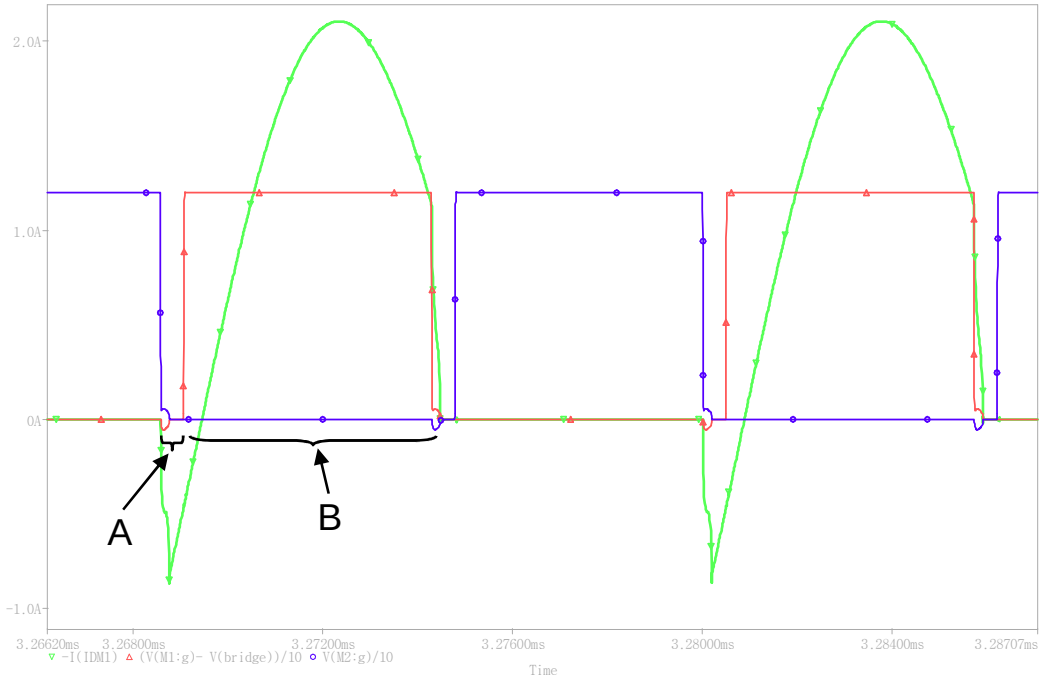
Comparison of Primary Currents

Single and split resonant capacitor solutions - 24 V / 10 A application

Parameter	Single Cap	Split Caps
I_{Cs_Pk}	2.16 A	1.08 A
$I_{Cs\ RMS}$	1.52 A	0.76 A
I_{IN_Pk}	2.16 A	1.08 A
I_{IN_RMS}	1.07 A	0.76 A

- Split solution offers 50% reduction in resonant capacitor current and 30% reduction in input rms current
- Select resonant capacitor(s) for current and voltage ratings

Primary switches dimensioning



- Body diode is conducting during the dead time only (A)
- MOSFET is conducting for the rest of the period (B)
- Turn ON losses are given by Q_g (burned in the driver not in MOSFET)
- MOSFET turns OFF under non-zero current => turn OFF losses

Primary switches dimensioning

MOSFET RMS current calculation

- The body diode conduction time is negligible
- Assume that the MOSFET current has half sinusoid waveform

$$I_{switch\_RMS} \approx \sqrt{\frac{1}{16} \cdot \left(\frac{{I_{out}}^2 \cdot \pi^2}{n^2} + \frac{{V_{bulk}}^2}{24 \cdot {L_m}^2 \cdot {f_{sw}}^2} \right)}$$

Turn OFF current calculation

- Assume that the magnetizing current increases linearly

$$\boldsymbol{I_{OFF} \approx \frac{V_{bulk}}{8 \cdot L_m \cdot f_{sw}}}$$

-Turn OFF losses (E_{OFF} @ I_{OFF}) can be find in the MOSFET datasheet or calculated

Total switch loses: $\boldsymbol{P_{switch\_total} \approx {I_{switch\_RMS}}^2 \cdot R_{dsON} + P_{OFF}}$

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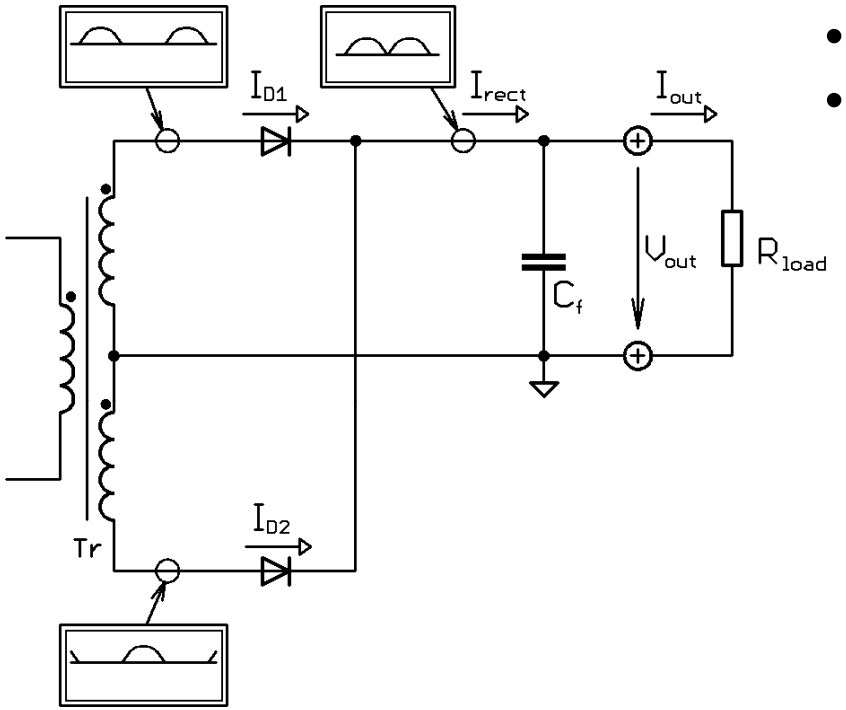
Secondary Rectifier Design



Push-Pull Configuration

- Secondary rectifiers work in ZCS
- Possible configurations:

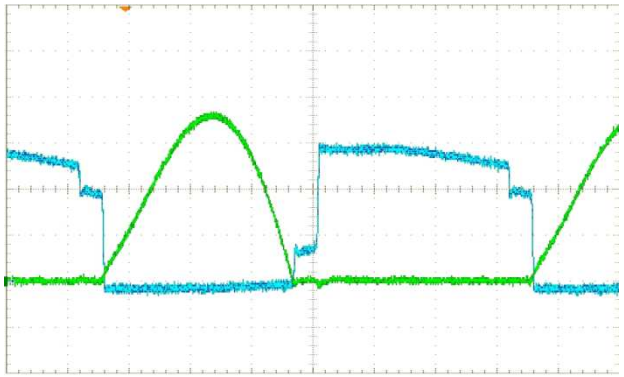
a) Push-Pull configuration – for low voltage / high current output
b) Bridge configuration – for high voltage / low current output
c) Bridge configuration with two secondary windings – for complementary output voltages

Advantages:
- Half the diode drops compared to bridge
- Single package, dual diode can be used
- Space efficient

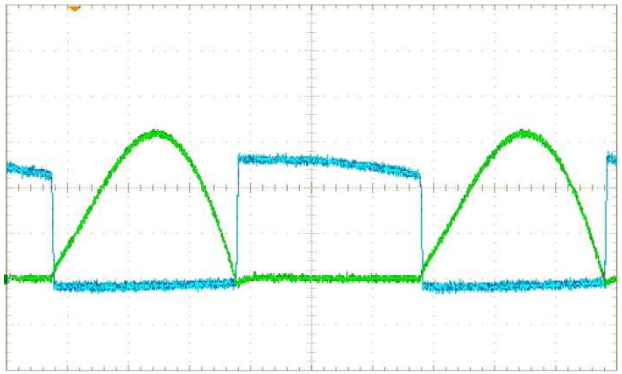
Disadvantages:
- Need additional winding
- Higher rectifier breakdown voltage
- Need good matching between windings

Secondary Rectifier Design

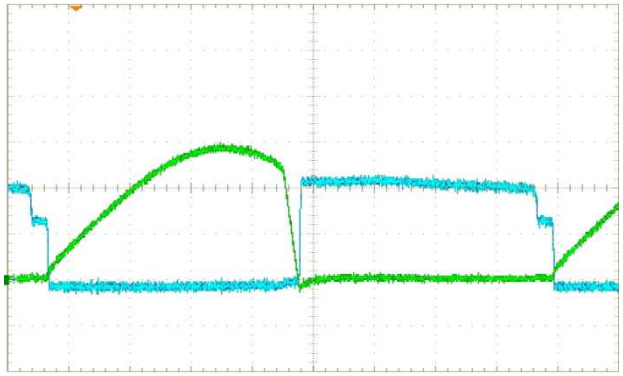
Rectifier waveforms for different operating states



a) $F_{op} < F_s$



b) $F_{op} = F_s$



c) $F_{op} > F_s$

- rectifier current
- rectifier voltage

Simplification by analyzing the operating state in the series resonant frequency F_s is used thereafter. Another simplification is done – assume that the secondary current has sinusoidal shape.

Secondary Current Calculations – Push-Pull

Equations	24 V/10 A output	12 V/20 A output
RMS diode current $I_{D\_RMS} = I_{out} \cdot \frac{\pi}{4}$	$I_{D\_RMS} = 7.85A$	$I_{D\_RMS} = 15.7A$
AVG diode current $I_{D\_AVG} = \frac{I_{out}}{2}$	$I_{D\_AVG} = 5A$	$I_{D\_AVG} = 10A$
Peak diode current $I_{D\_PK} = I_{out} \cdot \frac{\pi}{2}$	$I_{D\_PK} = 15.7A$	$I_{D\_PK} = 31.4A$

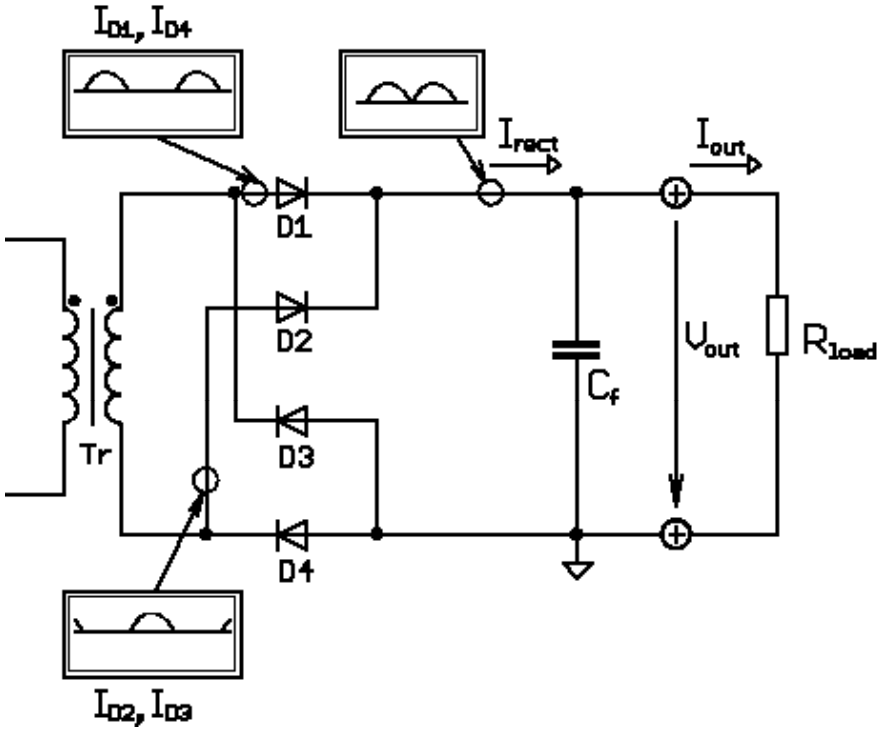
- To simplify calculations, assume sinusoidal current and $F_{op}=F_s$

Rectifier Losses – Push-Pull

Equations	24 V/10 A Vf=0.8 V, Rd=0.01 Ohm	12 V/20 A Vf=0.5 V, Rd=0.01 Ohm
Losses due to forward drop: $P_{DFW} = \frac{V_F \cdot I_{OUT}}{2}$	$P_{DFW} = 4.0\ \mathrm{W}$	$P_{DFW} = 5.0\ \mathrm{W}$
Losses due to dynamic resistance: $P_{DRd} = \frac{R_d \cdot I_{OUT}^{\ 2} \cdot \pi^2}{16}$	$P_{DRd} = 0.62\ \mathrm{W}$	$P_{DRd} = 2.48\ \mathrm{W}$

Equation	24 V/10 A	12 V/20 A
$P_{\mathrm{Rect\_total}} = (P_{DFW} + P_{DRd}) \cdot n_{rect}$	$P_{\mathrm{Rect\_total}} = 9.24\ \mathrm{W}$	$P_{\mathrm{Rect\_total}} = 15\ \mathrm{W}$

Secondary Rectifier - Bridge Configuration

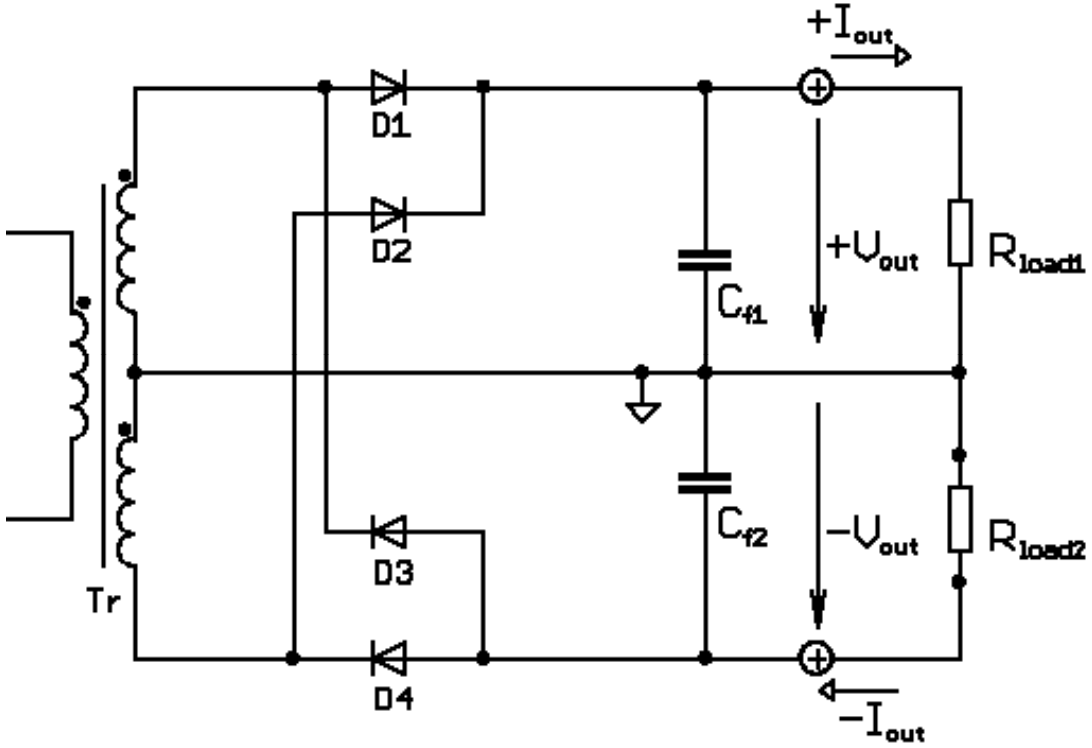


Advantages:
- Lower voltage rating
- Needs only one winding
- No matching needed for windings

Disadvantages:
- Higher diode drops
- Need four rectifiers

Secondary Rectifier – Complementary outputs

Bridge configuration – complementary output



Advantages:

- Needs only two windings
- Low power looses (one Vf only)

Disadvantages:

- Rectifiers with higher breakdown voltage (Vbr>2*Vout)
- Matching between secondary windings needed

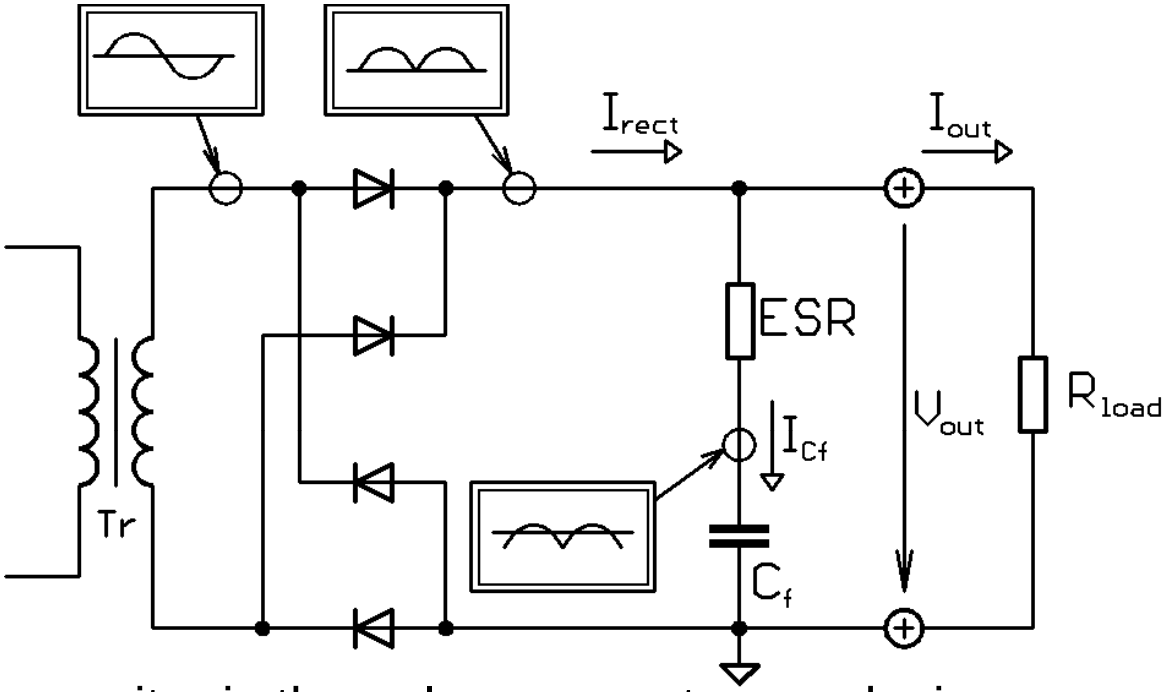
Secondary Rectifier Design Procedure

1. Select appropriate topology (push-pull or bridge)
2. Calculate rectifier peak, AVG and RMS current
3. Select rectifier based on the needed current and voltage ratings
4. Measure the diode voltage waveform in the application and design snubber to limit diode voltage overshoot and improve EMI signature (for LLC “weak” snubber is needed since diodes operate in ZCS mode)

Notes:

- The current ripple increases for $f_{op}<f_s$, the current waveform is still half “sinusoidal” but with dead times between each half period
- The peak current is very high for low voltage and high current LLC applications – example 12 V/20 A output: I_{peak}= 31.4 A and I_{RMS}= 9.7 A!! Each “mΩ” becomes critical - PCB layout. The secondary rectification paths should be as symmetrical as possible to assure same parameters for each switching half cycle.

Output Capacitor Dimensioning



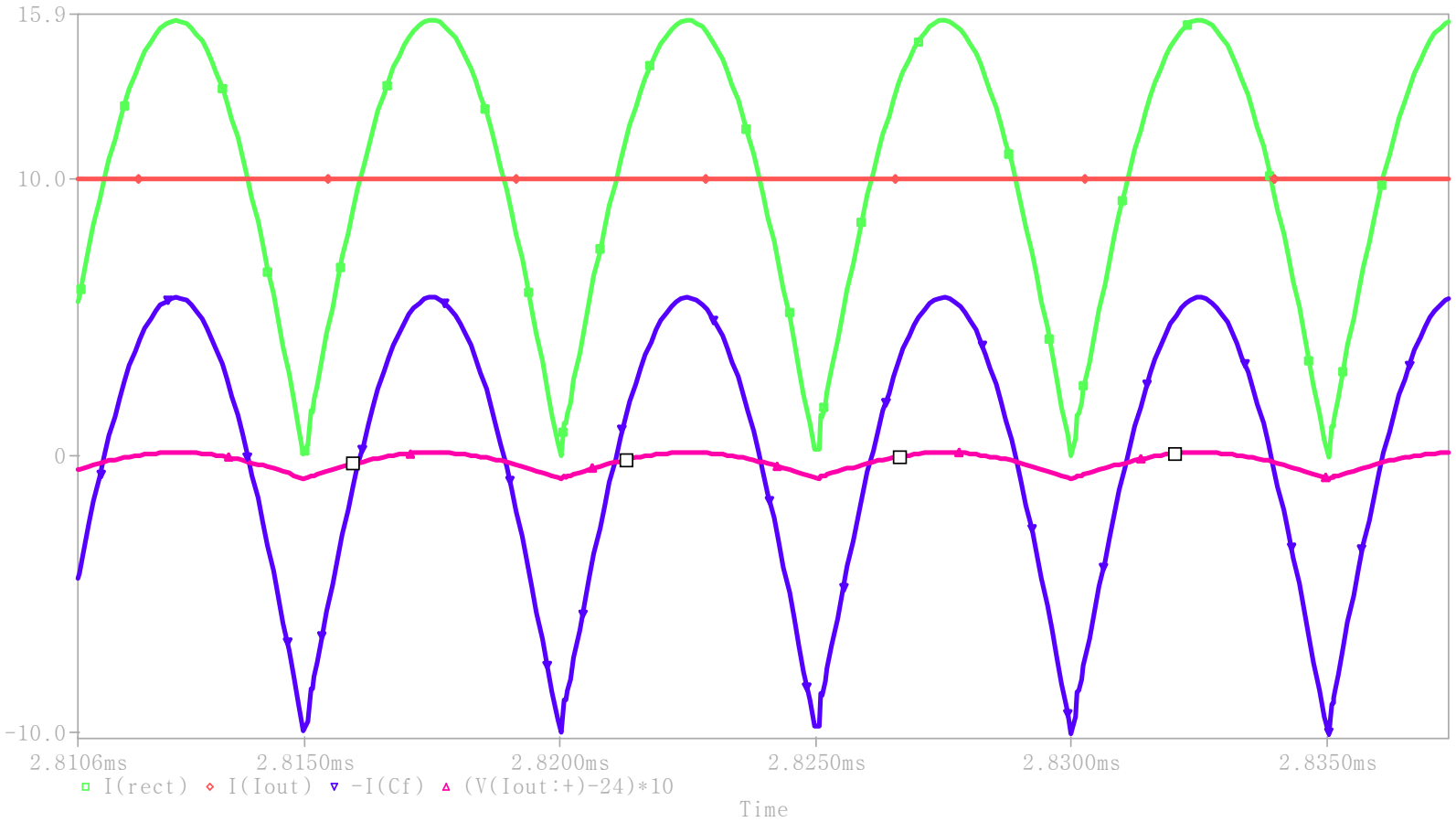
- Output capacitor is the only energy storage device
  - Higher peak/rms ripple current and energy
- Ripple current leads to:
  - Voltage ripple created by the ESR of output capacitor (dominant)
  - Voltage ripple created by the capacitance (less critical)

ESR Component of Output Ripple

- In phase with the current ripple and frequency independent
- Low ESR capacitors needed to keep ripple acceptable
  - Cost/performance trade-off (efficiency impact)

Equations:	**24 V/10 A example: Cf=5000 uF, ESR=6 mΩ**
Peak rectifier current $I_{rect\_peak} = I_{out} \cdot \frac{\pi}{2}$	$I_{rect\_peak} = 15.7A$
Output voltage ripple peak to peak $V_{out\_ripple\_pk-pk} = ESR \cdot I_{rect\_peak}$	$V_{out\_ripple\_pk-pk} = 94\,\mathrm{mV}$
Capacitor RMS current: $I_{Cf\_RMS} = I_{out} \cdot \sqrt{\frac{\pi^2}{8} - 1}$	$I_{Cf\_RMS} = 4.83\ \mathrm{A}$
ESR power losses $P_{ESR} = I_{Cf\_RMS}^{\ 2} \cdot ESR$	$P_{ESR} = 140\,\mathrm{mW}$

ESR Component of Output Ripple



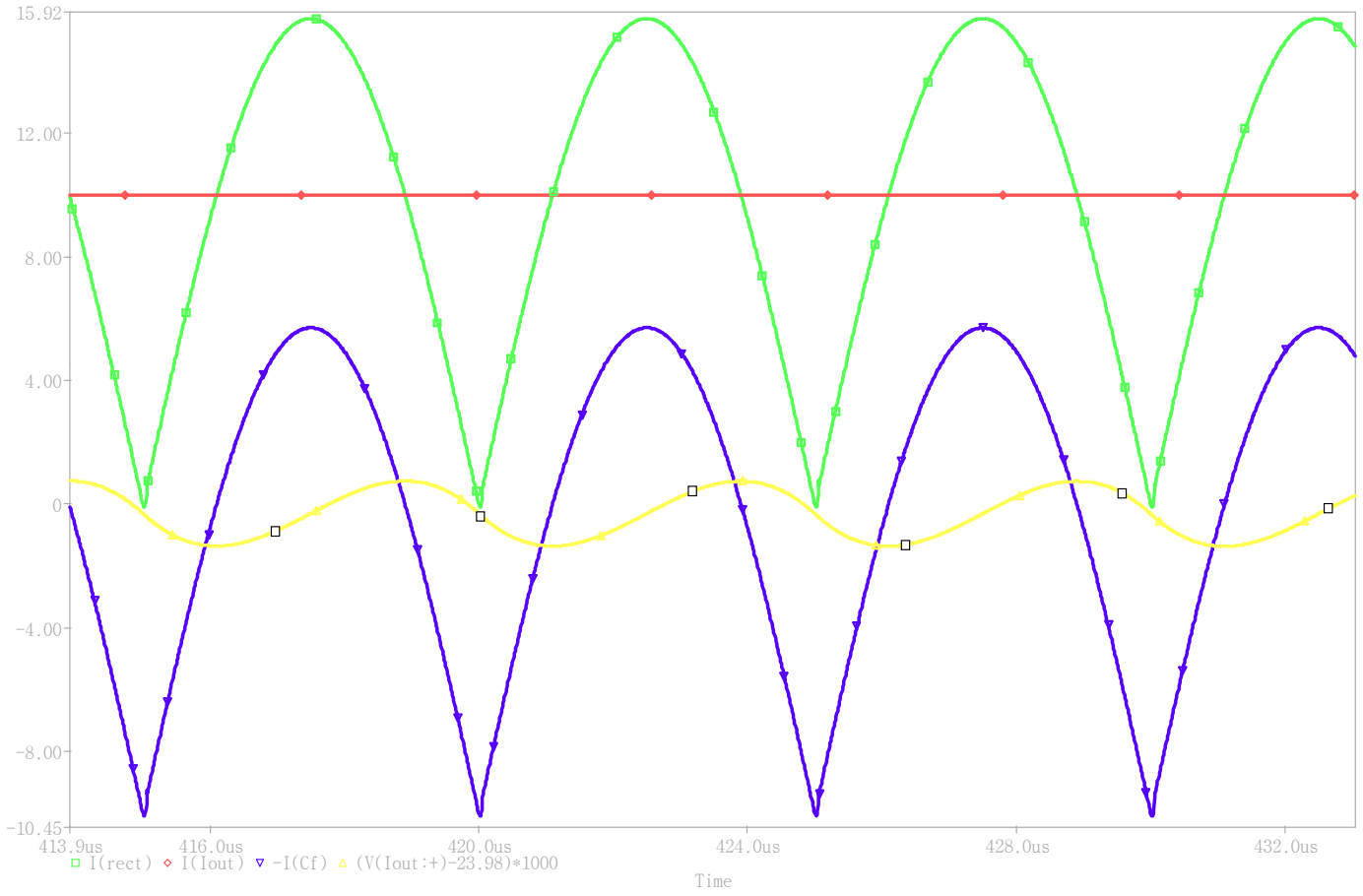
ESR component of the output voltage ripple is in phase with current ripple and is frequency independent.

Capacitive Component of Output Ripple

- Out of phase with current and frequency dependent
- Actual ripple negligible due to high value of capacitance chosen

Equation:	24 V/10 A output example: Cf=5000 uF, Fop=100 kHz $V_{out\_ripple\_cap} = 2.1\,\mathrm{mV}$
$V_{out\_ripple\_cap\_pk-pk} = \frac{I_{out}}{2 \cdot \sqrt{3} \cdot \pi \cdot f_{op} \cdot C_f} \cdot (\pi - 2)$	24 V/10 A output example: Cf=100 uF, Fop=100 kHz $V_{out\_ripple\_cap} = 104\,\mathrm{mV}$

Capacitive Component of Output Ripple



Capacitive component of the output voltage ripple is out of phase with current ripple and is frequency dependent.

Filter Capacitor Design Procedure

1. Calculate peak and rms rectifier and capacitor currents based on Io and Vout
2. Calculate needed ESR value that will assure that the output ripple will be lower than maximum specification
3. Select appropriate capacitor(s) to handle the calculated rms current and having calculated ESR or lower
4. Factor in price, physical dimensions and transient response
5. Check the capacitive component value of the ripple (usually negligible for high enough C_f)

Notes:

- The secondary rectification paths should be as symmetrical as possible to assure same parameters for each switching half cycle

Slide 86

f3 This slide may be better off getting split into two slides and add some more notes. Let's discuss.
ffmrmw; 3.9.2007

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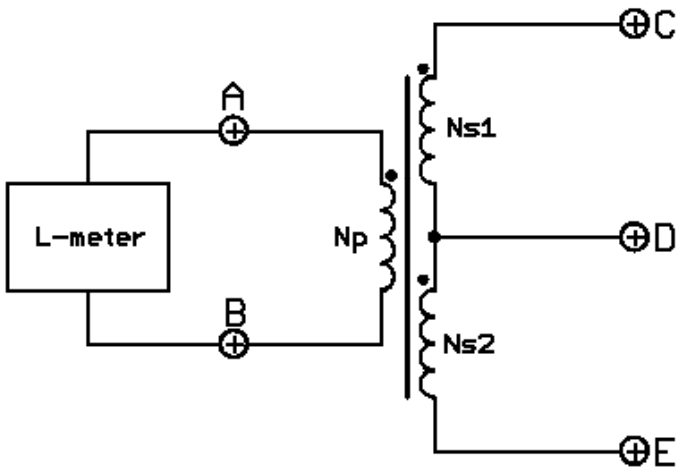
Resonant inductance balance

Transformer leakage inductance

- Total L_s is always affected by the transformer leakage inductance
- Special case for transformer with integrated leakage inductance - $L_s=L_{lk}$
- Push pull and mult. output app. are sensitive to the leakage inductance balance



Parameter	Measured between pins	Secondary pins configuration
$L_{lk(p-s1)}$	A-B	C-D short D-E open
$L_{lk(p-s2)}$	A-B	C-D open D-E short
$L_{lk(total)}$	A-B	C-D short D-E short
L_m	A-B	C-D open D-E open

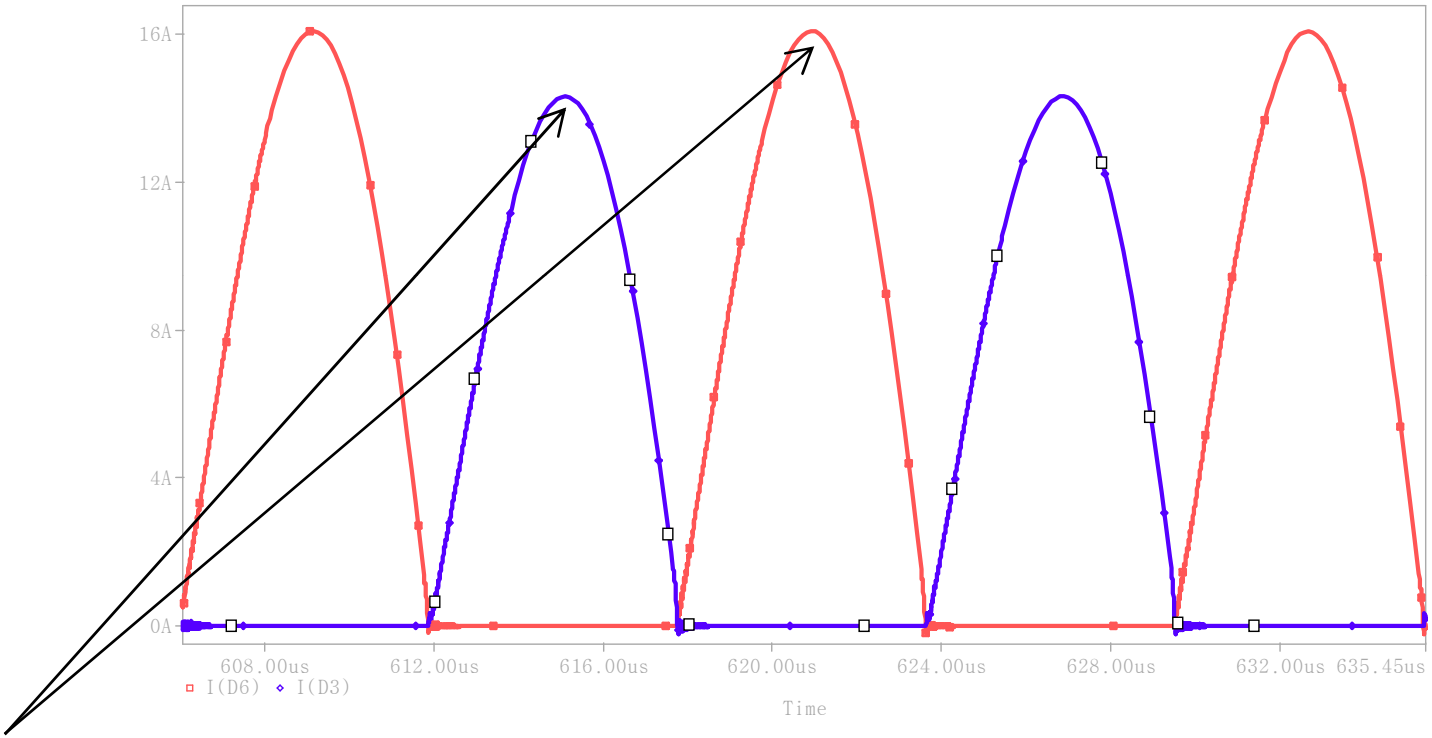
Example: $L_{lk(p-s1)}$ = 105 uH
$L_{lk(p-s2)}$ = 115 uH
ΔL_{lk} = 10 uH
$L_{lk(total)}$ = 100 uH
L_m = 600 uH
C_s = 33 nF

f_{s1} = 85.5 kHz
f_{s2} = 81.7 kHz

5 % difference

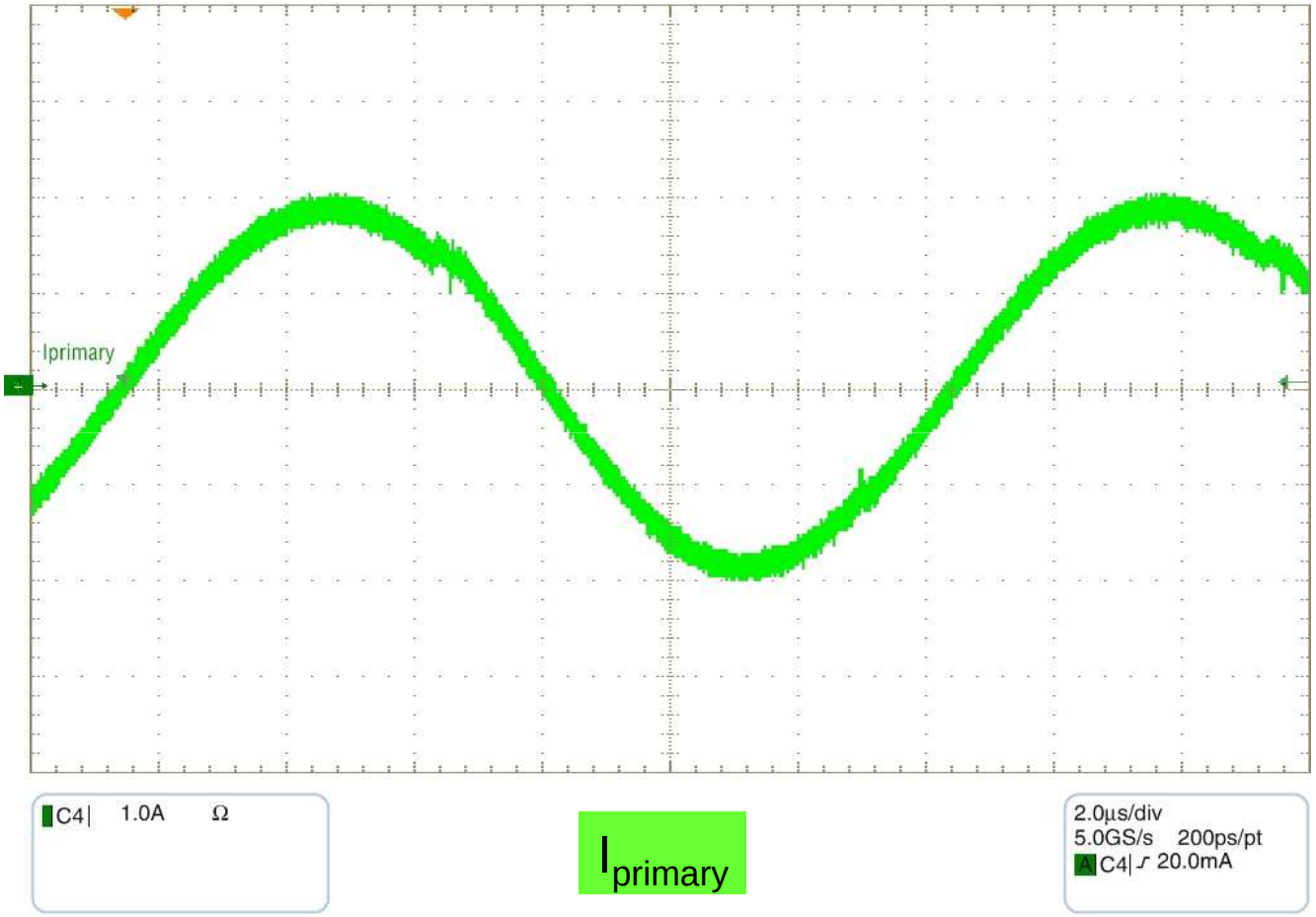
Resonant inductance balance

Series resonant frequency differs for each switching half-cycle that results in primary and mainly secondary current imbalance.



3 A difference in the peak secondary current – the power dissipation is different for each rectifier from pair as well as for the secondary windings.

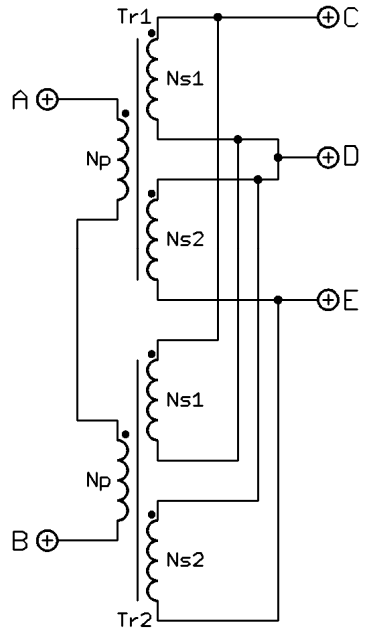
Resonant inductance balance



Converter works below series resonant frequency F_s for the one half of the switching cycle and in the F_s for the second half of the switching cycle.

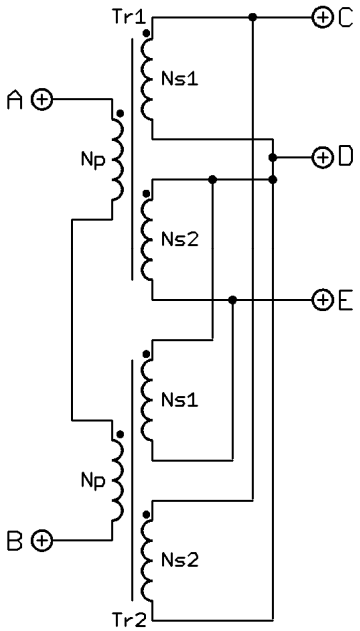
Resonant inductance balance

For high power app. it is beneficial to connect primary windings in series and secondary windings in parallel. There is possibility to compensate transformer leakage imbalance by appropriate connection of the secondary windings:



Wrong

$\Delta L_{lk\_total} = 2 * \Delta L_{lk}$

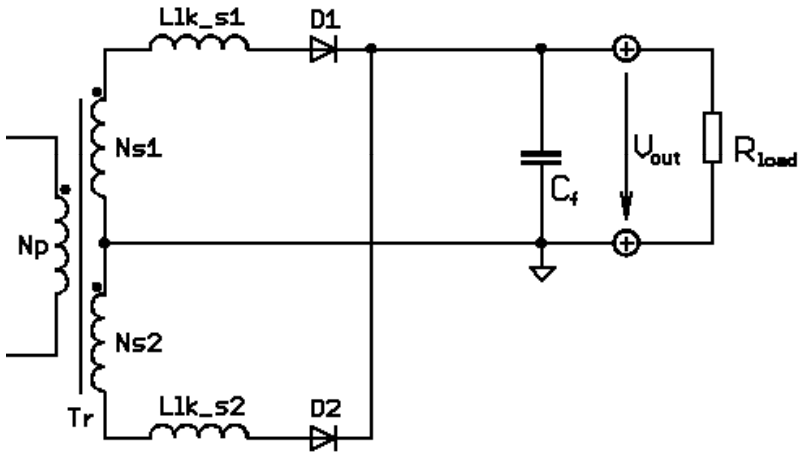


Right

$\Delta L_{lk\_total} = 0$

Resonant inductance balance

The secondary leakage inductance is transformed to the primary and increases the total resonant inductance value. Situation becomes critical for the LLC applications with high turns ratios.



12 V / 20 A application example:

N_p = 35 turns L_{lk_s1} = 100 nH

N_s = 2x2 turns L_{lk_s2} = 150 nH

$n = N_p/N_s$ = 17.5

L_s = 110 uH

L_m = 630 uH

ΔL_{lk_s} = 50 nH ⇒ $\Delta L_s = \Delta L_{lk\_s} \cdot n^2 = 15.3\mu H$

50 nH difference on the secondary causes 14 % difference of L_s !!!

Resonant inductance balance

Transformer construction and secondary layout considerations:

- Resonant tank parameters can change each switching half cycle when push pull configuration is used. This can cause the primary and secondary currents imbalance.

- For the transformer with integrated resonant inductance, it has to be checked how the transformer manufacturer specifies the leakage inductance. Specification for all secondary windings shorted is irrelevant. The particular leakage inductance values can differ.

- When using more transformers with primary windings in series and secondary windings in parallel the leakage inductance asymmetry can be compensated by appropriate secondary windings connection.

- Secondary leakage inductance can cause significant resonant inductance imbalance in applications with high transformer turns ratio. Layout on the secondary side of the LLC resonant converter is critical in that case.

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- Overcurrent protection sensing
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Transformer winding dimensioning

The primary current is sinusoidal for $F_{op} = F_s$. The secondary current is almost sinusoidal too – there is slight distortion that is given by the magnetizing current.

$$I_{primary\_RMS} \approx \sqrt{\frac{1}{8} \cdot \left(\frac{I_{out}^{\,2} \cdot \pi^2}{n^2} + \frac{V_{bulk}^{\,2}}{24 \cdot L_m^{\,2} \cdot f_{sw}^{\,2}} \right)}$$

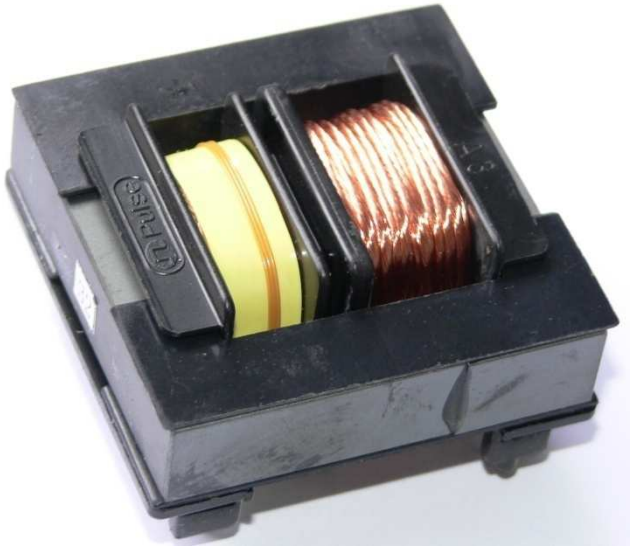
$$I_{secondary\_RMS} \approx I_{out} \cdot \frac{\pi}{2 \cdot \sqrt{2}} \qquad \text{(single winding solution)}$$

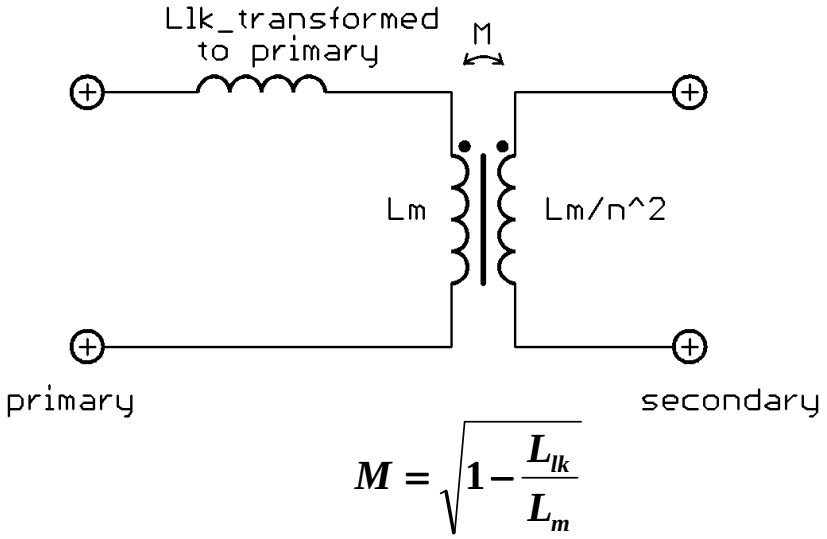
- The skin effect and mainly proximity effect decreases effective cooper area.
- Proximity effect can be overcome by the interleaved winding construction (for discrete resonant tank solution)

- The proximity effect becomes critical for the transformer with integrated leakage
- Wires that are located to the center of the bobbin “feels” much higher current density than the rest of the windings even when litz wire used!

Transformer with integrated leakage

- For the standard transformer with good coupling (L_{lk}<0.1*L_m) is the leakage inductance independent on the air gap thickness and position





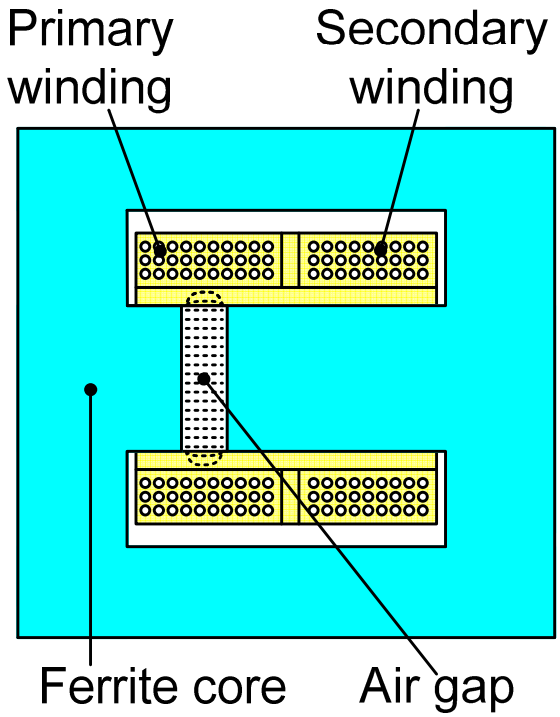
$$M = \sqrt{1 - \frac{L_{lk}}{L_m}}$$

- Transformer with divided bobbin exhibits high leakage inductance
- Significant energy is related to the stray flux
- The L_{lk} is dependent on air gap thickness and position

Transformer with integrated leakage

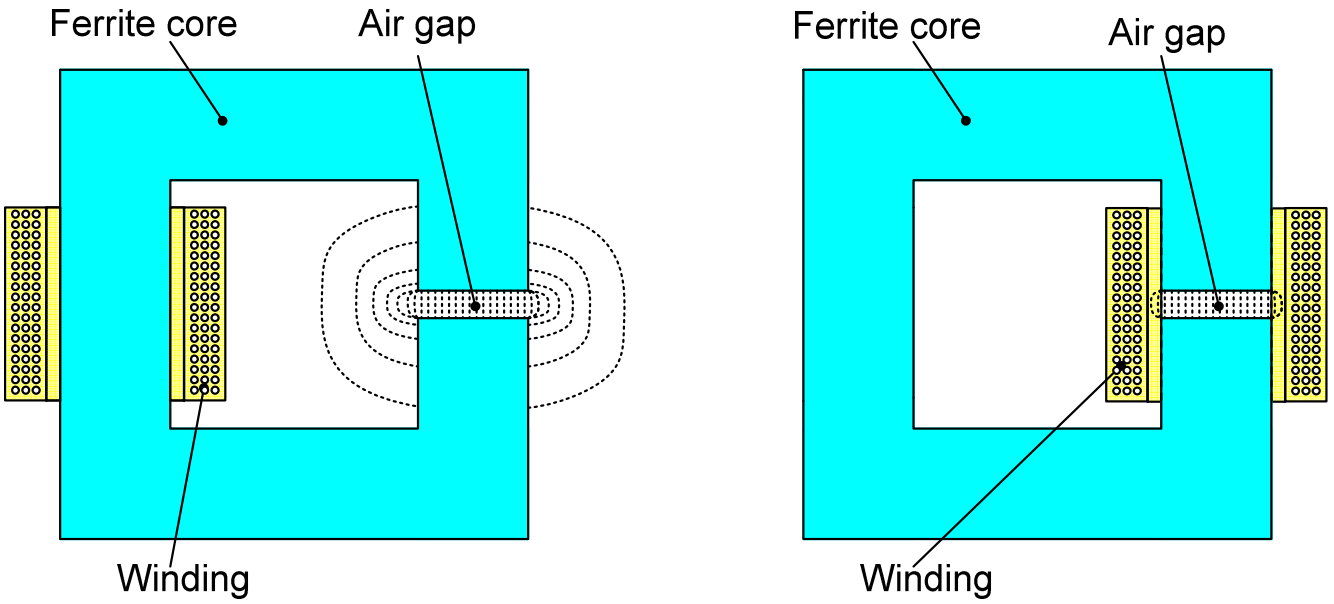
- A ferrite core with air gap on the center leg is used to allow for primary inductance adjustment.

- The air gap stores most of the magnetizing current energy related to the primary winding. Thus it is beneficial to place the air gap below the primary winding to minimize additional stray flux and reduce the proximity effect.



Transformer with integrated leakage

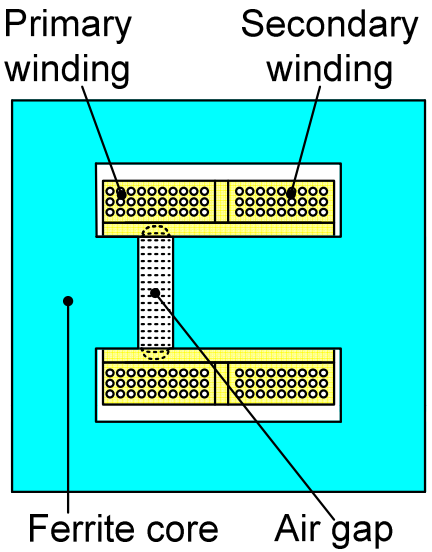
-The air gap position within the bobbin affects primary and secondary inductance
- Inductance inductor with gapped ferrite core is lower when the gap is located below the coil winding rather than outside of the winding
- The difference between both cases is due to the magnetic flux bulging out from the gap and coil



- Same coil features higher inductance when gap is not shielded !!

Transformer with integrated leakage

- Gap is shielded by primary winding only
- The magnetic conductivity for the primary winding $\Lambda_{primary}$ is lower than magnetic conductivity for the secondary winding $\Lambda_{secondary}$



$$\Lambda_{primary} = \frac{L_{primary}}{N_p^{\,2}} \qquad \Lambda_{secondary} = \frac{L_{secondary}}{N_s^{\,2}}$$

$$\Lambda_{primary} < \Lambda_{secondary}$$

- Thanks to this core non-homogeneity, the physical turns ratio (N) is not equal to the electrical turns ratio (n) that is given by the primary and secondary inductances:

$$\frac{N_p}{N_s} \neq \sqrt{\frac{L_{primary}}{L_{secondary}}}$$

N_p – is the primary winding turns number
N_s – is the secondary winding turns

=> It makes no sense to specify transformer turn number before we know real primary and secondary magnetic conductivities

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Overcurrent protection techniques for the LLC series resonant converters

Impedance of the resonant tank reaches very low values when LLC converter operates near the resonant frequency. Fast over current protection has thus be used to protect the primary switches in case of overload or short circuit.

There are few solutions how to protect the LLC power stage from over current:

A) Use current sense transformer in the primary path

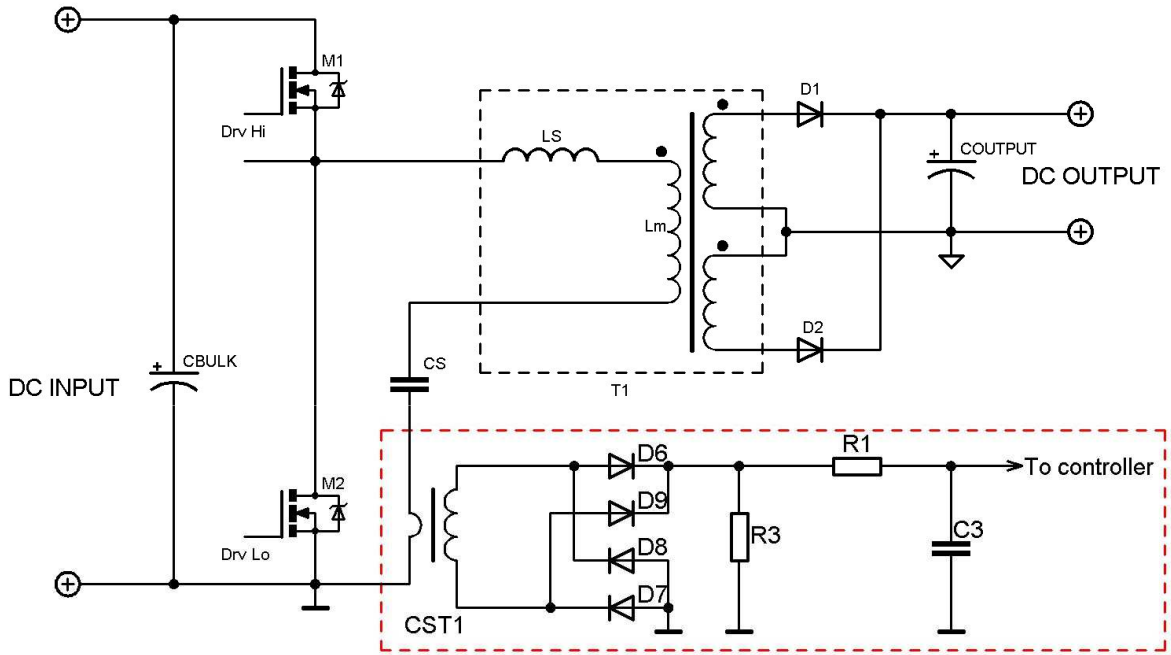
B) Use charge pump to monitor resonant capacitor voltage

C) Use split resonant capacitor with clamping diodes

D) Prepare design which will work always above fs (not very good solution from the efficiency point of view)

Operating frequency of the converter is pushed up by the current control loop in cases A) and B). Primary current is thus limited to the desired value.

A) Using current sense transformer to prepare OCP feature



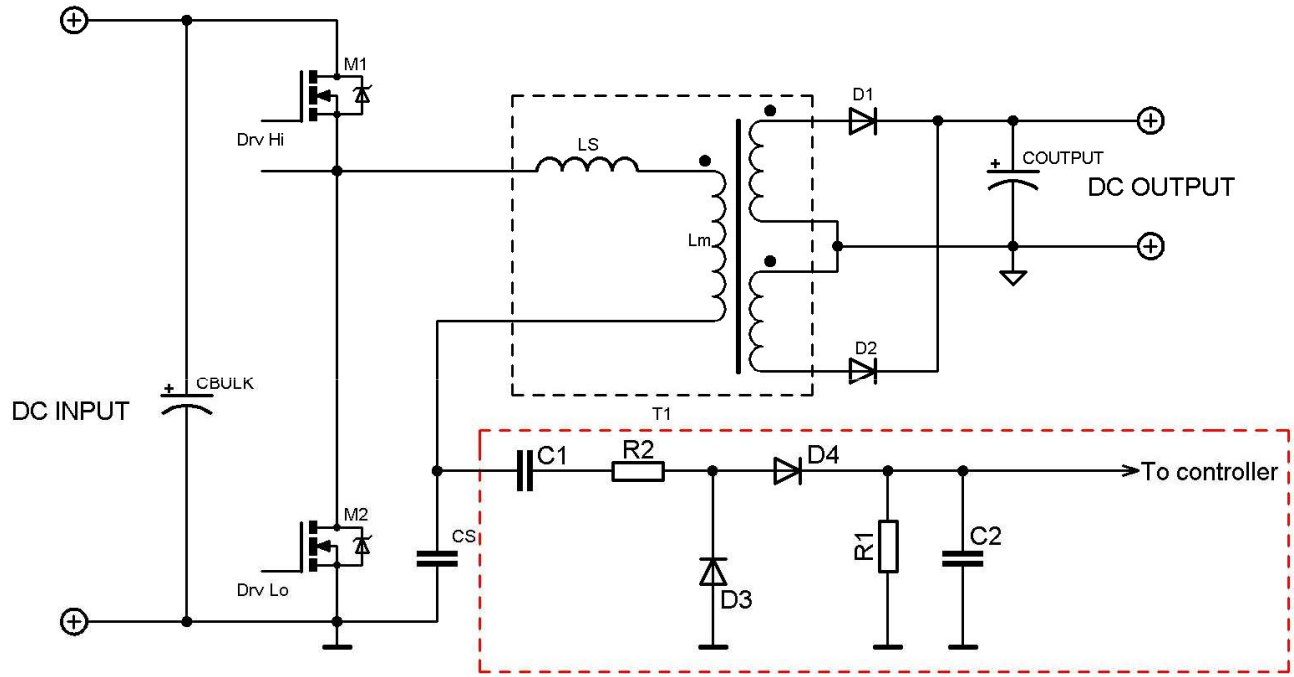
Advantages:

- Easy to implement
- Immediate reaction to the primary current changes
- Good accuracy of the output current limit when bulk voltage is stable (with PFC front stage)

Disadvantages:

- High component count
- CST transformer needed => higher cost

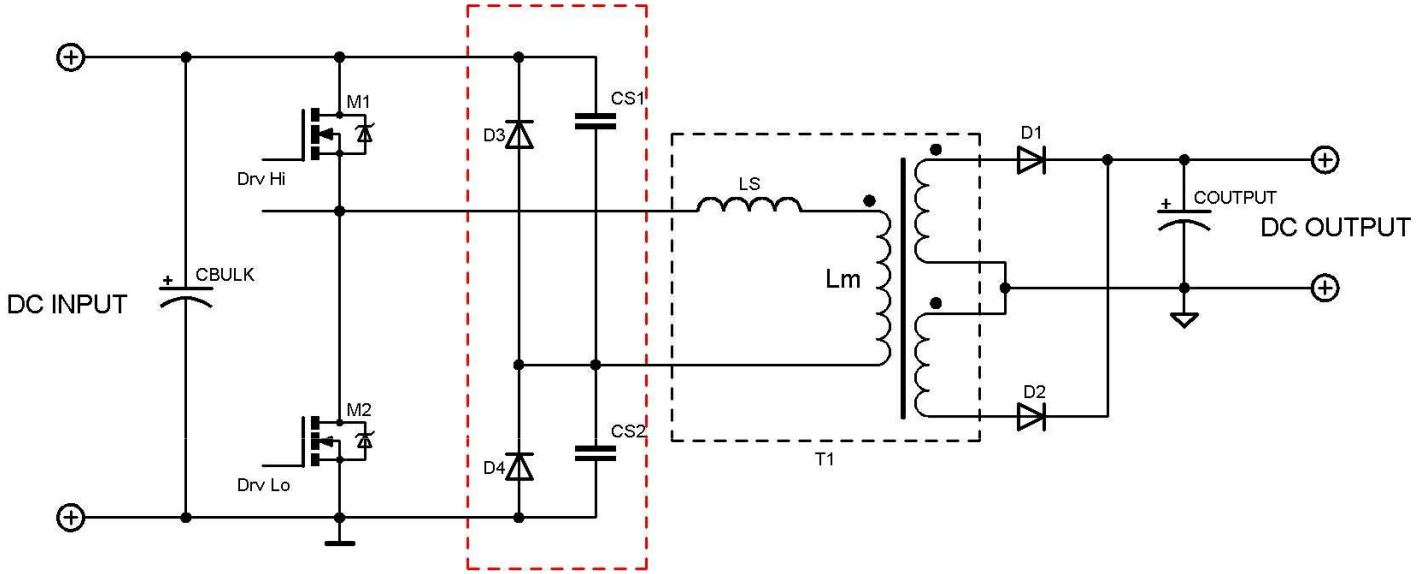
B) OCP with resonant capacitor voltage monitoring using charge pump



Advantages:
- Easy to implement
- Good accuracy of the output current limit when bulk voltage is stable (with PFC front stage)

Disadvantages:
- Another HV capacitor (C1) needed
- One half period delay in response

C) Use two resonant capacitors with voltage clamps



Advantages:

- Resonant capacitors voltage cannot go above bulk voltage, primary current and output power are thus limited automatically – no need for other control loop
- Converter will never enter ZCS region
- Input current ripple is lower in comparison to the one cap solution
- Resonant capacitors with lower voltage ratings can be used
- Can be also used in single resonant capacitor solution

Disadvantages:

- Output current limit has pure accuracy => can be used only as short circuit protection
- Limits the resonant capacitor value
- Is bulk voltage dependent

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Design Example
12 V / 20 A LLC converter with synchronous rectification - AND8460

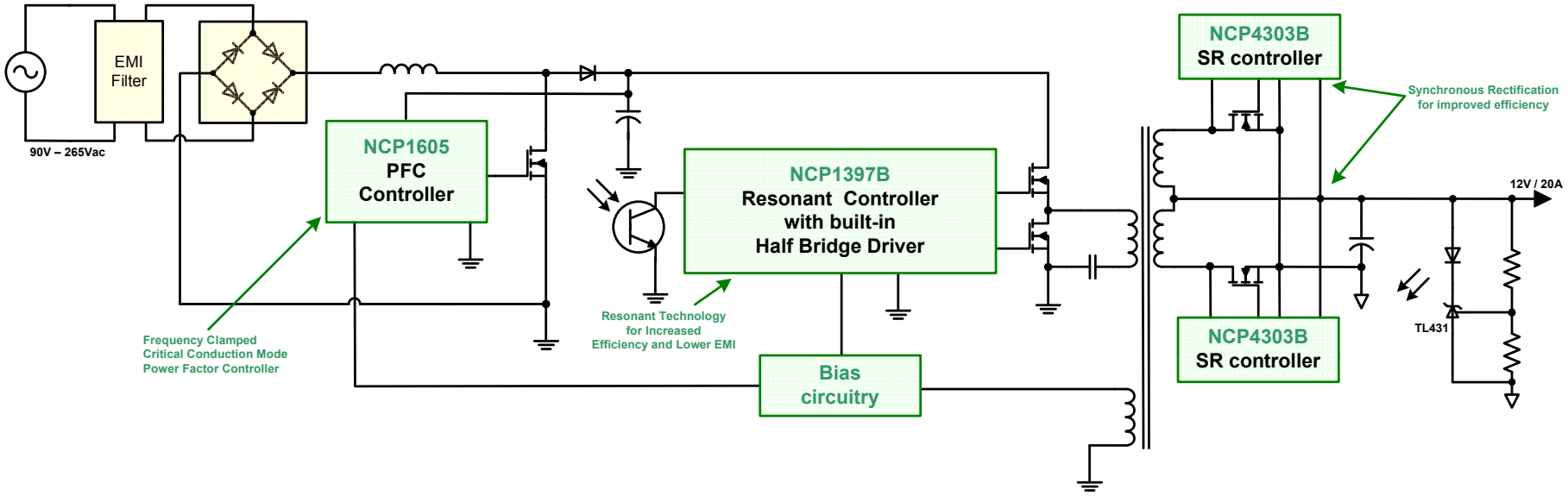
LLC stage requirements

Requirement	Min	Nom	Max	Unit
Input voltage (dc)	350	395	425	V
Output voltage (dc)	-	12	-	V
Output current	0	-	20	A
Total output power	0	-	240	W
Consumption a 500 mW output load in STBY mode	-	-	1.7	W
Consumption a 100 mW output load in STBY mode	-	-	1.2	W
No load consumption SR operating	-	-	870	mW
No load consumption SR turned off	-	-	1	W
Load regulation	-	-	20	mV
Average Efficiency	95	-	-	%

-High efficiency is required

=> secondary SR is needed to fulfill this requirement

SMPS block diagram



- Bulk voltage is provided by PFC stage driven by NCP1605
- NCP1397B is used to implement latched OCP protection
- NCP4303 control SR MOSFETs to maximize efficiency
- TL431 regulates output voltage by modulating LLC stage operating frequency via optocoupler and NCP1397B

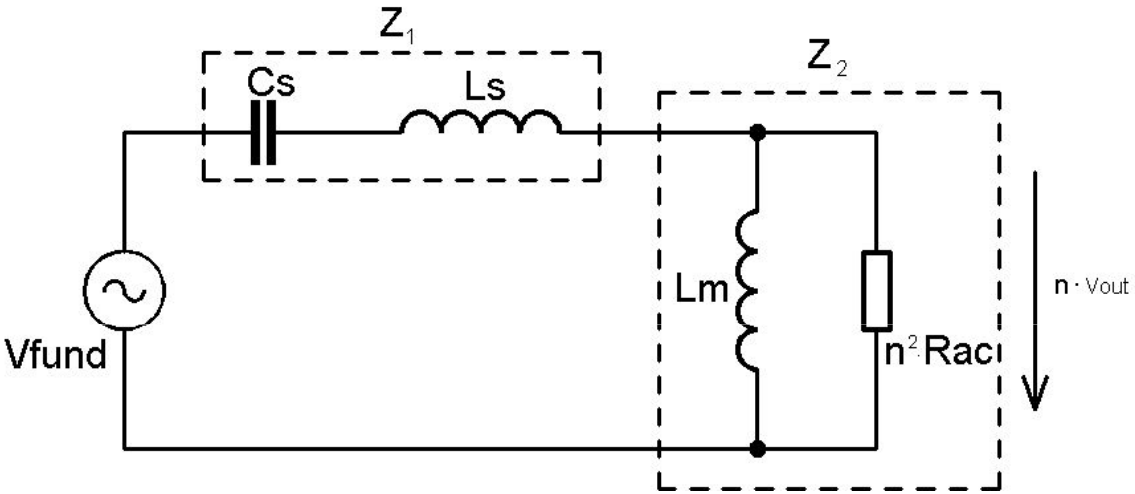
Resonant tank design

Selection of some design parameters:

- Resonant tank type: Integrated resonant inductance (cost constrains)
- Nominal operating frequency: 80 kHz (Efficiency constrains)
- Resonant frequency: same as nominal operating frequency 80 kHz
- Minimum operating frequency: > 60 kHz (transformer size constrains)
- Maximum full load operating frequency: < 100 kHz
- Maximum light load operating frequency: 110 kHz (then skip)
- Nominal resonant capacitor voltage: < 350 V pk

Step 1 – calculate Rac needed for FHA analysis

- Small signal AC analysis is desirable for accurate resonant tank design



- Equivalent load resistance (Rac) has to be used for FHA:

$$R_{ac} = \frac{8}{\pi^2} \cdot \frac{V_{out}}{I_{out\_nom} \cdot \eta} = \frac{8}{\pi^2} \cdot \frac{12}{20 \cdot 0.95} = 0.51\Omega$$

Step 2 – calculate needed LLC stage gain

- Calculate needed converter gain for maximum bulk voltage:

$$G_{\min} = \frac{2 \cdot (V_{out} + V_{f\_SR})}{V_{bulk\_\max}} = \frac{2 \cdot (12 + 0.2)}{425} = 0.057$$

- Calculate needed converter gain for nominal bulk voltage:

$$G_{nom} = \frac{2 \cdot (V_{out} + V_{f\_SR})}{V_{bulk\_nom}} = \frac{2 \cdot (12 + 0.2)}{395} = 0.0618$$

- Calculate needed converter gain for minimum bulk voltage:

$$G_{\max} = \frac{2 \cdot (V_{out} + V_{f\_SR})}{V_{bulk\_\min}} = \frac{2 \cdot (12 + 0.2)}{350} = 0.0697$$

Step 3 – Cs value selection/calculation

- Optimization criterion has to be selected
- Maximum efficiency is required for this design

$$Z_0 = \sqrt{\frac{L_s}{C_s}} \qquad f_s = \frac{1}{2 \cdot \pi \cdot \sqrt{L_s \cdot C_s}} \qquad Q = \frac{n^2 \cdot R_{ac}}{Z_0}$$

Several facts can be considered from above equations:
- The lower Cs is, the higher characteristic impedance and lower quality factor are
- The lower Cs is the higher Ls needs to be used to keep required res. frequency
- The higher Ls is used the lower frequency range is needed for regulation
- The higher Ls is used the higher Lm will be and thus lower magnetizing current

⇒Design with minimized Cs brings two main advantages
- low operating frequency range for regulation
- high efficiency

Step 3 – Cs value selection/calculation

- Resonant capacitor voltage reaches too high level if low capacitance is used
- It is beneficial to keep Vcs below Vbulk for nominal operating conditions because:
  - Low voltage caps. handle higher RMS current with small dimensions, lower cost and good reliability
  - Lower voltage stress occurs to the PCB and transformer primary

Step 3 with regards to above considerations is finally as follows:
Calculate ICs_RMS_nom based on load current value:

$$I_{Cs\_RMS\_nom} \approx I_{sec\_RMS\_mon} \cdot G_{nom} \approx \frac{\pi}{2 \cdot \sqrt{2}} \cdot I_{out\_nom} \cdot G_{nom} \approx \frac{\pi}{2 \cdot \sqrt{2}} \cdot 20 \cdot 0.062 \approx 1.38A$$

Calculated Cs value based on the Ics_RMS_mon and selected Vcs_peak_nom:

$$C_s = \frac{I_{Cs\_RMS\_nom} \cdot \sqrt{2}}{2 \cdot \pi \cdot f_{op\_nom} \cdot \left(V_{Cs\_peak\_nom} - \frac{V_{bulk\_nom}}{2} \right)} = \frac{1.38 \cdot \sqrt{2}}{2 \cdot \pi \cdot 80 \cdot 10^3 \cdot \left(320 - \frac{395}{2} \right)} = 31.6nF \Rightarrow 2*15nF$$

Note: Some error is induced because we did not included magnetizing current component into calculation as it is not know yet.

Step 4 – Ls calculation

- Resonant inductor value can be calculated based on selected resonant frequency and previously calculated resonant capacitor value using modified Thompson law:

$$L_s = \frac{1}{C_s \cdot (2 \cdot \pi \cdot f_s)^2} = \frac{1}{30 \cdot 10^{-9} \cdot (2 \cdot \pi \cdot 80 \cdot 10^3)^2} = 131.9 \mu H \Rightarrow 130 \mu H$$

Step 5 – maximum Lm calculation

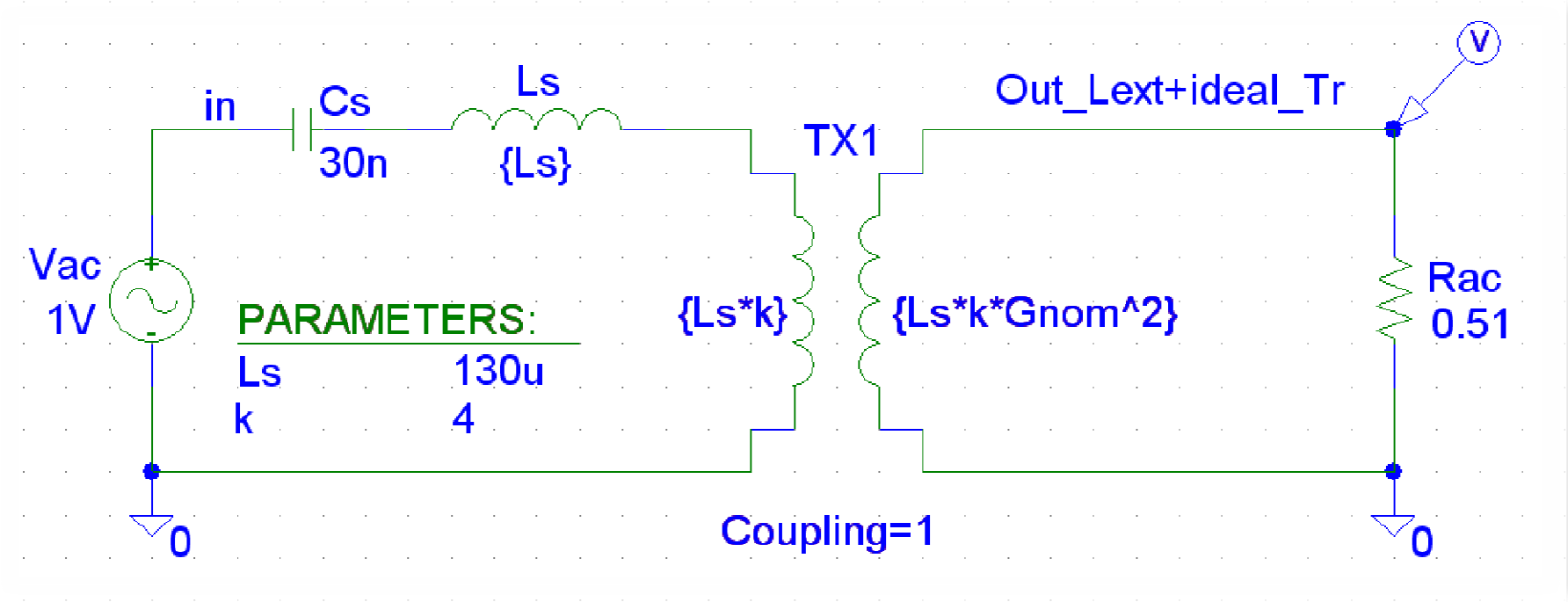
-The maximum Lm value is given by total bridge parasitic capacitance (Coss of MOSFETs and stray capacitance). Magnetizing inductance has to provide enough energy to overcharge bridge parasitic capacitance and prepare ZVS condition within selected deadtime.

$$L_{m\_\max} = \frac{DT}{8 \cdot f_{op\_\max} \cdot C_{HB\_total}} = \frac{350 \cdot 10^{-9}}{8 \cdot 110 \cdot 10^3 \cdot 360 \cdot 10^{-12}} = 1.1 mH$$

Future transformer magnetizing inductance should not be higher than this value.

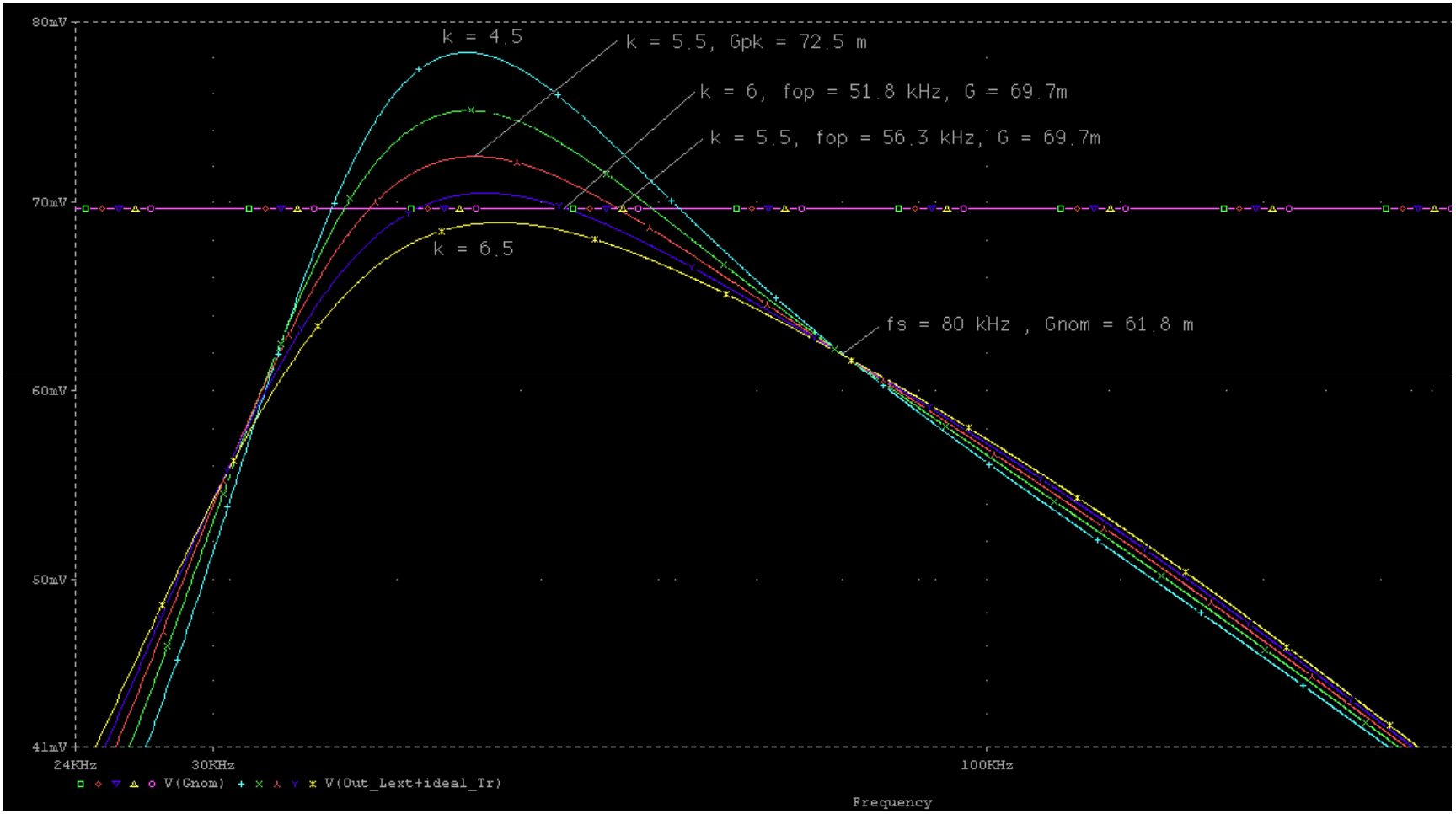
Step 6 – Ls/Lm ratio selection

-The most appropriate Ls/Lm ratio can be selected based on application gain characteristics simulation. Simulation schematic for gain characteristics analysis:



- Use Lm = k*Ls as a parameter we will get several gain characteristics

Step 6 – Ls/Lm ratio selection



-It is evident that k = 5.5 provides optimum performance + some gain margin

=> Lm = Lprimary = 130u * 5.5 = 715 uH

Step 7 – Integrated resonant tank turns ratio

- The turns ration for discrete resonant tank solution that uses transformer with negligible leakage is inverse of nominal gain at resonant frequency

$$n_{discrete} = \frac{1}{G_{nom}} = \sqrt{\frac{L_{primary}}{L_{secondary}}} = \frac{V_{bulk\_nom}}{2 \cdot (V_{out} + V_f)} = \frac{395}{2 \cdot (12 + 0.2)} = 16.18$$

- The gain is boosted when using integrated resonant tank solution because the leakage inductance is not located just only before Lm like in used model

$$G_{nom\_integrated} > \frac{1}{n_{discrete}}$$

- The higher leakage inductance is the higher gain boost will occur.The integrated resonant tank turns ratio can be then calculated as:

$$n_{integrated} = \frac{n_{discrete}}{\sqrt{1 - \frac{L_s}{L_m}}} = \frac{16.18}{\sqrt{1 - \frac{130}{715}}} = 17.88$$

Step 8 – Secondary inductance calculation

- The secondary inductance Lsec can be calculated using nint. and Lprimary

$$L_{secondary} = \frac{L_{secondary}}{n^2_{integrated}} = \frac{715 \cdot 10^{-6}}{17.88^2} = 2.23 \mu H$$

Step 9 – Final resonant tank gain simulation

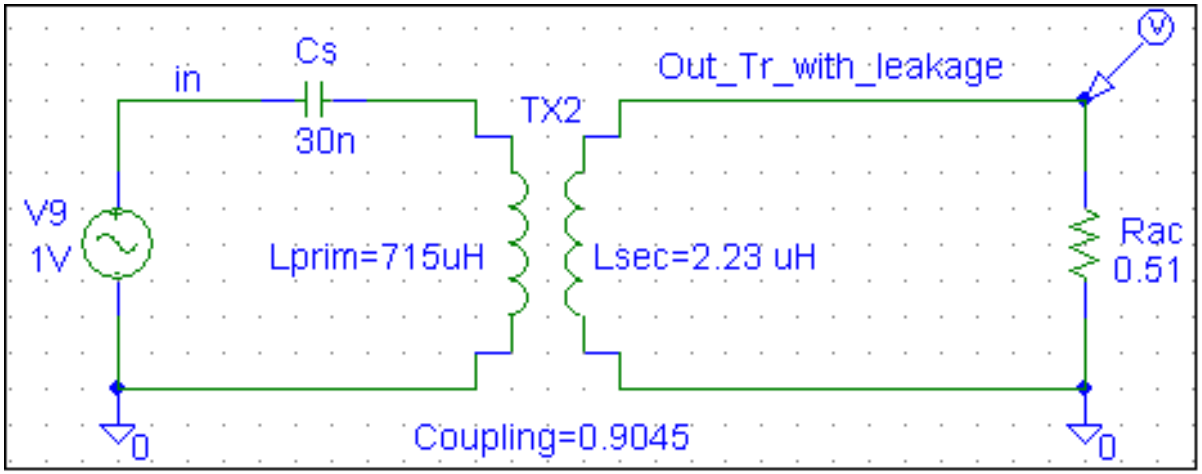
Calculated components of future integrated resonant tank:

Cs = 30 nF (2 x 15 nF)

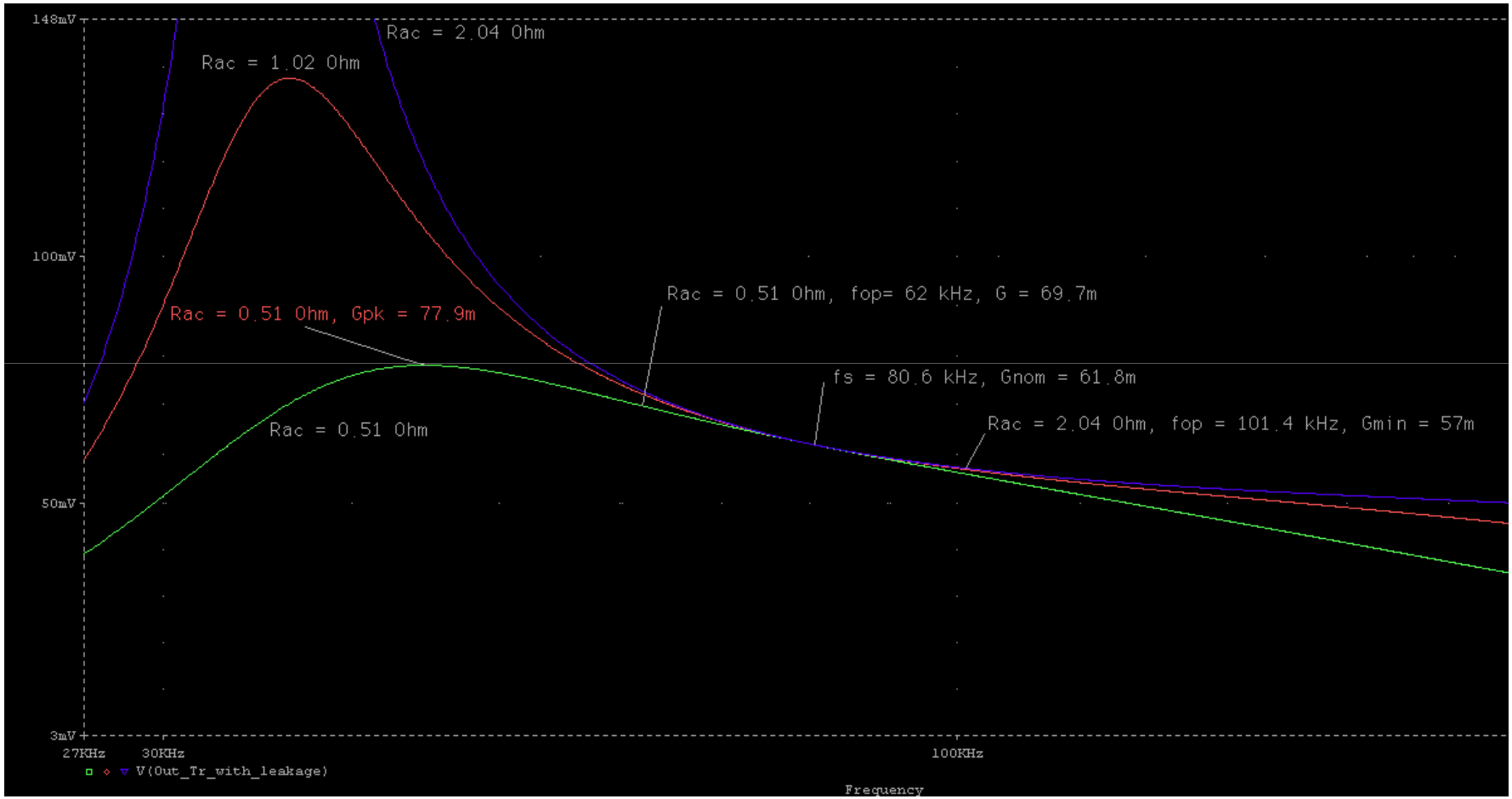
Llk_primary = 130 uH

Lprimary= 715 uH

Lsecondary= 2.23 uH

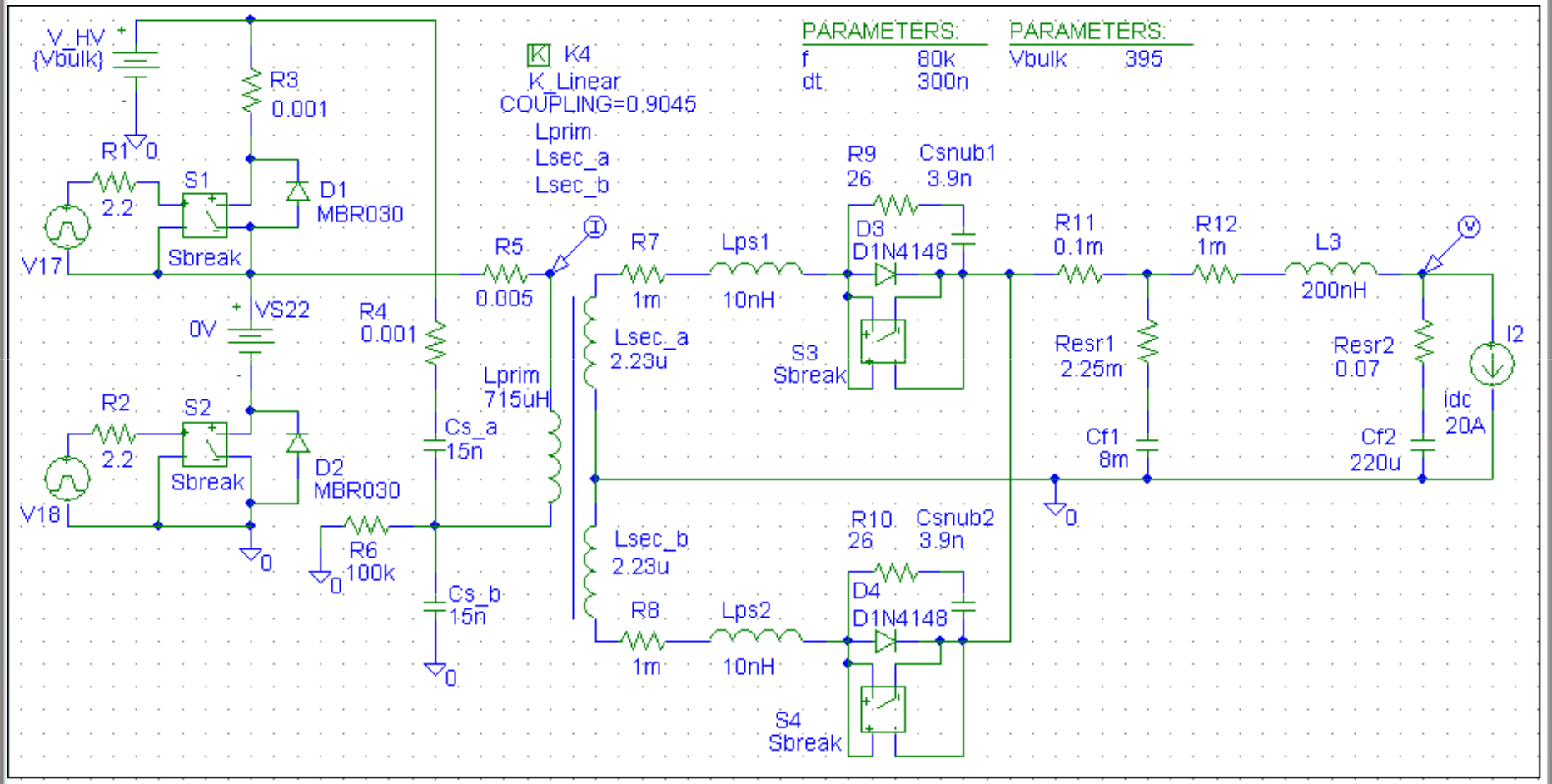


Step 10 – Final gain characteristic review



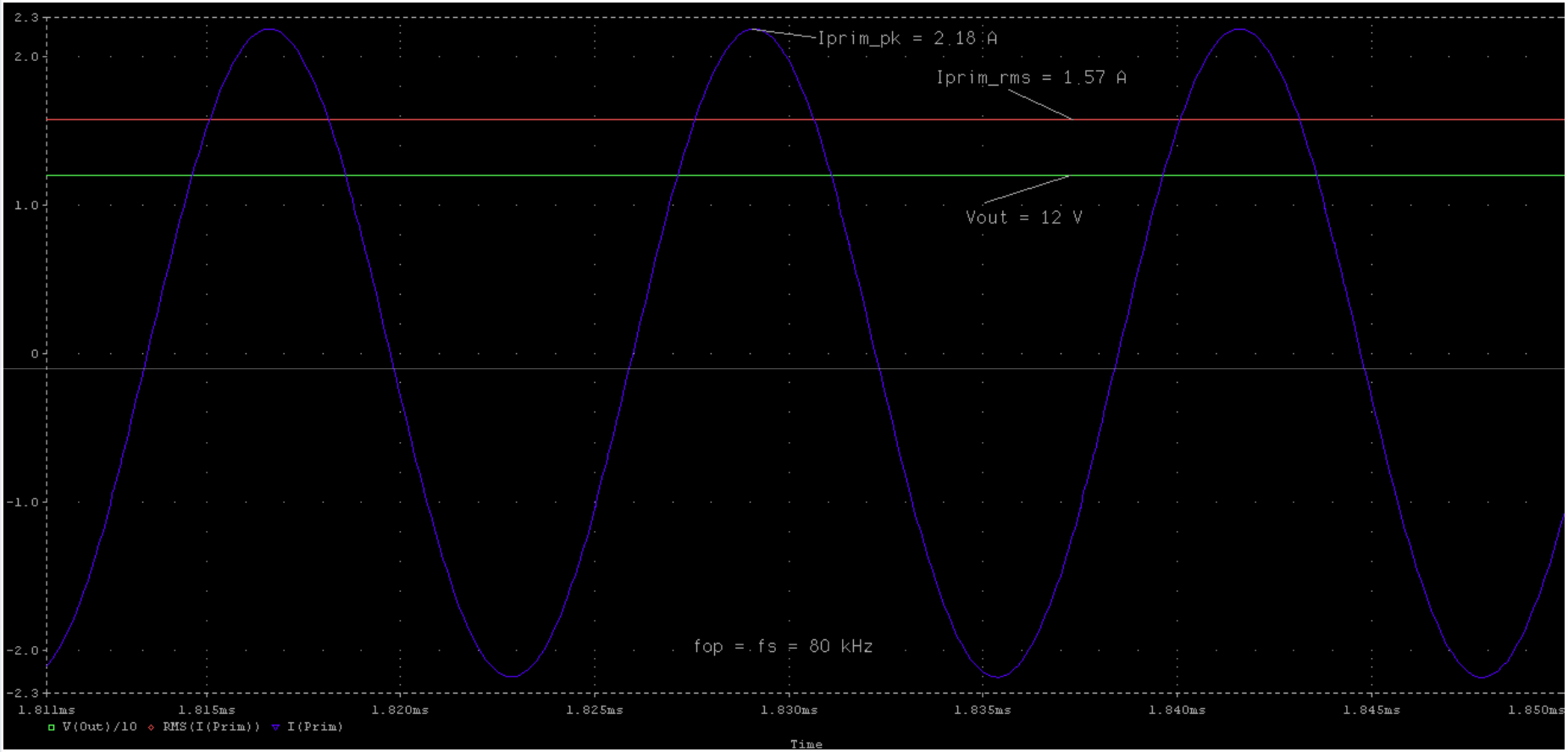
- Integrated resonant tank provides higher peak gain margin (~12 % above Gmax)

Step 11 – Transient simulation



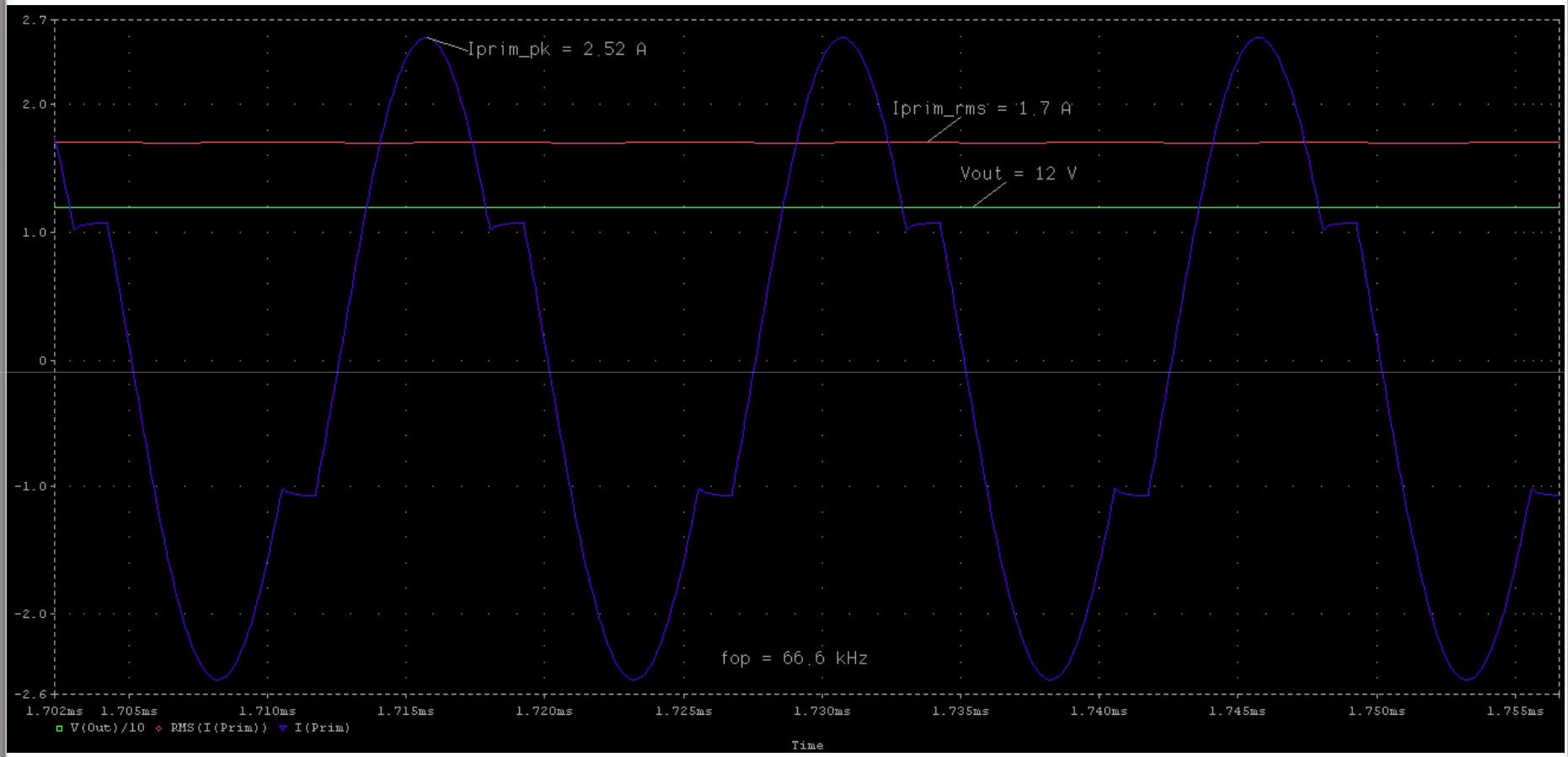
- Simple model for transient simulation using elementary simulator libraries

Step 11 – Transient simulation



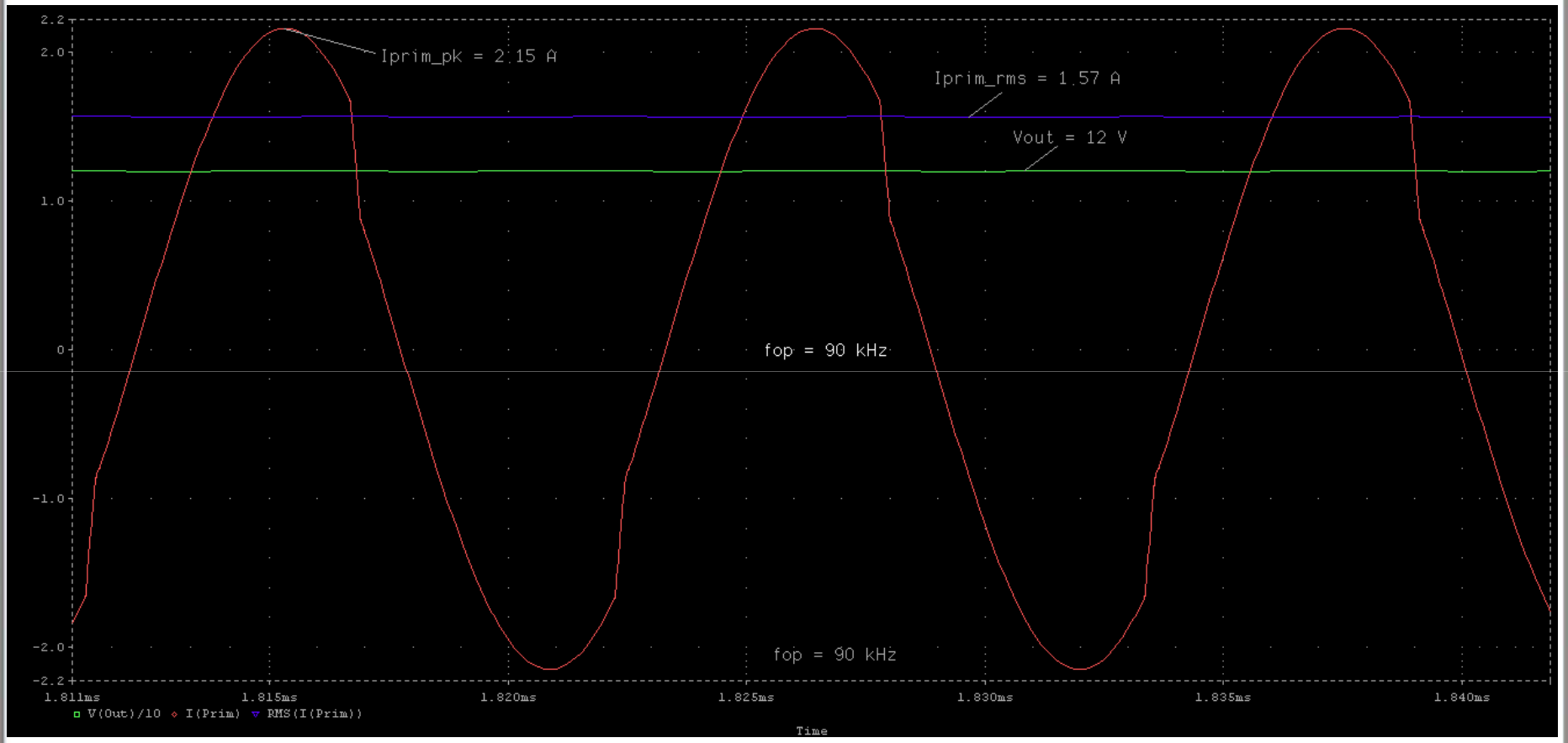
- Proposed resonant tank operates at fs for full load and nominal Vbulk conditions
- Ics_rms = 1.57 A can be measured more precisely

Step 11 – Transient simulation



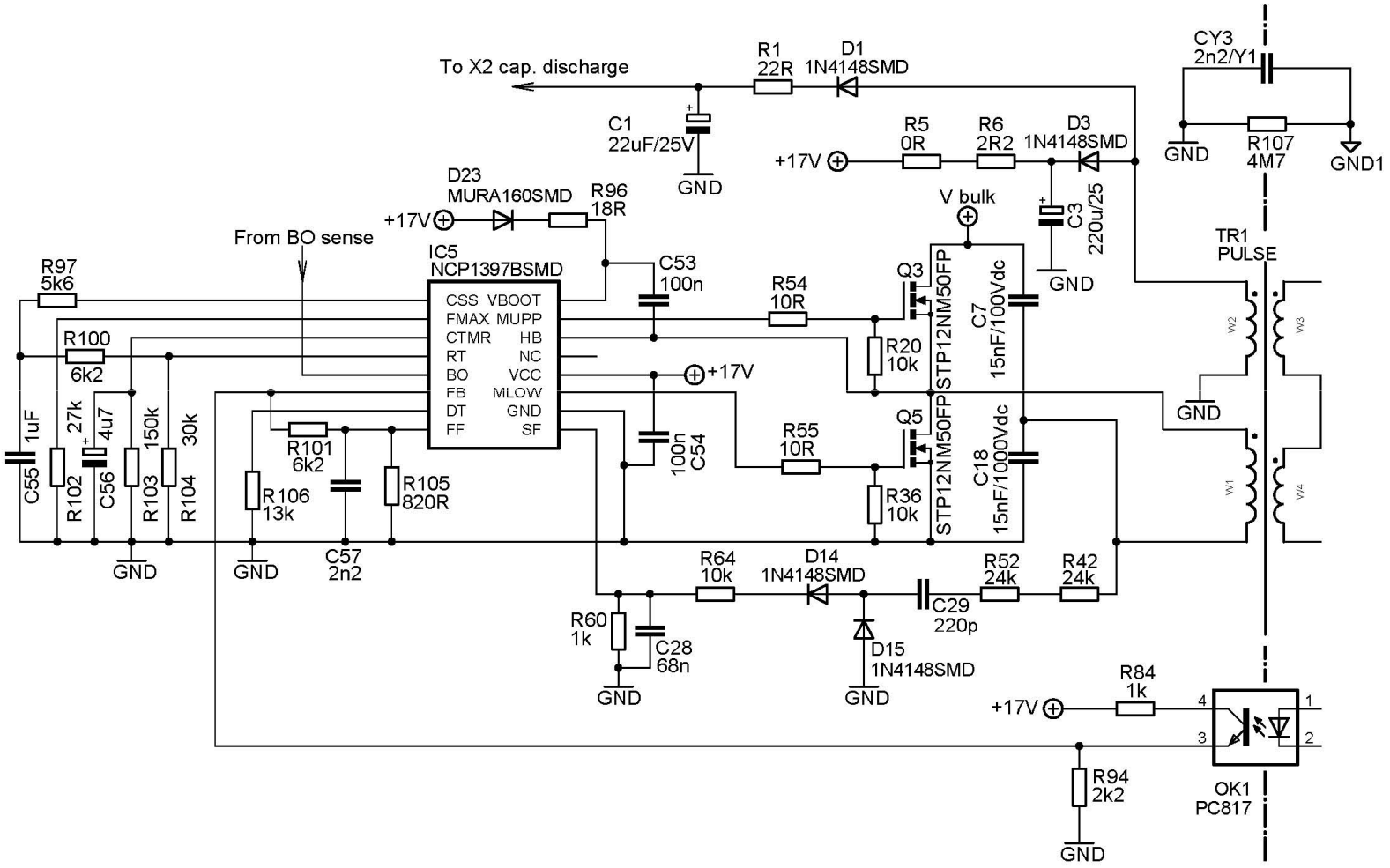
- Operating frequency has to drop to 66.6 kHz to maintain full load regulation for Vbulk = 350 Vdc

Step 11 – Transient simulation



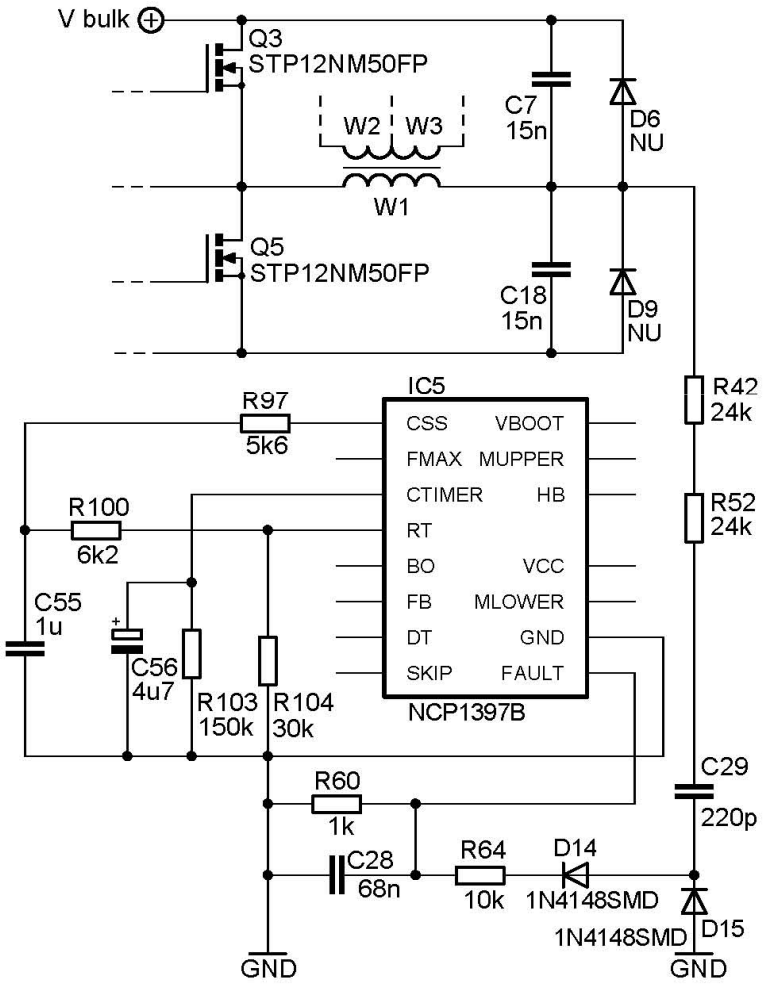
- Operating frequency has to increase to 90 kHz to maintain full load regulation for Vbulk = 425 Vdc

LLC stage primary side components design



- Typical NCP1397B connection with minimum component count

OCP network design



- Charge pump OCP sensing is used in consumer electronics due to cost reasons

- AC voltage on the resonant capacitor causes AC current through C29

- Current goes through D14 and causes voltage drop on R60 when upslope occurs on the Vcs voltage i.e. each half period only

- Charge pump sensor features natural delay as it delivers current information only during one switching half period

OCP network design

- Calculate or simulate primary RMS current during overload:

$$I_{Primary\_rms} \approx \sqrt{\frac{1}{8}\cdot\left(I_{out\_max}^{\ 2}\cdot\pi^2\cdot G_{nom}^{\ 2}+\frac{V_{bulk\_nom}^{\ 2}}{24\cdot L_m^{\ 2}\cdot f_{op\_ovld}^{\ 2}}\right)} = 1.68A$$

- Calculate resonant capacitor AC voltage during overload:

$$V_{Cs\_ac} = \frac{I_{Primary\_rms}}{2\cdot\pi\cdot f_{op\_ovld}\cdot C_s} = \frac{1.68}{2\cdot 3.14\cdot 78\cdot 10^3\cdot 30\cdot 10^{-9}} = 114Vac$$

- Calculate series limiting resistors and OCP charge pump capacitor value:

$$R_s = \frac{V_{Cs\_peak}}{I_{f\_limit}} = \frac{1\cdot 10^3}{20\cdot 10^{-3}} = 50k\Omega$$

$$C_{29} = \frac{1}{2\cdot\pi\cdot f_{op\_ovld}\cdot\sqrt{\left|2\cdot\left(\frac{V_{Cs\_ac}\cdot R_{60}}{\pi\cdot V_{ref\_faul}\cdot 0.9}-\frac{(R_{60}+R_{64})}{2}\right)^2-(R_{42}+R_{52})^2\right|}} = 214.6\,pF$$

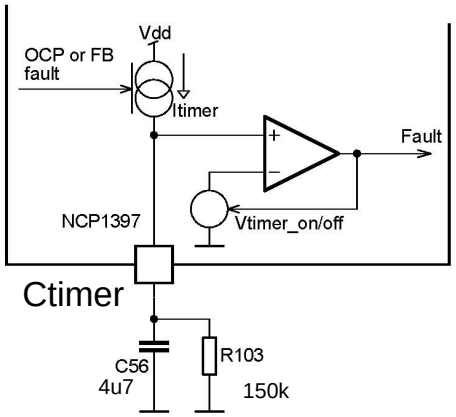
- Calculate filtering capacitor value and check power loss :

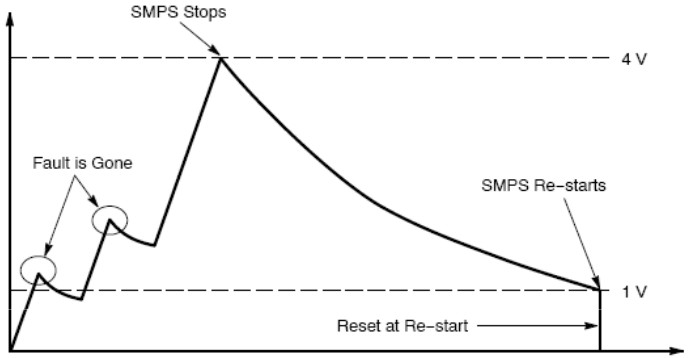
$$C_{28} = \frac{5}{f_{op\_ovld}\cdot R_{23}} = \frac{5}{78\cdot 10^3\cdot 1000} \approx 68nF$$

$$P_{Rs} = \left(\frac{\pi\cdot V_{ref\_fault}\cdot 0.9}{\sqrt{2}\cdot R_{60}}\right)^2\cdot R_s = 0.208W$$

Fault timer components selection

- NCP1397 uses cumulative fault timer that allows for fault and also auto-recovery periods adiustment





- Time to fault confirmation:

$$T_{fault} = -R_{103} \cdot C_{56} \cdot \ln\left(1 - \frac{V_{timer(on)}}{R_{103} \cdot I_{timer1}}\right) = -150 \cdot 10^3 \cdot 4.7 \cdot 10^{-6} \cdot \ln\left(1 - \frac{4}{150 \cdot 10^3 \cdot 175 \cdot 10^{-6}}\right) = 117ms$$

- Time to auto-recovery time:

$$T_{off} = R_{103} \cdot C_{56} \cdot \ln\left(\frac{V_{timer(on)}}{V_{timer(off)}}\right) = 150 \cdot 10^3 \cdot 4.7 \cdot 10^{-6} \cdot \ln\left(\frac{4}{1}\right) = 977ms$$

DT, Fmin, Fmax resistor values

- Use NCP1397 DT, Fmin and Fmax nomograms from DS or calculate based on below equations:

- Deadtime calculation

$$T_{DT} = 4.28 \cdot 10^{-8} + \left(R_{DT} \cdot 2.41 \cdot 10^{-11} \right)$$

- Fmin calculation based on Rdt and Rt

$$f_{\min} = \frac{1}{4.64 \cdot 10^{-10} \cdot R_t + 4.8 \cdot 10^{-11} \cdot R_{DT} + 8 \cdot 10^{-8}} - \frac{8.9 \cdot 10^{-7}}{R_t}$$

- Fmax calculation based on Rdt, Rt and Rfmax

$$f_{\max} = \frac{1}{\frac{7.3 \cdot 10^{-11} \cdot R_{f\max} \cdot R_t}{0.1 \cdot R_t + 0.157 \cdot R_{f\max}} + 4.8 \cdot 10^{-11} \cdot R_{DT} + 8 \cdot 10^{-8}} - \frac{8 \cdot 10^{7}}{R_{f\max}}$$

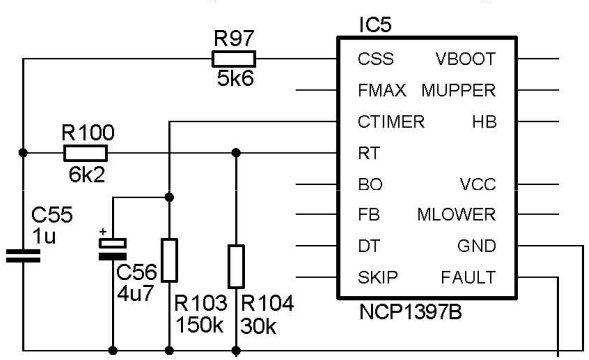
=> Values for our design: Rdt = 13 kΩ, Rfmin = 30 kΩ Rfmax = 27 kΩ

Note: Excel sheet available

Soft Start and frequency shift components

- R97 is used to slow down the frequency shift slope in order to overcome oscillations during slight overloading

- Startup frequency is given by the total resistance connected to Rt pin during application start:



$$R_{Rt\_start} = \frac{R_{104} \cdot (R_{97} + R_{100})}{R_{104} + R_{97} + R_{100}}$$

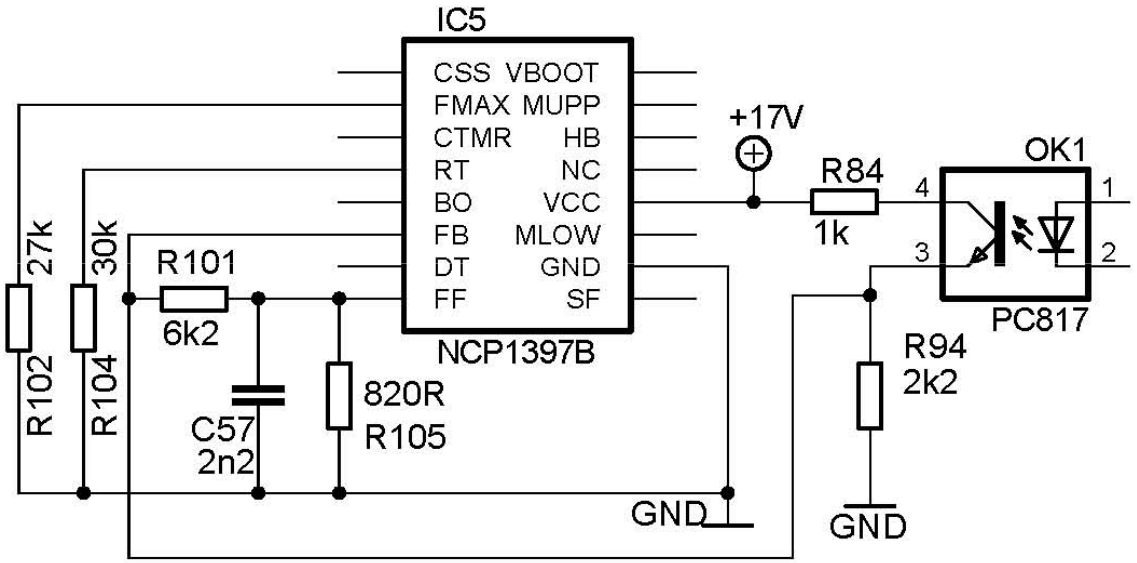
- RRrt_start value can be calculated from above equations or find in the Fmin vs. Rfmin nomogram. The value of R100 can be then calculated as:

$$R_{100} = \frac{R_{Rt\_start} \cdot R_{104} + R_{Rt\_start} \cdot R_{104} - R_{97} \cdot R_{104}}{R_{104} - R_{Rt\_start}} = 6.2k\Omega$$

- Soft Start capacitor value C55 = 1 uf has been used to provide SS time constant of ~ 6 ms (C55 - R100).

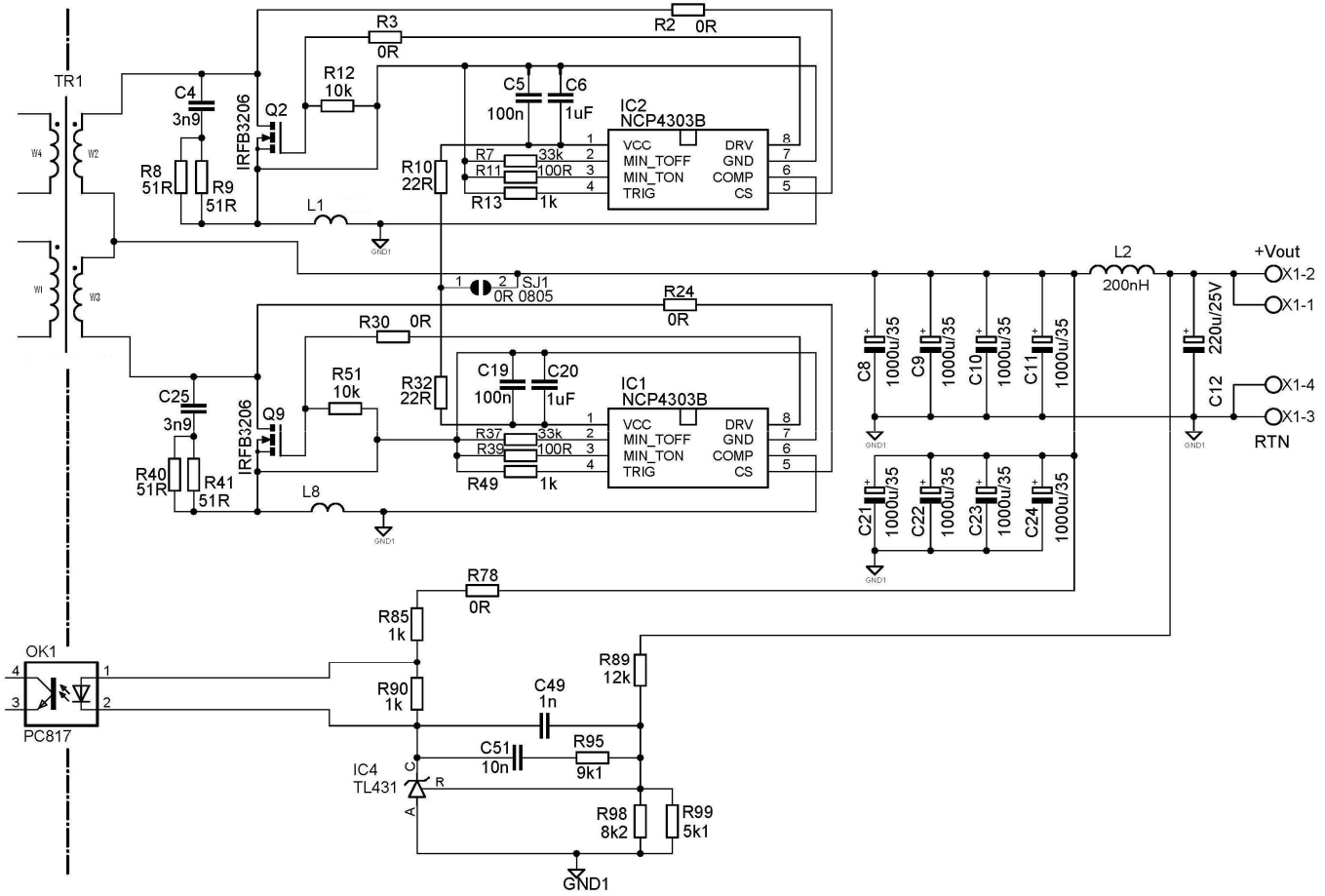
FB pin and skip mode components

- R84 and R94 values has been used as compromise between optocoupler pole position and light load consumption. R84 limits max. voltage on FB pin.



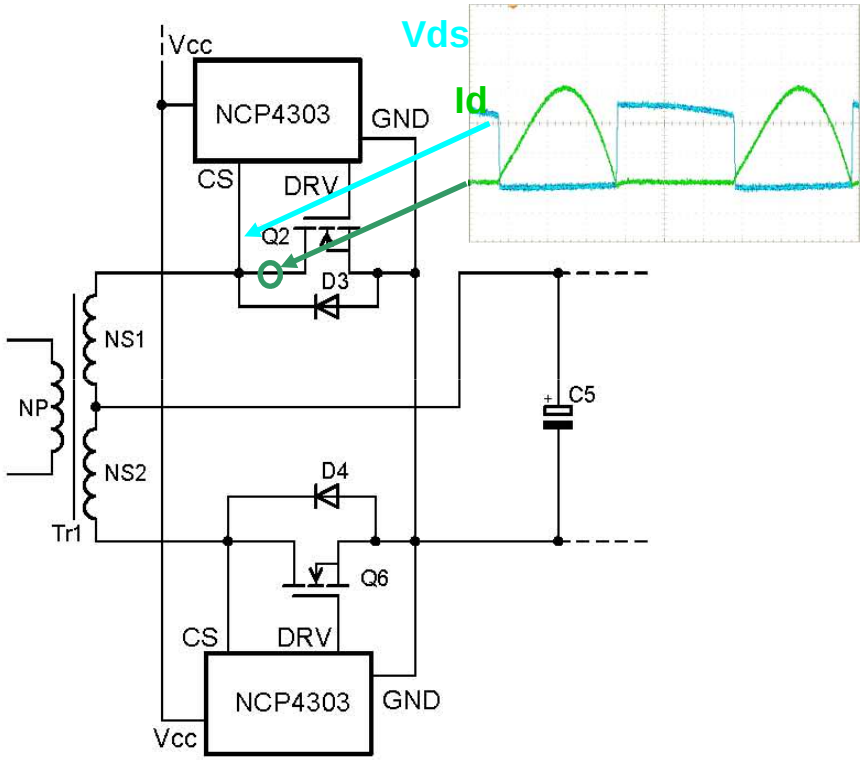
- FB pin voltage overshoot above 5.1 V during skip is given by FB loop response and Skip pin divider R101, R105. The higher overshoot is the longer time SMPS stays in skip mode – reducing switching losses.

Secondary side design



- SR with parasitic inductance compensation is used to maximize efficiency when SR MOSFETs in TO220 package are used

SR design



SR controllers consumption and gate drive losses in standby will affect light load efficiency

SR MOSFET losses:

- Conduction losses

$$P_{COND} = \left(Iout \cdot \frac{\pi}{4} \right)^2 \cdot R_{ds\_on@Vgs\_clamp}$$

=> Rds_on selection

- Gate drive losses

$$P_{DRV} = Vcc \cdot V_{clamp} \cdot C_{g\_ZVS} \cdot f_{sw\_max}$$

=> gate charge selection

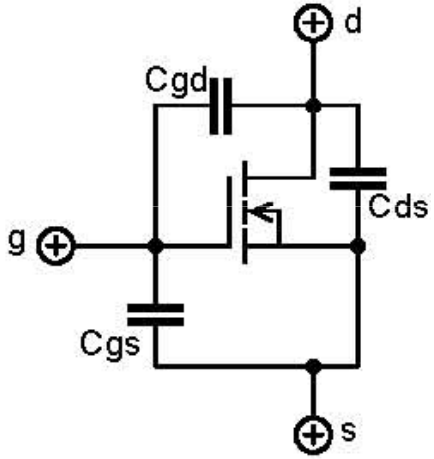
- Body diode losses

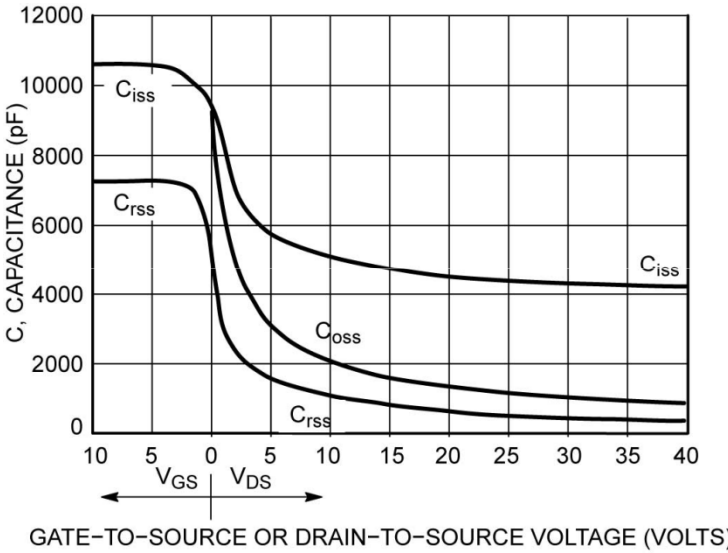
$$P_{body} = \frac{I_{out}}{2} \cdot V_f + \left(I_{out} \cdot \frac{\pi}{4} \right)^2 \cdot R_{dyn}$$

=> Affected by diode Vf and dynamic resistance

SR design – MOSFET selection

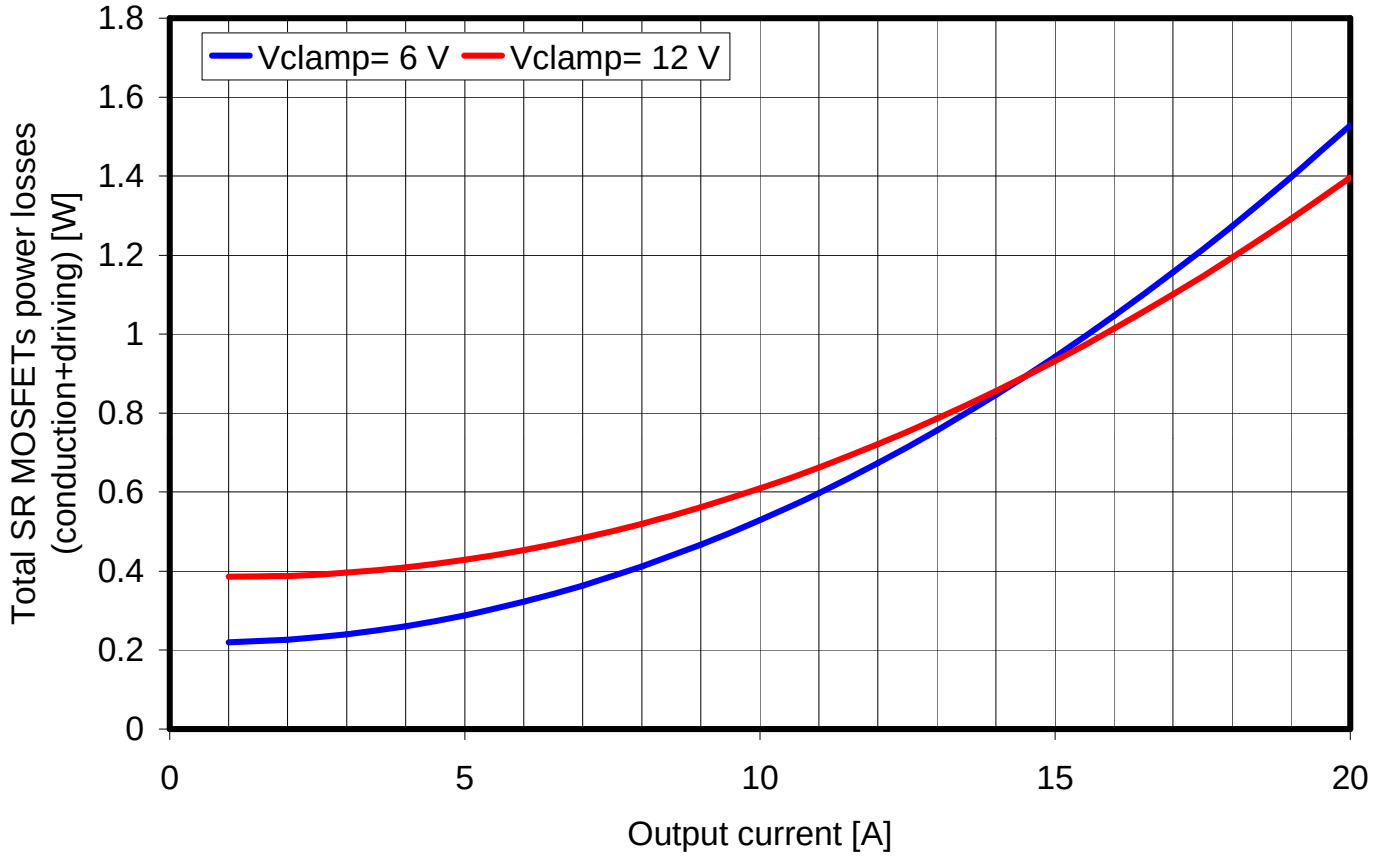
- SR MOSFET works under ZVS conditions
  => Gate charge is given by Ciss capacitance (Cgs+Cgd) and gate voltage



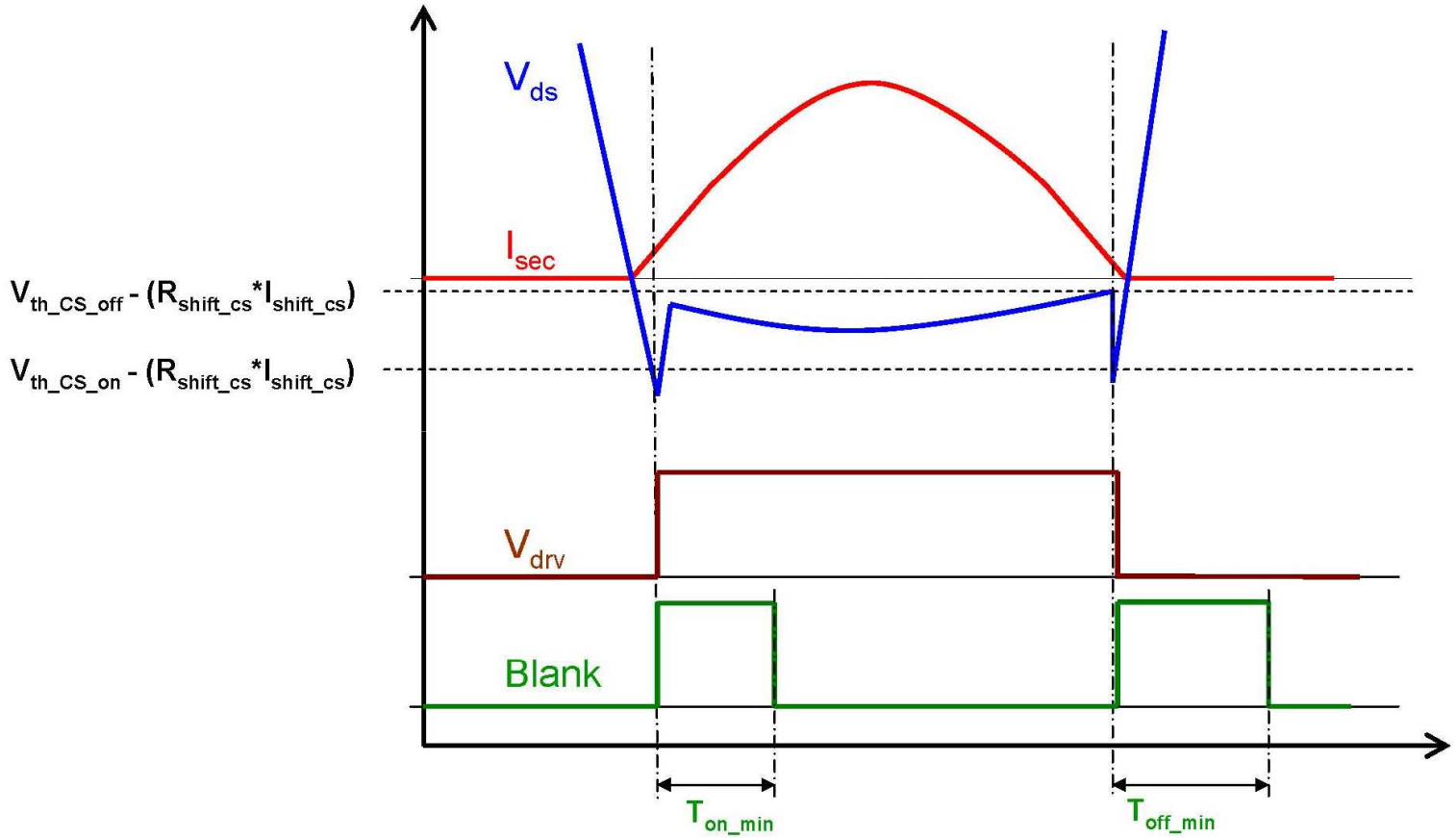


MOSFET type	Qg @ 5 V [nC]	Qg @ 12 V [nC]	Rds_on @ 5V [mΩ]	Rds_on @ 12V [mΩ]
IPP015N04N	101	245	1.9	1.2
FDP047AN	39	96	5.8	4
IRFB3206	**55**	**133**	**3.3**	**2.3**

Lpar compensation

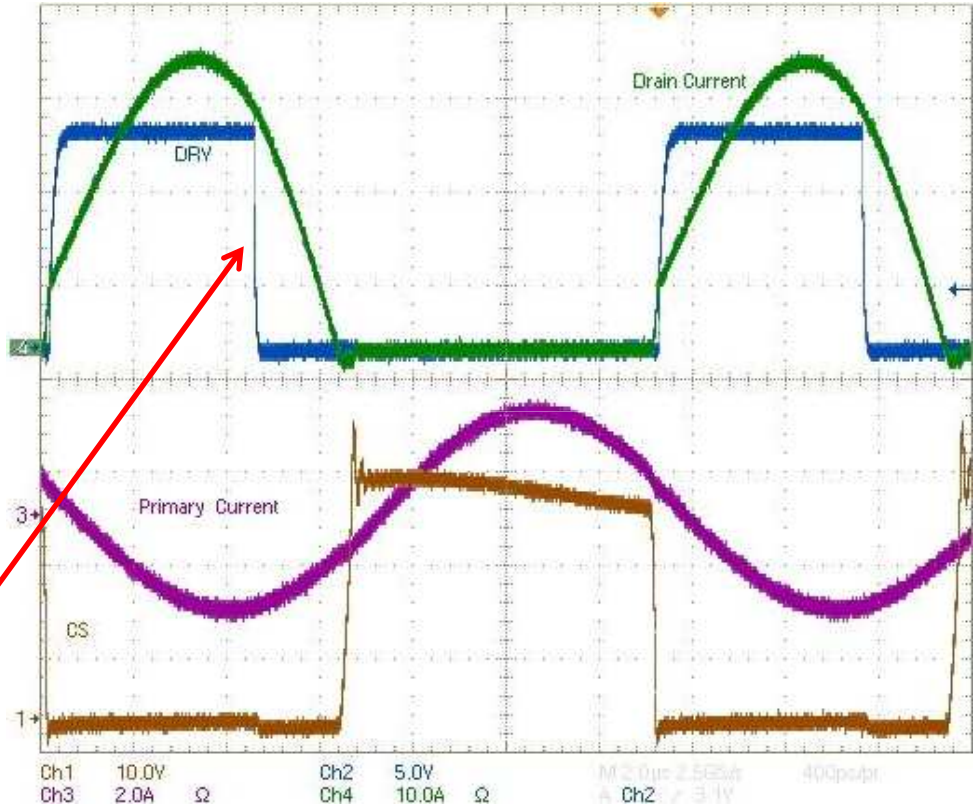


NCP4303 Zero Current Detection



- The Vcs_off threshold is 0 mV in case no resistor is used in CS
- Maximum conduction period of SR MOSFET is desirable for max efficiency

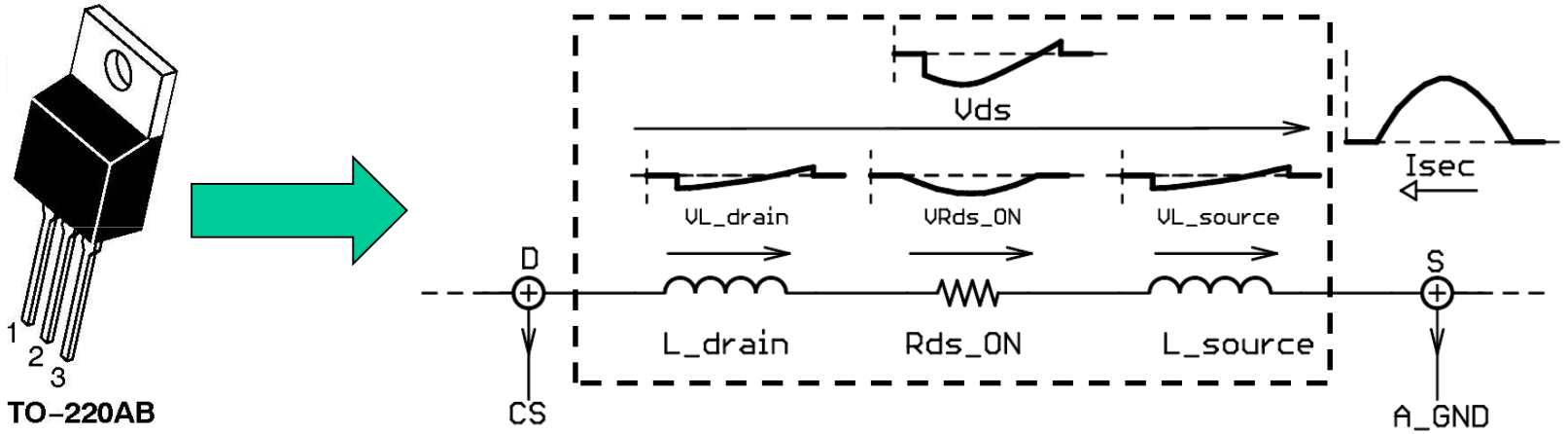
SR MOSFET parasitic inductance impact



- The SR MOSFET conduction time is shortened when MOSFET in TO220 package is used

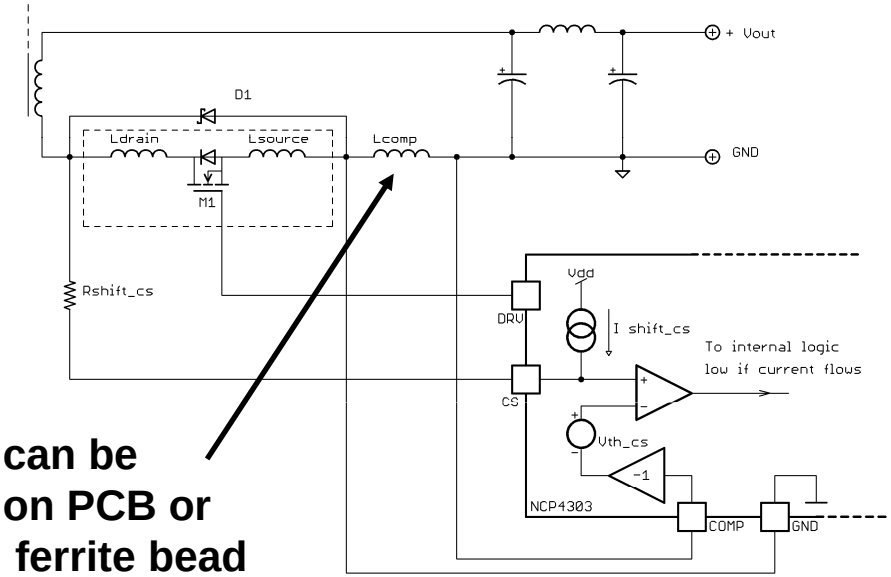
SR MOSFET parasitic inductance impact

- TO220 package is mostly used due to cost and also simple soldering process

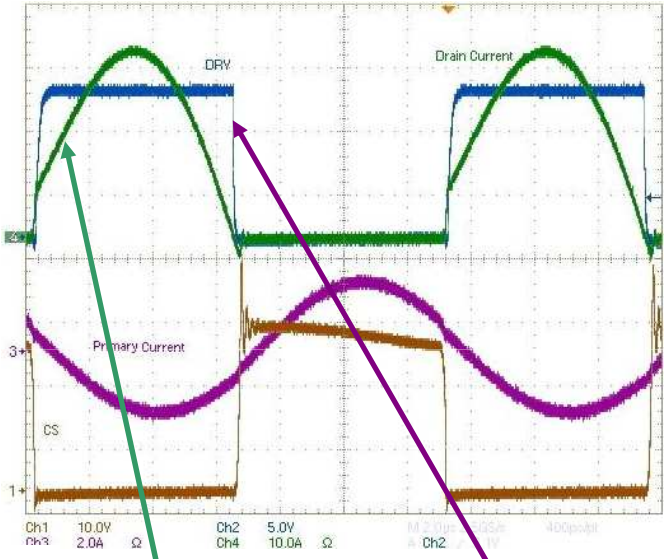


- Parasitic inductances L_{drain} and L_{source} create voltage drop that is proportional to the secondary current $I_{sec(t)}$ derivative.
- The V_{ds} voltage reaches zero level prior secondary current
- SR controller detects zero voltage in the time the secondary current has still significant level => efficiency degradation
- Higher frequency or $dI_{sec(t)}/dt$ is, higher efficiency drop will be

NCP4303 parasitic inductance compensation

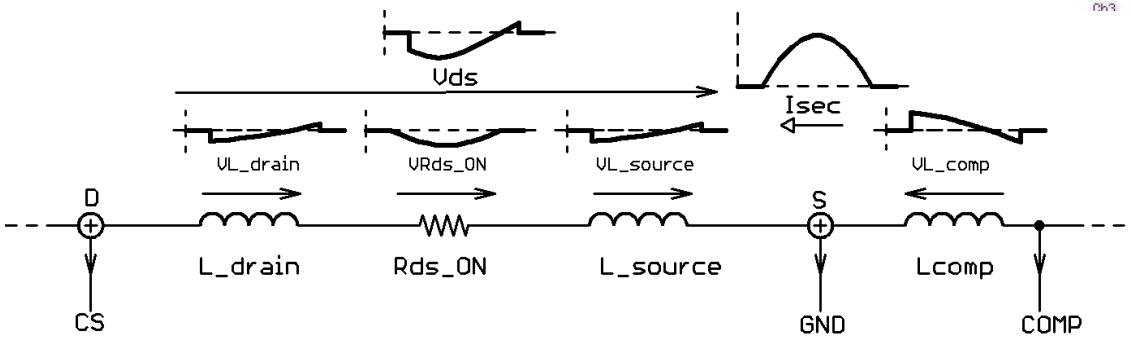


L_{comp} can be done on PCB or using ferrite bead



Secondary current

SR MOSFET gate voltage



SR MOSFET conduction period is maximized when NCP4303 implemented with compensation Inductance

SR MOSFET driver power dissipation

- Vcc related power dissipation

$$P_{Icc} = V_{cc} \cdot I_{cc} = 35mW$$

- Driving losses related power dissipation

$$P_{DRV\_IC} = \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{clamp}{}^2 \cdot f_{SW} \cdot \left(\frac{R_{drv\_low\_eq}}{R_{drv\_low\_eq} + R_{g\_int}} \right) + C_{g\_ZVS} \cdot V_{clamp} \cdot f_{SW} \cdot (V_{cc} - V_{clamp}) + \frac{1}{2} \cdot C_{g\_ZVS} \cdot V_{clamp}{}^2 \cdot f_{SW} \cdot \left(\frac{R_{drv\_high\_eq}}{R_{drv\_high\_eq} + R_{g\_int}} \right) = 76mW$$

- DIE temperature related to above losses

$$T_{DIE} = (P_{DRV\_IC} + P_{Icc}) \cdot R_{\theta J-A} + T_A = (0.076 + 0.035) \cdot 180 + 60 = 80^{o}C$$

SR MOSFET snubbers

- Snubber is needed to suppress voltage ringing

$$R_{snubber} = \sqrt{\frac{L_{\sec,leak}}{C_{oss}}} \qquad C_{snubber} \approx 3 \rightarrow 4 \cdot C_{oss}$$

Minimum Ton and Toff blanking times

$$R_{T\_on\_\min} = \frac{T_{on\_\min} - 4.66 \cdot 10^{-8}}{9.82 \cdot 10^{-11}} = \frac{1.1 \cdot 10^{-6} - 4.66 \cdot 10^{-8}}{9.82 \cdot 10^{-11}} \approx 11k\Omega$$

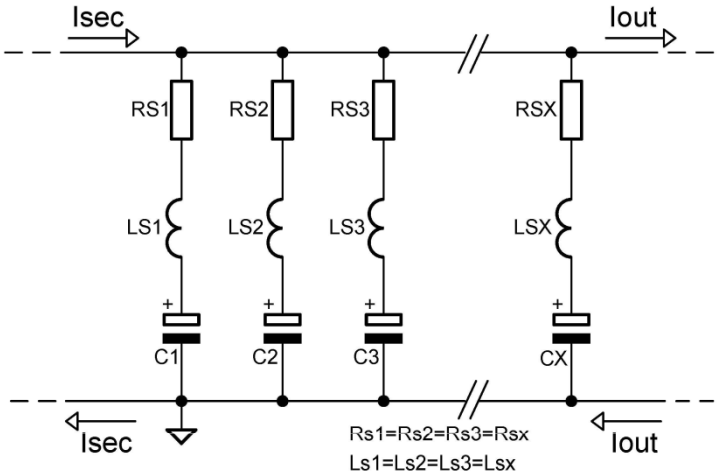
$$R_{T\_off\_\min} = \frac{T_{off\_\min} - 5.4 \cdot 10^{-8}}{9.56 \cdot 10^{-11}} = \frac{3.9 \cdot 10^{-6} - 5.4 \cdot 10^{-8}}{9.56 \cdot 10^{-11}} \approx 39k\Omega$$

Secondary filtering capacitor

- Filtering capacitor RMS current in LLC:

$$I_{Cf\_RMS} = I_{out\_nom} \cdot \sqrt{\frac{\pi^2}{8} - 1} = 20 \cdot 0.483 = 9.7A$$

= > 8 x 1mF/35 V to be used



- ESR related ripple:

$$V_{Cf\_ripple\_pk-pk} = ESR \cdot I_{rect\_peak} = 2.2 \cdot 10^{-3} \cdot \frac{\pi}{2} \cdot 20 = 69mV$$

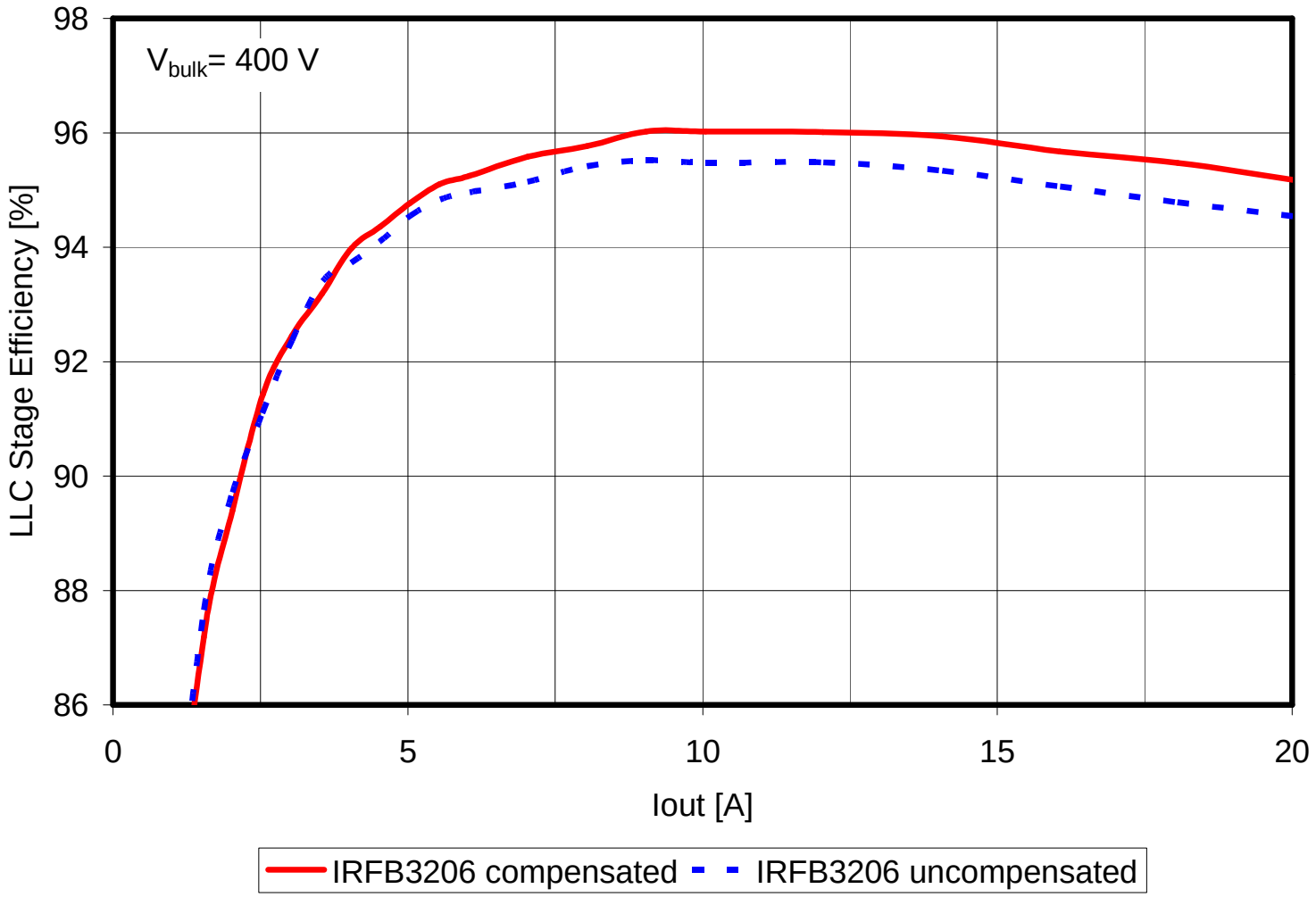
- Capacitance related ripple:

$$V_{out\_ripple\_cap\_pk-pk} = \frac{I_{out\_nom}}{2 \cdot \sqrt{3} \cdot \pi \cdot f_{op\_nom} \cdot C_f} \cdot (\pi - 2) = \frac{20}{2 \cdot \sqrt{2} \cdot \pi \cdot 80 \cdot 10^3 \cdot 8 \cdot 10^{-3}} \cdot (\pi - 2) = 4mV$$

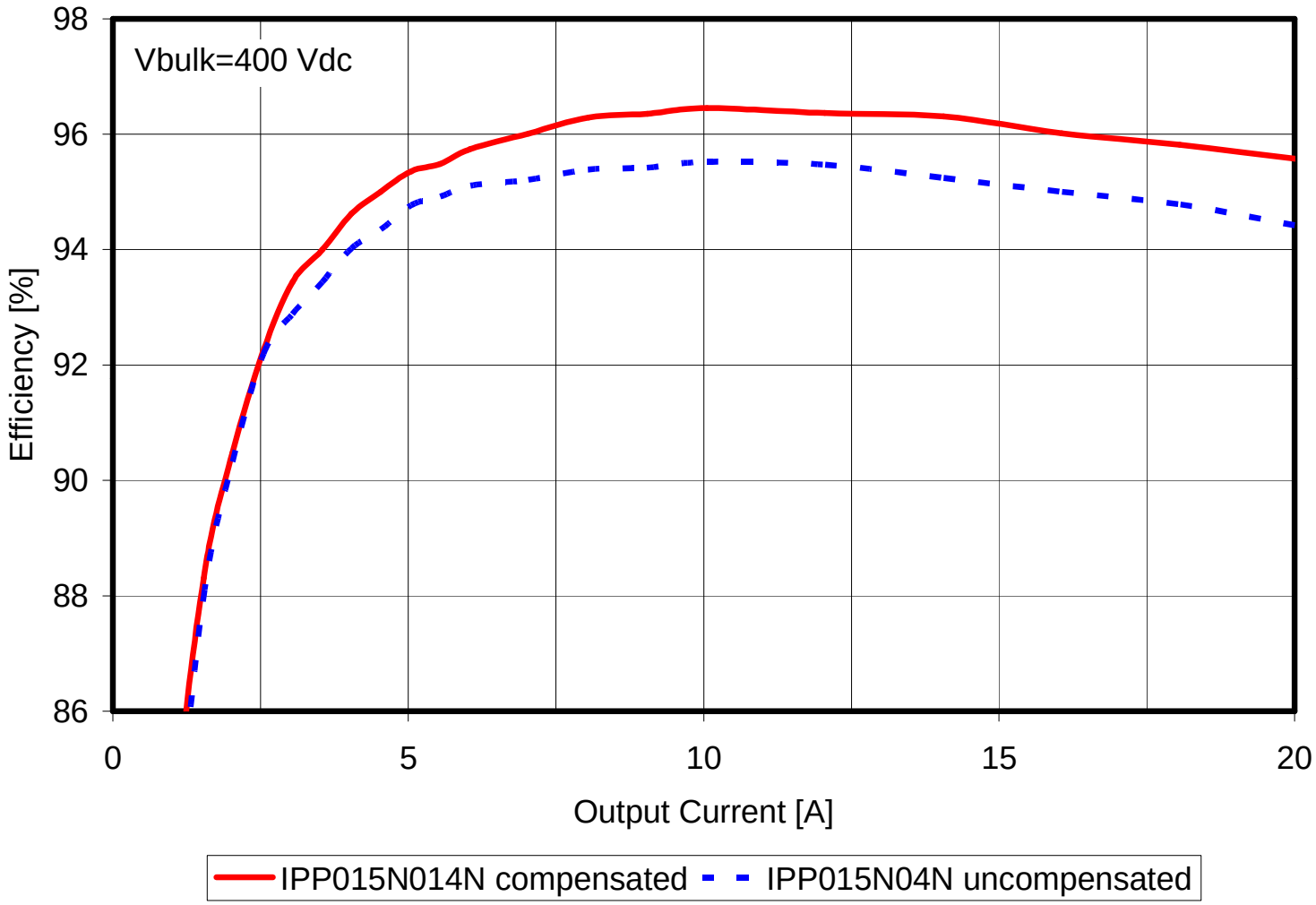
- Filtering capacitor losses:

$$P_{Cf\_ESR} = \left(I_{out\_nom} \cdot \sqrt{\frac{\pi^2}{8} - 1} \right)^2 \cdot ESR = \left(20 \cdot \sqrt{\frac{\pi^2}{8} - 1} \right)^2 \cdot 2.25 \cdot 10^{-3} = 0.21W$$

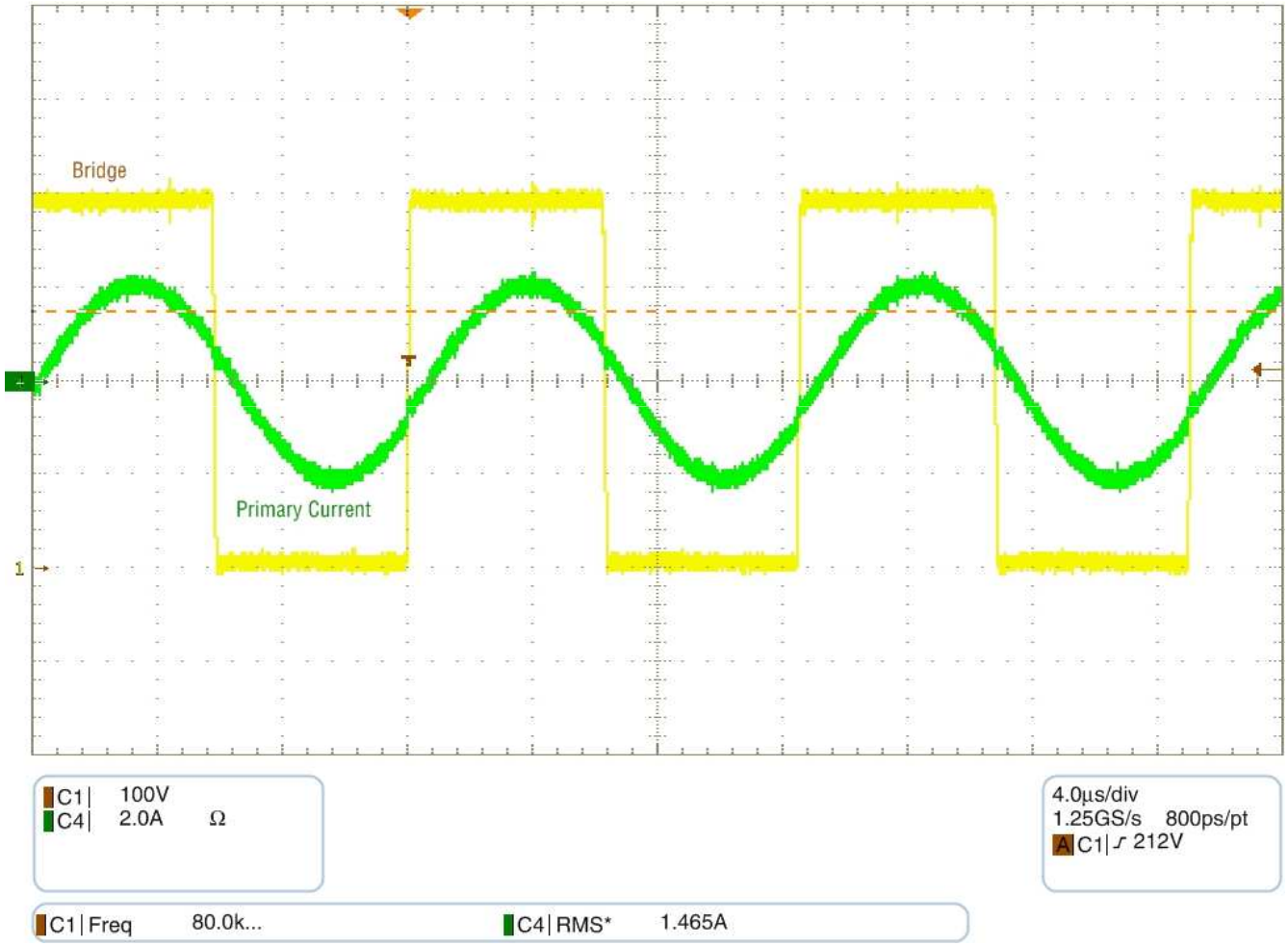
Efficiency results



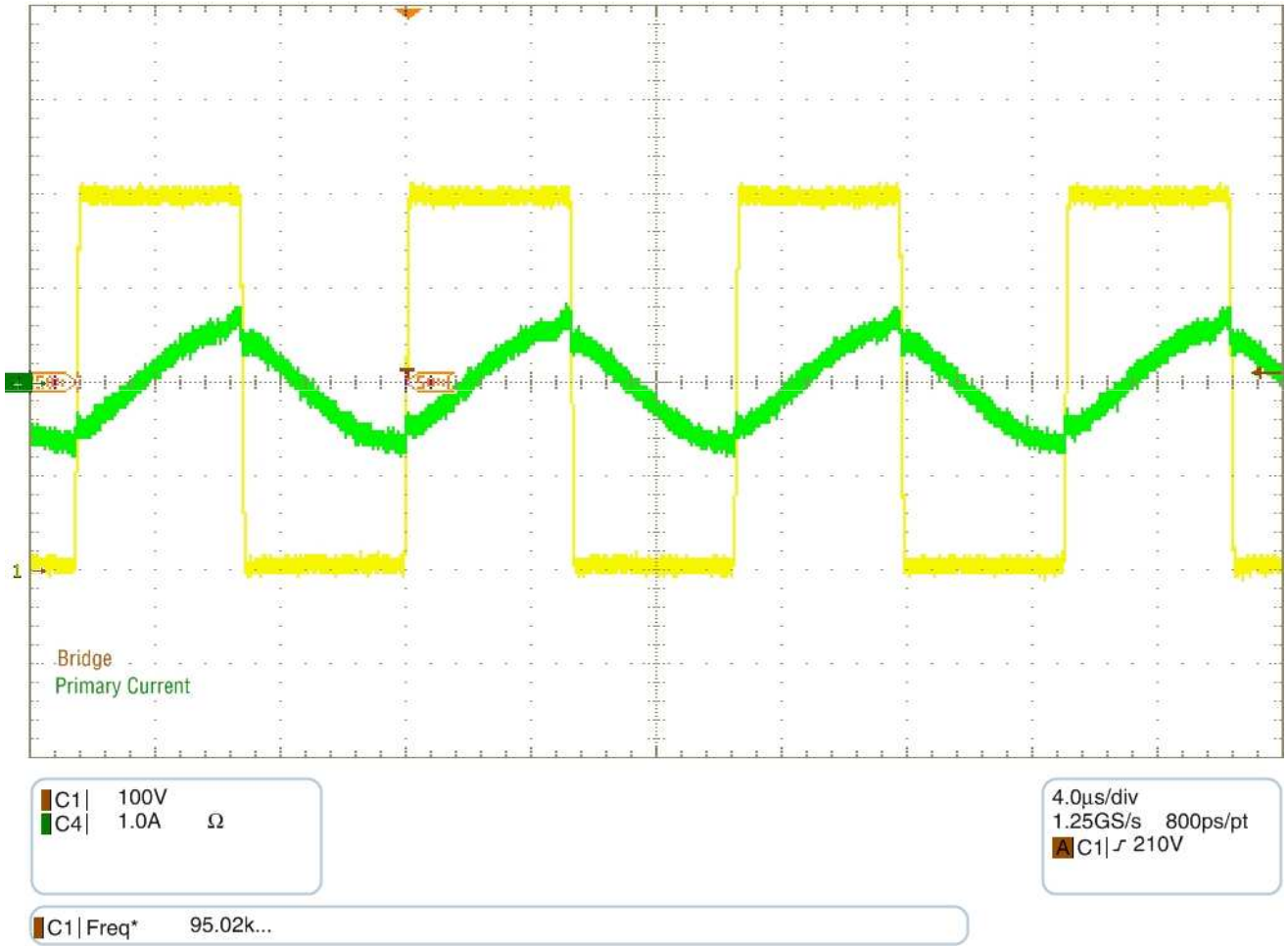
Efficiency results



Operating wfms. – Full load operation



Operating wfms. – light load (Iout=2.5 A)



Thank you for your attention!

Backup slides!

Operating states of the LLC converter

Discrete resonant tank solution

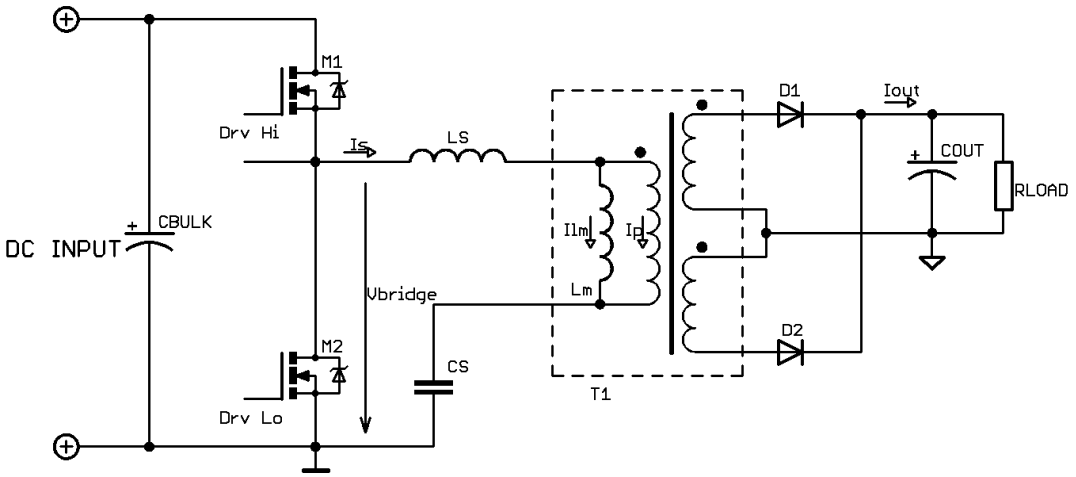
Two resonant frequencies can be defined:

$$F_s = \frac{1}{2 \cdot \pi \cdot \sqrt{C_s \cdot L_s}}$$

$$F_{min} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_s \cdot (L_s + L_m)}}$$

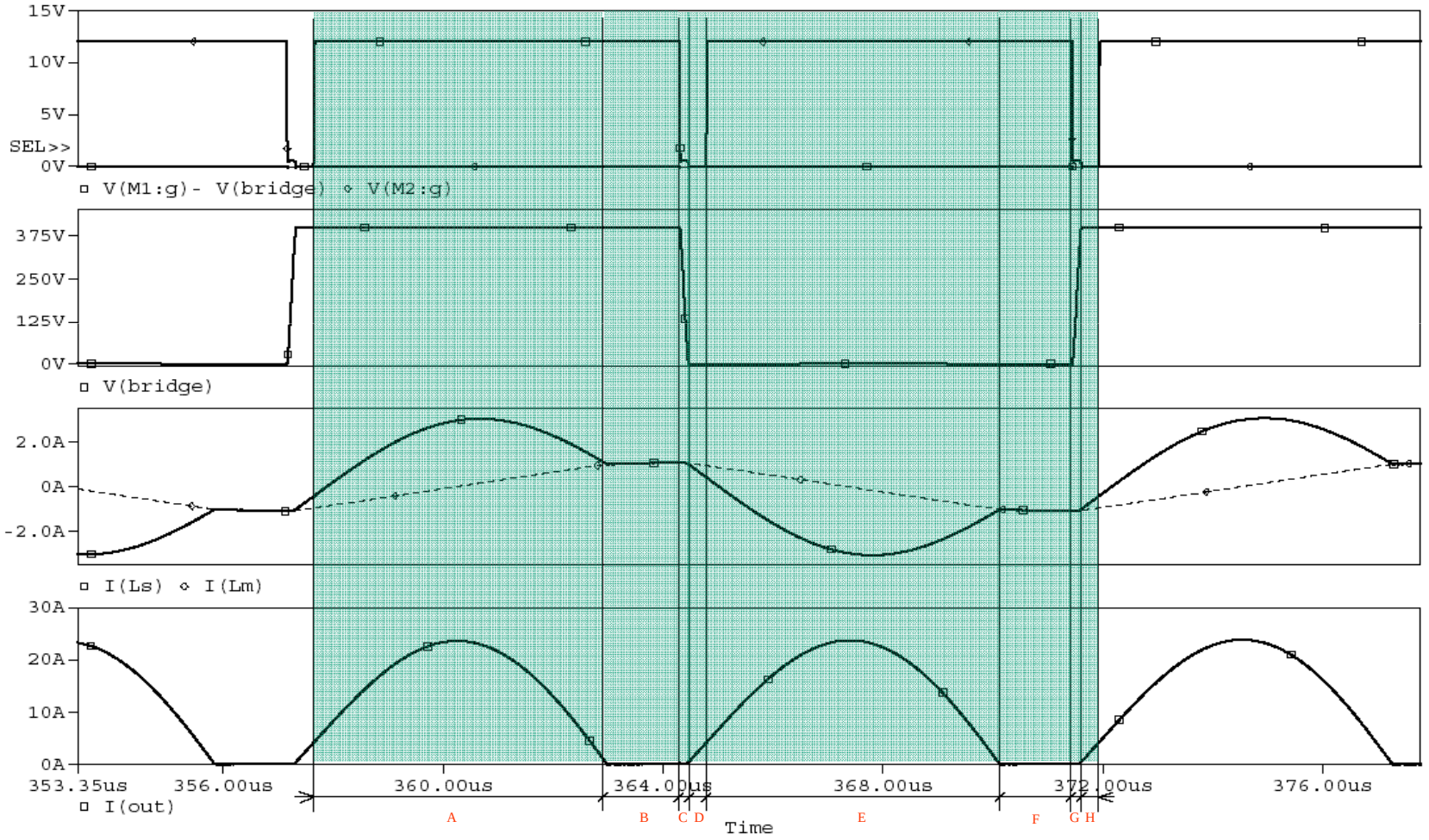
LLC converter can operate:

a) between F_{min} and F_s
b) direct in F_s
c) above F_s
d) between F_{min} and F_s - overload
e) below F_{min}



Operating states of the LLC converter – Discrete resonant tank solution:

A) Operating waveforms for $f_{min} < f_{op} < f_s$



Operating states of the LLC converter – Discrete resonant tank solution:

Operating intervals explanation – $f_{min} < f_{op} < f_s$:

A - Switch M1 has been turned ON (ZVS) and conducts together with secondary diode D1, primary current has sinusoidal wave shape because the Cs and Ls form series resonant circuit, Lm doesn't participate in the resonance now because it is clamped by the output impedance. Diode D1 current is nearly sinusoidal with a slight distortion that is given by the primary magnetizing current that flows into Lm. Energy is taken from bulk.

B - Secondary current reached zero and corresponding diode D1 has been closed (ZCS), resonant circuit has therefore been reconfigured to Cs - (Ls+Lm), primary current further increases but with slighter slope while accumulating energy in the Lm and Ls. Energy is taken from bulk.

C - Switch M1 has been turned OFF, energy stored in the Lm and Ls prepares ZVS condition for opposite switch M2 – overcharges the total parasitic capacitance on the bridge and opens M2 body diode. Energy is supplied by Ls and Lm.

D - M2 body diode conducts current until M2 is turned ON by the controller. Diode D2 starts to conduct. Energy is supplied by Ls and Lm until Is = 0. One part of the Lm+Ls energy holds ZVS for M2 and the other part goes to the output.

E - Switch M2 has been turned ON (ZVS) and conducts together with secondary diode D2, primary current has sinusoidal wave shape because the Cs and Ls form series resonant circuit, Lm doesn't participate in the resonance now because it is clamped by the output impedance. Diode D2 current is nearly sinusoidal with a slight distortion that is given by the primary magnetizing current that flows into Lm. Energy is taken from Cs.

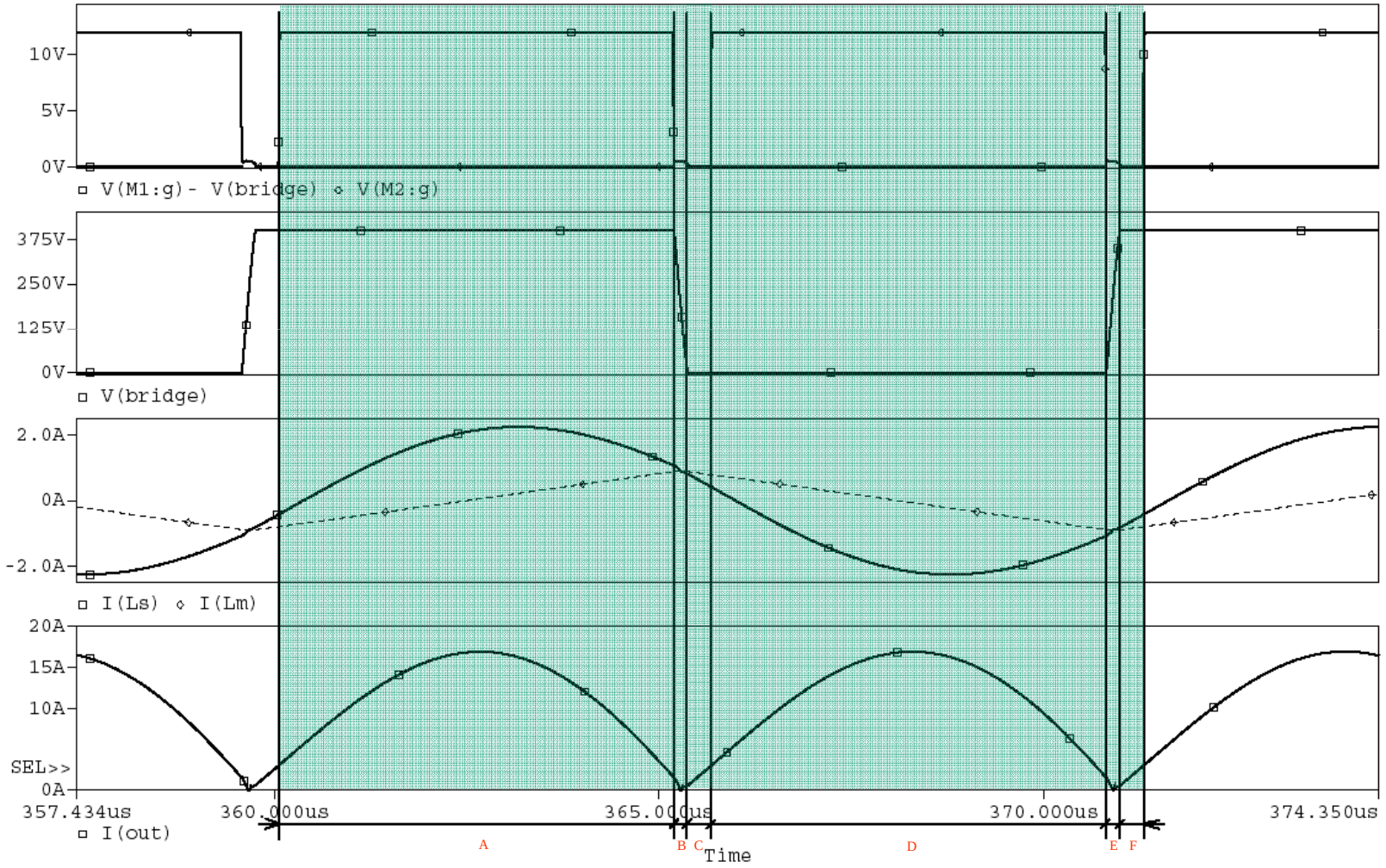
F - Secondary current reached zero and corresponding diode D2 has been closed (ZCS), resonant circuit has therefore been reconfigured to Cs - (Ls+Lm), primary current further increases but with slighter slope while accumulating energy in the Lm and Ls. Energy is taken from Cs.

G - Switch M2 has been turned OFF, energy stored in the Lm and Ls prepares ZVS condition for opposite switch M1 – overcharges the total parasitic capacitance on the bridge and opens M1 body diode. Energy is supplied by Ls and Lm.

H – M1 body diode conducts current until M1 is turned ON by the controller. Diode D1 starts to conduct. Energy is supplied by Ls and Lm until Is = 0. One part of the Lm+Ls energy holds ZVS for M1 and the other part goes to the output.

Operating states of the LLC converter – Discrete resonant tank solution:

b) Operating waveforms for $f_{op} = f_s$



Operating states of the LLC converter – Discrete resonant tank solution:

Operating intervals explanation – $f_{op} = f_s$:

A - Switch M1 has been turned ON (ZVS) and conducts together with secondary diode D1, primary current has sinusoidal wave shape because the Cs and Ls form series resonant circuit, Lm doesn't participate in the resonance now because it is clamped by the output impedance. Diode D1 current is nearly sinusoidal with a slight distortion that is given by the primary magnetizing current that flows into Lm. Energy is taken from bulk. Diode D1 current reaches zero in the end of this interval (ZCS).

B - Switch M1 has been turned OFF, energy stored in the Lm and Ls prepares ZVS condition for opposite switch M2 – overcharges the total parasitic capacitance on the bridge and opens M2 body diode. Energy is supplied by Ls and Lm. Diode D2 starts to conduct.

C - M2 body diode conducts current until M2 is turned ON by the controller. Diode D2 conducts. Energy is supplied by Ls and Lm until Is = 0. One part of the Lm+Ls energy holds ZVS for M2 and the other part goes to the output.

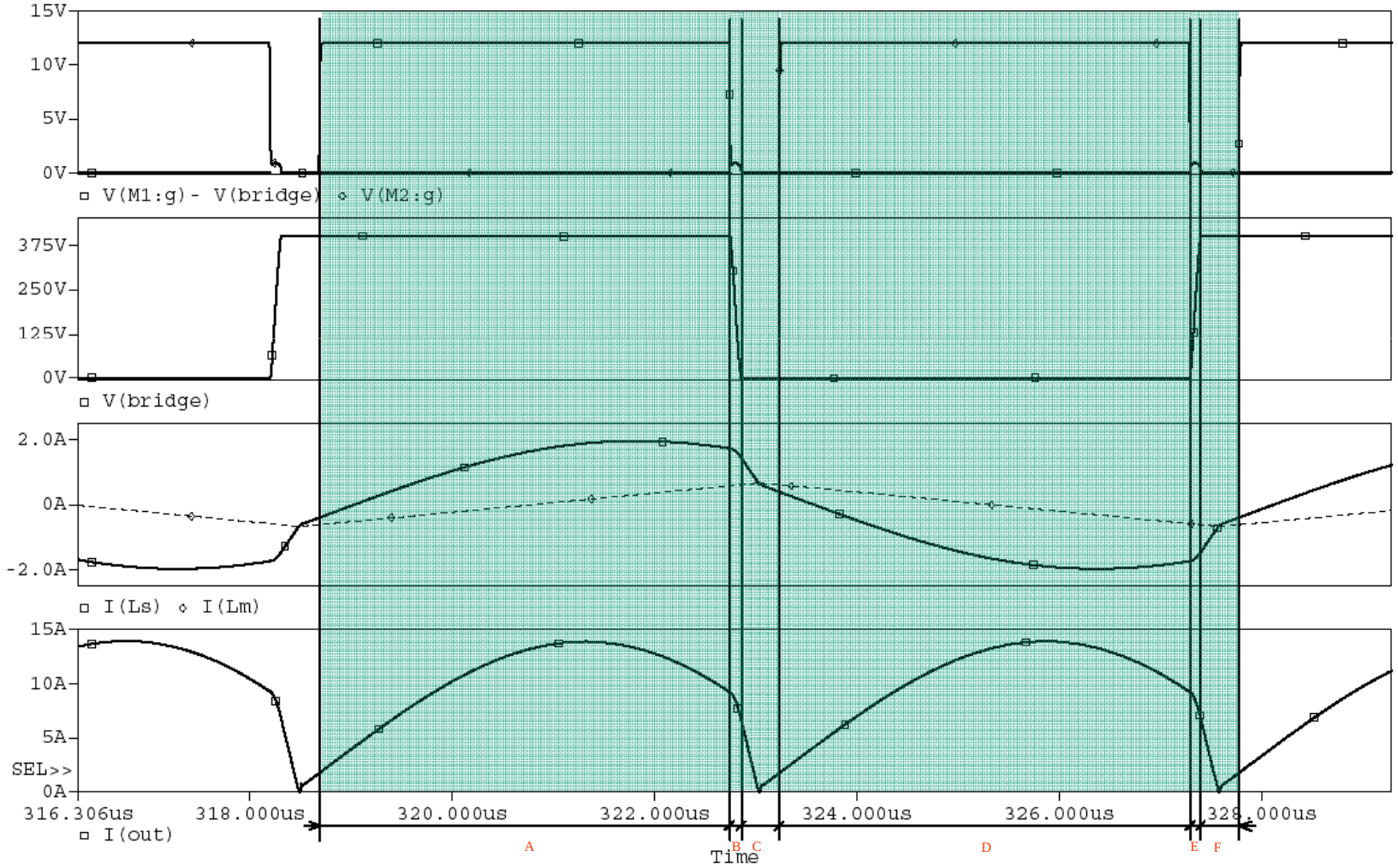
D - Switch M2 has been turned ON (ZVS) and conducts together with secondary diode D2, primary current has sinusoidal wave shape because the Cs and Ls form series resonant circuit, Lm doesn't participate in the resonance now because it is clamped by the output impedance. Diode D2 current is nearly sinusoidal with a slight distortion that is given by the primary magnetizing current that flows into Lm. Energy is taken from Cs. Diode D2 current reaches zero in the end of this interval (ZCS).

E - Switch M2 has been turned OFF, energy stored in the Lm and Ls prepares ZVS condition for opposite switch M1 – overcharges the total parasitic capacitance on the bridge and opens M1 body diode. Energy is supplied by Ls and Lm. Diode D1 starts to conduct.

F – M1 body diode conducts current until M1 is turned ON by the controller. Diode D1 conducts. Energy is supplied by Ls and Lm until Is = 0. One part of the Lm+Ls energy holds ZVS for M2 and the other part goes to the output.

Operating states of the LLC converter – Discrete resonant tank solution:

c) Operating waveforms for $f_{op} > f_s$



Operating states of the LLC converter – Discrete resonant tank solution:

Operating intervals explanation – $f_{op} > f_s$:

A - Switch M1 has been turned ON (ZVS) and conducts together with secondary diode D1, primary current has sinusoidal wave shape because the Cs and Ls form series resonant circuit, Lm doesn't participate in the resonance now because it is clamped by the output impedance. Diode D1 current is nearly sinusoidal with a slight distortion that is given by the primary magnetizing current that flows into Lm. Energy is taken from bulk.

B - Switch M1 has been turned OFF, energy stored in the Ls prepares ZVS condition for opposite switch M2 – overcharges the total parasitic capacitance on the bridge and opens M2 body diode. Energy is supplied by Ls.

C - M2 body diode conducts current until M2 is turned ON by the controller. Current of the Lm Increases, current of the Ls decreases until ILs=ILm. At the time ILs=ILm Diode D1 current reaches zero and transformer voltage reverses D1 has been turned OFF with ZSC. Diode D2 is opened (by the energy stored in the Lm and Ls). The Lm and Ls supply energy until the Is=0. Part of the Lm+Ls energy holds ZVS for M2 and part goes to the output.

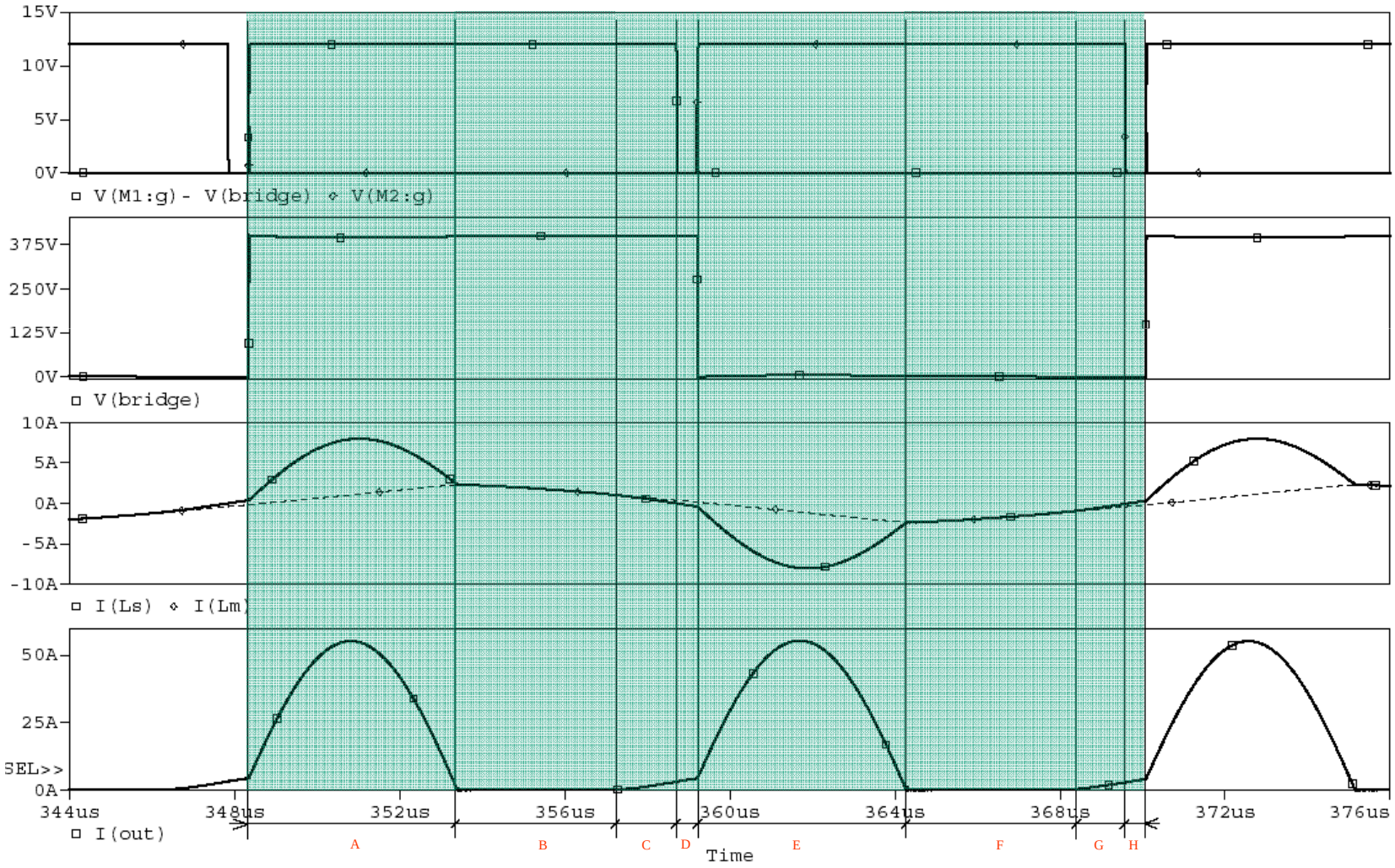
D – Switch M2 has been turned ON (ZVS) and conducts together with secondary diode D2, primary current has sinusoidal wave shape because the Cs and Ls form series resonant circuit, Lm doesn't participate in the resonance now because it is clamped by the output impedance. Diode D2 current is nearly sinusoidal with a slight distortion that is given by the primary magnetizing current that flows into Lm. Energy is taken from Cs.

E – Switch M2 has been turned OFF, energy stored in the Ls prepares ZVS condition for opposite switch M1 – overcharge total parasitic capacitance on the bridge and opens body diode of M1. Energy is supplied by Ls.

F – M1 body diode conducts until M1 is turned ON by the controller. Current of the Lm Increases, current of the Ls decreases until ILs=ILm. At the time ILs=ILm Diode D2 current reaches zero and transformer voltage reverses D2 has been turned OFF with ZSC. Diode D1 is opened (by the energy stored in the Lm and Ls). The Lm and Ls supply energy until the Is=0. Part of the Lm+Ls energy holds ZVS for M1 and part goes to the output.

Operating states of the LLC converter – Discrete resonant tank solution:

d) Operating waveforms for fmin < fop < fs – strong overload



Operating states of the LLC converter – Discrete resonant tank solution:

Operating intervals explanation – $f_{op} < f_{min}$ - strong overload :

A - Switch M1 has been turned ON (hard switching!) and conducts together with secondary diode D1, primary current has sinusoidal wave shape because the Cs and Ls form series resonant circuit, Lm don't participate on the resonance now because it is clamped by the output impedance. Diode D1 current is nearly sinusoidal with a slight distortion that is given by the primary magnetizing current that flows into Lm. D1 closes at the end of this period (ZCS).
B - D1 has been closed, resonant circuit has thus been reconfigured to Cs - (Ls+Lm), primary current continues to flow but with different slope because Lm contributes on the resonance now.
C - Primary current crossed zero and continues in a opposite way – resonant tank supplies energy now.
D - Switch M1 has been turned OFF. Current is further flowing through the M1 body diode until switch M2 is turned ON by the controller – we have prepared hard switching condition for the M1 body diode!!!
E - Switch M2 has been turned ON (hard switching!) and conducts together with secondary diode D2, primary current has sinusoidal wave shape because the Cs and Ls form series resonant circuit, Lm don't participate on the resonance now because it is clamped by the output impedance. Diode D2 current is nearly sinusoidal with a slight distortion that is given by the primary magnetizing current that flows into Lm. D2 closes at the end of this period (ZCS).
F – D2 has been closed, resonant circuit has thus been reconfigured to Cs - (Ls+Lm), primary current continues to flow but with different slope because Lm contributes on the resonance now.
G - Primary current crossed zero and continues in a opposite way – resonant tank supplies energy now!
H - Switch M2 has been turned OFF. Current is further flowing through the M2 body diode until switch M1 is turned ON by the controller – we have prepared hard switching condition for the M2 body diode!!!

Note: This operating mode is extremely dangerous because hard switching is achieved for the MOSFET that is going to be turn ON and also for the body diode of the opposite MOSFET. This situation can lead to the MOSFETs failure.

FAIRCHILD
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Design Considerations for an LLC Resonant Converter

Hangseok Choi
Power Conversion Team

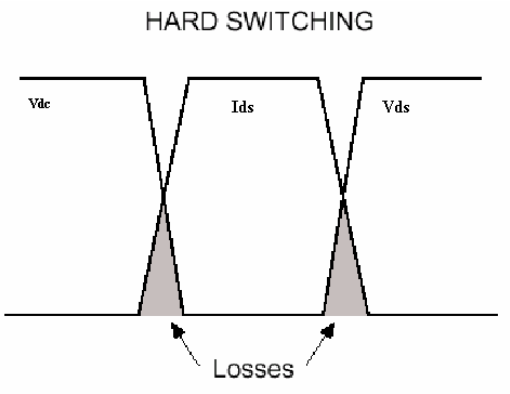
the power franchise™

1. Introduction

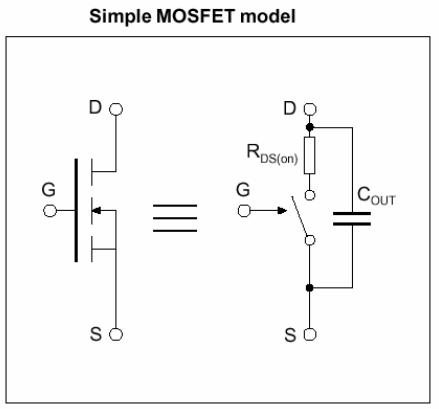
- Growing demand for higher power density and low profile in power converter has forced to increase switching frequency
- However, **Switching Loss** has been an obstacle to high frequency operation

High frequency operation

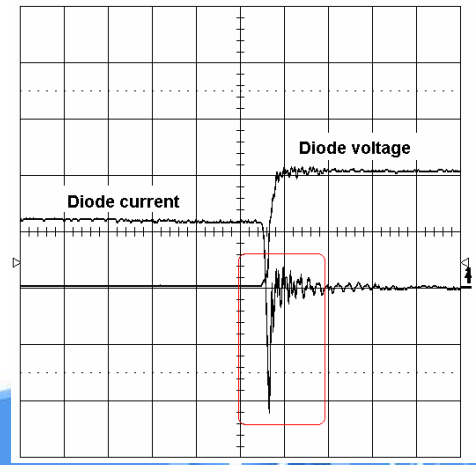
Overlap of voltage and current



Capacitive loss

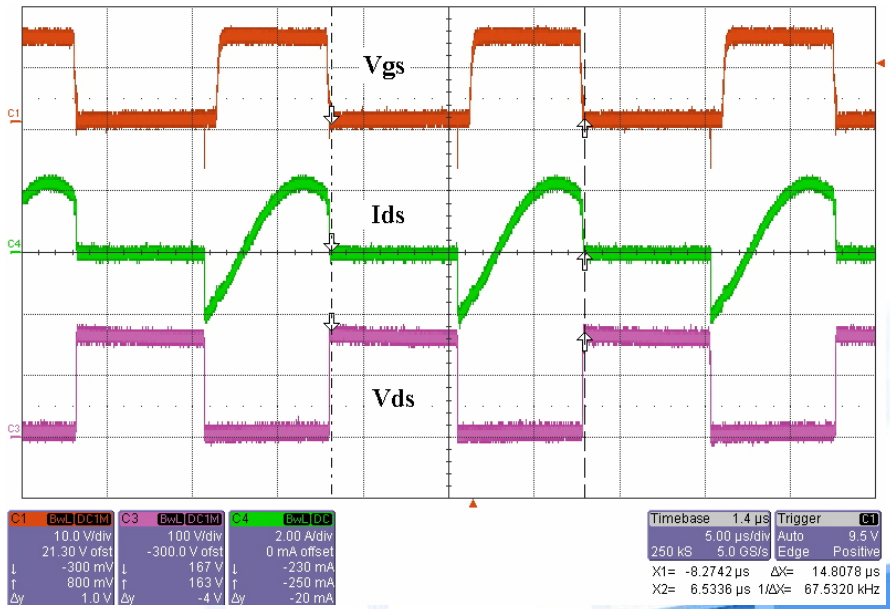


Reverse recovery loss

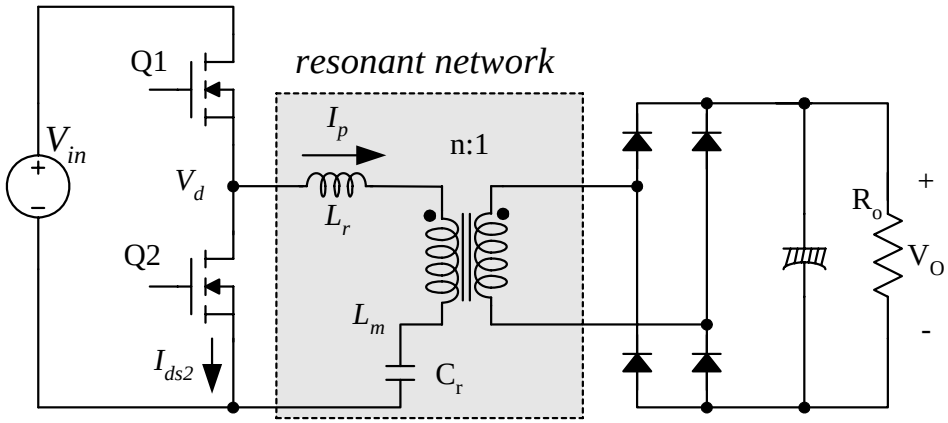


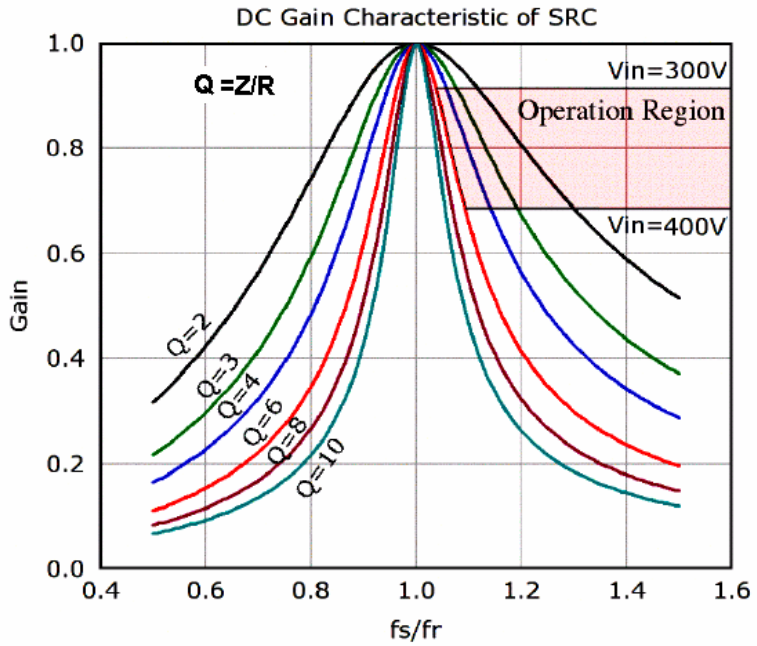
1. Introduction

- **Resonant converter: processes power in a sinusoidal manner and the switching devices are softly commutated**
  - ✓ Voltage across the switch drops to zero before switch turns on (ZVS)
    - Remove overlap area between V and I when turning on
    - Capacitive loss is eliminated
- **Series resonant converter / Parallel resonant converter**



Series Resonant (SR) converter





- The resonant inductor (Lr) and resonant capacitor (Cr) are in series
- The resonant capacitor is in series with the load
  - ✓ The resonant tank and the load act as a voltage divider→ DC gain is always lower than 1 (maximum gain happens at the resonant frequency)
  - ✓ The impedance of resonant tank can be changed by varying the frequency of driving voltage (V_d)

1. Introduction

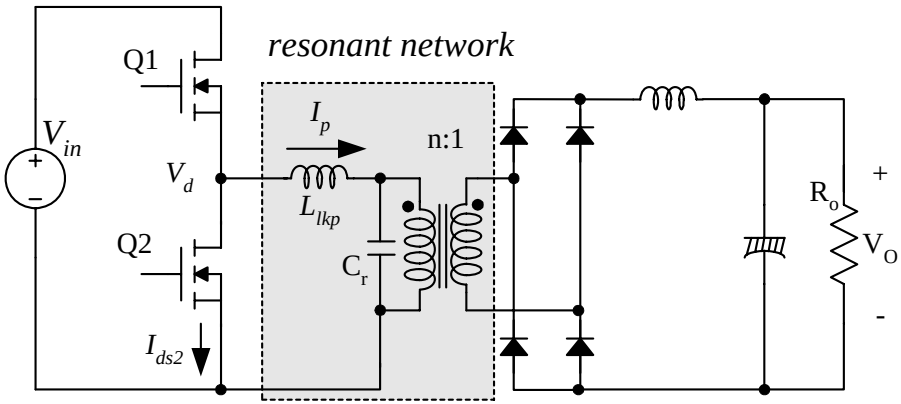
Series Resonant (SR) converter

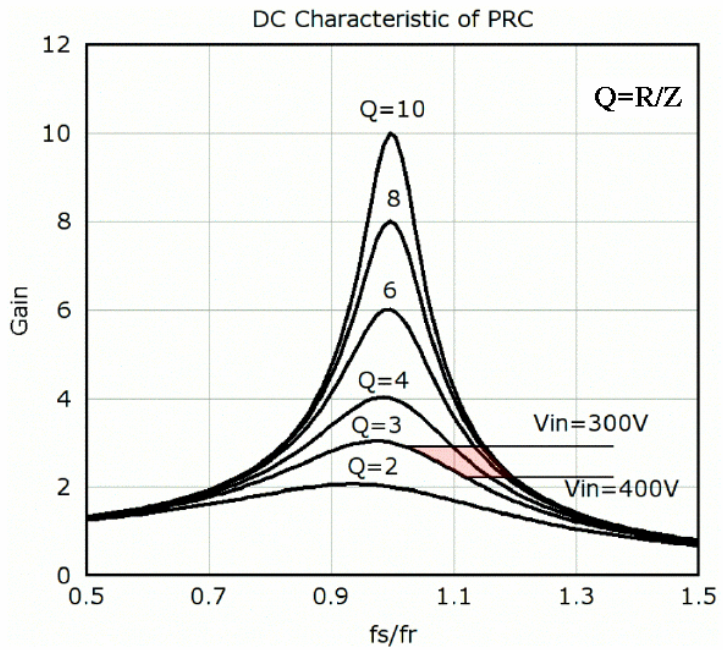
- Advantages
  - ✓ Reduced switching loss and EMI through ZVS → Improved efficiency
  - ✓ Reduced magnetic components size by high frequency operation

- Drawbacks
  - ✓ Can optimize performance at one operating point, but not with wide range of input voltage and load variations
  - ✓ Can not regulate the output at no load condition
  - ✓ Pulsating rectifier current (capacitor output): limitation for high output current application

1. Introduction

Parallel Resonant (PR) converter





- The resonant inductor (Lr) and resonant capacitor (Cr) are in series
- The resonant capacitor is in parallel with the load
  - ✓ The impedance of resonant tank can be changed by varying the frequency of driving voltage (V_d)

1. Introduction

Parallel Resonant (PR) converter

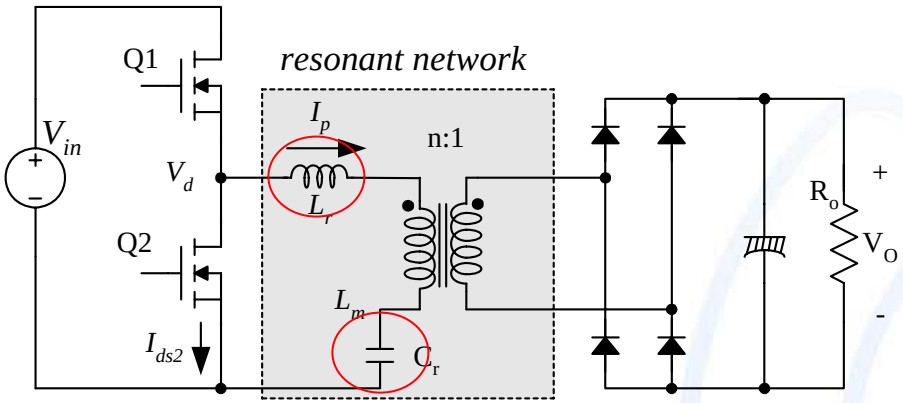
- Advantages
  - ✓ No problem in output regulation at no load condition
  - ✓ Continuous rectifier current (inductor output): suitable for high output current application

- Drawbacks
  - ✓ The primary side current is almost independent of load condition: significant current may circulate through the resonant network, even at the no load condition
  - ✓ Circulating current increases as input voltage increases: limitation for wide range of input voltage

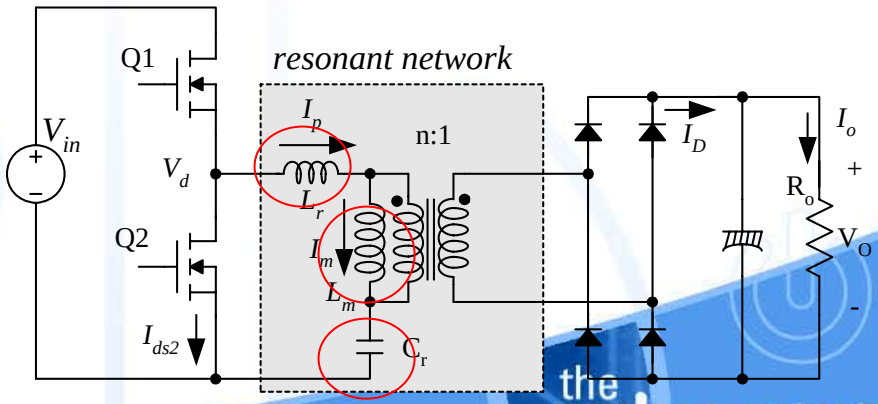
1. Introduction

- **What is LLC resonant converter?**
  - ✓ Topology looks almost same as the conventional LC series resonant converter
  - ✓ Magnetizing inductance (L_m) of the transformer is relatively small and involved in the resonance operation
  - ✓ Voltage gain is different from that of LC series resonant converter

LC Series resonant converter



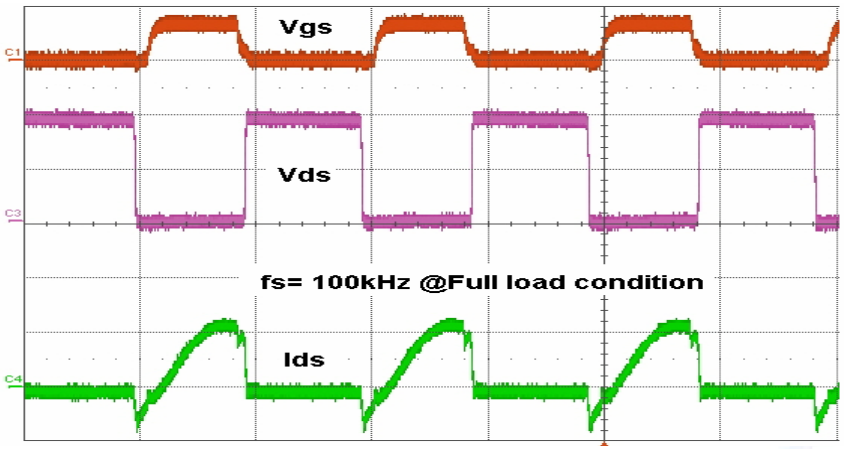
LLC resonant converter

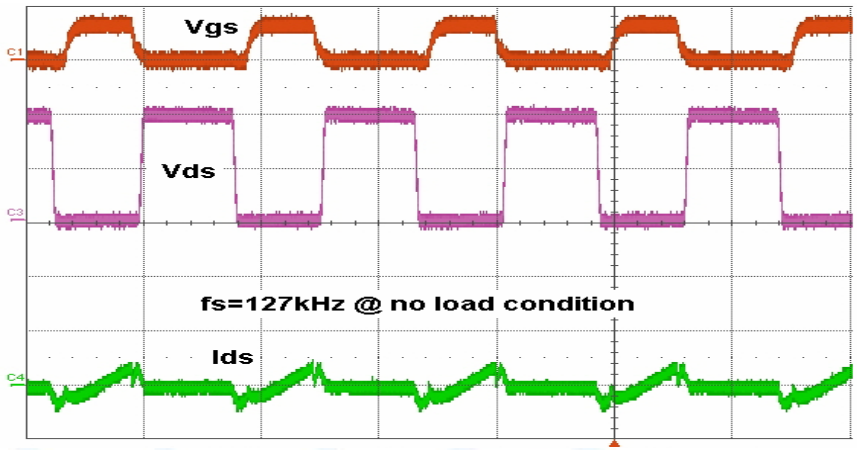


1. Introduction

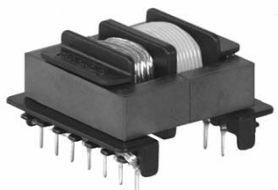
- **Features of LLC resonant converter**

  - Reduced switching loss through ZVS: Improved efficiency
  - Narrow frequency variation range over wide load range
  - Zero voltage switching even at no load condition



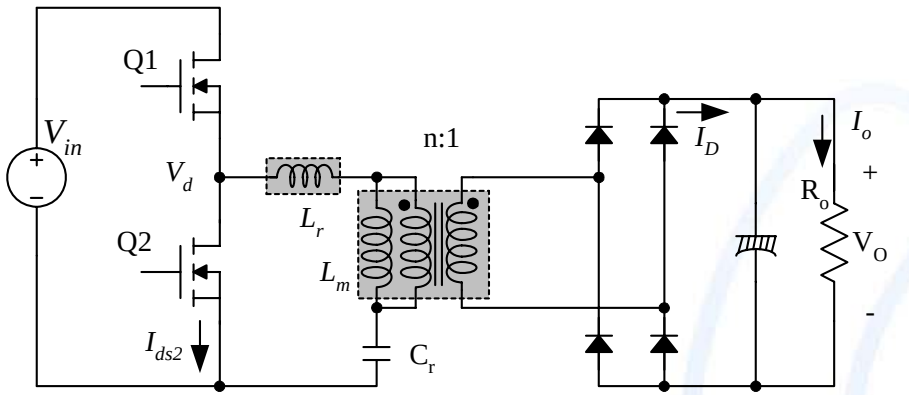


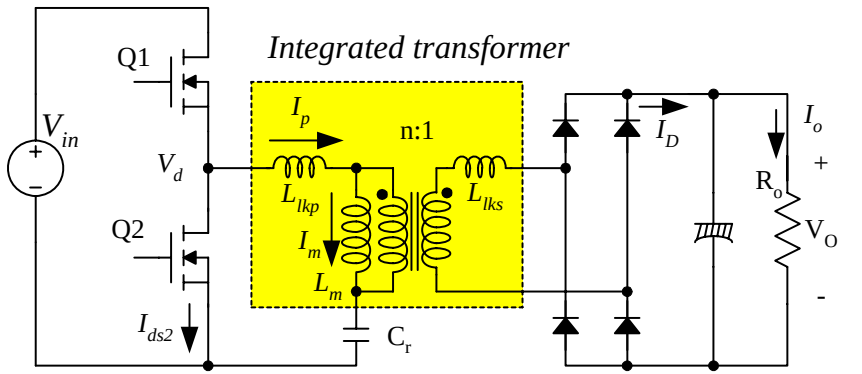
- Typically, integrated transformer is used instead of discrete magnetic components



1. Introduction

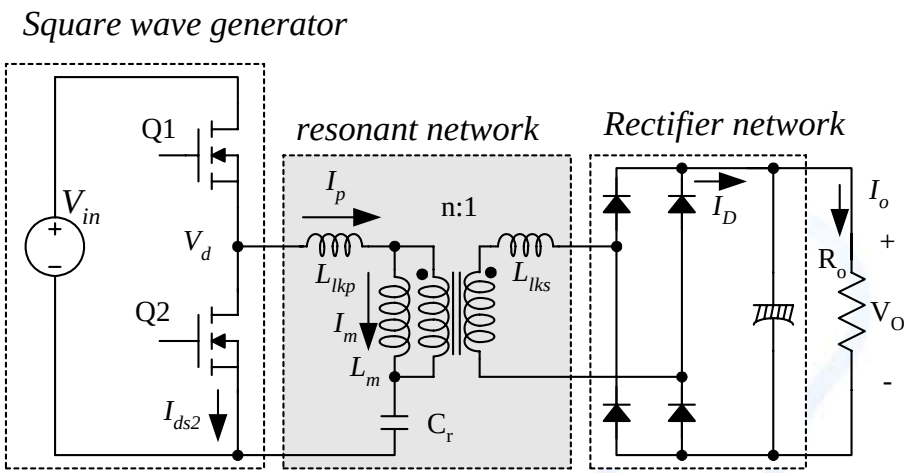
- **Integrated transformer in LLC resonant converter**
  - ✓ Two magnetic components are implemented with a single core (use the primary side leakage inductance as a resonant inductor)
  - ✓ One magnetic components (Lr) can be saved
  - ✓ Leakage inductance not only exists in the primary side but also in the secondary side
  - ✓ Need to consider the leakage inductance in the secondary side

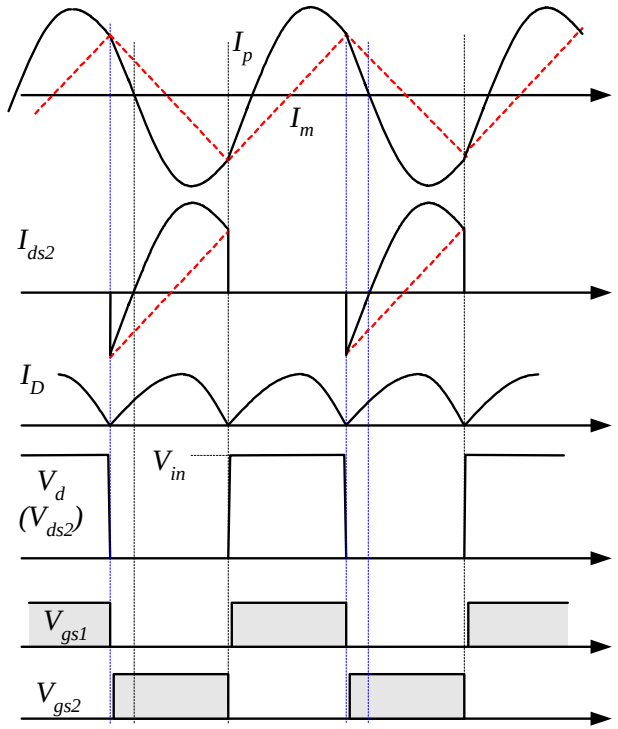




2. Operation principle and Fundamental Approximation

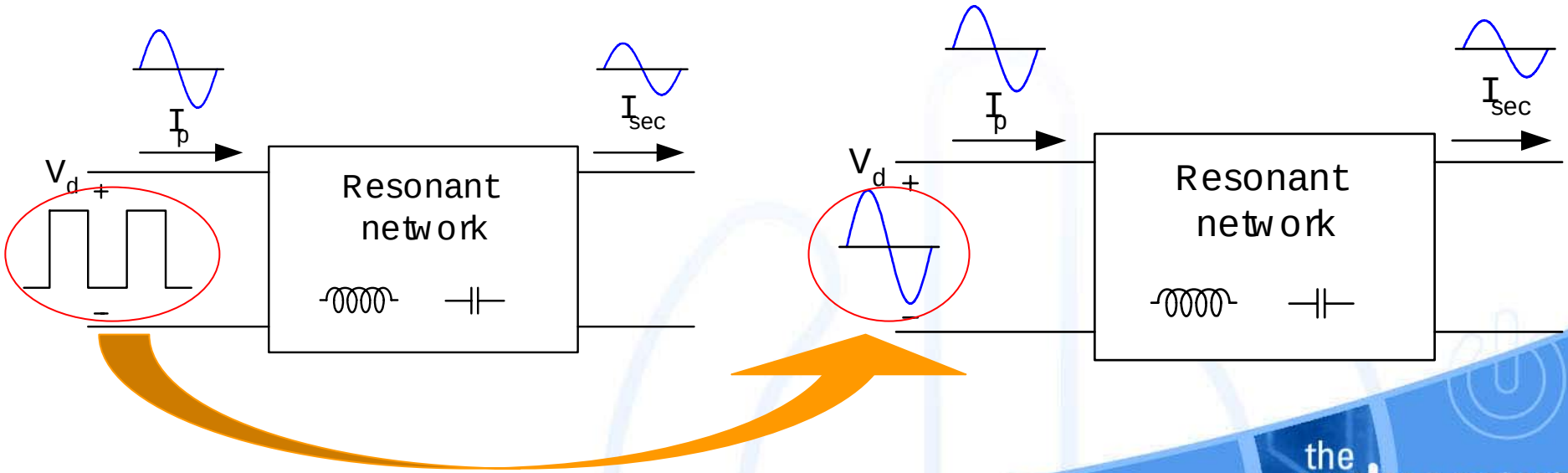
- Square wave generator: produces a square wave voltage, V_d by driving switches, Q1 and Q2 with alternating 50% duty cycle for each switch.
- Resonant network: consists of L_{lkp}, L_{lks}, L_m and C_r. The current lags the voltage applied to the resonant network which allows the MOSFET's to be turned on with zero voltage.
- Rectifier network: produces DC voltage by rectifying AC current





2. Operation principle and Fundamental Approximation

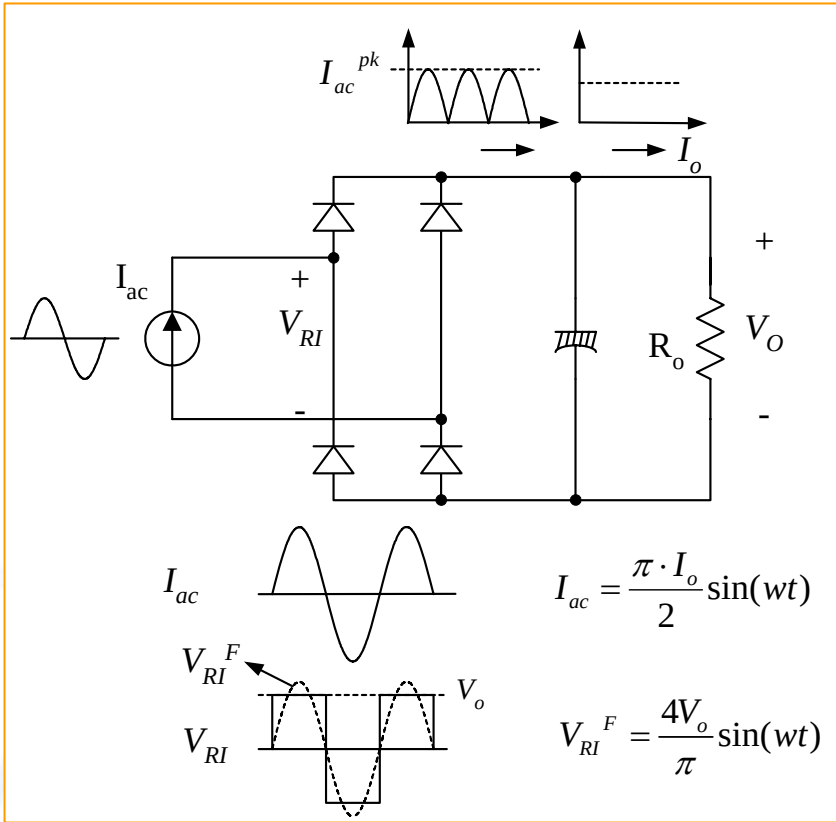
- The resonant network filters the higher harmonic currents. Thus, essentially only sinusoidal current is allowed to flow through the resonant network even though a square wave voltage (V_d) is applied to the resonant network.
- Fundamental approximation: assumes that only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to the output.
- The square wave voltage can be replaced by its fundamental component



2. Operation principle and Fundamental Approximation

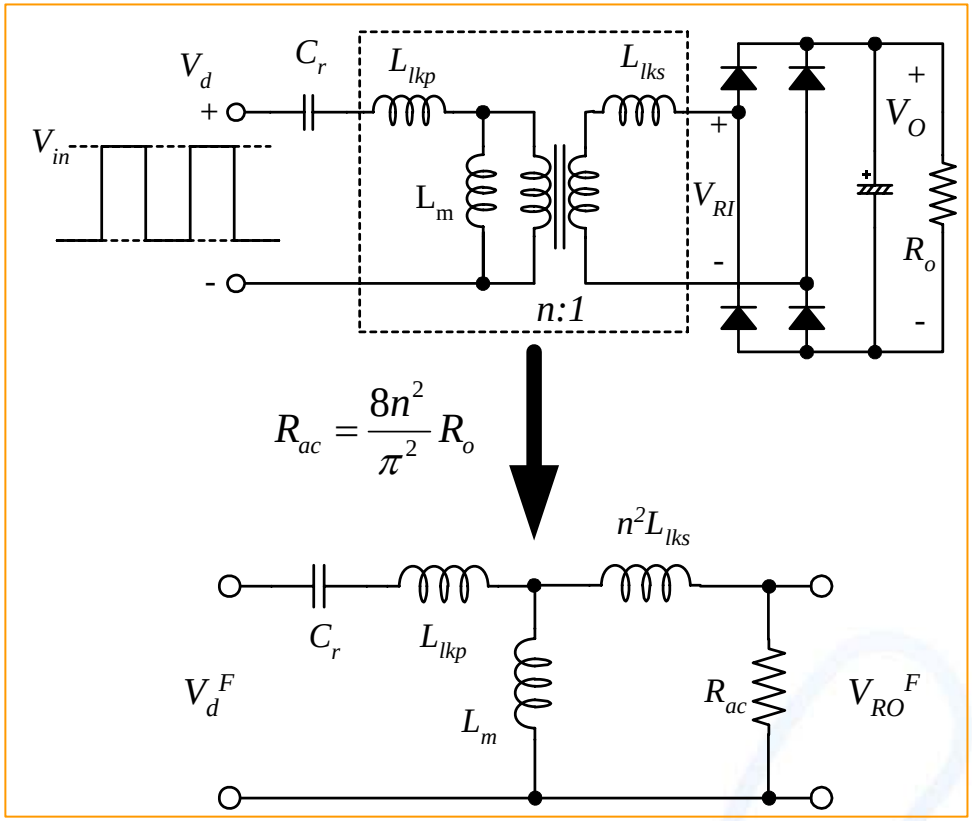
- Because the rectifier circuit in the secondary side acts as an impedance transformer, the equivalent load resistance is different from actual load resistance.
- The primary side circuit is replaced by a sinusoidal current source (I_{ac}) and a square wave of voltage (V_{RI}) appears at the input to the rectifier.
- The equivalent load resistance is obtained as

$$R_{ac} = \frac{V_{RI}^{\ F}}{I_{ac}^{\ F}} = \frac{V_{RI}^{\ F}}{I_{ac}} = \frac{8}{\pi^2}\frac{V_o}{I_o} = \frac{8}{\pi^2}R_o$$



2. Operation principle and Fundamental Approximation

- **AC equivalent circuit (L-L-L-C)**



$$M = \frac{V_{RO}^F}{V_d^F} = \frac{n \cdot V_{RI}^F}{V_d^F} = \frac{\frac{4n \cdot V_o}{\pi}\sin(\omega t)}{\frac{4}{\pi}\frac{V_{in}}{2}\sin(\omega t)} = \frac{2n \cdot V_o}{V_{in}}$$

$$= \left| \frac{\omega^2 L_m R_{ac} C_r}{j\omega \cdot (1 - \frac{\omega^2}{\omega_o^2}) \cdot (L_m + n^2 L_{lks}) + R_{ac}(1 - \frac{\omega^2}{\omega_p^2})} \right|$$

$$R_{ac} = \frac{8n^2}{\pi^2} R_o$$

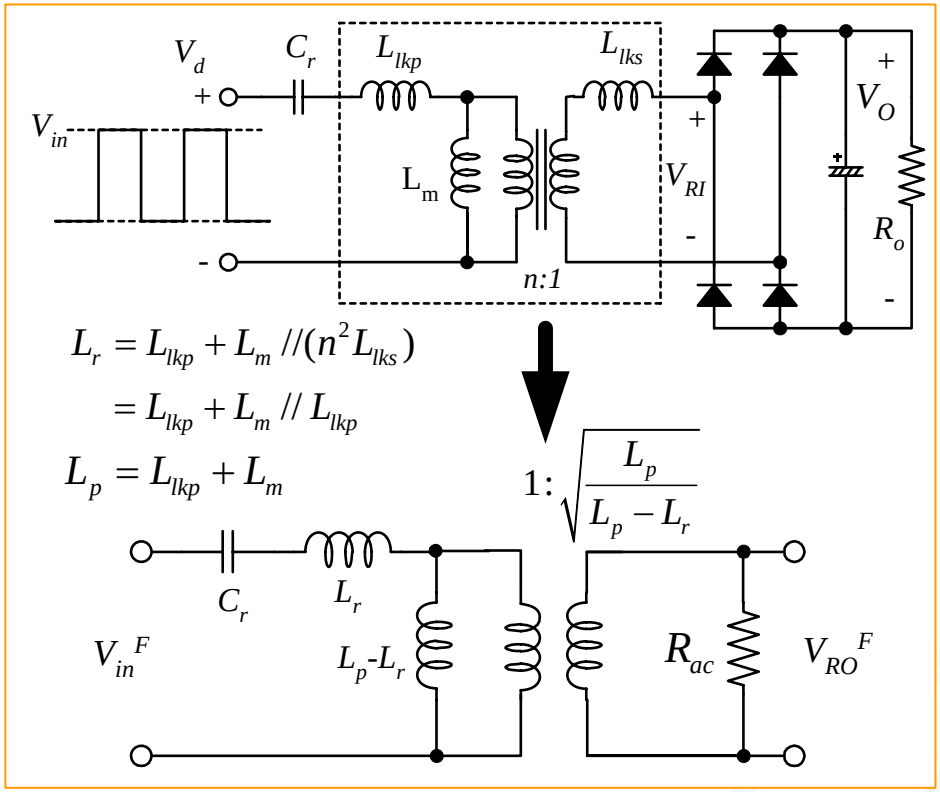
$$\omega_o = \frac{1}{\sqrt{L_r C_r}} \quad , \quad \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

$$L_p = L_m + L_{lkp} \quad , \quad L_r = L_{lkp} + L_m // (n^2 L_{lks})$$

- Lr is measured in primary side with secondary winding short circuited
- Lp is measured in primary side with secondary winding open circuited

2. Operation principle and Fundamental Approximation

- **Simplified AC equivalent circuit (L-L-C)**



Assuming $L_{lkp}=n^2L_{lks}$

$$M = \frac{2n \cdot V_O}{V_{in}} = \left| \frac{(\frac{\omega^2}{\omega_p{}^2}) \frac{k}{k+1}}{j(\frac{\omega}{\omega_o}) \cdot (1 - \frac{\omega^2}{\omega_o{}^2}) \cdot Q \frac{(k+1)^2}{2k+1} + (1 - \frac{\omega^2}{\omega_p{}^2})} \right|$$

$$Q = \frac{\sqrt{L_r / C_r}}{R_{ac}} \qquad k = \frac{L_m}{L_{lkp}}$$

Expressing in terms of L_p and L_r

$$M = \frac{2n \cdot V_O}{V_{in}} = \left| \frac{(\frac{\omega^2}{\omega_p{}^2}) \sqrt{\frac{L_p - L_r}{L_p}}}{j(\frac{\omega}{\omega_o}) \cdot (1 - \frac{\omega^2}{\omega_o{}^2}) \cdot Q \frac{L_p}{L_r} + (1 - \frac{\omega^2}{\omega_p{}^2})} \right|$$

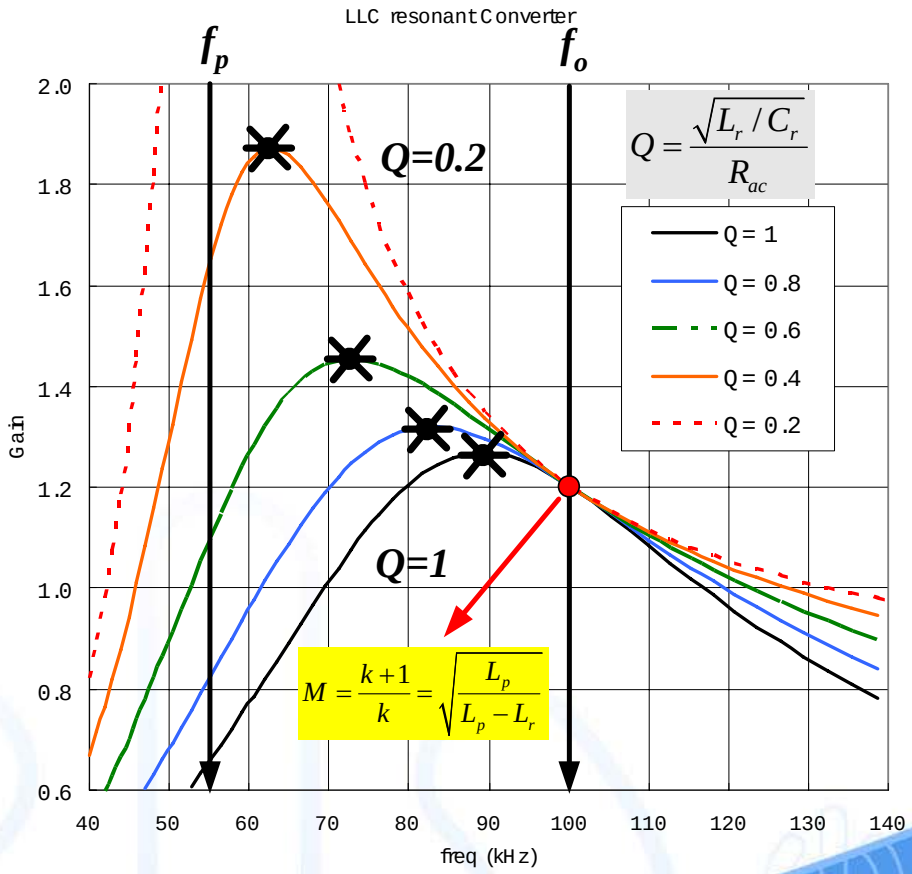
- Lr is measured in primary side with secondary winding short circuited
- Lp is measured in primary side with secondary winding open circuited

2. Operation principle and Fundamental Approximation

- Gain characteristics
  - ✓ Two resonant frequencies (f_o and f_p) exist
  - ✓ The gain is fixed at resonant frequency (f_o) regardless of the load variation

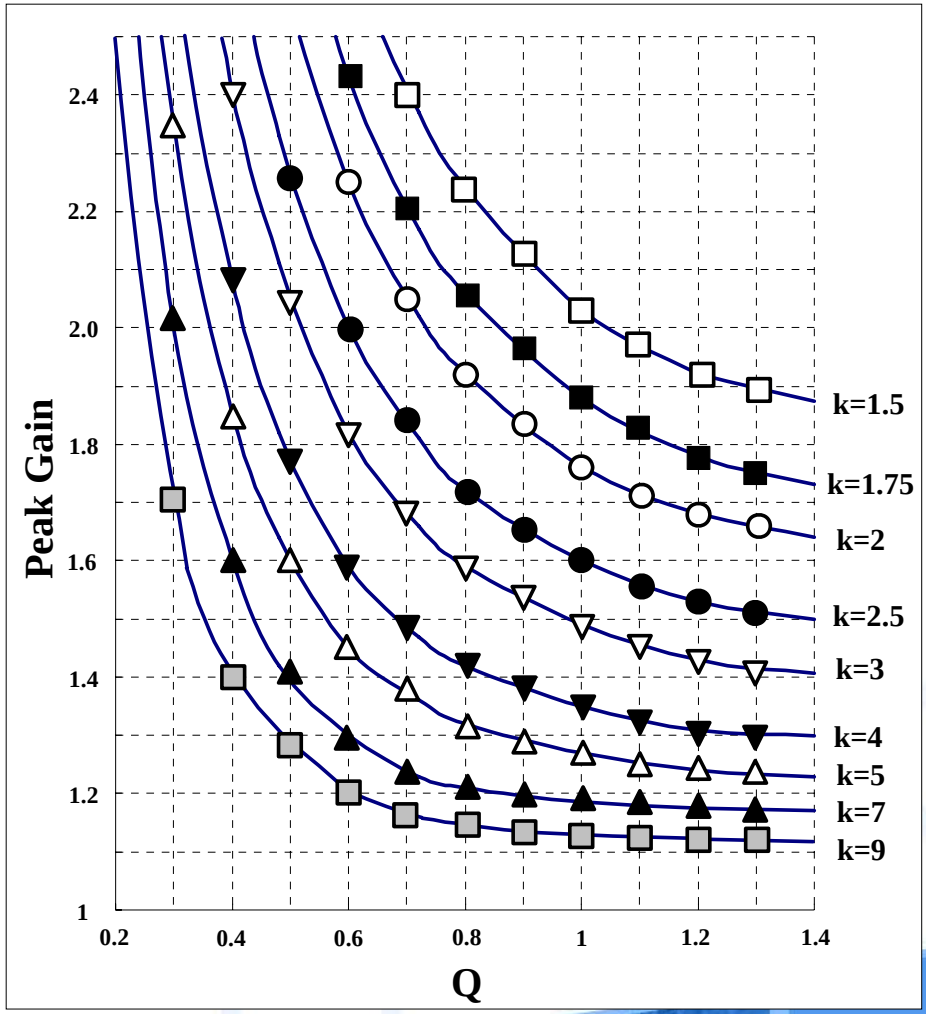
$$M_{@\omega=\omega_o} = \frac{k+1}{k} = \sqrt{\frac{L_p}{L_p - L_r}}$$

  - ✓ Peak gain frequency exists between f_o and f_p
  - ✓ As Q decreases (as load decreases), the peak gain frequency moves to f_p and higher peak gain is obtained.
  - ✓ As Q increases (as load increases), peak gain frequency moves to f_o and the peak gain drops



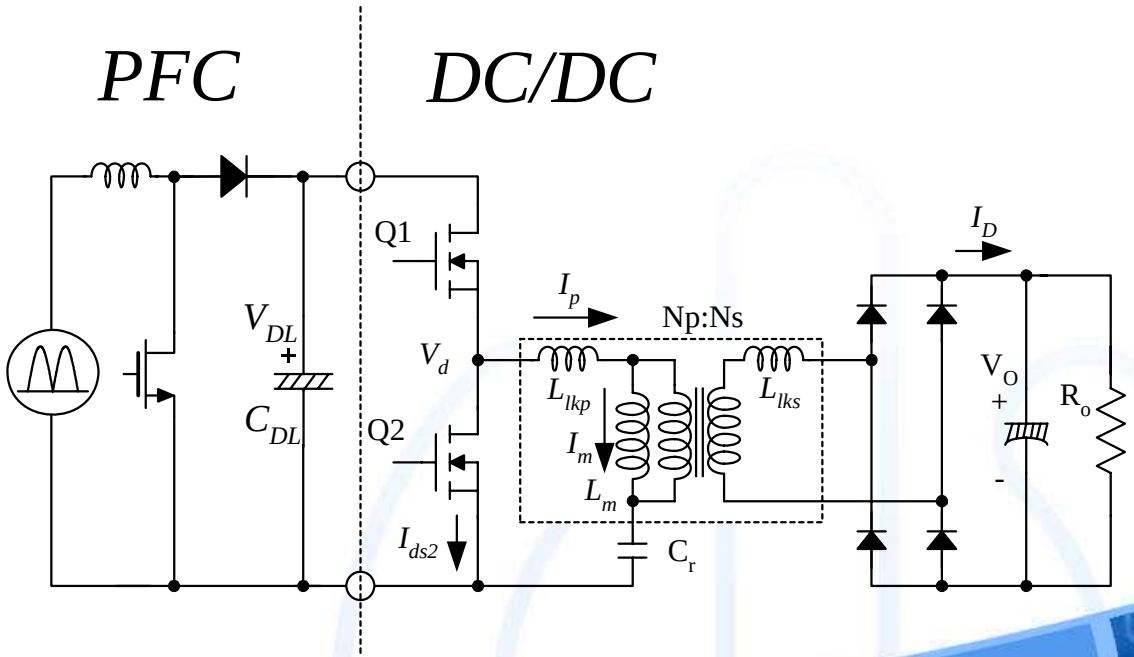
2. Operation principle and Fundamental Approximation

- Peak gain (attainable maximum gain) versus Q for different k values



3. Design procedure

- Design example
  - Input voltage: 380Vdc (output of PFC stage)
  - Output: 24V/5A (120W)
  - Holdup time requirement: 17ms
  - DC link capacitor of PFC output: 100uF



3. Design procedure

[STEP-1] Define the system specifications

- ✓ Estimated efficiency (*E*ff)
- ✓ Input voltage range: hold up time should be considered for minimum input voltage

$$V_{in}^{\min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{DL}}}$$

(Design Example) Assuming the efficiency is 95%,

$$P_{in} = \frac{P_o}{E_{ff}} = \frac{120}{0.95} = 126W$$

$$V_{in}^{\min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{DL}}}$$

$$= \sqrt{380^2 - \frac{2 \cdot 126 \cdot 17 \times 10^{-3}}{100 \times 10^{-6}}} = 319V$$

$$V_{in}^{\max} = V_{O.PFC} = 380V$$

3. Design procedure

[STEP-2] Determine the maximum and minimum voltage gains of the resonant network by choosing k $(k = L_m / L_{lkp})$

- it is typical to set k to be 5~10, which results in a gain of 1.1~1.2 at f_o

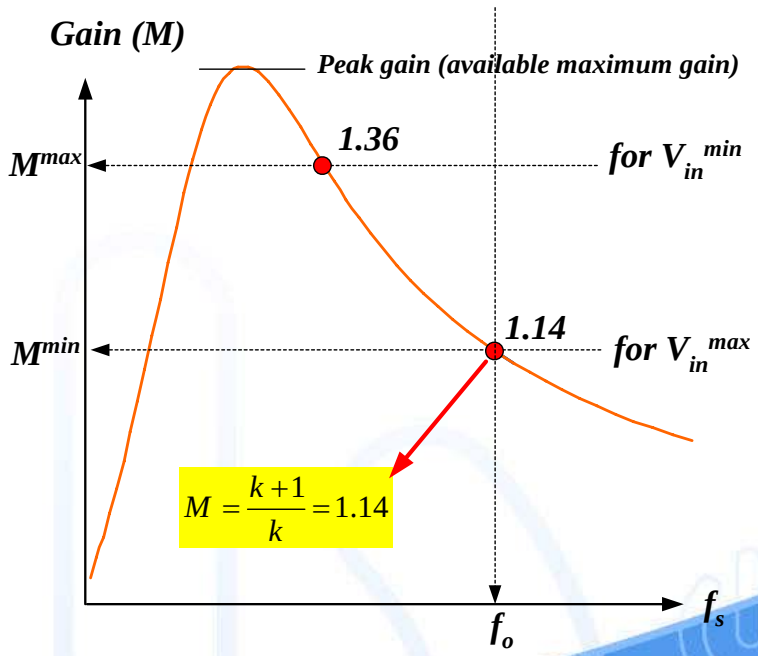
$$M^{\min} = \frac{V_{RO}}{\frac{V_{in}^{\max}}{2}} = \frac{L_m + n^2 L_{lks}}{L_m} = \frac{L_m + L_{lkp}}{L_m} = \frac{k+1}{k}$$

$$M^{\max} = \frac{V_{in}^{\max}}{V_{in}^{\min}} M^{\min}$$

(Design Example) The ratio (k) between L_m and L_{lkp} is determined as 7, which results in the minimum gain as

$$M^{\min} = \frac{V_{RO}}{\frac{V_{in}^{\max}}{2}} \cong \frac{k+1}{k} = \frac{7+1}{7} = 1.14$$

$$M^{\max} = \frac{V_{in}^{\max}}{V_{in}^{\min}} M^{\min} = \frac{380}{319} \cdot 1.14 = 1.36$$



3. Design procedure

[STEP-3] Determine the transformer turns ratio (n=Np/Ns)

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{\max}}{2(V_o + V_F)} \cdot M^{\min}$$

(Design Example)

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{\max}}{2(V_o + V_F)} \cdot M_{\min} = \frac{380}{2(24 + 1.2)} \cdot 1.14 = 8.6$$

[STEP-4] Calculate the equivalent load resistance (Rac)

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{V_o^2}{P_o}$$

(Design Example)

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{V_o^2}{P_o} = \frac{8 \cdot 8.6^2 \cdot 24^2}{\pi^2 \cdot 120} = 288\Omega$$

3. Design procedure

[STEP-5] Design the resonant network

- With k chosen in STEP-2, read proper Q from gain curves

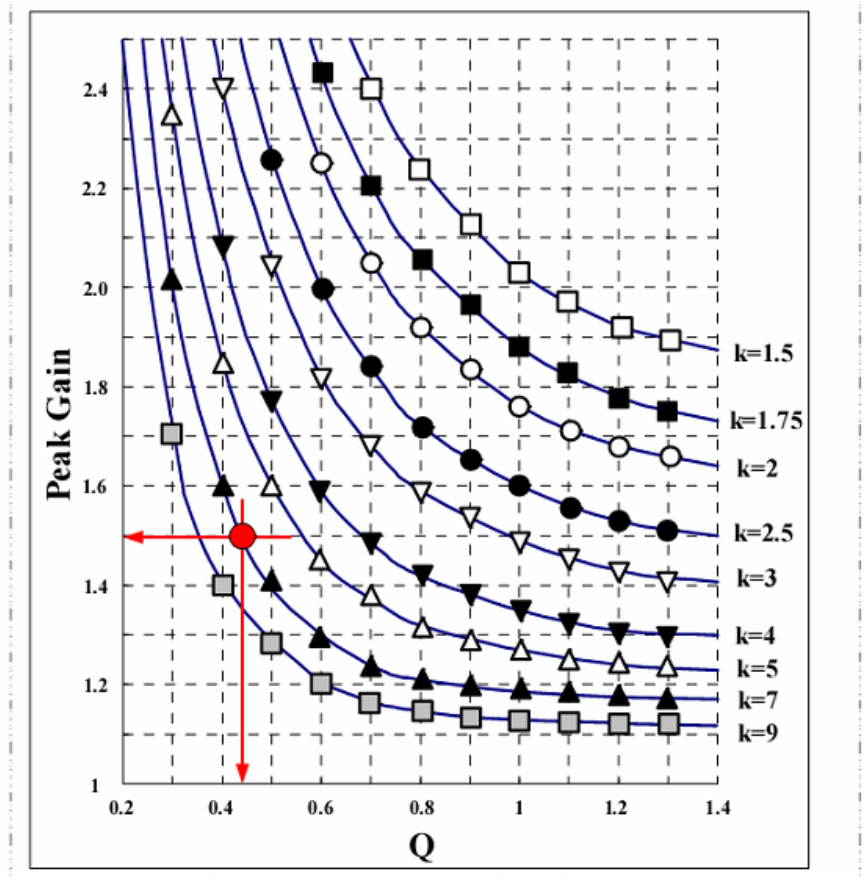
$$k = 7,\ M^{\max} = 1.36$$
$$peak\ gain = 1.36 \times 110\% = 1.5$$

(Design Example)
As calculated in STEP-2, the maximum voltage gain (M^{max}) for the minimum input voltage (V_{in}^{min}) is 1.36. With 10% margin, a peak gain of 1.5 is required. k has been chosen as 7 in STEP-2 and Q is obtained as 0.43 from the peak gain curves in Fig. 12. By selecting the resonant frequency as 85kHz, the resonant components are determined as

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} = \frac{1}{2\pi \cdot 0.43 \cdot 85 \times 10^3 \cdot 288}$$
$$= 15nF$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} = \frac{1}{(2\pi \cdot 85 \times 10^3)^2 \cdot 15 \times 10^{-9}}$$
$$= 234uH$$

$$L_p = \frac{(k+1)^2}{(2k+1)} L_r = 998uH$$



3. Design procedure

[STEP-6] Design the transformer

- Plot the gain curve and read the minimum switching frequency. Then, the minimum number of turns for the transformer primary side is obtained as

$$N_p^{\min} = \frac{n(V_o + V_F)}{2 f_s^{\min} \cdot \Delta B \cdot A_e}$$

(Design Example) EER3541 core (A_e=107mm^2) is selected for the transformer. From the gain curve of Fig .12, the minimum switching frequency is obtained as 66kHz. Then, the minimum primary side turns of the transformer is given as

$$N_p^{\min} = \frac{n(V_o + V_F) \times 10^6}{2 f_s^{\min} \Delta B \cdot A_e}$$

$$= \frac{8.6 \times 25.2 \times 10^6}{2 \cdot 66 \times 10^3 \cdot 0.3 \cdot 107} = 51.1 \; turns$$

$$\therefore N_p = n \cdot N_s = 8.6 \times 6 = 51.6 > N_p^{\min}$$

Choosing Ns as 6 turns, Np is given as

$$N_p = n \cdot N_s = 8.6 \times 6 = 51.6 \Rightarrow 52 > N_p^{\min}$$

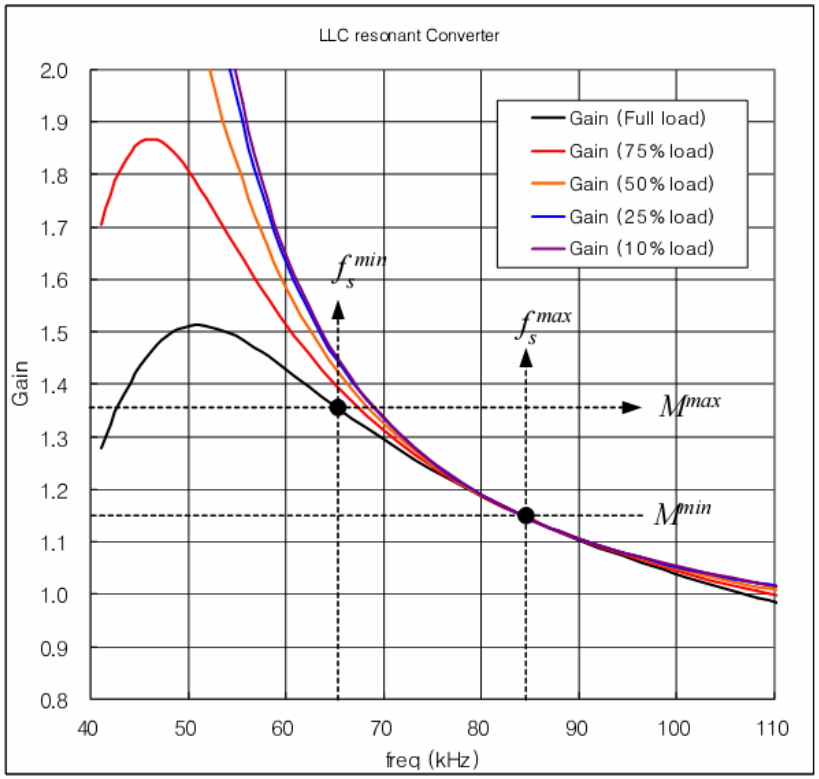
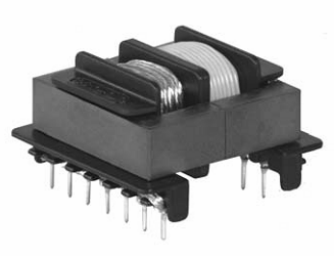


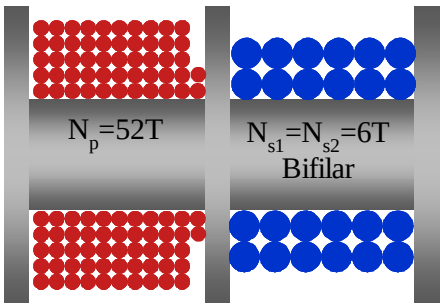
Fig. 12 Gain curve

3. Design procedure

[STEP-7] Transformer Construction

- Since LLC converter design results in relatively large L_r, usually sectional bobbin is typically used
- # of turns and winding configuration are the major factors determining Lr
- Gap length of the core does not affect Lr much
- Lp can be easily controlled with gap length





Gap length	L_p	L_r
0.0 mm	5,669 µH	237 µH
0.05 mm	2,105 µH	235 µH
0.10 mm	1,401 µH	233 µH
0.15 mm	**1,065 µH**	**230 µH**
0.20 mm	890 µH	225 µH
0.25 mm	788 µH	224 µH
0.30 mm	665 µH	223 µH
0.35 mm	623 µH	222 µH

Design value: L_r=234uH, L_p=998uH

3. Design procedure

[STEP-8] Select the resonant capacitor

$$I_{C_r}{}^{RMS} \cong \sqrt{\left[\frac{\pi I_o}{2\sqrt{2}n}\right]^2 + \left[\frac{n(V_o + 2\cdot V_F)}{4\sqrt{2}\, f_o L_m}\right]^2} \qquad V_{C_r}{}^{\max} \cong \frac{V_{in}{}^{\max}}{2} + \frac{\sqrt{2}\cdot I_{Cr}{}^{RMS}}{2\cdot\pi\cdot f_o\cdot C_r}$$

(Design Example)

$$I_{C_r}{}^{RMS} \cong \sqrt{\left[\frac{\pi I_o}{2\sqrt{2}n}\right]^2 + \left[\frac{n(V_o + 2\cdot V_F)}{4\sqrt{2}\, f_o L_m}\right]^2}$$

$$= \sqrt{\left[\frac{\pi\cdot 5}{2\sqrt{2}\cdot 8.6}\right]^2 + \left[\frac{8.6\cdot(24+1.2)}{4\sqrt{2}\cdot 873\times 10^{-6}\cdot 85\times 10^{3}}\right]^2}$$

$$= 0.87A$$

$$V_{C_r}{}^{\max} \cong \frac{V_{in}{}^{\max}}{2} + \frac{\sqrt{2}\cdot I_{Cr}{}^{RMS}}{2\cdot\pi\cdot f_o\cdot C_r}$$

$$= \frac{380}{2} + \frac{\sqrt{2}\cdot 0.916}{2\cdot\pi\cdot 85\times 10^{3}\cdot 15\times 10^{-9}} = 343V$$

4. Conclusion

- Using a fundamental approximation, gain equation has been derived
- Leakage inductance in the secondary side is also considered (L-L-L-C model) for gain equation
- L-L-L-C equivalent circuit has been simplified as a conventional L-L-C equivalent circuit
- Practical design consideration has been presented

Appendix - FSFR-series

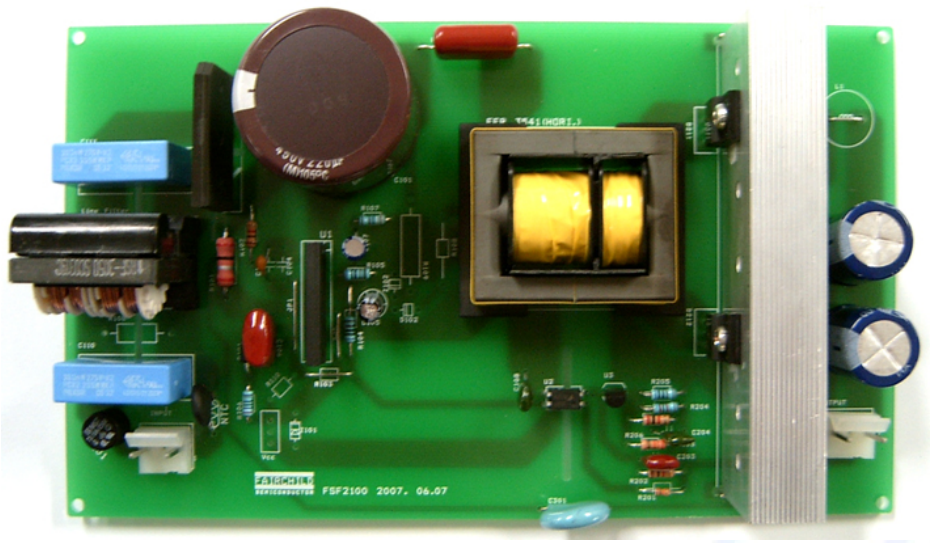
- Variable frequency control with 50% duty cycle for half-bridge resonant converter topology
- High efficiency through zero voltage switching (ZVS)
- Internal Super-FETs with Fast Recovery Type Body Diode (trr=120ns)
- Fixed dead time (350ns)
- Up to 300kHz operating frequency
- Pulse skipping for Frequency limit (programmable) at light load condition
- Simple remote ON/OFF control
- Various Protection functions: Over Voltage Protection (OVP), Over Current Protection (OCP), Abnormal Over Current Protection (AOCP), Internal Thermal Shutdown (TSD)

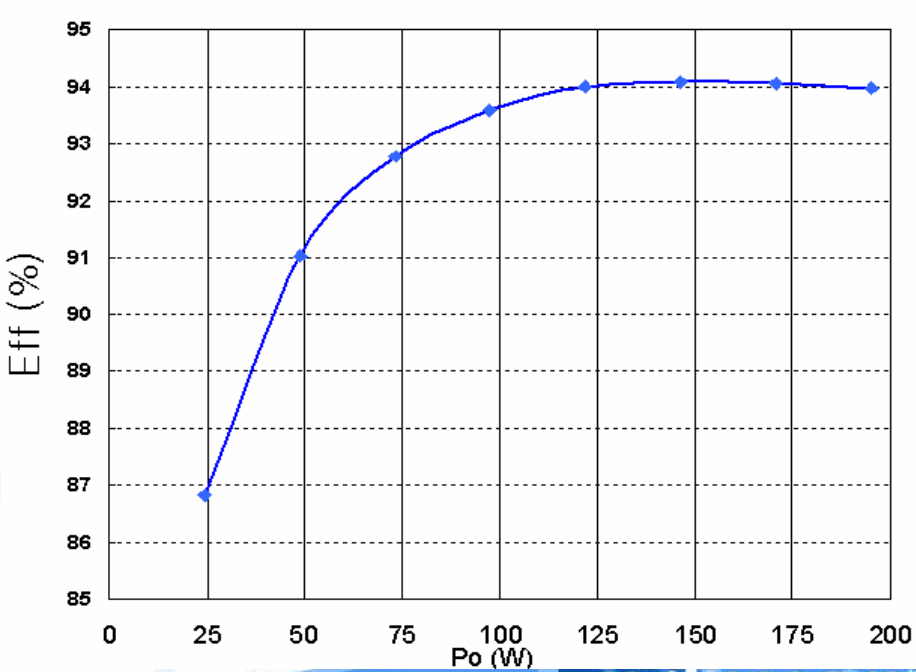
Part Number	Package	Operating Ambient Temperature Ranges	$R_{DS(ON)}$ (MAX)	Maximum Output Power without heat sink (Vin=350~400V) (1) (2)	Maximum Output Power with heat sink (Vin=350~400V) (1) (2)
FSFR2100	9-SIP	-40 to +85 °C	0.38Ω	200W	450W
FSFR2000	9-SIP	-40 to +85 °C	0.6Ω	160W	350W
FSFR1900	9-SIP	-40 to +85 °C	0.8Ω	140W	300W

Appendix - FSFR-series demo board

Application	FPS device	Input voltage range	Rated output power	Output voltage (Rated current)
LCD TV	FSFR2100	Vin nominal : 390Vdc* (340~400Vdc) Vcc supply: 16~20V	192W	24V-8A

*** 20ms hold up time for Vin=390Vdc**





Appendix - FSFR-series demo board

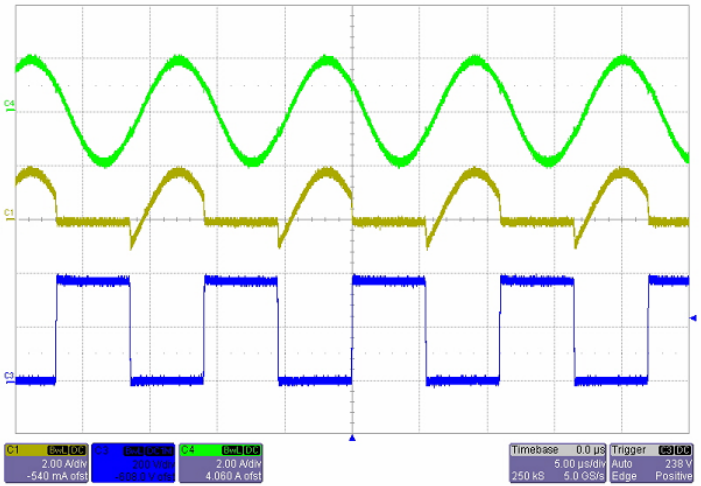


Figure 6. Operation waveforms at nominal input voltage [Vin=390Vdc, Po=192W (24V/8A)]
C4: Transformer Primary side current (2A/div), **C1**: Low side MOSFET current (2A/div)
C3: Low side MOSFET Vds (200V/div), time: 5us/div

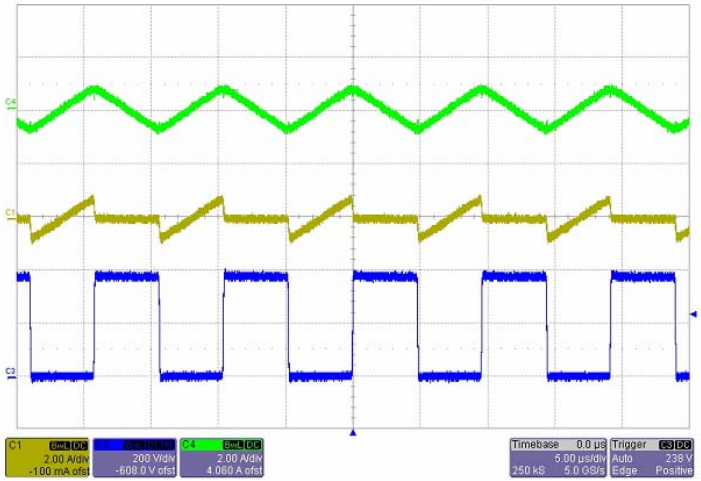


Figure 7. Operation waveforms at nominal input voltage [Vin=390Vdc, Po=0W (24V/0A)]
C4: Transformer Primary side current (2A/div), **C1**: Low side MOSFET current (2A/div)
C3: Low side MOSFET Vds (200V/div), time: 5us/div

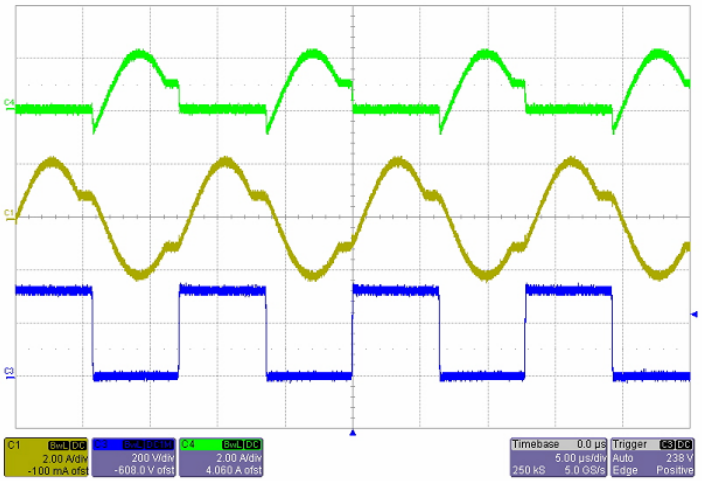


Figure 8. Operation waveforms at minimum input voltage [Vin=340Vdc, Po=192W (24V/8A)]
C4: Transformer Primary side current (2A/div), **C1**: Low side MOSFET current (2A/div)
C3: Low side MOSFET Vds (200V/div), time: 5us/div

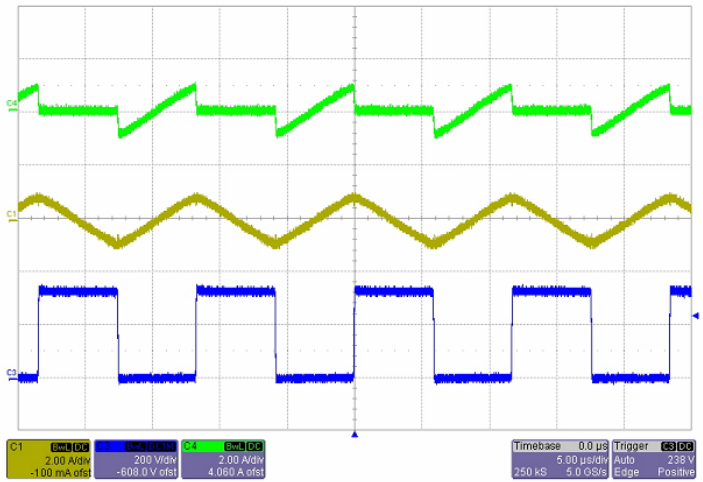


Figure 9. Operation waveforms at minimum input voltage [Vin=340Vdc, Po=0W (24V/0A)]
C4: Transformer Primary side current (2A/div), **C1**: Low side MOSFET current (2A/div)
C3: Low side MOSFET Vds (200V/div), time: 5us/div

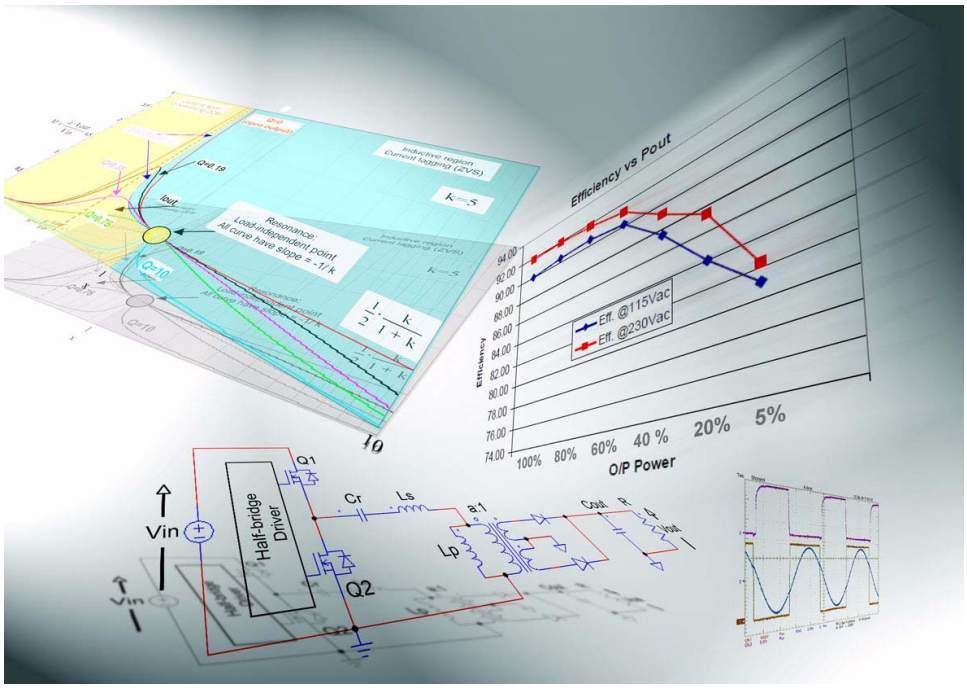
AN2644
Application note

An introduction to LLC resonant half-bridge converter

Introduction

Although in existence for many years, only recently has the LLC resonant converter, in particular in its half-bridge implementation, gained in the popularity it certainly deserves. In many applications, such as flat panel TVs, 85+ ATX PCs or small form factor PCs, where the requirements on efficiency and power density of their SMPS are getting tougher and tougher, the LLC resonant half-bridge with its many benefits and very few drawbacks is an excellent solution. One of the major difficulties that engineers are facing with this topology is the lack of information concerning the way it operates. The purpose of this application note is to provide insight into the topology and help familiarize the reader with it, therefore, the approach is essentially descriptive.

Figure 1. LLC resonant topology schematics and waveforms



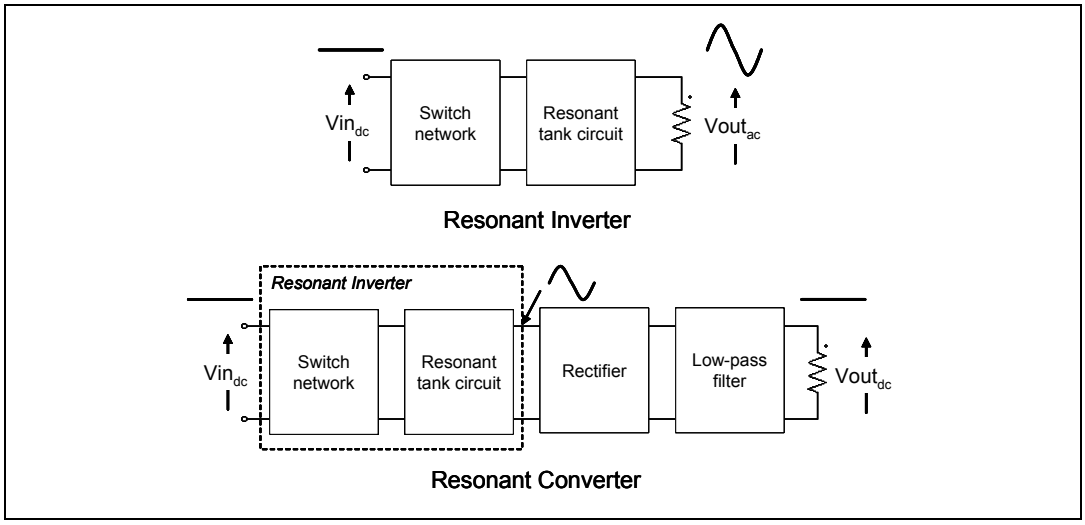
Contents

List of figures

1 Classification of resonant converters

Resonant conversion is a topic that is at least thirty years old and where much effort has been spent in research in universities and industry because of its attractive features: smooth waveforms, high efficiency and high power density. Yet the use of this technique in off-line powered equipment has been confined for a long time to niche applications: high-voltage power supplies or audio systems, to name a few. Quite recently, emerging applications such as flat panel TVs on one hand, and the introduction of new regulations, both voluntary and mandatory, concerning an efficient use of energy on the other hand, are pushing power designers to find more and more efficient AC-DC conversion systems. This has revamped and broadened the interest in resonant conversion. Generally speaking, resonant converters are switching converters that include a tank circuit actively participating in determining input-to-output power flow. The family of resonant converters is extremely vast and it is not an easy task to provide a comprehensive picture. To help find one's way, it is possible to refer to a property shared by most, if not all, of the members of the family. They are based on a "resonant inverter", i.e. a system that converts a DC voltage into a sinusoidal voltage (more generally, into a low harmonic content ac voltage), and provides ac power to a load. To do so, a switch network typically produces a square-wave voltage that is applied to a resonant tank tuned to the fundamental component of the square wave. In this way, the tank will respond primarily to this component and negligibly to the higher order harmonics, so that its voltage and/or current, as well as those of the load, will be essentially sinusoidal or piecewise sinusoidal. As shown in *Figure 2*, a resonant DC-DC converter able to provide DC power to a load can be obtained by rectifying and filtering the ac output of a resonant inverter.

Figure 2. General block diagram of a resonant inverter, the core of resonant converters



Different types of DC-AC inverters can be built, depending on the type of switch network and on the characteristics of the resonant tank, i.e. the number of its reactive elements and their configuration [*1*].

As to switch networks, we will limit our attention to those that drive the resonant tank symmetrically in both voltage and time, and act as a voltage source, namely the half-bridge and the full-bridge switch networks. Borrowing the terminology from power amplifiers,

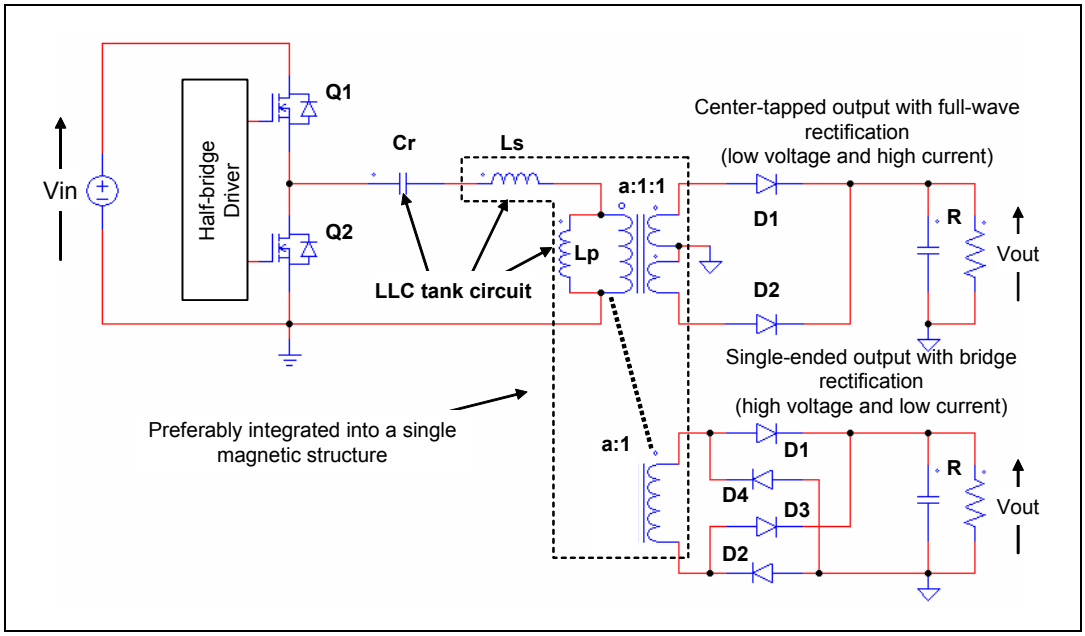
switching inverters driven by this kind of switch network are considered part of the group called "class D resonant inverters".

As to resonant tanks, with two reactive elements (one L and one C) there are a total of eight different possible configurations, but only four of them are practically usable with a voltage source input. Two of them generate the well-known series resonant converter and parallel resonant converter considered in [2] and thoroughly treated in literature.

With three reactive elements the number of different tank circuit configurations is thirty-six, but only fifteen can be used in practice with a voltage source input. One of these, commonly called LCC because it uses one inductor and two capacitors, with the load connected in parallel to one C, generates the LCC resonant inverter commonly used in electronic lamp ballast for gas-discharge lamps. Its dual configuration, using two inductors and one capacitor, with the load connected in parallel to one L, generates the LLC inverter.

As previously stated, for any resonant inverter there is one associated DC-DC resonant converter, obtained by rectification and filtering of the inverter output. Predictably, the above-mentioned class of inverters will originate the "class D resonant converters". Considering off-line applications, in most cases the rectifier block will be coupled to the resonant inverter through a transformer to guarantee the isolation required by safety regulations. To maximize the usage of the energy handled by the inverter, the rectifier block can be configured as either a full-wave rectifier, which needs a center tap arrangement of transformer's secondary winding, or a bridge rectifier, in which case tapping is not needed. The first option is preferable with a low voltage / high current output; the second option with a high voltage / low current output. As to the low-pass filter, depending on the configuration of the tank circuit, it will be made by capacitors only or by an L-C type smoothing filter. The so-called "series-parallel" converter described in [2], typically used in high-voltage power supply, is derived from the previously mentioned LCC resonant inverter. Its dual configuration, the LLC inverter, generates the homonymous converter, addressed in [3], [4] and [5], that will be the subject of the following discussion. In particular we will consider the half-bridge implementation, illustrated in *Figure 3*, but the extension to the full-bridge version is quite straightforward.

Figure 3. LLC resonant half-bridge schematic



In resonant inverters (and converters too) power flow can be controlled by the switch network either by changing the frequency of the square wave voltage, or its duty cycle, or both, or by special control schemes such as phase-shift control. In this context we will focus on power flow control by frequency modulation, that is, by changing the frequency of the square wave closer to or further from the tank circuit's resonant frequency while keeping its duty cycle fixed.

2 The LLC resonant half-bridge converter

2.1 General overview

According to another way of designating resonant converters, the LLC resonant half-bridge belongs to the family of multiresonant converters. Actually, since the resonant tank includes three reactive elements (Cr, Ls and Lp, shown in *Figure 3*), there are two resonant frequencies associated to this circuit. One is related to the condition of the secondary winding(s) conducting, where the inductance Lp disappears because dynamically shorted out by the low-pass filter and the load (there is a constant voltage a V_{out} across it):

Equation 1

$$f_{R1} = \frac{1}{2\pi\sqrt{Ls \cdot Cr}}$$

the other resonant frequency is relevant to the condition of the secondary winding(s) open, where the tank circuit turns from LLC to LC because Ls and Lp can be unified in a single inductor:

Equation 2

$$f_{R2} = \frac{1}{2\pi\sqrt{(Ls + Lp)Cr}}$$

It will be of course $f_{R1} > f_{R2}$. Normally, f_{R1} is referred to as the resonance frequency of the LLC resonant tank, while f_{R2} is sometimes called the second (or lower) resonance frequency. The separation between f_{R1} and f_{R2} depends on the ratio of Lp to Ls. The larger this ratio is, the further the two frequencies will be and vice versa. The value of Lp/Ls (typically > 1) is an important design parameter.

It is possible to show that for frequencies $f > f_{R1}$ the input impedance of the loaded resonant tank is inductive and that for frequencies $f < f_{R2}$ the input impedance is capacitive. In the frequency region $f_{R2} < f < f_{R1}$ the impedance can be either inductive or capacitive depending on the load resistance R. A critical value R_{crit} exists such that if $R < R_{crit}$ then the impedance will be capacitive, inductive for $R > R_{crit}$. For a given tank circuit the value of R_{crit} depends on f. More precisely, in [*6*] it is shown that for any tank circuit configuration (then for the LLC in particular):

Equation 3

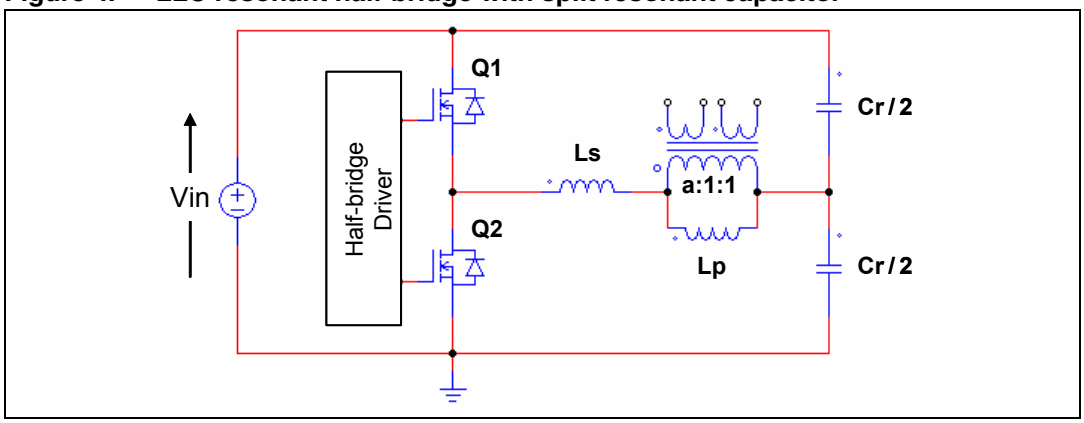
$$R_{crit} = \sqrt{Zo_0 \cdot Zo_\infty}$$

where Zo_0 and Zo_∞ are the resonant tank output impedances with the source input short-circuited and open-circuited, respectively.

For certain reasons that will be clarified in the following sections, the LLC resonant converter is normally operated in the region where the input impedance of the resonant tank has inductive nature, i.e. it increases with frequency. This implies that power flow can be controlled by changing the operating frequency of the converter in such a way that a reduced power demand from the load produces a frequency rise, while an increased power demand causes a frequency reduction.

The Half-bridge Driver switches the two power MOSFETs Q1 and Q2 on and off in phase opposition symmetrically, that is, for exactly the same time. This is commonly referred to as "50% duty cycle" operation even if the conduction time of either power MOSFET is slightly shorter than 50% of the switching period. In fact, a small deadtime is inserted between the turn-off of either switch and the turn-on of the complementary one. The role of this deadtime is essential for the operation of the converter. It goes beyond ensuring that Q1 and Q2 will never cross-conduct and will be clarified in the next sections as well. For the moment it will be neglected, and the voltage applied to the resonant tank will be a square-wave with 50% duty cycle that swings all the way from 0 to V_{in}. Before going any further, however, it is important to make one concept clear.

Figure 4. LLC resonant half-bridge with split resonant capacitor



A few paragraphs above, the impedance of the tank circuit was mentioned. Impedance is a concept related to linear circuits under sinusoidal excitation, whereas in this case the excitation voltage is a square wave.

However, as a consequence of the selective nature of resonant tanks, most power processing properties of resonant converters are associated with the fundamental component of the Fourier expansion of voltages and currents in the circuit. This applies in particular to the input square wave and is the foundation of the First Harmonic Approximation (FHA) modeling methodology presented in [2] as a general approach and used in [4] and [5] for the LLC resonant converter specifically. This approach justifies the usage of the concept of impedance as well as those coming from complex ac circuit analysis.

Coming back to the input square wave excitation, it has a DC component equal to $V_{in}/2$. In the LLC resonant tank the resonant capacitor Cr is in series to the voltage source and under steady state conditions the average voltage across inductors must be zero. As a result, the DC component $V_{in}/2$ of the input voltage must be found across Cr which consequently plays the double role of resonant capacitor and DC blocking capacitor.

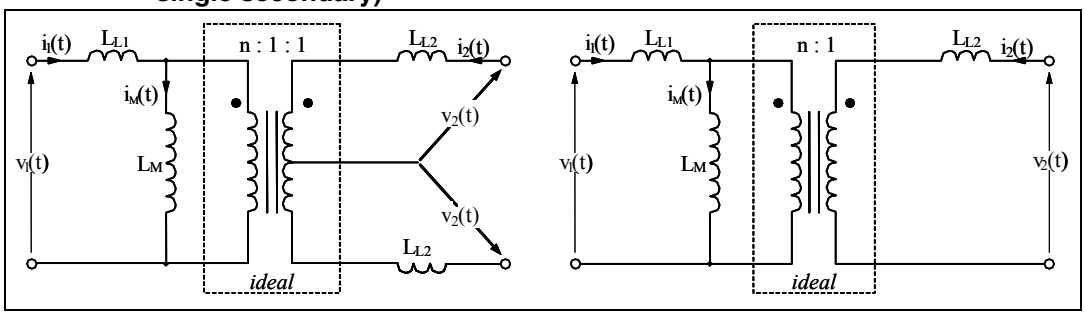
It is possible to see, especially at higher power levels, a slightly modified version of the LLC resonant half-bridge converter, where the resonant capacitor is split as illustrated in *Figure 4*. This configuration can be useful to reduce the current stress in each capacitor

and, in certain conditions, the initial imbalance of the V·s applied to the transformer at start up (see "Converter's start-up" section). Additionally, it makes the input current to the converter look like that of a full-bridge converter, as shown in *Appendix E*, with a resulting reduction in both the input differential mode noise and the stress of the input capacitor. Obviously, the currents through Q1 and Q2 will be unchanged. It is easy to recognize that the two Cr/2 capacitors are dynamically in parallel, so that the total resonant tank's capacitance is again Cr.

The system appears quite bulky, with its three magnetic components. However, the LLC resonant topology lends itself well to magnetic integration. With this technique inductors and transformers are combined into a single physical device to reduce component count, usually with little or no penalty to the converter's characteristics, sometimes even enhancing its operation. To understand how magnetic integration can be done, it is worth looking at the well-known equivalent schematics of a real transformer in *Figure 5* and comparing them to the inductive component set of *Figure 3*.

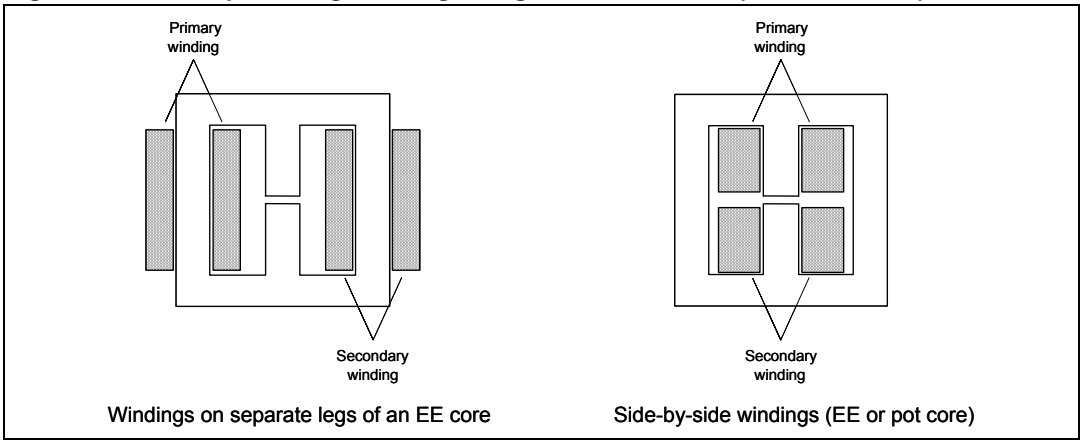
Lp occupies the same place as the magnetizing inductance L_M, Ls the same place as the primary leakage inductance L_{L1}. Then, assuming that we are going to use a ferrite core plus bobbin assembly, Lp can be used as the magnetizing inductance of the transformer with the addition of an air gap into the magnetic circuit and leakage inductance can be used to make Ls.

Figure 5. Equivalent schematic of a real transformer (left, tapped secondary; right, single secondary)



To do so, however, a leaky magnetic structure is needed, which is contrary to the traditional transformer design practice that aims at minimizing leakage inductance. The usual concentric winding arrangement is not recommended here, although higher leakage inductance values can be achieved by increasing the space between the windings.

Figure 6. Example of high-leakage magnetic structures (cross-section)



It is difficult, however to obtain reproducible values, because they depend on parameters (such as winding surface irregularities or spacer thickness) difficult to control. Other fashions are recommended, such as placing the windings on separate core legs (using E or U cores) or side by side on the same leg which is possible with both E and pot cores and shown in *Figure 6*. They permit reproducible leakage inductance values, because related to the geometry and the mechanical tolerances of the bobbin, which are quite well controlled. In addition, these structures possess geometric symmetry, so they lead to magnetic devices with an excellent magnetic symmetry.

However, in the real transformer model of *Figure 5* there is the secondary leakage inductance L_{L2} that is not considered in the model of *Figure 3*. The presence of L_{L2} is not a problem from the modeling point of view because the transformer's equivalent schematic can be manipulated so that L_{L2} disappears (it is transferred to the primary side and incorporated in L_{L1}). This is exactly what has been done in the transformer model shown in *Figure 3*. Then, it is important to underline that Ls and Lp are not real physical inductances (L_{L1}, L_M and L_{L2} are), their numerical values are different ($L_s \neq L_{L1}$, $Lp \neq L_M$), and, finally, the turn ratio a is not the physical turn ratio $n=N_1/N_2$. Ls and Lp can be given a physical interpretation. L_s is the inductance of the primary winding measured with the secondary winding(s) shorted, while Lp is the difference between the inductance of the primary winding measured with the secondary windings open and L_s.

However, L_{L2} is not free from side effects. For a given impressed voltage, L_{L2} decreases the voltage available on the secondary winding, which carries a current i_2, by the drop $L_{L2} \cdot di_2/dt$. This is an effect that is taken into account by the above mentioned manipulation of the transformer model. In addition, in multioutput converters, where there is leakage inductance associated to each output winding, cross-regulation between the various outputs will be adversely affected because of their decoupling effect.

Finally, there is one more adverse effect to consider in the center-tapped output configuration. With reference to *Figure 3* and *5*, when one half-winding is conducting, the voltage $v_2(t)$ externally applied to that half-winding is $V_{out}+V_F$ (V_F is the rectifier forward drop of the conducting diode). With no secondary leakage inductance, this voltage will be found across the secondary winding of the ideal transformer and then coupled one-to-one to the nonconducting half-winding. Consequently, the reverse voltage applied to the reverse-biased rectifier will be $2 \cdot V_{out}+V_F$. If now we introduce the leakage inductance L_{L2}, the drop $L_{L2} \cdot di_2/dt$ adds up to $V_{out}+V_F$ and is reflected to the other half-winding as well. As a result, the reverse voltage applied to the nonconducting rectifier will be increased by $L_{L2} \cdot di_2/dt$. Note that in case of single-winding secondary with bridge rectification, the voltage applied to reverse-biased diodes of the bridge is only $V_{out}+V_F$ and is not affected by L_{L2}. The reason is that the negative voltage of the secondary winding is fixed at $-V_F$ externally and is not determined by internal coupling like in the case of tapped secondary.

It is worth pointing out that the 50% duty cycle operation of the LLC half-bridge equalizes the stress of secondary rectifiers both in terms of reverse voltage - as just seen - and forward conduction current. In fact, each rectifier carries half the total output current under all operating conditions. Then, if compared to similar PWM converters (such as the ZVS Asymmetrical Half-bridge, or the Forward converter), in the center-tapped output configuration the equal reverse voltage typically allows the use of lower blocking voltage rating diodes. This is especially true when using common cathode diodes housed in a single package. A lower blocking voltage means also a lower forward drop for the same current rating, and then lower losses.

It must be said, however, that in the LLC resonant converter the output current form factor is worse, so the output capacitor bank is stressed more. Although the stress level is

considerably lower than that in a flyback converter, as shown in *Table 1*, this is one of the few real drawbacks of the topology.

Table 1. Output stress for LLC resonant half-bridge vs. PWM topologies @ 50% duty cycle

Output current form factors	Forward - ZVS AHB	LLC resonant HB	Flyback (CCM-DCM boundary)
Peak-to-DC ratio	≈1.05÷1.15	$\approx \frac{\pi}{2} = 1.57$	4
Rms-to-DC ratio	≈1	$\approx \frac{\pi}{2\sqrt{2}} = 1.11$	$\sqrt{\frac{8}{3}} \approx 1.63$
AC-to-DC ratio	≈0.03÷0.09	$\approx \sqrt{\frac{\pi^2}{8} - 1} = 0.48$	$\sqrt{\frac{8}{3} - 1} \approx 1.29$

Additional details concerning power losses will be discussed in *Analysis of power losses on page 41*.

To complete the general picture on the LLC resonant converter, there is another aspect that needs to be addressed concerning parasitic components which affect the behavior of the circuit.

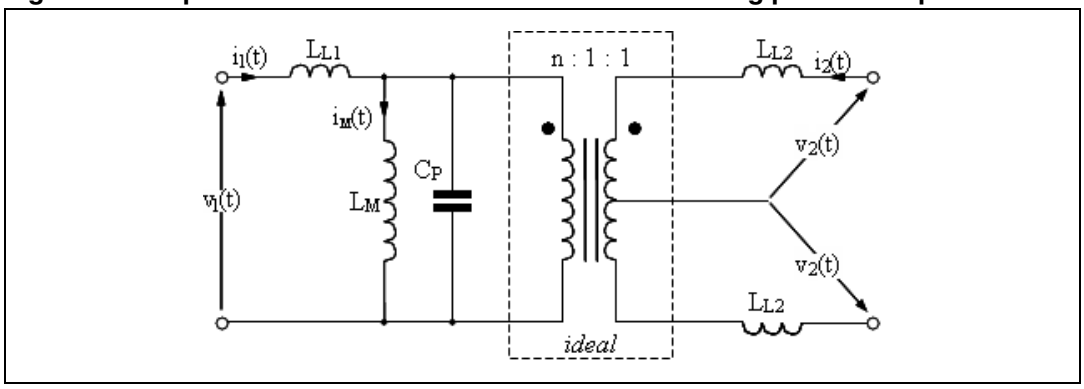
The first parasitic element to consider is the capacitance of the midpoint of the half-bridge structure, the node common to the source of the high-side power MOSFET and to the drain of the low-side power MOSFET. Its effect is that the transitions of the half-bridge midpoint will require some energy and take a finite time to complete. This is linked to the previously mentioned deadtime inserted between the turn-off of either switch and the turn-on of the complementary one, and will be discussed in more detail in *Section 2.2*.

The second parasitic element to consider is the distributed capacitance of transformer's windings. This capacitance, which exists for both the primary and the secondary windings, in combination with windings' inductance, originates what is commonly designated as the transformer "self-resonance". In addition to this capacitance one needs to consider also the junction capacitance of the secondary rectifiers, which adds up to that of the secondary windings and lowers the resulting self-resonance frequency (loaded self-resonance).

The effect of all this parasitic capacitance can be modeled with a single capacitor C_P connected in parallel to L_M as illustrated in *Figure 7*. The resonant tank, as a consequence, turns from LLC to LLCC. This 4^{th}- order tank circuit features a third resonance frequency at the transformer's loaded self-resonance ($f_{LSR} > f_{R1}$). When the operating frequency is considerably lower than f_{LSR} the effect of C_P is negligible. However, at frequencies greater than f_{R1} and if the load impedance is high enough, its effect starts making itself felt, eventually resulting in reversing the transferable power vs. frequency relationship as frequency approaches f_{LSR}. Power now increases with the switching frequency, feedback becomes positive and the converter loses control of the output voltage. The onset of this "feedback reversal" in closed-loop operation is revealed by a sudden frequency jump to its maximum value as the load falls below a critical value (i.e. the frequency exceeds a critical value) and a simultaneous output voltage rise.

In some way, either appropriately choosing the operating frequency range ($<< f_{LSR}$) or increasing f_{LSR}, the converter must work away from feedback reversal. This usually sets the practical upper limit to a converter's operating frequency range.

Figure 7. Equivalent schematic of a transformer including parasitic capacitance



2.2 The switching mechanism

Still another way of classifying resonant converters would include the LLC resonant half-bridge in the family of "resonant-transition" converters. This nomenclature refers to the fact that in this class of converters power switches are driven in such a way that a resonant tank circuit is stimulated to create a zero-voltage condition for them to turn-on.

To understand how this can be achieved in the LLC half-bridge, it is instructive to consider the circuits illustrated in *Figure 8* where the switches Q1 and Q2 that generate the square wave input voltage to the resonant tank are power MOSFETs. Their body diodes DQ1, DQ2 are pointed out because they play an important role. In circuit a), the drain-to-source parasitic capacitances C_{oss1}, C_{oss2} are pointed out as well. In fact, as far as voltage changes of the node HB are concerned, the parasitic capacitances Cgd and Cds are effectively in parallel, then Cgd+Cds=C_{oss} has to be considered.

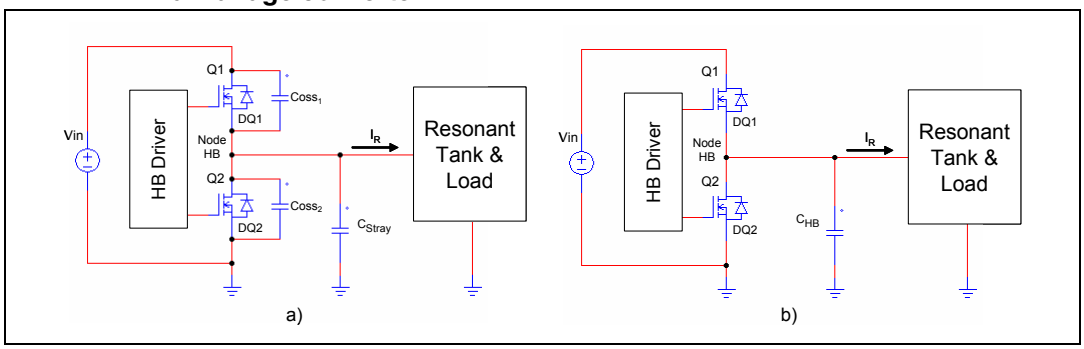
Additionally, other contributors to the parasitic capacitance of the node HB (e.g. that formed between the case of the power MOSFETs and the heat sink, the intrawinding capacitance of the resonant inductor, etc.) are lumped together in the capacitor C_{Stray}. Note that C_{oss1}, like C_{oss2}, is connected between the node HB and a node having a fixed voltage (V_{in} for C_{oss1}, ground for C_{oss2}). Then, as far as voltage changes of the node HB are concerned, C_{oss1} is effectively connected in parallel to C_{oss2} and C_{Stray}. It is convenient to lump all of them together in a single capacitor C_{HB} from the node HB to ground, as shown in the circuit b):

Equation 4

$$C_{HB} = C_{OSS1} + C_{OSS2} + C_{Stray}$$

which we will refer to in the following discussion. Note also that C_{oss1} and C_{oss2} are non-linear capacitors, i.e. their value is a function of the drain-to-source voltage. It is intended that their time-related equivalent value will be considered (see *Appendix A*).

Figure 8. Power MOSFET totem-pole network driving a resonant tank circuit in a half-bridge converter

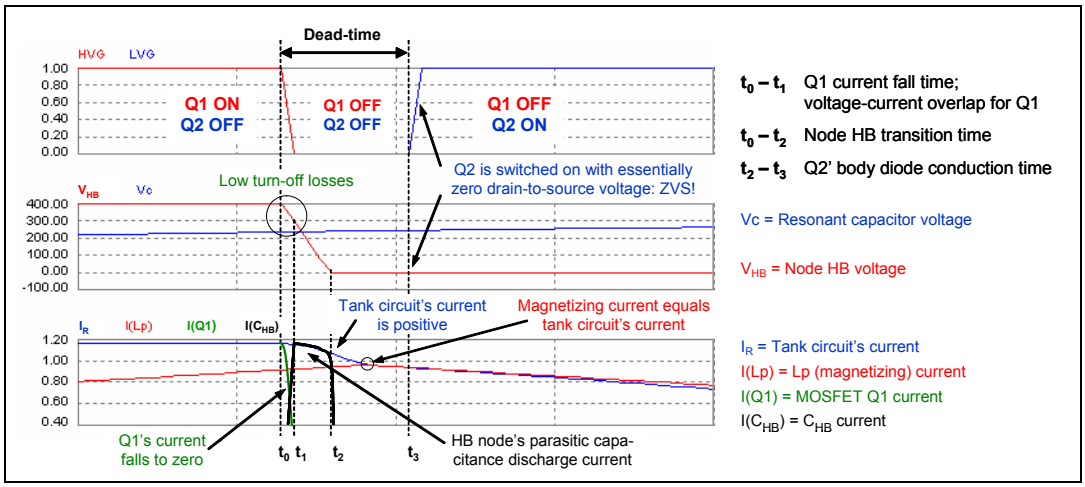


As previously stated, there is no overlap between the conduction of Q1 and Q2. Additionally, a deadtime T_D between the transitions from one state to the other of either switch, where they both are open, is intentionally inserted. It is intended that when Q1 is closed and Q2 is open, the voltage applied to the resonant tank circuit is positive. Similarly we will define as negative the voltage applied to the resonant tank circuit when Q1 is open and Q2 is closed. Consistently with two-port circuits sign convention, the input current to the resonant tank, I_R, will be positive if entering the circuit, negative otherwise.

Let us assume Q1 closed and Q2 open. It is then $I_R = I(Q1)$. Despite that the voltage applied to the circuit is positive ($V_{HB} = V_{in}$), I_R can flow in either direction since we are in presence of reactive elements. Let us suppose that I_R is entering the tank circuit (positive current) in the instant t_0 when Q1 opens, and refer to the timing diagram of *Figure 9*.

The current through Q1 falls quickly and becomes zero at $t = t_1$. Q2 is still open and I_R must keep on flowing almost unchanged because of the inductance of the resonant tank that acts as a current flywheel. The electrical charge necessary to sustain I_R will come initially from C_{HB}, initially charged at V_{in}, which will be now discharged. Provided $I_R(t_1)$ is large enough, the voltage of the node HB will then fall at a certain rate until $t = t_2$, when its voltage becomes negative and the body diode of Q2, DQ2, becomes forward biased, thus clamping the voltage at a diode forward drop V_F below ground. I_R will go on flowing through DQ2 for the remaining part of the deadtime T_D until $t = t_3$, when Q2 turns on and its $R_{DS(on)}$ shunts DQ2. When this occurs, the voltage across Q2 is $-V_F$, a value negligible as compared to the input voltage V_{in}. In the end, this is what is called zero-voltage switching (ZVS): the turn-on transition of Q2 is done with negligible dissipation due to voltage-current overlap and with C_{HB} already discharged, there will be no significant capacitive loss either. Note, however, that there will be nonnegligible power dissipation associated to Q1's turn-off because there will be some voltage-current overlap during the time interval $t_0 - t_1$.

Figure 9. Detail of Q1 ON-OFF and Q2 OFF-ON transitions with soft-switching for Q2



There is an additional positive side effect in turning on Q2 with zero drain-to-source voltage. It is the absence of the Miller effect, normally present in power MOSFETs at turn-on when hard-switched. In fact, as the drain-to-source voltage is already zero when the gate is supplied, the drain-to-gate capacitance Cgd cannot "steal" the charge provided to the gate. The so-called "Miller plateau", the flat portion in the gate voltage waveform, as well as the associated gate charge, is missing here and less driving energy is therefore required. Note that this property provides a method to check if the converter is running with soft-switching or not by looking at the gate waveform of Q2 (which is more convenient because it is source-grounded), as shown in *Figure 10* and *11*.

Figure 10. Q2 gate voltage at turn-on: with soft-switching

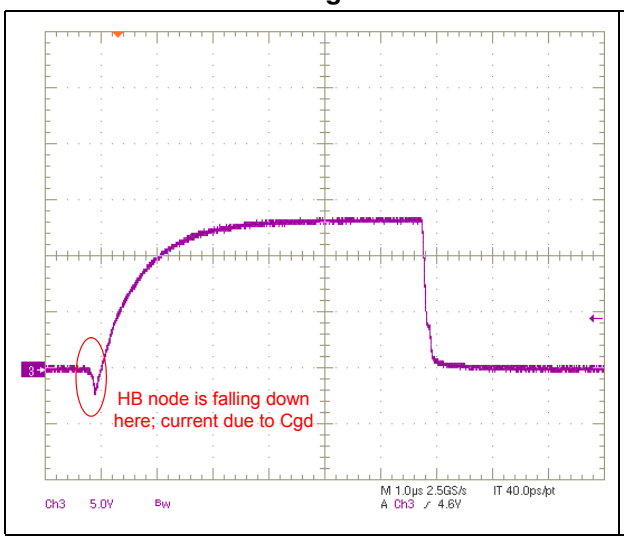
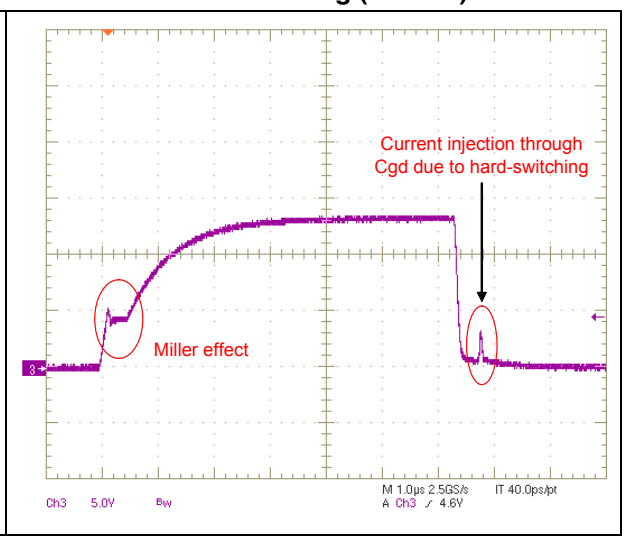


Figure 11. Q2 gate voltage at turn-on: with hard-switching (no ZVS)



With similar reasoning it is possible to understand that the same ZVS mechanism occurs to Q1 when it turns on if I_R is flowing out of the resonant tank circuit (negative current).

In the end we can conclude that, if the tank current at the instant of half-bridge transitions has the same sign as the impressed voltage, both switches will be "soft-switched" at turn-on, i.e. turned on with zero voltage across them (ZVS). It is intuitive that this sign coincidence

occurs if the tank current lags the impressed voltage (e.g. it is still positive while voltage has already gone to zero), which is a condition typical of inductors. In other words, ZVS occurs if the resonant tank input impedance is inductive. The frequency range where tank current lags the impressed voltage is therefore called the "inductive region".

It is worth emphasizing the essential role of DQ1 and DQ2 in ensuring continuity to current flow and clamping the voltage swing of the node HB at $V_{in}+V_F$ and $-V_F$ respectively (the LLC resonant half-bridge belongs to the family of ZVS clamped-voltage topologies). Power MOSFETs, with their inherent body diodes are therefore the best suited power switches to be used in this converter topology. Other types of switches, such as BJT or IGBT, would need the addition of external diodes.

Going back to the state when Q1 is closed and Q2 open, let us now assume that at the instant t_0 when Q1 opens, current is flowing out of the resonant tank towards the input source, i.e. it is negative. This operation is shown in the timing diagrams of *Figure 12*.

With Q1 now open the current will go on flowing through DQ1 throughout the deadtime, and will eventually be diverted through Q2 only when Q2 closes at $t = t_1$, the end of the deadtime. As far as Q1 is concerned, then, there will be no loss associated to turn-off because the voltage across it does not change significantly (it is essentially the same situation seen at turn-on when the converter works in the inductive region).

Q2, instead, will experience now a totally different situation. As DQ1 is conducting during the deadtime, the voltage across Q2 at $t = t_1$ equals $V_{in}+V_F$ so that there will be not only a considerable voltage-current overlap but the energy of C_{HB} will be dissipated inside its $R_{DS(on)}$ as well. In this respect, it is a "hard-switching" condition identical to what normally happens in PWM-controlled converters at turn-on. The associated power dissipation $½C_{HB}V_{in}^2f$ may be considerably higher than that normally dissipated under "soft-switching" conditions and this may easily lead to Q1 overheating, since heat sinking is not usually sized to handle this abnormal condition.

In addition to that, at $t = t_1$ the body diode of Q1, DQ1, is conducting current and its voltage is abruptly reversed by the node HB being forced to ground by Q2. Hence, DQ1 will keep its low impedance and there will be a condition equivalent to a shoot-through between Q1 and Q2 until it recovers (at $t = t_2$).

It is well-known the power MOSFET's body diodes do not have brilliant reverse recovery characteristics. Hence DQ1 will undergo a reverse current spike large in amplitude (it can be much larger than the forward current it was carrying at $t=t_1$) and relatively long in duration (in the hundred ns) that will go through Q2 as well. This spike, in fact, cannot flow through the resonant tank because Ls does not allow for abrupt current changes.

This is a potentially destructive condition not only because of the associated power dissipation that adds up to the others previously considered, but also due to the current and voltage of DQ1 which are simultaneously high during part of its recovery. In fact, there will be an extremely high dv/dt (many tens of V/ns!) experienced by Q1 as DQ1 recovers and the voltage of the node HB goes to zero. This dv/dt may exceed Q1 rating and lead to an immediate failure because of the second breakdown of the parasitic bipolar transistor intrinsic in power MOSFET structure. Finally, it is also possible that Q1 is parasitically turned on if the current injected through its Cgd and flowing through the gate driver's pull down, which is holding the gate of Q1 low, is large enough to raise the gate voltage close to the turn-on threshold (see the spike after turn-off in the graph of *Figure 11*). This would cause a lethal shoot-through condition for the half-bridge leg.

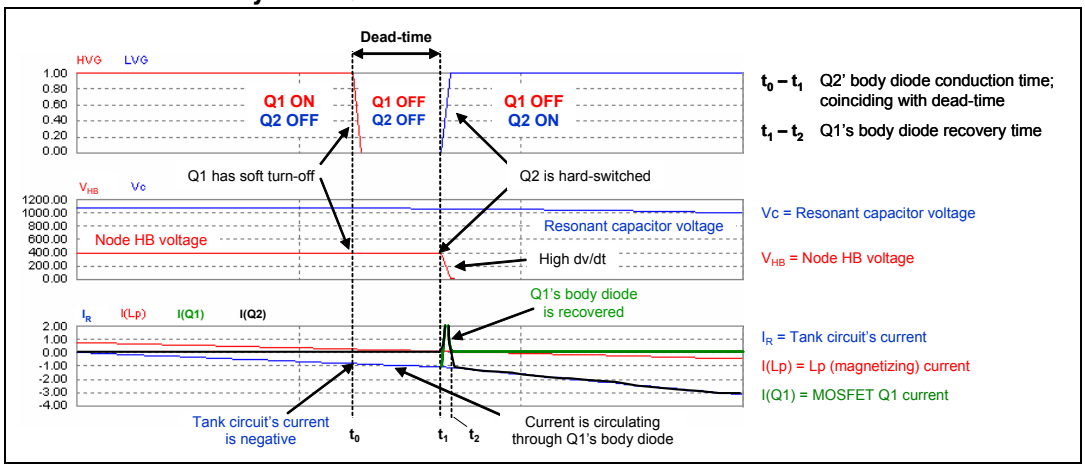
An additional drawback of this operation is the large and energetic negative voltage spikes induced by the recovery of DQ1 because of the unavoidable parasitic inductance of the PCB

subject to its di/dt, which may damage any control IC coupled to the half-bridge leg, not to mention the big EMI generation.

Similarly, it is possible to show that the same series of adverse events will happen to Q1 and Q2, with exchanged roles, when Q2 is turned off if I_R is flowing into the resonant tank circuit (positive current).

The obvious conclusion is that, if the tank current and the impressed voltage at the instant of half-bridge transitions have opposite signs, both switches will be hard-switched and the reverse recovery of their body diodes will be invoked, with all the resulting negative effects. It is intuitive that this sign opposition occurs if the tank current leads the impressed voltage, which is typical of capacitors and then occurs if the resonant tank input impedance is capacitive. This kind of operation is often termed "capacitive mode" and the frequency range where tank current leads the impressed voltage is called the "capacitive region".

Figure 12. Q1 ON-OFF and Q2 OFF-ON transitions with hard switching for Q2 and recovery for DQ1



Then, the converter must be operated in the region where the input impedance is inductive (the inductive region), that is, for frequencies $f > f_{R1}$ or in the range $f_{R2} < f < f_{R1}$ provided the load resistance R is such that $R > R_{crit}$. This is a necessary condition in order for Q1 and Q2 to achieve ZVS, which is evidently a crucial point for the good operation of the LLC resonant half-bridge.

To summarize, ZVS brings the following benefits:

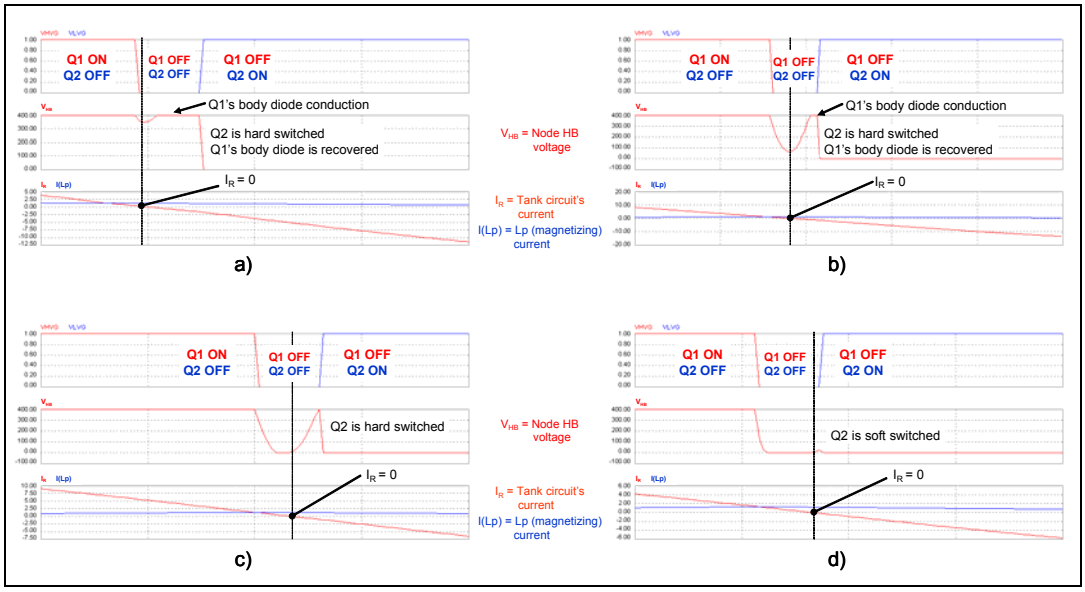
1. low switching losses: either high efficiency can be achieved if the half-bridge is operated at a not too high switching frequency (for example < 100 kHz) or high switching frequency operation is possible with a still acceptably high efficiency (definitely out of reach with a hard-switched converter);
2. reduction of the energy needed to drive Q1 and Q2, thanks to the absence of Miller effect at turn-on. Not only is turn-on speed unimportant because there is no voltage-current overlap but also gate charge is reduced, then a small source capability is required from the gate drivers.
3. low noise and EMI generation, which minimizes filtering requirements and makes this converter extremely attractive in noise-sensitive applications.
4. all of the above-mentioned adverse effects of capacitive mode, which not only impair efficiency but also jeopardize the converter, are prevented.

Note, however, that working in the inductive region is not a sufficient condition in order for ZVS to occur.

In the above discussion, it has been said that the voltage of the node HB could swing from V_{in} to zero "provided I_R is large enough". Of course the same holds if we consider node HB's swing from zero up to V_{in}. What actually happens when Q1 turns off with positive I_R current is that the associated inductive energy level of the resonant tank circuit is maintained at the expense of the energy contained in the capacitance C_{HB}. If the inductive energy ($\propto I_R^2$) is greater than that owned by C_{HB} ($\propto V_{in}^2$) C_{HB} will be completely depleted and the voltage of the node HB will be able to reach $-V_F$, injecting DQ2 and allowing Q2 to turn-on with essentially zero drain-to-source voltage. Similarly, when Q2 turns off with negative current, part or all of the associated inductive energy will be transferred to C_{HB}. If the available inductive energy is greater than that needed to charge C_{HB} up to $V_{in}+V_F$, the node HB will be allowed to swing all the way up until DQ1 is injected, thus clamping the voltage, and Q1 will be able to turn-on with essentially zero drain-to-source voltage.

Seen from a different perspective, the inductive part of the tank circuit resonates with C_{HB}, and this is the origin of the term "resonant transition" used for designating resonant converters having this property. This "parasitic" tank circuit active during transitions is formed by C_{HB} with the series inductance Ls if during the half-bridge transition there is current circulating on the secondary side (so that Lp is shorted out) or with the total inductance Ls + Lp if there is no current conduction on the secondary side.

Figure 13. Bridge leg transitions in the neighborhood of inductive-capacitive regions boundary



The above mentioned energy balance considerations, however, are not still sufficient to guarantee ZVS under all operating conditions. There is an additional element that needs to be considered, the duration of the deadtime T_D.

The first obvious consideration is that the duration of the deadtime represents an upper limit to the time the node HB takes to swing from one rail to the other: in order for the mosfet that is about to turn on to achieve ZVS (i.e. to be turned on with zero drain-to-source voltage), the transition has to be completed within T_D as depicted in *Figure 9*. However, the way the

deadtime and ZVS are related is actually more complex and depends on converter's operating conditions.

It is instructive to see this in *Figure 13*, which shows typical node HB waveforms occurring when working in the inductive region but too close to the capacitive region, so that ZVS is not achieved. They refer to the Q1 →OFF, Q2 → ON transition; those related to the opposite transition are obviously turned upside down.

- Case a) is very close to the boundary between inductive and capacitive regions. Tank current reverses just after Q1 is switched off, a portion of node HB ringing appears as a small "dip", then the tank current becomes negative enough to let the body diode of Q1 start conducting. When Q2 turns on there are capacitive losses and the recovery of the Q1's body diode with all the related issues.
- Case b) is slightly more in the inductive region but still I_R crosses zero within the deadtime. The node HB ringing becomes larger and the body diode of Q1 still conducts for a short time and its recovery is invoked as Q2 turns on.
- Case c) Is even more in the inductive region but still not sufficiently away from the capacitive-inductive boundary. The ringing of the node HB is large enough to reach zero but I_R reverses within the deadtime and the voltage goes up again. At the end of the deadtime the voltage does not reach Vin, hence the body diode of Q1 does not conduct and Q2, when turned on, will experience only capacitive losses.
- Case d) Is further in the inductive region and I_R crosses zero nearly at the end of the deadtime. Q2 is now almost soft-switched with no losses. This can be considered as the boundary of the operating region where ZVS can be achieved with the given duration of T_D.

Note that the resonant tank's current during node HB ringing is lower than the one flowing through Lp. This means that their difference is flowing into the transformer and, consequently, that one of the secondary half-windings is conducting. Therefore, C_{HB} is resonating with Ls only.

This analysis shows that there is a "border belt" in the inductive region, close to the boundary with the capacitive region ($f_{R2} < f < f_{R1}$, $R = R_{crit}$) and that as converter's operation is moved away from the capacitive-inductive boundary and pushed more deeply in the inductive region there is a progressive behavior change from hard-switching to soft-switching. In the cases a and b the inductive energy in the resonant tank is too small to let the node HB even swing "rail-to-rail"; moving away from the boundary, as shown in case c, the energy is higher and allows a rail-to-rail swing, but it is not large enough to keep the node HB "hooked" to the rail throughout the deadtime T_D. If the converter is operated in this border belt, Q1 and Q2 will be hard-switched at turn-on and, in cases such as case a and case b, the body diode of the just turned off power MOSFET is injected and then recovered as the other power MOSFET turns on.

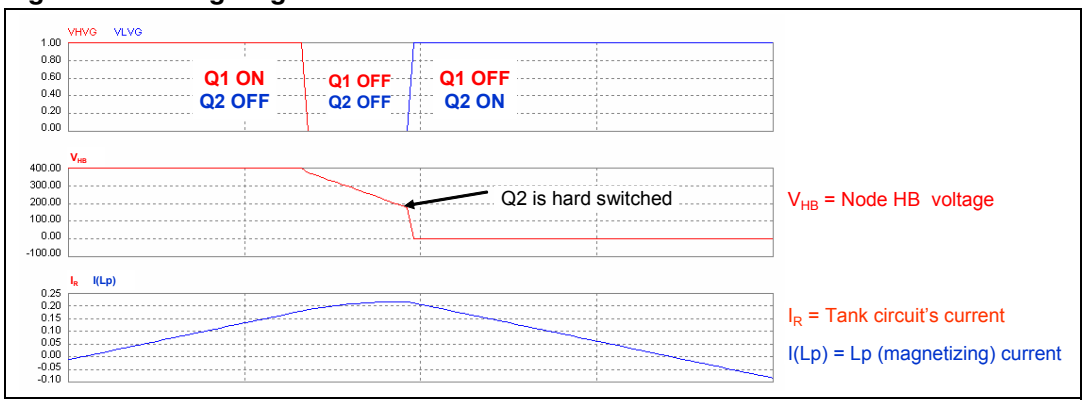
Case b and, especially, case c highlight that it is possible to look at the deadtime T_D also from another standpoint: looking at those waveforms, one might conclude that the current I_R at the beginning of the deadtime is too low or, conversely, that the deadtime is too long. In case c, for example, if the dead-time had been approximately half the value actually shown, Q2 would have been soft-switched at turn-on. Of course, the more appropriate interpretation depends on whether T_D is fixed or not.

These cases are related to heavy load conditions.

Figure 14 shows a case typical of no-load conditions, where ZVS is not achieved because of a too slow transition of the node HB so that it does not swing completely within the deadtime T_D. In this case the situation seems less stressful than operating in the capacitive region.

There is no body diode conduction and, consequently, no recovery. Q1 will be almost soft-switched at turn-off, while Q2 will have capacitive losses at turn-on. It is true that the turn-on voltage is lower than V_{in}, thus the associated energy of C_{HB} is lower, but at no-load the operating frequency is usually considerably higher than in the capacitive region, then these power losses may easily overheat Q1 and Q2. Finally, note in *Figure 14* that I(Lp) is exactly superimposed on I_R, then the secondary side of the transformer is open and C_{HB} is resonating with the total inductance Ls+Lp.

Figure 14. Bridge leg transitions under no-load conditions



From what we have seen we can conclude that the conditions in order for the half-bridge switches to achieve ZVS are:

1. Under heavy load conditions, as one switch turns off, the tank current must have the same sign as the impressed voltage and be large enough so that both the rail-to-rail transition of the node HB is completed and the current itself does not reverse before the end of the deadtime, when the other switch turns on.
2. With no-load, the tank current at the moment one switch turns off (which has definitely the same sign as the impressed voltage) must be large enough to complete the node HB transition within the deadtime, before the other switch turns on.

Both conditions can be translated into specifying a minimum current value I_{Rmin} that needs to be switched when either power MOSFET turns off. In general, different I_{Rmin} values are needed to ensure ZVS at heavy load and at no-load. One can simply pick the greater one to ensure ZVS under any operating condition by design. On the other hand, this minimum required amount of current is to the detriment of efficiency.

At light or no-load a significant current must be kept circulating in the tank circuit, just to maintain ZVS, in spite of the current delivered to the load that is close to zero or zero. Using ac-analysis terminology, a certain amount of reactive energy is required even with no active energy.

Finally, also at heavy load the value of I_{Rmin} to be specified is the result of a trade-off. In fact, its value is directly related to the turn-off losses of both Q1 and Q2. The higher the switched current is, the larger the switching loss due to voltage-current overlap will be.

The discussion on the switching mechanism has been focused on the primary-side switches, and the conditions in order for them to achieve soft-switching (ZVS at turn-on, precisely) have been found. One important merit of the LLC resonant converter is that also the rectifiers on the secondary side are soft-switched. They feature zero-current switching (ZCS) at both turn-on and turn-off. In fact, at turn-on the initial current is always zero and ramps up with a relatively low di/dt, so that forward recovery does not come into play. At turn-off they become reverse biased when their forward current is already zero, so that their

reverse recovery is not invoked. This topic will be addressed in *Section 2.3*, where it will be shown that this property is inherent in the topology, hence it occurs regardless of converter's design or operating conditions.

2.3 Fundamental operating modes

The LLC resonant half-bridge converter features a considerable number of different operating modes, which stem from its multiresonant nature. Essentially, the term "multiresonant" means that the configuration of the resonant tank may change within a single switching cycle. We have seen that there are two resonant frequencies, one (the higher) associated to either of the secondary rectifiers conducting, the lower one associated to both rectifiers non-conducting. Then, depending on the input-to-output voltage ratio, the output load and the characteristics of the resonant tank circuit, the secondary rectifiers can be always conducting (with the exception of a single point in time), which is referred to as CCM (Continuous Conduction Mode) like in PWM converters, or there can be finite time intervals during which neither of the secondary rectifiers is conducting. This will obviously be called a DCM (Discontinuous Conduction Mode) operating mode.

Different kinds of CCM and DCM operating modes exist, although not all of them can be seen in a given converter, some are not even recommended, like those associated with capacitive mode operation. However, in all CCM modes the parallel inductance Lp is always shunted by the load resistance reflected back to the primary side, so that it never participates in resonance, rather it acts as an additional load to the remaining LC resonant circuit. Similarly, in all DCM modes, there will be some finite time intervals where Lp, being no longer shunted from the secondary side, becomes part of resonance.

In the following we will consider four fundamental operating modes and use the nomenclature defined in [*3*]:

1. Operation at resonance, when the converter works exactly at $f = f_{R1}$;
2. Above-resonance operation, when the converter works at a frequency $f > f_{R1}$. Moving away from resonance, we will consider three sub-modes:
   a) CCMA operation at heavy load;
   b) DCMA operation at medium load;
   c) DCMAB operation at light load;
3. Below-resonance operation, when the converter works at a frequency $f_{R2} < f < f_{R1}$ with a load resistor $R > R_{crit}$. Moving away from resonance, we will consider two sub-modes:
   a) DCMAB operation at medium-light load;
   b) DCMB operation at heavy load;
4. Below-resonance operation, when the converter works at a frequency $f_{R2} < f < f_{R1}$ with a load resistor $R < R_{crit}$ (capacitive mode), corresponding to the CCMB operating mode defined in [*3*];

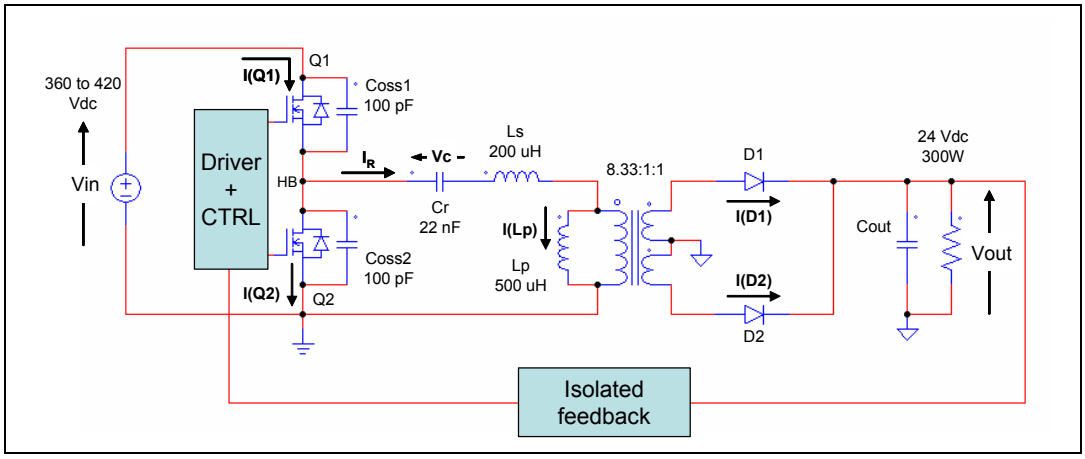
In addition, two extreme operating conditions will be considered:

1. No-load operation (cutoff)
2. Output short-circuit operation

It is interesting to point out that, unlike PWM converters where DCM operation is invariably associated to light load operation and CCM to heavy load operation, in the LLC resonant converter this combination does not hold.

To illustrate the above-mentioned operating modes we will refer to the reference converter shown in *Figure 15*. The discussion will start from the inspection of the main waveforms in a switching cycle, highlighting each subinterval where the circuit assumes a topological state and deducing the properties of the converter when operated in that mode from those waveforms. Half-bridge leg transitions are considered instantaneous. Their features have been already discussed.

Figure 15. Reference LLC converter for the analysis of the fundamental operating modes



2.3.1 Operation at resonance ($f = f_{R1}$)

In this operating mode it is possible to distinguish six fundamental time subintervals within a switching cycle, which are illustrated in *Figure 16*.

The first subinterval and, then, the instant t_0 can be chosen quite arbitrarily. We fix t_0 as the instant when, with Q1 conducting and Q2 open, the tank current I_R has a positive-going zero-crossing.

a) $t_0 \rightarrow t_1$. Q1 is ON and Q2 is OFF. This is the "energy taking" phase, when current flows from the input source to the tank circuit, so that energy is positive and both refills the resonant tank and supplies the load. The operating point of Q1 is in the first quadrant (current is flowing from drain to source). D2 is reverse-biased with a voltage $-2 \cdot V_{out}$ (it is actually larger because of the contribution from the secondary leakage inductance L_{L2}). D1 is conducting, so Lp is shorted by the output load reflected back to the primary side and the voltage across it is fixed at $a \cdot V_{out}$. Lp, then, is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. During this phase, which ends when Q1 is switched off at $t=t_1$, I_R reaches its maximum value, after that it starts decaying. Note that at $t=t_1$ I_R=I(Lp) and then I(D1)=0.

b) $t_1 \rightarrow t_2$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_1$ I(Q1)=I(Lp)=I_R is greater than zero and provides the energy to let the node HB swing from V_{in} to 0, so that the body diode of Q2, DQ2, is injected. This allows I_R to flow. The voltage across Lp reverses to $-a \cdot V_{out}$ and the slope of its current changes sign. D2 starts conducting while D1 is reverse biased with a negative voltage approximately equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). This phase ends when Q2 is switched on at $t=t_2$.

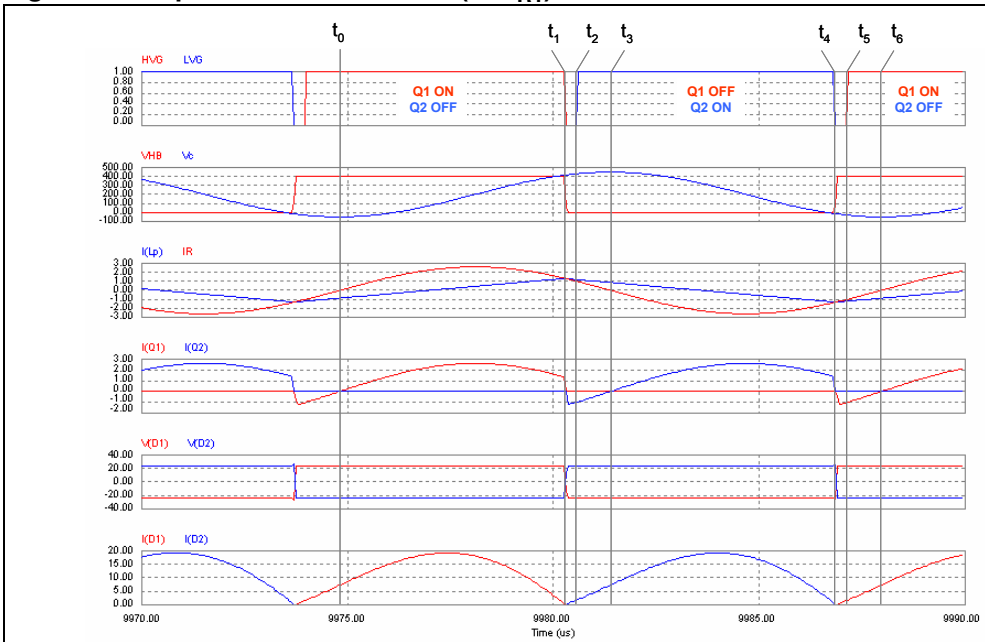
c) $t_2 \rightarrow t_3$. Q1 is OFF and Q2 is ON. At $t=t_2$ I_R is diverted from DQ2 to the $R_{DS(on)}$ of Q2, so that no significant energy is lost during the turn-on transient. Note that now

the operating point of Q2 is in the third quadrant, current is flowing from the source to drain. D2 keeps on conducting and the voltage across Lp is $-a \cdot V_{out}$, so that Lp is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. This phase ends when $I_R=0$ at $t=t_3$.

d) $t_3 \rightarrow t_4$. Q1 is OFF and Q2 is ON. Tank circuit current, which is zero at $t=t_3$ becomes negative. D1 is non-conducting and its reverse voltage is approximately $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). Lp's current has a negative slope, so the voltage across Lp must be negative. Since the diode D2 is conducting, this voltage will be equal to $-a \cdot V_{out}$. Lp, then, is not participating in resonance, Cr is resonating with Ls only and I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. During this phase, which ends when Q2 is switched off at $t=t_4$, I_R reaches its minimum value, after that it starts increasing. Note that at $t=t_4$ $I_R=I(Lp)$ and then $I(D2)=0$.

e) $t_4 \rightarrow t_5$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_4$ $I(Q2)=-I(Lp)=-I_R$ is greater than zero and provides the energy to let the node HB swing from 0 to V_{in}, so that the body diode of Q1, DQ1, is injected. This allows I_R to flow back to the input source. The voltage across Lp reverses to a V_{out} and its current slope changes sign. D1 starts conducting while D2 is reverse biased with a negative voltage approximately equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). This phase ends when Q1 is switched on at $t=t_5$.

Figure 16. Operation at resonance ($f = f_{R1}$): main waveforms



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

f) $t_5 \rightarrow t_6$. Q1 is ON and Q2 is OFF. At $t=t_5$ I_R is diverted from DQ1 to the $R_{DS(on)}$ of Q1, so that no significant energy is lost during the turn-on transient. Note that now the operating point of Q1 is in the third quadrant, current is flowing from the source to drain. This phase, along with the preceding one can be referred to as the "external energy recirculation phase": current is negative (coming out of the input terminal) despite that the impressed voltage is positive so that the input energy is

negative, i.e. it is returned to the input source. D1 keeps on conducting and the voltage across Lp is $a \cdot V_{out}$, so that Lp is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. This phase ends when $I_R=0$ at $t=t_6$ and another switching cycle starts.

Remarks

1. Parallel inductor Lp never resonates and its current is essentially triangular (note: the real magnetizing current is sinusoidal and cannot be seen on the oscilloscope). The LLC converter, then, can be regarded as a series LC resonant half-bridge (composed by Ls and Cr) that supplies a reactive RL load (composed by Lp and R_{ac}, the equivalent ac resistor loading the converter, as defined in [2] and reflected back to the primary side). This standpoint provides considerable insight into the operation of the converter, as shown in some of the following remarks.
2. In a resistively loaded series LC tank operating at resonance, the impressed voltage and the tank current are exactly in-phase, hence the switched current is zero and, thereby, ZVS cannot be achieved. The effect of adding an inductor (Lp) in parallel to the resistive load is to provide tank current with the phase shift (lagging) necessary to switch a current greater than zero, so that ZVS becomes now possible at resonance. As shown in the diagrams of *Figure 16*, the tank circuit current lags the impressed voltage by an angle φ equal to:

Equation 5

$$\varphi = 2\pi\frac{t_6 - t_4}{t_6 - t_0}$$

so that they have the same sign at half-bridge leg transitions. Furthermore, the switched currents $I_R(t_1)$ and $I_R(t_4)$ are large enough to complete the HB node swing well within the deadtimes (t_1, t_2) and (t_4, t_5) respectively. It is not difficult to recognize that the angle φ is the phase of the input impedance of the loaded resonant tank evaluated at $f=f_{R1}$. Additionally, since the impedance of a series LC tank operating at resonance is zero, it is possible to state that the input impedance of the LLC resonant tank at resonance equals the impedance of the RL load.

3. Generally speaking, in a series LC tank operating at resonance, the voltage drop across L is equal in module and opposite in sign to the drop across C at all times (this is why its impedance is zero). In our specific case the drop across the series Cr-Ls will be zero, so that it is possible to write the following voltage balance equations:

Equation 6

$$V_{in} - \frac{V_{in}}{2} = a \cdot V_{out} \qquad \text{Q1 ON, Q2 OFF}$$

$$-\frac{V_{in}}{2} = -a \cdot V_{out} \qquad \text{Q1 OFF, Q2 ON}$$

both of them resulting in the following relationship:

Equation 7

$$\frac{V_{in}}{2} = a \cdot V_{out}$$

This is a fundamental property of the LLC resonant half-bridge: operating at $f=f_{R1}$ implies that input and output voltages fulfill (1) and, vice versa, if input and output voltages meet *Equation 7* the converter is operating at $f=f_{R1}$. Then, the fact that the converter operates at resonance or not, for a given output voltage V_{out} and a given turn

ratio a (n), depends only on the input voltage, not on the load and on the parameters of the resonant tank. From the design point of view, since V_{in} and V_{out} are specified, one can decide the input voltage where to operate at resonance by choosing the turns ratio a. $V_{in}/2=a \cdot V_{out}$ considered as the 1:1 conversion ratio for the LLC resonant half-bridge.

4. The logical consequence of LLC converter's ability to operate at resonance independently of the output load is that the LLC resonant half-bridge can deliver any power if operated at resonance. This can be seen also in another way. As the impedance of the series Cr-Ls is zero, the RL load R_{ac}//Lp "sees" the impressed voltage directly or, in other words, it is supplied by an ideal voltage source. This is a "singularity" in LLC converter's operation, sometimes referred to as the "load-independent" point, where the usual energy vs. frequency relationship does not hold. Actually, the inevitable voltage drops across the resistive elements of the real-world circuit (such as power MOSFETs' $R_{DS(on)}$, winding resistance, secondary rectifier's drop, etc.) cause a slight dependence of the frequency on the load. Note that this is a situation analog to that of CCM-operated PWM converters, where duty cycle is ideally independent of the load, in reality slightly dependent because of losses.
5. Energy is taken from the input source only from t_0 to t_1, the "energy taking" phase, then for less than half the switching period, while from t_1 to t_4 energy recirculates internally to allow energy flow to the load while Q1 is not conducting. This low "duty cycle" of the input current can be a limiting factor in terms of power handling capability, especially if the input voltage is low. This consideration suggests the use of the half-bridge topology in high input voltage applications (e.g. with a PFC front-end, which provides a 400 V input rail). The natural improvement to this limitation is the full-bridge topology, where phase d) becomes active as well.
6. Tank circuit current lag φ originates the external energy recirculation phase from t_4 to t_6 during which energy flow is negative (impressed voltage and input current have opposite signs). This energy subtracts to that drawn from the input during the energy taking phase a), hence reducing the net energy flow from the input source to the load each cycle. This energy can be regarded as reactive energy and cos φ as the input power factor. Making φ as small as possible (i.e. increasing Lp) would shorten the duration of the external energy recirculation phase and reduce the amount of reactive energy, thus improving the energy transfer process. This, however, would also reduce $I_R(t_1)$ and $I_R(t_4)$, hence φ can be reduced as long as ZVS is maintained.
7. Recalling that the current switched at turn-off by Q1, $I_R(t_1)$ and by Q2, $I_R(t_4)$ determine their switching losses, it is straightforward that keeping φ to the minimum value that ensures ZVS of Q1 and Q2 provides an optimum design. Of course, component tolerance must be adequately accounted for, thus φ must be larger than the minimum required and the typical operation will be suboptimal.
8. The secondary rectifiers D1 and D2 start conducting as Q2 and Q1 turn-off respectively. The initial current is zero and also its di/dt is low, thus they have a soft turn-on. D1 and D2 cease to conduct exactly when Q1 and Q2 turn-off, respectively. These are also the moments when the voltages across D1 and D2 reverse. As a result, neither D1 nor D2 experience a voltage reversal while conducting a forward current. Reverse recovery, with all its adverse effects, does not occur. Note that, in this respect, this is a situation identical to that of a PWM converter operating on the boundary between CCM and DCM.

2.3.2 Operation above resonance ($f > f_{R1}$)

In this operating mode the converter exhibits its usual frequency vs. load characteristic. We will consider three submodes where, in a closed-loop regulated system, CCM operation

progressively turns into DCM operation as the output load is reduced and frequency is moved away from resonance.

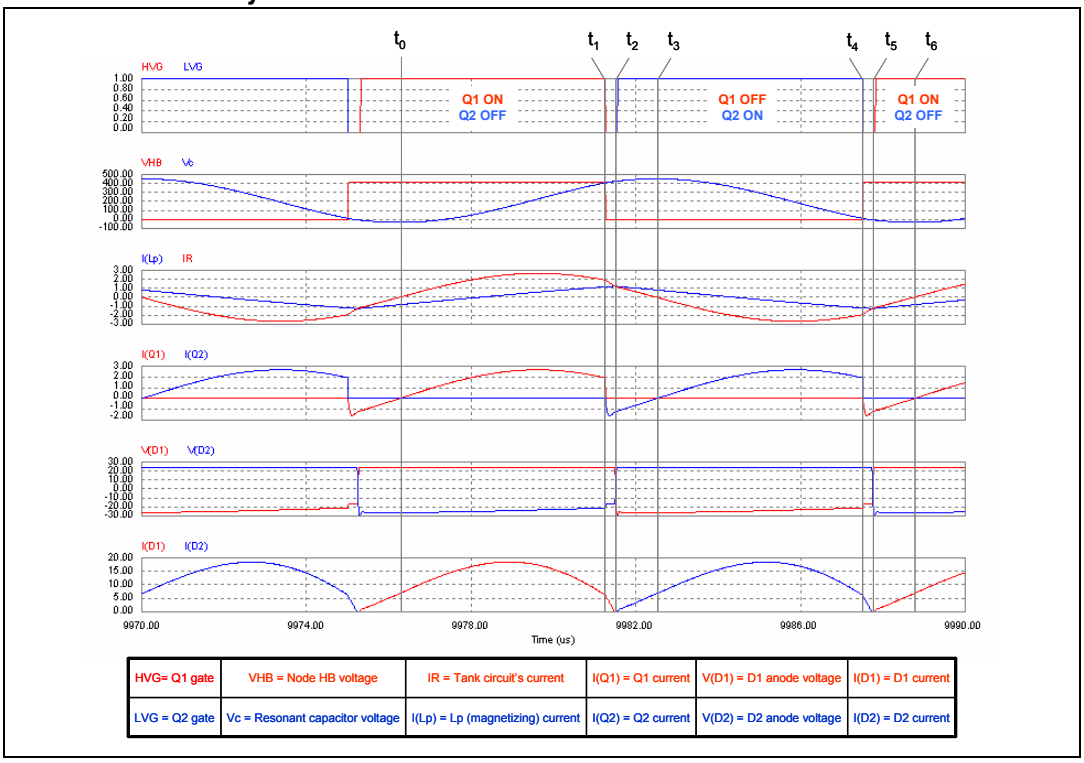
CCMA operation at heavy load

Also in this case it is possible to identify six fundamentals subintervals. The relevant waveforms are illustrated in the timing diagram of *Figure 17*. Again, t_0 is the instant when, with Q1 conducting and Q2 open, the tank current I_R has a positive-going zero-crossing.

a) $t_0 \rightarrow t_1$. Q1 is ON and Q2 is OFF. This is the "energy taking" phase. It is identical to the corresponding phase seen in the operation at resonance with the only difference that at the end of this phase, at $t=t_1$, it is still $I_R > I(Lp)$ and then $I(D1)>0$.

b) $t_1 \rightarrow t_2$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_1$ I_R is greater than zero and provides the energy to let the node HB swing from V_{in} to 0, so that the body diode of Q2, DQ2, is injected. This allows I_R to flow; I_R slope changes to a higher negative value, so that it quickly approaches I(Lp), which is still increasing with the same slope. D1 conducts until I_R equals I(Lp), and then becomes reverse biased, with a negative voltage equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown), I(Lp) slope changes sign and D2 starts conducting. This phase ends when Q2 is switched on at $t=t_2$. Note that the time Tz needed for I_R to hit I(Lp) is related to their values at $t=t_1$ and their slopes after $t=t_1$ and not to the duration of the deadtime T_D. Here it is $Tz = T_D$ just by chance.

Figure 17. Operation above resonance ($f > f_{R1}$): main waveforms in CCMA operation at heavy load



c) $t_2 \rightarrow t_3$. Q1 is OFF and Q2 is ON. At $t=t_2$ I_R is diverted from DQ2 to the $R_{DS(on)}$ of Q2, so that no significant energy is lost during the turn-on transient. This phase, which ends when $I_R=0$ at $t=t_3$, is identical to the (t_2, t_3) phase of the operation at resonance.

d) $t_3 \rightarrow t_4$. Q1 is OFF and Q2 is ON. It is identical to the phase (t_3, t_4) seen in the operation at resonance with the only difference that at the end of this phase, at $t=t_4$, it is still $I_R < I(Lp)$ and then $I(D2)>0$.

e) $t_4 \rightarrow t_5$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_4$ I_R is (in absolute value) greater than zero and provides the energy to let the node HB swing from 0 to V_{in}, so that the body diode of Q1, DQ1, is injected. This allows I_R to flow back to the input source. I_R changes to a higher slope, so that it quickly approaches I(Lp), which is still decreasing with the same slope. D2 conducts until I_R equals I(Lp), after that it becomes reverse biased, with a negative voltage approximately equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown), I(Lp) slope changes sign and D1 starts conducting. This phase ends when Q1 is switched on at $t=t_5$. Again, the time Tz needed for I_R to hit I(Lp) is only by chance equal to T_D as shown.

f) $t_5 \rightarrow t_6$. Q1 is ON and Q2 is OFF. At $t=t_5$ I_R is diverted from DQ1 to the $R_{DS(on)}$ of Q1, so that no significant energy is lost during the turn-on transient. This phase, which ends when $I_R=0$ at $t=t_6$, is identical to the (t_5, t_6) phase of the operation at resonance.

Remarks

1. In this "above-resonance" CCM submode the parallel inductor Lp never resonates and the LLC converter can be regarded as a series LC resonant half-bridge supplying a reactive RL load.
2. As shown in the diagrams of *Figure 17*, the tank circuit current lags the impressed voltage by an angle φ equal to:

Equation 8

$$\varphi = 2\pi \frac{t_6 - t_4}{t_6 - t_0}$$

so that they have the same sign at half-bridge leg transitions. Furthermore, the switched currents $I_R(t_1)$ and $I_R(t_4)$ are large enough to complete the HB node swing well within the deadtimes (t_1, t_2) and (t_4, t_5) respectively. Still φ is the phase of the input impedance of the loaded resonant tank evaluated at $f=f_{R1}$, but now since the impedance of the series LC tank is no longer zero, it is different from the impedance of the RL load.

3. In the series Cr-Ls tank circuit operating above resonance the voltage drop across it is positive (the inductive reactance is larger in module than the capacitive reactance), i.e. the plus sign is located on the side of the node HB. The obvious conclusion is that:

Equation 9

$$a \cdot V_{out} < \frac{V_{in}}{2}$$

Then, when operating above resonance, for a given input voltage the LLC resonant half-bridge will provide an output voltage lower than that available at resonance and vice versa, with a given output voltage the LLC resonant half-bridge will operate above resonance with an input voltage greater than $2 \cdot n \cdot V_{out}$. In this case the conversion ratio, intended as previously mentioned is < 1, then the LLC is said to have a "step-down" or "buck" characteristic when operating above resonance.

4. When operating above resonance, the Thevenin-equivalent schematic of the LLC resonant tank as seen by the load has finite impedance (no more zero as when operating at resonance). When the load current increases, for a given frequency (open-

loop operation) the voltage conversion ratio diminishes. For a given V_{out} (closed-loop operation) operating frequency needs to get back closer to resonance.

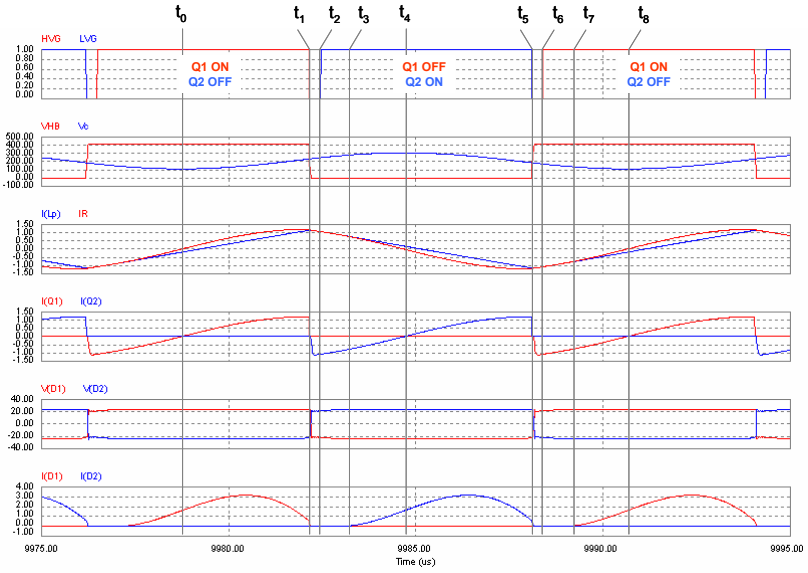
5. The secondary rectifiers D1 and D2 start conducting as Q1 and Q2 turn-on respectively. The initial current is zero and also its di/dt is low, thus they have a soft turn-on. D1 and D2 cease to conduct when tank circuit's current I_R equals Lp's current I(Lp). The transformer's secondary current is a·[I_R-I(Lp)], then the equality I_R = I(Lp) means that the secondary rectifiers current is zero as well. Unlike when operating at resonance, this does not happen synchronously with the half-bridge leg transitions (I_R < I(Lp) at t=t_1 and I_R > I(Lp) at t=t_4). However as the leg transition occurs I_R and I(Lp) are "forced" to become equal, then the current of the conducting diode goes to zero. The physical reason for that is the presence of Ls. When there is a transition of the half-bridge leg the resulting voltage change is not immediately directly impressed on the transformer (C can be considered as a short circuit during transitions, i.e. the voltage across it can be considered constant) but falls across Ls that acts as a "shock absorber". This leaves I(Lp) unchanged but pushes I_R towards I(Lp), forcing a rate of change that is approximately:

Equation 10

$$\frac{dI_R}{dt} \approx \begin{cases} -\dfrac{Vc + a \cdot V_{out}}{Ls} & t \in (t_1, t_2) \\ \dfrac{V_{in} - Vc + a \cdot V_{out}}{Ls} & t \in (t_4, t_5) \end{cases}$$

Only when I_R equals I(Lp) and no current is flowing through the secondary rectifier previously conducting can the voltage across the primary winding of the transformer reverse and hence also the voltage across the secondary rectifiers. In the end, also in this case they are reverse-biased only when their current has gone to zero, thus ensuring ZCS.

Figure 18. Operation above resonance (f > f_{R1}): main waveforms in DCMA operation at medium load



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

DCMA at medium load

In this "above-resonance" DCM submode it is possible to identify eight fundamentals subintervals. The relevant waveforms are illustrated in the timing diagram of *Figure 18*.

Two new subintervals, namely (t_2, t_3) and (t_6, t_7), appear just after the deadtimes of the half-bridge leg transitions (t_1, t_2), (t_5, t_6), respectively. The other six phases are exactly identical to those of the CCM above-resonance mode.

a) $t_2 \rightarrow t_3$. Q1 is OFF and Q2 is ON. At $t=t_2$ I_R is diverted from DQ2 to the $R_{DS(on)}$ of Q2, so that no significant energy is lost during the turn-on transient. Note that the operating point of Q2 is in the third quadrant, current is flowing from the source to drain. D1 is nonconducting but the voltage across the secondary windings is still too low to let D2 conduct, then still I_R = I(Lp) is a portion of a sinusoid having a frequency $f = f_{R2}$. This phase ends when D2 starts conducting at $t=t_3$.

b) $t_6 \rightarrow t_7$. Q1 is ON and Q2 is OFF. At $t=t_6$ I_R is diverted from DQ1 to the $R_{DS(on)}$ of Q1, so that no significant energy is lost during the turn-on transient. Note that the operating point of Q1 is in the third quadrant, current is flowing from the source to drain. D2 is nonconducting but the voltage across the secondary windings is still too low to let D1 conduct, then still I_R = I(Lp) is a portion of a sinusoid having a frequency $f = f_{R2}$. This phase ends when D1 starts conducting at $t=t_7$.

Remarks

1. In this "above-resonance" DCM submode the multiresonant nature of the LLC converter shows up. In a switching cycle there are two time intervals just after bridge-leg transitions during which no current is flowing on the secondary side (hence this is DCM operation), then the entire transformer's primary inductance Ls+Lp resonates and the second resonance frequency f_{R2} appears. At the transitions of the half-bridge leg the resonant current I_R is still slightly greater than I(Lp) in absolute value, so it takes a very small portion of the deadtimes for the two currents to equal each other. Then, the first one starts as I_R equals I(Lp) slightly after t_1 and ends at $t= t_3$. The second one starts slightly after t_5 and ends at $t= t_7$.
2. As shown in the diagrams of *Figure 18*, the tank circuit current is still lagging the impressed voltage, so that they have the same sign at half-bridge leg transitions. Furthermore, the switched currents $I_R(t_1)$ and $I_R(t_5)$ are large enough to complete the HB node swing well within the deadtimes (t_1, t_2) and (t_5, t_6) respectively. However, as compared to CCM mode, the duration of the energy taking phase (t_0, t_1) is shorter, the external recirculation phase is longer and the displacement angle φ:

Equation 11

$$\varphi = 2\pi\frac{t_8 - t_6}{t_8 - t_0}$$

gets close to $\pi/2$. Using ac terminology, the active energy is lower and the reactive energy is higher.

3. The secondary rectifiers D1 and D2 start conducting during the conduction period of Q1 and Q2, respectively. Both the initial current and also its di/dt are zero, thus they have a soft turn-on. D1 and D2 cease to conduct when tank circuit's current I_R equals Lp's current I(Lp). In this case this is almost synchronous with either switch turn-off. Again, only when I_R equals I(Lp) and no current is flowing through the secondary rectifier previously conducting can the voltage across the primary winding of the transformer reverse and hence also the voltage across the secondary rectifiers. In the

end, also in this case they are reverse-biased only when their current has gone to zero, thus ensuring ZCS.

4. Essentially, the reason why D2 does not conduct during (t_2, t_3) and D1 does not during (t_6, t_7) is that the voltage across the transformer (given by V_{in} - Vc) is not large enough so that the voltage developed across Lp (given by the inductive divider ratio Lp/(Ls+Lp)) and reflected to the secondary side can forward-bias D2 or D1. In formulae, this is expressed as:

Equation 12

$$(V_{in}(t) - Vc(t))\frac{Lp}{Ls + Lp} \leq a \cdot V_{out}$$

DCMAB at light load

In this "above-resonance" DCM sub-mode it is possible to identify ten fundamental subintervals. The relevant waveforms are illustrated in the timing diagram of *Figure 19*.

Two more new subintervals, namely (t_1, t_2), (t_6, t_7) appear just before the deadtimes of the half-bridge leg transitions (t_2, t_3), (t_7, t_8), respectively. The remaining eight phases are exactly identical to those of the DCMA above-resonance mode.

a) $t_1 \rightarrow t_2$. Q1 is ON and Q2 is OFF. At $t=t_1$ I_R equals I(Lp) and then I(D1) becomes zero before Q1 turns off at $t=t_2$, when this phase ends, and remains zero until $t=t_2$. During this interval the *Equation 12* is met and the current I_R = I(Lp) is a portion of a sinusoid having a frequency f = f_{R2}.

b) $t_6 \rightarrow t_7$. Q1 is OFF and Q2 is ON. At $t=t_6$ I_R equals I(Lp) and then I(D2) becomes zero before Q2 turns off at $t=t_7$, when this phase ends, and remains zero until $t=t_7$. During this interval the *Equation 12* is met and the current I_R = I(Lp) is a portion of a sinusoid having a frequency f = f_{R2}.

Remarks

1. The transition between this DCMAB mode and the previous DCMA is marked by the I_R = I(Lp) condition occurring exactly at t = t_1 of *Figure 18*.
2. In this "above-resonance" DCM submode, in a switching cycle there are two time intervals (t_1, t_4), (t_6, t_9) during which no current flows on the secondary side (hence this is DCM operation) and then the entire transformer's primary inductance Ls+Lp resonates and f_{R2} appears. Considering each half-cycle, nonconductive intervals appear at the beginning and the end.
3. As shown in the diagrams of *Figure 19*, the tank circuit current is still lagging the impressed voltage, so that they have the same sign at half-bridge leg transitions. Furthermore, the switched currents $I_R(t_2)$ and $I_R(t_6)$ are large enough to complete the HB node swing well within the deadtimes (t_2, t_3) and (t_7, t_8) respectively. As compared to DCMA mode, the duration of the energy taking phase (t_0, t_1) is even shorter, the external recirculation phase is longer and the displacement angle φ:

Equation 13

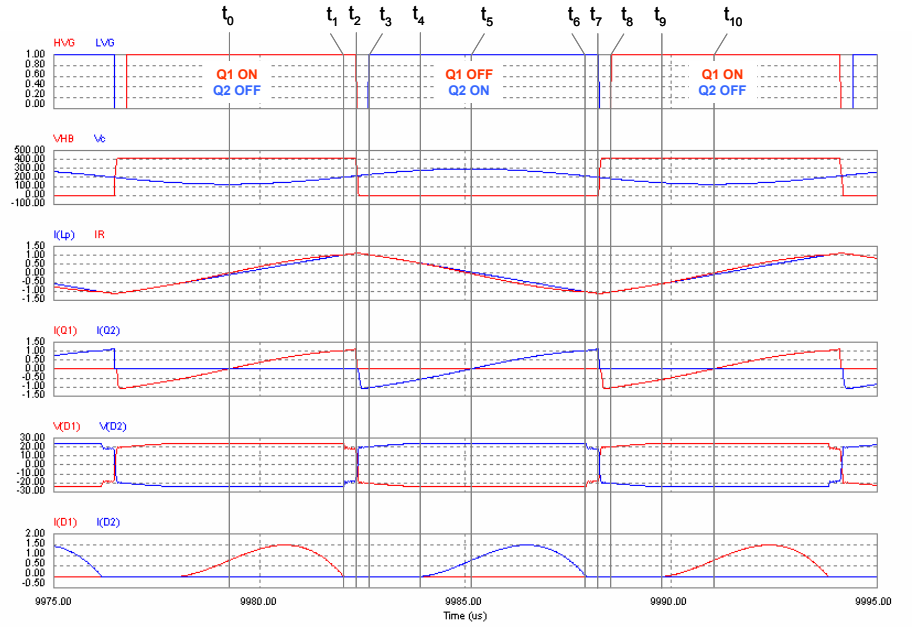
$$\varphi = 2\pi\frac{t_{10} - t_8}{t_{10} - t_0}$$

is even closer to $\pi/2$. Most of the energy in the tank circuit is reactive.

4. As to the secondary rectifiers, they start conducting during the conduction period of Q1 and Q2, respectively. Both the initial current and also its di/dt are zero, thus they have a

soft turn-on. They cease to conduct before the transitions of the half-bridge. The operation is DCM, then ZCS occurs by definition.

Figure 19. Operation above resonance (f > f_{R1}): main waveforms in DCMAB operation at light load



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

2.3.3 Operation below resonance (f_{R2} < f < f_{R1}, R>R_{crit})

In this operating mode the converter still exhibits its usual frequency vs. load characteristic. We will consider two submodes where, in a closed-loop regulated system, DCM operation gets deeper and deeper as the output load is increased and frequency is moved away from resonance.

DCMAB at medium-light load

This "below-resonance" DCM submode is exactly equal to the above-resonance DCMAB submode previously considered. The waveforms are shown in *Figure 20* and it is possible to see that they match those shown in *Figure 19*.

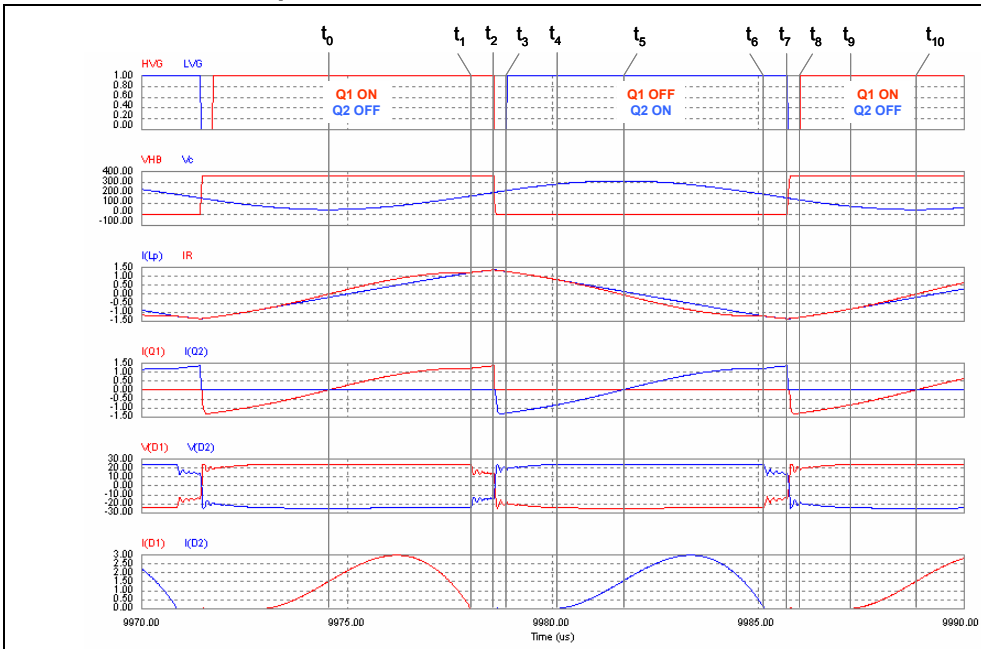
Note only that in this case the condition I_R = I(Lp) at t=t_1 occurs at a considerably higher power level than in the case of the above-resonance DCMAB submode (2:1 in the example shown).

DCMB at heavy load

This "below-resonance" DCM submode, which is unique to below resonance operation, actually comprises two submodes (DCMB2 & DCMB1) as frequency goes away from resonance. Their waveforms do not differ much, only those of DCMB2 will be shown. It is possible to identify eight fundamentals subintervals and the relevant waveforms are

illustrated in the timing diagram of *Figure 21*. Again, t_0 is the instant when, with Q1 conducting and Q2 open, the tank current I_R has a positive-going zero-crossing.

Figure 20. Operation below resonance ($f_{R2} < f < f_{R1}$, $R>R_{crit}$): main waveforms in DCMAB operation



a) $t_0 \rightarrow t_1$. Q1 is ON and Q2 is OFF. This is the "energy taking" phase, when current flows from the input source to the tank circuit, so that energy is positive. The operating point of Q1 is in the first quadrant (current is flowing from drain to source). D2 is nonconducting and its reverse voltage is approximately $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). D1 is conducting as well, so the voltage across Lp is a V_{out}. Lp, then, is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. During this phase, which ends when I_R equals I(Lp) and, then, I(D1)=0 at $t=t_1$, I_R reaches its maximum value, after that it starts decaying.

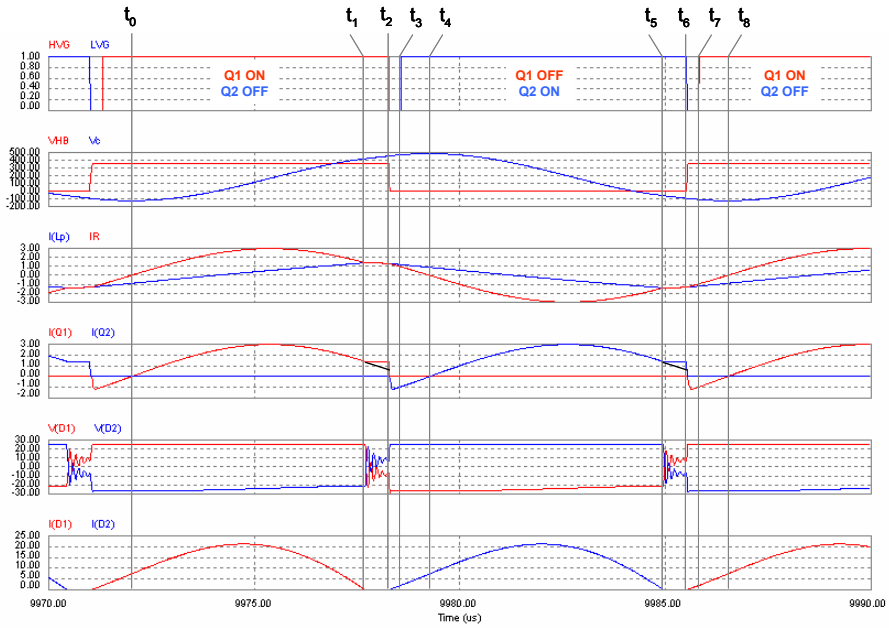
b) $t_1 \rightarrow t_2$. Q1 is ON and Q2 is OFF. At $t=t_1$ I(D1) becomes zero and I_R equals I(Lp), that is before the conduction time of Q2 ends. Both D1 and D2 are nonconducting and Lp, no longer shunted by the load reflected to the primary side, goes effectively in series to Ls and participates to resonance. I_R is a portion of a sinusoid having a frequency $f = f_{R2}$. Depending on the tank circuit's parameters and on the operating conditions, this portion can be similar to a straight line, as shown in the diagrams of *Figure 21*. This phase ends when Q1 is switched off at $t=t_2$.

c) $t_2 \rightarrow t_3$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_2$ $I(Q1)=I(Lp)=I_R$ is greater than zero and provides the energy to let the node HB swing from V_{in} to ground, so that the body diode of Q2, DQ2, is injected. This allows I_R to flow. The voltage across Lp reverses to $-a \cdot V_{out}$. D2 starts conducting while D1 is reverse biased with a negative voltage approximately equal to $2 \cdot V_{out}$

(plus the contribution from L_{L2}, not shown here). This phase ends when Q2 is switched on at $t=t_3$.

d) $t_3 \rightarrow t_4$. Q1 is OFF and Q2 is ON. At $t=t_3$ I_R is diverted from DQ2 to the $R_{DS(on)}$ of Q2, so that no significant energy is lost during the turn-on transient. Note that now the operating point of Q2 is in the third quadrant, current is flowing from the source to drain. D2 keeps on conducting and the voltage across Lp is $-a \cdot V_{out}$, so that Lp is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. This phase ends when $I_R=0$ at $t=t_4$.

Figure 21. Operation below resonance ($f_{R2} < f < f_{R1}$, $R>R_{crit}$): main waveforms in DCMB2 operation



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

e) $t_4 \rightarrow t_5$. Q1 is OFF and Q2 is ON. The tank circuit current, which is zero at $t=t_4$ becomes negative. D1 is nonconducting and its reverse voltage is approximately $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). Lp's current has a negative slope, so the voltage across Lp must be negative. Since the diode D2 is conducting this voltage will be equal to $-a \cdot V_{out}$. Lp, then, is not participating in resonance, Cr is resonating with Ls only and I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. During this phase, which ends when I_R equals I(Lp) and, thereby, I(D2) is zero at $t=t_{15}$. I_R reaches its minimum value, after that it starts increasing.

f) $t_5 \rightarrow t_6$. This phase mirrors (t_1, t_2). At $t=t_5$ I(D2) becomes zero and I_R equals I(Lp), that is before the conduction time of Q1 ends. Both D1 and D2 are nonconducting and Lp, no longer shunted by the load reflected to the primary side, goes effectively in series to Ls and participates to resonance. I_R is now a portion of a sinusoid having a frequency $f = f_{R2}$. This phase ends when Q2 is switched off at $t=t_6$.

g) $t_6 \rightarrow t_7$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_6$ $I_R = I(Lp)$ is (in absolute value) greater than zero and provides the energy to let the node HB swing from 0 to V_{in}, so that the body diode of Q1, DQ1, is injected. This allows I_R to flow back to the input source. The voltage across Lp reverses to a V_{out}, D1 starts conducting while D2 is reverse biased with a negative voltage approximately equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). This phase ends when Q1 is switched on at $t=t_7$.

h) $t_7 \rightarrow t_8$. Q1 is ON and Q2 is OFF. At $t=t_7$ I_R is diverted from DQ1 to the $R_{DS(on)}$ of Q1, so that no significant energy is lost during the turn-on transient. Note that now the operating point of Q1 is in the third quadrant, current is flowing from the source to drain. This phase, along with the preceding one is the "external energy recirculation phase": current is negative (coming out of the input terminal) despite that the impressed voltage is positive so that the input energy is negative, i.e. it is returned to the input source. D1 is still conducting and the voltage across Lp is a V_{out}, so that Lp is not participating in resonance anymore and Cr is resonating with Ls only. I_R is again a portion of a sinusoid having a frequency $f = f_{R1}$. This phase ends when $I_R=0$ at $t=t_8$ and another switching cycle begins.

Remarks

1. Also in this "below-resonance" DCM submode the multiresonant nature of the LLC converter shows up. From t_1 to t_2 and from t_5 to t_6 the secondary rectifiers are both open and the second resonance frequency f_{R2} appears. This is one of the fundamental advantages of the LLC resonant converter over the traditional LC series-resonant converter. In fact it helps keep operation away from capacitive mode. Although the tank circuit current I_R lags the impressed voltage (being $R>R_{crit}$ by assumption) so that they have the same sign at half-bridge leg transitions, the switching period is longer than the resonant period, $1/f_{R1}$. Then I_R, which is decaying (in absolute value), might come close to zero or even reverse if it still evolved according to the same sinusoid at frequency $f=f_{R1}$ (see the extrapolated black lines drawn in (t_1, t_2) and (t_5, t_6)). This lower frequency sinusoid "holds up" the tank current, hence ensuring that the switched currents $I_R(t_2)$ and $I_R(t_6)$ do not change sign and have amplitude large enough to complete the HB node swing well within the deadtimes (t_2, t_3) and (t_6, t_7) respectively, i.e. ZVS.
2. In the series LC tank Ls-Cr operating below resonance with $R>R_{crit}$ the voltage drop across the L-C series is negative (the capacitive reactance is larger in module than the inductive reactance), i.e. a minus sign is located at the node HB. As a result:

Equation 14

$$a \cdot V_{out} > \frac{V_{in}}{2}$$

Then, when operating below resonance, for a given input voltage, the LLC resonant half-bridge will provide an output voltage higher than that available at resonance, and vice versa, with a given output voltage the LLC resonant half-bridge will operate below a resonance if the input voltage is lower than $2 \cdot V_{out}$. In other words, the conversion ratio, intended as previously mentioned, is > 1, then the LLC is said to have a "step-up" characteristic when operating below resonance.

3. The secondary rectifiers D1 and D2 start conducting when Q2 and Q1 are switched off, respectively. The initial current is zero and its di/dt is low, thus they have a soft turn-on.

They cease to conduct before the transitions of the half-bridge. The operation is DCM, then ZCS occurs by definition.

4. Essentially, the reason why D2 does not conduct during (t_1, t_2) and D1 does not during (t_5, t_6) is that during these subintervals the condition expressed by *Equation 12* is met.
5. The waveforms in DCMB1 are very similar, only the portion of sinusoid at f = f_{R2} decays to zero more quickly. While DCMB2 is characterized by the duration of the intervals (t_1, t_2) and (t_5, t_6) that gets longer as frequency is reduced, in DCMB1 the duration of these intervals starts decreasing quite rapidly to reach zero at the boundary with capacitive mode operation. The "border belt" adjacent to the capacitive region is included in the region where DCMB1 occurs, thus it can be a good design practice to limit the operation of the converter to the DCMB1-DCMB2 boundary.

2.3.4 Capacitive-mode operation below resonance ($f_{R2} < f < f_{R1}$, $R<R_{crit}$)

In this operating mode, unique to below-resonance operation and corresponding to the CCMB operating mode defined in [3], it is possible to distinguish six fundamental time subintervals within a switching cycle, as illustrated in the timing diagrams of *Figure 22*.

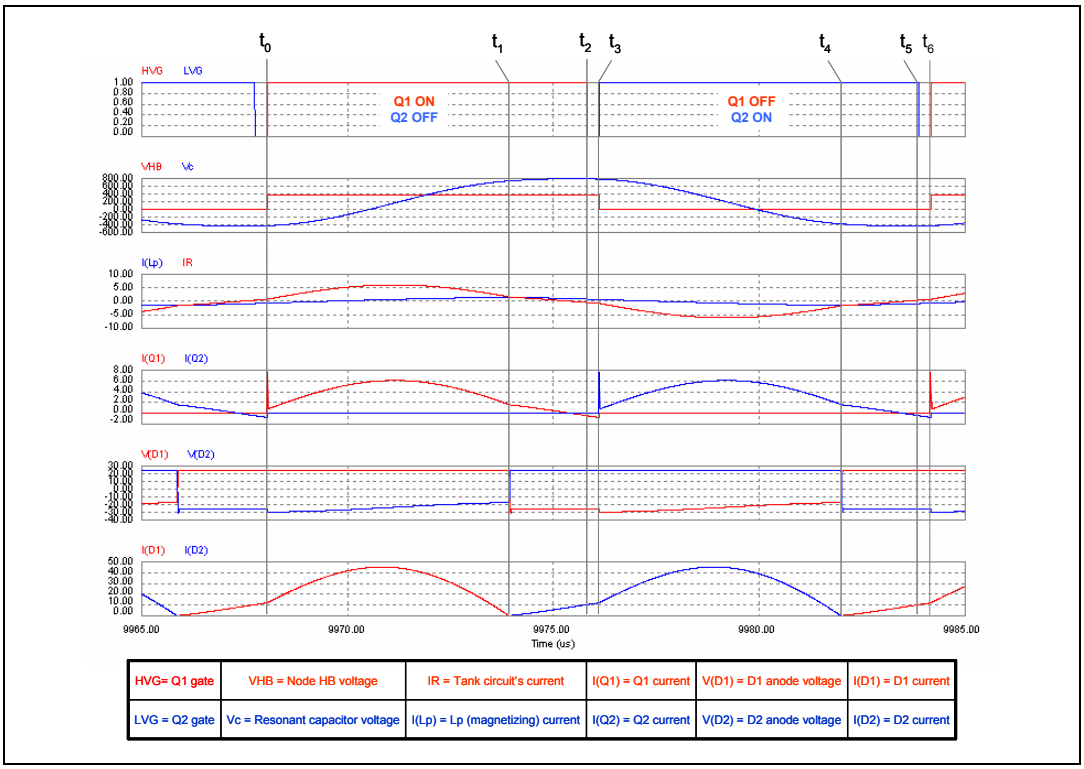
In this case it is convenient to define t_0 as the instant when Q1 is switched on.

a) $t_0 \rightarrow t_1$. The tank current $I_R(t_0)$ as Q1 is switched on is already positive: this means that in the just finished deadtime it was flowing through the body diode of Q2, DQ2. Actually, this is confirmed by the voltage V_{HB} of the half-bridge midpoint which was previously zero and is abruptly pulled up to V_{in} exactly at $t=t_0$ with a large dv/dt. The body diode DQ2 is then reverse-recovered and a large current spike flows through Q1 and DQ2 until the latter recovers completely. Functionally this is similar to a cross-conduction of the half-bridge leg. Very high di/dt may occur and, as a result, large voltage spikes are generated across the parasitic inductances experiencing this large di/dt. The voltage V_{HB} may have large positive overshoots. During this phase when energy is taken from the input source, the tank current reaches its maximum value and then decays. The phase ends when I_R=I(Lp) and, then, I(D1)=0 at $t=t_1$.

b) $t_1 \rightarrow t_2$. Unlike what happens in the below-resonance DCMB2 submode, where there was insufficient voltage across the resonant capacitor to forward-bias D2, here Vc is much larger and D2 starts conducting immediately at $t=t_1$. I_R starts decreasing, becoming lower than I(Lp) and eventually crosses zero before Q1 turns off, which marks the end of the this phase at $t=t_2$.

c) $t_2 \rightarrow t_3$. This is the deadtime during which both Q1 and Q2 are OFF. During this phase I_R is already negative and further decreasing. Since Q1 is off, it is flowing through DQ1. Note that the voltage of the half-bridge midpoint V_{HB} does not change. This phase ends when Q2 turns on at $t=t_3$.

Figure 22. Capacitive mode operation below resonance ($f_{R2} < f < f_{R1}$, $R<R_{crit}$): main waveforms



d) $t_3 \rightarrow t_4$. The tank current $I_R(t_3)$ as Q2 is switched on is already negative and flowing through the body diode of Q1, DQ1. The voltage of the half-bridge midpoint, V_{HB}, is abruptly pulled down to ground at $t=t_3$ with a large dv/dt. The body diode DQ1 is then reverse-recovered and a large current spike flows through Q2 and DQ1 until the latter recovers completely. Again there is a condition functionally equivalent to a cross-conduction of the half-bridge leg. Very high di/dt may occur and, as a result, large voltage spikes are generated across the parasitic inductances experiencing this large di/dt. The voltage V_{HB} may have large negative undershoots. During this phase energy is internally recirculated, the tank current reaches its minimum value and then increases. The phase ends when I_R=I(Lp) and, then, I(D2)=0 at $t=t_4$.

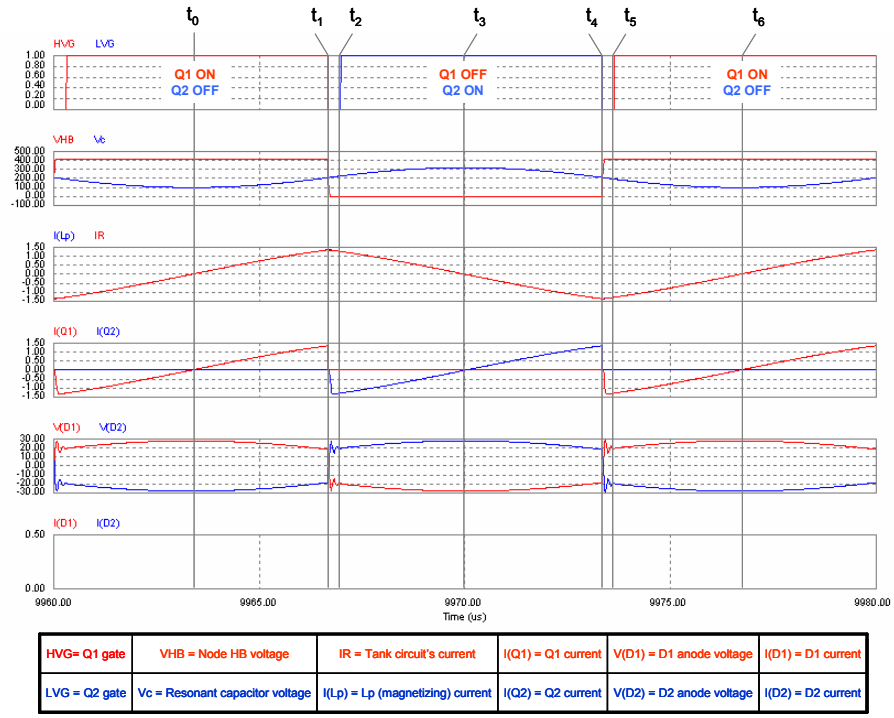
e) $t_4 \rightarrow t_5$. This phase mirrors exactly (t_1, t_2). The voltage across the resonant capacitor is so large that D1 is forward-biased and, thereby, starts conducting immediately at $t=t_4$. I_R starts increasing, becoming higher than I(Lp) and eventually crosses zero before Q2 turns off, which marks the end of this phase at $t=t_5$.

f) $t_5 \rightarrow t_6$. This is the deadtime during which both Q1 and Q2 are OFF. During this phase I_R is already positive and increasing. Since Q2 is off, it is flowing through DQ2. Note again that the voltage of the half-bridge midpoint V_{HB} does not change. This phase ends when Q2 turns on at $t=t_3$ and another switching cycle begins.

Remarks

1. In the below-resonance capacitive mode operation, since current is continuously flowing on the secondary side, this is a CCM mode (as already stated, it corresponds to the CCMB mode defined in [3].
2. The physical reason of this CCMB operation is, as previously pointed out, the large voltage developed across the resonant capacitor. A large energy level must be circulating in the tank circuit and this is consistent with $R<R_{crit}$ condition in order for the capacitive mode to take place. Capacitive operating mode is then likely to occur under heavy load, overload or short circuit conditions and appropriate countermeasures must be taken to handle this.
3. Note that in all the inductive modes the absolute value of the switched currents (i.e. the current I_R when either power MOSFET is switched off) is always greater than (in CCM mode above resonance) or equal to (in all DCM modes) the current I(Lp). In the capacitive mode, instead, the absolute value of the switched currents is lower than that in Lp. This consideration is useful when analyzing the transitions of the node HB.
4. Unlike the other modes, in capacitive mode the secondary rectifiers D1 and D2 start conducting during the conduction period of Q2 and Q1, respectively. The initial current is zero and its di/dt is low, thus they have a soft turn-on. Also in this case the voltage across the secondary rectifiers reverses as a result of their currents going to zero. Then, ZCS is maintained even under these conditions and it is possible to conclude that the secondary rectifiers are soft-switched at both turn-on and turn-off under all operating conditions and that this property is inherent in the topology. In fact no assumption has been made about the tank circuit's parameters.

Figure 23. No-load operation (cutoff): main waveforms



2.4 No-load operation

The ability to operate under no-load conditions is another peculiar characteristic of the LLC resonant half-bridge converter. The typical waveforms in this operating mode, called also "cutoff" mode, which can occur at frequencies both above, below and at the resonant frequency f_{R1}, as demonstrated in [3], are illustrated in the timing diagrams of *Figure 23*.

Note that it is I_R=I(Lp), then I(D1)=I(D2)=0, throughout the entire switching cycle. I_R is made by portions of sinusoid at f=f_{R2}, but looks very much like a triangular waveform. In order for this operation to occur, the voltage developed across Lp and reflected to the secondary side has to be lower than the output voltage throughout the entire switching cycle, so that either secondary rectifier cannot be forward-biased. In other words, *Equation 12* has to be met for $t \in (t_0, t_6)$. The ability of the converter to operate with no-load can be easily deducted by *Equation 12* itself. However big the peak value of $V_{in}(t)$-Vc(t) is and provided $a \cdot V_{out}$ is not zero, it is possible to find a value of Lp that meets condition (α). In the end, no-load operation is not an intrinsic property of the LLC resonant converter (like ZCS for the secondary rectifiers) but it can be achieved with an appropriate design of the tank circuit.

The difference with respect to the LC series resonant converter is apparent. If $Lp \rightarrow \infty$ the LLC converter turns into the LC one but $Vc \rightarrow 0$ because there is no current through the resonant tank and the only possible equilibrium condition is $V_{in} = a \cdot V_{out}$. If the input and output voltage have a different ratio, output voltage regulation will be impossible.

Seen from a different standpoint, under no load conditions and at a frequency considerably higher than f_{R1}, the resonant capacitor Cr "disappears" ($Vc(t) \approx V_{in}/2$) and the output voltage is given by the inductive divider made up by Ls and Lp as shown by the equivalent circuit of *Figure 24*. Then, if the voltage conversion ratio is greater than the inductive divider ratio, regulation will be possible at some finite frequency, otherwise it will not be. From *Equation 12*, substituting $V_{in(t)} = V_{in}$ and, then, $Vc(t) = V_{in}/2$, it is possible to find a necessary condition in order for the converter to be able to regulate at zero load:

Equation 15

$$\frac{Lp}{Ls + Lp} \leq 2\frac{a \cdot V_{out}}{V_{in}}$$

Lp, then, plays a key role. It not only makes zero load operation possible but allows soft-switching under these conditions too, as already discussed. The price to pay for that is the considerable tank current I_R=I(Lp) circulating in the circuit and illustrated in *Figure 23*. This circulation is not lossless. Power is dissipated in power MOSFET, the resonant capacitor and the transformer.

This prevents the LLC resonant converter from achieving extremely low input power levels at no load, unless appropriate countermeasures are taken. The most effective way to reduce no-load consumption to a very low level is to let the converter operate intermittently ("burst-mode" or "pulse-skipping" operation). In this way, the average value of the tank current can be reduced at an almost negligible value. Furthermore, the average switching frequency will be considerably lowered thus minimizing the residual turn-off switching losses.

2.5 Overload and short circuit operation

The equivalent schematic of the converter under short circuit conditions is illustrated in *Figure 25*. The inductance Lp is actually shunted by an extremely low impedance, so that the LLC circuit reduces to a series LC circuit. The transformer will work as a "current transformer", so that the output current will be a times the primary (input) current Iin. It is

intuitive that the impedance of the Ls-Cr resonant tank plays a key role. Note that this impedance becomes zero at f = f_{R1}. Two cases will be considered:

1. The converter always works above resonance (some means is provided to bottom-limit the operating frequency at a value $f_m > f_{R1}$). The control loop, in the attempt to keep the output voltage regulated, will reduce the switching frequency to the minimum value f_m. In this case the converter still operates in the inductive region (CCM submode) and ZVS is ensured. However, the impedance of the Ls-Cr tank circuit can be very low and then the current Iin can reach very high values, the closer the minimum frequency to f_{R1} is, the lower the impedance and the higher the current will be.
2. The converter can operate below resonance (some means is provided to bottom-limit the operating frequency at a value f_m such that $f_{R2} < f_m < f_{R1}$). Again, the control loop, in the attempt to keep the output voltage regulated, will reduce the switching frequency to the minimum value f_m. In this case, the input current will be limited by the impedance of the Ls-Cr tank circuit at a value that is as lower as f_m is lower. However the capacitive region is entered and ZVS is lost, with all the consequent troubles previously mentioned. The waveforms will be similar to those in *Figure 22*.

Figure 24. Circuit's equivalent schematic under: no-load conditions

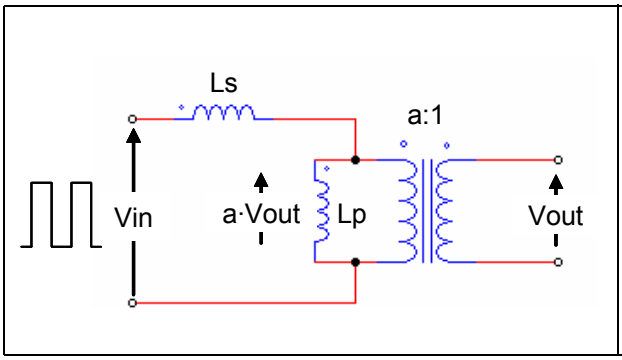
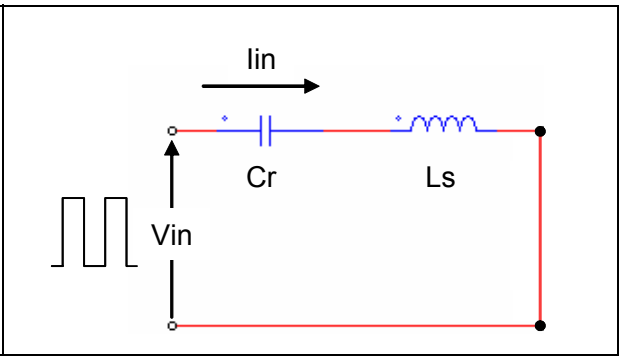


Figure 25. Circuit's equivalent schematic under: short-circuit conditions



It is interesting to see what happens under short circuit if the converter is operating at resonance (f = f_{R1}). Tank circuit's impedance is zero, then the short circuit is directly connected across the input source and the current Iin is theoretically unlimited. Theoretically, switching frequency should not change (the system is working in the load-independent point). In real-world operation, Iin, though reaching very high values, will be limited by the parasitic resistance of the short-circuit mesh, the ESR of Cr and by transformer's nonidealities. Additionally, the drop across the secondary rectifiers does not reflect a true short circuit on the primary side. Because of the parasitic resistances, the output voltage will drop and the control loop will react pushing the operating frequency to the minimum f_m, which, realistically, must be lower than f_{R1} if operation at resonance is allowed. In the end this will fall into case 2.

Still with reference to case 2, it is worth remembering that the capacitive region is entered and ZVS for MOSFETs is lost as $R_{crit} = \sqrt{Zo_0 \cdot Zo_\infty}$, well before short circuit.

From the above analysis it is possible to draw the following conclusions:

1. Two major issues arise under overload or short circuit conditions: very high current levels, and capacitive mode operation (with loss of ZVS, etc.). This makes the operation of the LLC resonant converter under overload or short circuit inherently unsafe if no overcurrent protection (OCP) is used, just like in conventional PWM-controlled converters. OCP will have to prevent not only the tank current from exceeding unsafe

values but also ZVS from being lost. In principle, its setpoint must be such that the condition $R>R_{crit}$ is always fulfilled.

2. Limiting the minimum operating frequency of the converter is not always effective. It prevents losing ZVS under overload or short circuit only if this minimum value is above the resonant frequency f_{R1}. Thereby, relying on just limiting the minimum operating frequency would force giving up the below-resonance operating region and its interesting properties, severely limiting the usability range of the converter. Furthermore, the problem of having too high circulating current would be still unsolved.
3. Converters are often specified to have peak load demands that are considerably higher than the maximum continuous power, and whose duration is such that it cannot be averaged by the output capacitor bank. While these peak loads may be thermally irrelevant, from the electrical standpoint they must be considered as steady-state. OCP circuits must not be triggered and the converter must be designed so that the condition $R>R_{crit}$ is not violated under these transient conditions as well.

The inspection of the waveforms under heavy load conditions shows that, unlike PWM-controlled converters, the peak current in a switching cycle is not reached at the end of the conduction time of either MOSFET. This suggests that the usual cycle-by-cycle current limitation so widely used in PWM-controlled converters is not applicable to LLC resonant converters.

The simplest and also most immediate action to take in response to the detection of an overload or short circuit condition is to increase the operating frequency. It is advantageous to push the frequency well above the resonance frequency f_{R1}, so that the converter definitely operates in the inductive region, and ZVS is maintained, with the input current kept under control by the inductive reactance of the tank circuit.

However, this frequency rise is not typically sufficient to effectively limit the short-circuit output current at safe values. In fact, on one hand, the input impedance of the tank circuit in the inductive region is essentially proportional to frequency. Since there are practical limits on the maximum operating frequency (it rarely exceeds 3-4 times f_{R1}), the short circuit tank current can still be considerably large. On the other hand, as the output voltage drops because of the action of the OCP circuits, the voltage reflected across Lp becomes smaller and smaller. Then, less and less current flows through Lp and the transformer tends to transfer all the primary current to the output.

As a consequence, the short circuit output current can be still much higher than the nominal full-load current and the resulting stress, especially for the secondary rectifiers, might be unacceptable. In addition to current limiting it is therefore advisable to provide some timed shutdown protection that either forces an intermittent operation of the converter to drastically reduce the average value of the output current or latches it off if the OCP circuits are active for more than some time.

2.6 Converter's startup

Like in PWM-controlled converters, startup is quite a critical moment that needs to be properly handled in LLC resonant converter as well. When the converter is first switched on (or also while it is recovering after a protection shutdown) the energy flow should be progressively increased to allow a slow buildup in output current and voltage. This is commonly known as "soft-start". Doing otherwise, high and potentially destructive currents might be drawn from the input source and through the power devices in an attempt to charge the output capacitors and bring the output voltage to the regulated value.

Since at startup the output capacitors are discharged, the startup phase can be regarded as a "temporary short circuit" (where, however, the output voltage is allowed to increase) and actually it has to be handled like a short circuit as mentioned in the previous section. To minimize energy flow, the initial switching frequency will have to be much higher than the resonance frequency f_{R1}, so that the converter operates in the inductive region, ZVS is maintained and the input current is kept under control by the inductive reactance of the tank circuit. The frequency will be allowed to progressively decay until the output voltage comes close to the regulated value and the control loop closes and takes over.

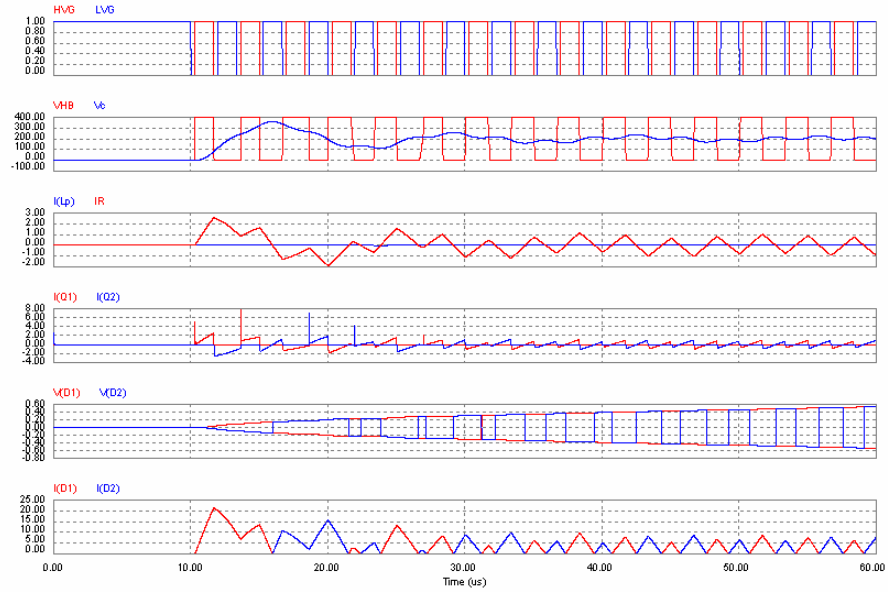
Some typical waveforms at startup for the converter of *Figure 15* are shown in *Figure 26*, where the initial frequency is set at 300 kHz (against $f_{R1} \approx$ 76 kHz).

In the LLC resonant converter there is an additional phenomenon that shows up just at the very beginning and causes higher resonant tank current to flow and ZVS loss.

As mentioned in the *Section 2*, the resonant capacitor Cr plays the double role of resonant capacitor and DC blocking capacitor. This essentially means that the resonant voltage on Cr is superimposed on a DC value that equals $V_{in}/2$ because the half-bridge is driven with 50% duty cycle. As a result, the primary of the transformer is symmetrically driven by a $\pm V_{in}/2$ square wave. This is true when steady-state operation has been reached.

At startup the initial voltage across Cr is zero and for the first few cycles the voltage seen by the transformer when the high-side power MOSFET Q1 is on is considerably different from the voltage seen when Q2 is on. The transformer driving voltage will tend to become symmetrical as switching cycles follow one another and Cr is charged at the steady state DC level. During the Cr charge transient the v·s unbalance can be quite high and this makes the tank current irregular in the first few cycles, with peak values that can be considerably higher than the steady-state peak-to-peak current expected at the starting frequency. Additionally, the fundamental ZVS conditions ("when one switch turns off, the tank current must have the same sign as the impressed voltage") may be violated so that even capacitive mode operation can be observed.

Figure 26. Converter's startup: main waveforms



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

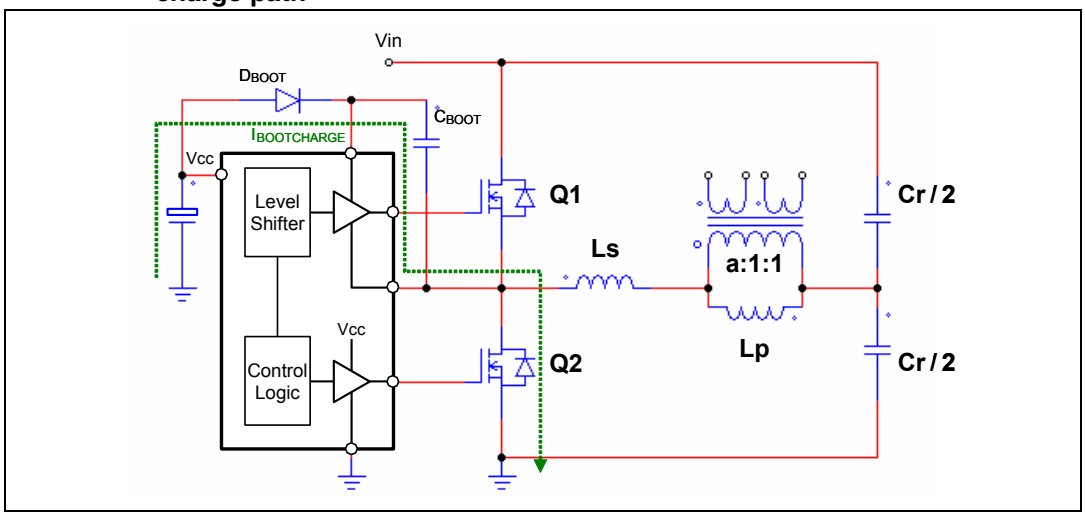
This phenomenon is well-known in push-pull and half-bridge topologies and is sometimes referred to as "flux doubling" because the transformer's magnetic flux excursion, which normally swings by $2B_{pk}$ from $-B_{pk}$ to $+B_{pk}$ under steady state operation, in the first cycle goes from 0 to $2B_{pk}$. Fortunately, if the integrated magnetics approach is used, there will be no risk of saturation. Flux doubling will concern only the resonant inductor Ls, which is mostly associated to the transformer's leakage inductance that, by definition, cannot saturate because the relevant flux is developed in air.

Although not inherently hazardous, (capacitive mode and ZVS loss will typically occur in the first two-three cycles, then the associated stress level is practically negligible) this phenomenon is not nice to see. To eliminate or, at least, minimize it, the split capacitor configuration of *Figure 4* can be used in some cases. In fact, the initial voltage across each capacitor will be close to $V_{in}/2$ (equal to $V_{in}/2$ if the two capacitors had exactly the same value), then there will be only a minimum transient.

However, this is ineffective with many control ICs with high-side MOSFET driving capability using capacitive bootstrap. To guarantee an adequate precharge of the bootstrap capacitor to correctly drive the high-side MOSFET Q1 since the first cycle, the low-side MOSFET Q2 is turned on for some time before starting to operate (as shown in *Figure 26*), which discharges completely the lower Cr/2 capacitor. This bootstrap precharge mechanism, shown in *Figure 27*, makes ineffective also any pull-up that could precharge Cr.

In this case the initial current peak cannot be completely eliminated, just reduced by either using a higher starting frequency or by forcing the duty cycle to start from a value considerably smaller than 50% and letting it widen progressively.

Figure 27. High-side driving with bootstrap approach and bootstrap capacitor charge path



2.7 Analysis of power losses

Conduction power losses on the primary side are located in the power MOSFETs, in the resonant capacitor Cr and the transformer (for convenience the secondary winding losses can be incorporated). On the secondary side, losses will be essentially located in the secondary rectifiers, although those in the output capacitors cannot be neglected, at least as far as capacitor selection is concerned.

Unless the converter is running at very high frequency, which would make turn-off losses dominant, $R_{DS(on)}$ is usually the major source of power loss in power MOSFET. In the total loss budget, however, the power wasted in power MOSFETs is usually a minor contributor, especially when the converter is powered from the output of a PFC preregulator (400 V typ.). It is not uncommon to see power MOSFETs running cool with minimum heat sinking.

The resonant capacitor Cr dissipates because of its own ESR. For this reason, especially when very high efficiency is required, Cr should be a low-loss one, suited for AC/pulse applications. Polypropylene film capacitors are the preferred choice.

Concerning the transformer, high frequency copper losses need to be particularly addressed. In fact, eddy currents and proximity losses are considerable, especially in the side-by-side winding arrangement because of the high transverse flux. Litz-type or multistrand wire is a must for both primary and secondary windings.

Switching losses are essentially located in the power MOSFET Q1 and Q2. As previously stated, the value of the switched current at heavy load (I_{Rmin}) is a trade-off between the need for ensuring ZVS for both Q1 and Q2 and their turn-off losses. The higher the switched current is, the higher the margin for ZVS will be, but at the expense of larger switching loss due to voltage-current overlap. It is intuitive that the optimum design, in terms of total dynamic losses minimization, is the one that uses for I_{Rmin} the minimum value necessary to achieve ZVS. It still provides zero capacitive turn-on losses with minimum switching losses at turnoff. Since component tolerance must be accounted for, and losing ZVS must be avoided not only for efficiency reasons but also to prevent troubles, adequate margin needs to be considered and the typical operation will be suboptimal.

Secondary rectifiers are usually the components where the majority of power losses occur. Assuming the rectifiers are identical, their cumulative conduction losses are given by:

Equation 16

$$Pd = \begin{cases} V_{th} I_{out-dc} + R_d I_{out-rms}^2 & \text{full - wave rectification} \\ 2(V_{th} I_{out-dc} + R_d I_{out-rms}^2 & \text{bridge rectification} \end{cases}$$

where V_{th} is the rectifier's threshold voltage and R_d its dynamic resistance. With bridge rectification, losses are almost double because there are always two diodes in the conduction path (we say "almost" because of the lower blocking voltage rating, so that V_{th} and R_d are expected to be slightly lower for the same current rating). Hence this arrangement is preferred when the output voltage is high. Firstly, the efficiency loss due to the rectifiers (which is $\propto 2\ V_F/V_{out}$) becomes less significant. Secondly, the higher the output voltage is, the more a lower blocking voltage requirement becomes beneficial.

As compared to the ZVS Asymmetrical Half-bridge and the Forward converter, conduction losses (for the same technology and blocking voltage) would be slightly greater because of the worse current form factor that would increase the term, but this is compensated by the absence of recovery and its associated losses. In the end, considering also that in the LLC resonant half-bridge there is no secondary choke with its associated losses, it is expected that the total secondary losses will be lower.

2.8 Small-signal behavior

It is essential to know the small-signal behavior of the LLC resonant converter to be able to design the feedback loop. In line with the approach followed to describe its steady-state

operation, here only a qualitative description will be given, which is the result of a characterization by simulation [7] (refer to *Section 4*).

As stated many times, the operating frequency is the parameter that allows regulation of the input-to-output energy flow. The control-to-output transfer function G(jω) that characterizes the small-signal behavior of the LLC resonant converter will then be defined as:

Equation 17

$$\frac{\hat{V}_o}{\hat{f}} = G(j\omega)$$

In the overall converter's dynamics it is convenient to separate the contribution of the "inverter" part and that of the rectifying and filtering block that transforms the inverter in a converter. This is quite a useful concept of superposition because it gives considerable physical insight. Regardless of the operating mode of the inverter and, then, of its contribution to converter's dynamics, the rectifying and filtering block always introduces a low frequency pole associated to the output capacitor, the load resistance and the open-loop output impedance Zo_0 of the resonant tank, plus a zero due to the output capacitor and its ESR (equivalent series resistor). This pole moves with the load (frequency is higher at heavy load, lower at light load) because of the changes in Zo_0, while the zero is at an essentially fixed frequency, exactly like in PWM converters.

Different types of dynamic behavior, corresponding to different pole distributions of G(jω), can be observed depending on the operating mode. Again we will consider operation at, above and below resonance.

2.8.1 Operation above resonance ($f > f_{R1}$)

In this operating mode the converter features a special characteristic typical of resonant converters, the so-called "beat frequency double pole", i.e. two complex and conjugate poles having their imaginary part at the difference between the switching frequency f and the resonant frequency f_{R1}. In addition to this double pole, contributed by the inverter part, there is the pole-zero pair associated to the output filter. If f is significantly higher than f_{R1}, the system can be regarded as a single-pole system.

As switching frequency moves close to resonant frequency, the beat frequency double pole will move to lower frequency. When the switching frequency is very close to resonant frequency, the beat frequency double pole will eventually split and become two real poles. One moves to higher frequencies and the other moves to lower frequencies as switching frequency gets closer and closer to resonant frequency. Finally, the split pole moving to low frequency will merge with the low frequency pole caused by the output filter and form a double pole. This type of characteristic is very similar to that of the conventional series LC converter.

Provided the converter is not operating too close to resonance, as long as it runs in CCM, the pole distribution tends not to change significantly. In DCM operation, instead, the beat frequency double pole will more pronouncedly move to higher frequencies and the low frequency pole to lower frequencies. At light load, the converter can then be regarded as a single-pole system.

Concerning how the resonant tank characteristics affect the small-signal behavior, the parallel inductor Lp has no practical effect. Conversely, increasing the impedance of the resonant tank (i.e. increasing Ls and reducing Cr while keeping the same f_{R1}), the DC gain will increase. Also the low frequency pole changes with the resonant tank impedance (it

gets higher at low impedance). In fact, the low frequency pole is not determined by the load resistor alone but by the output impedance of the tank circuit as well.

2.8.2 Operation below resonance ($f_{R2} < f < f_{R1}$, $R>R_{crit}$)

In this operating mode the converter's dynamics changes considerably. In the left half-plane, there are three poles and one zero but no beat frequency double pole. The pole distribution is quite insensitive to switching frequency as compared to that in the above resonance operation. The pole that in the above resonance operation was moving to higher frequency when switching frequency was approaching resonance here moves back to lower frequencies as switching frequency is further reduced going away from resonance. Its position, however does not change much. The low-frequency double pole is minimally affected too.

A Right Half Plane Zero (RHPZ) can be observed that moves with switching frequency but, fortunately, it stays typically away from the low frequency region of interest in the design of the feedback loop.

Approaching capacitive region, beat frequency dynamics tends to appear again. The phase has an abrupt 180º shift just beyond the capacitive region threshold (feedback from negative turns into positive).

Starting from heavy load conditions, at first the Q associated to the low frequency double pole decreases. The RHPZ shifts to higher frequencies and leaves the stage. Further reducing the load, the Q of the low frequency double pole increases. At very light load the low frequency double pole splits, one moves to higher frequencies and the other to lower frequencies. Again, at very light load the converter can be regarded as a single-pole system.

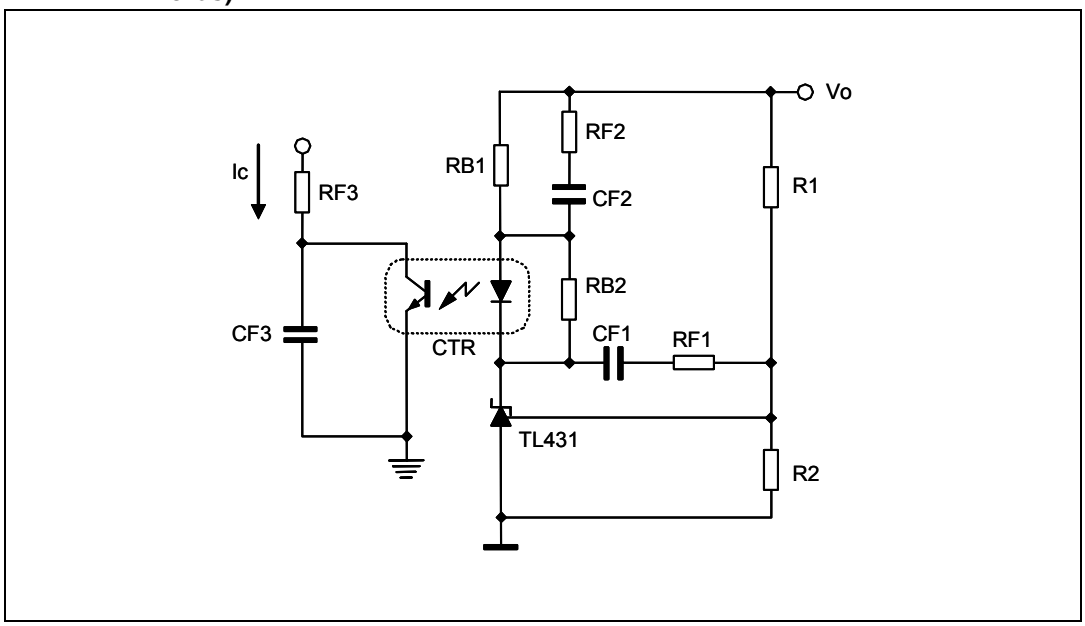
Unlike in the above resonance operation, in this case the parallel inductor Lp has a considerable impact on the DC gain of the converter. Additionally, it affects the RHPZ as well. Larger values for Lp tends to shift it to lower frequencies. As far as the impedance of the resonant tank is concerned, the effect is the same as in the above resonance operation.

2.8.3 Operation at resonance ($f = f_{R1}$)

Operation at resonance can be regarded as the borderline between the two previously considered operating modes. The behavior will not be different from that seen just above (and just below) resonance: two low-frequency poles, one high-frequency pole and the ESR zero. The same behavior can be seen as far as load dependence is concerned.

The compensation of the error amplifier must consider the different types of small-signal behavior that the converter can exhibit, especially if it is designed to operate both above and below resonance. The challenge comes essentially from its second-order behavior exhibited in its operation close to resonance frequency due to the low frequency double pole. To properly compensate that, the best option is a type 3 amplifier, i.e. a compensator with one pole at the origin plus two poles and two zeros at finite frequencies. The pole at the origin gives excellent load and line regulation characteristics. The two zeros are placed at low frequency to compensate the double pole of the control-to-output transfer function, by counteracting their phase lag. The poles are placed to compensate the ESR zero and provide more attenuation at switching frequency. A practical implementation of this compensator is shown in *Figure 28* along with the relationship between the component values and its transfer function.

Figure 28. Frequency compensation with an isolated type 3 amplifier (3 poles + 2 zeros)



Equation 18

$$\frac{\hat{I}_C}{\hat{V}_o} = \frac{CTR}{s(R1 \cdot RB1 \cdot CF1)} \cdot \frac{1 + s(RB1 + RF2)CF2}{1 + sRF2 \cdot CF2} \cdot \frac{1 + s(R1 + RF1)CF1}{1 + sRF3 \cdot CF3}$$

3 Conclusion

The operation of the LLC resonant converter has been examined in detail and its most important properties have been deduced by inspection of its salient waveforms under different operating conditions. To summarize, the most significant merits of this topology are:

- Soft-switching of all semiconductor devices: ZVS (zero-voltage switching) at turn-on for the MOSFETs and ZCS (zero-current switching) at both turn-on and turn-off for the secondary rectifiers. The first property results from a correct design of the resonant tank. The second one is a natural feature of the topology.
- Ability to accommodate an extremely broad load range, including zero load, with an acceptable frequency variation. Also this property results from a correct design of the resonant tank.
- Magnetic integration, which allows the combination of different magnetic devices into a single physical device.
- Smooth waveforms: the current is piecewise sinusoidal with no steep edges. The voltage, although a square wave, does not have very high dv/dt edges. EMI emissions are considerably low and filtering requirements are relatively loose.
- As a result of all the above merits, high-efficiency, high switching frequency capability, high power density are typical characteristics of the converters based on this topology.

The most significant facts concerning the design of an LLC resonant converter are:

- The quantities that determine whether the converter operates at resonance, above resonance or below resonance are essentially the input and the output voltages and the transformer's turn ratio. There is just a second-order dependence on the load current due to the variation of the voltage drop across parasitic elements such as winding resistance, rectifier drop, etc.
- Operation at resonance looks like the preferred operating point, where load regulation is ideally zero, where tank current is maximally sinusoidal and where CCM operation minimizes peak tank current for a given power throughput. Whenever possible (e.g. when the LLC converter is powered by a PFC preregulator) it seems a good design strategy to design the converter to work at resonance under nominal conditions, and use below resonance operation to handle mains voltage dips and above resonance operation to handle light load or transient overshoots of the input voltage.
- The ability to operate under no-load conditions and to ensure ZVS operation depend essentially on the transformer's magnetizing inductance. Its value has to be traded off against the switching losses at full load operation and the input consumption at no-load.
- Avoiding capacitive mode operation is a must. It is a too risky operating mode and any design procedure should not leave this fundamental aspect out of consideration.
- Overcurrent and short circuit protection must be provided. They will not only have to prevent excessive currents from flowing in both the resonant tank, the transformer and the output rectifiers but also avoid entering capacitive mode operation.
- Soft-start is highly recommended. At startup there is a situation very similar to a short circuit and, if not properly controlled, potentially destructive currents might flow in the half-bridge leg and the resonant tank.

4 References

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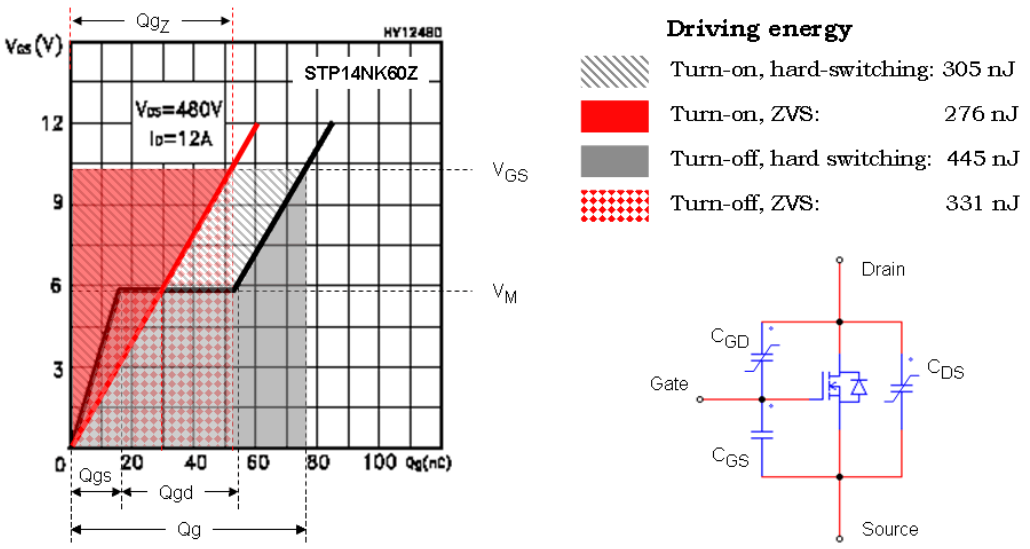
Appendix A Power MOSFET driving energy in ZVS operation

When power MOSFETs are switched on under ZVS conditions, i.e. when their drain-to-source is already zero, Miller effect due to drain-to-source voltage modulation is absent. This reduces the gate charge required to turn the power MOSFET fully on, the turn-on energy, as well as the total driving energy. This can be conveniently examined on the gate-charge characteristic of the device (see *Figure 29*).

Figure 29. Comparison of gate-charge characteristics with and without ZVS



The black curve is the normal piecewise-linear gate-charge curve. The first portion is that related to the charge of the input capacitance C_{GS}+C_{GD}, and Qgs is the charge needed to bring the gate voltage up to the plateau value V_M that lets the power MOSFET carry the specified current. The flat portion is the so-called "Miller plateau", where the gate voltage does not increase because the drain-to-source voltage is falling and C_{GD} is wiping out the charge supplied to the gate until the charge Qgd has been supplied. The third rising portion is related to the overcharge of C_{GS}+C_{GD} needed to minimize $R_{DS(on)}$. Note that the slope of this line is lower than that of the first portion. This is due to the modulation of C_{GD}, which is now considerably larger (C_{GS} is essentially constant). The total gate charge supplied to the gate to bring its voltage up to the final value V_{GS} is Qg. The values of Qgs, Qgd, Qg are specified on the datasheet for given V_{GS}, V_{DS}, I_D.

The grey-hatched area included between the gate-charge curve and the V_{GS} horizontal line is the energy lost in the gate driver to charge the gate up to the final value V_{GS} and turn the power MOSFET fully on. Its value can be found with simple geometric considerations:

Equation 19

$$E_{ONHS} = \frac{1}{2}[QgsV_M + (Qg + Qgs + Qgd)(V_{GS} - V_M)]$$

The grey-shaded area below the gate charge curve represents the energy lost in the gate driver to discharge the gate from V_{GS} to zero. Its value can be simply found from the difference of the total driving energy, represented by the rectangle enclosed by the Q-V axes and the Qg and V_{GS} lines:

Equation 20

$$E_{HS} = Qg \cdot V_{GS}$$

and E_{ON_HS}:

Equation 21

$$E_{OFF\_HS} = Qg \cdot V_{GS} - E_{ON\_HS}$$

In case of ZVS, instead, the associated gate-charge curve is the red line. Its slope is equal to that of the third portion of the normal gate-charge characteristic, because C_{GD} has the final value since the beginning. By geometrical considerations, the total gate charge Qg_Z to provide in this case will be:

Equation 22

$$Qg_Z = \frac{V_{GS}}{V_{GS} - V_M}[Qg - (Qgs + Qgd)]$$

while the energy lost in the gate driver to charge the gate up to the final value V_{GS} and turn the power MOSFET fully on and represented by the red-shaded area will be:

Equation 23

$$E_{ON\_ZVS} = \frac{1}{2} Qg_Z V_{GS} = \frac{1}{2} \cdot \frac{V^2_{GS}}{V_{GS} - V_M}[Qg - (Qgs + Qgd)]$$

At turn-off, the Miller effect will be present but to a lower degree. In fact, the operating point will initially move along the red line until the gate voltage reaches the Miller plateau V_M (that associated to the switched current at turn-off). From that point on, it will move along the black curve. The energy associated to turn-off will be:

Equation 24

$$E_{OFF\_ZVS} = \frac{1}{2(V_{GS} - V_M)}[(V^2_{GS} + V^2_M)(Qg - Qgd) - V_{GS}(V_{GS} + V_M)Qgs]$$

and the total driving energy:

Equation 25

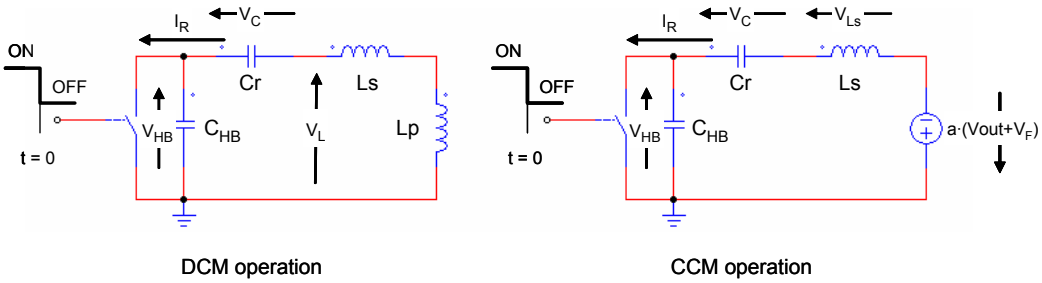
$$E_{ZVS} = \frac{1}{2(V_{GS} - V_M)}[(2V^2_{GS} + V^2_M)(Qg - Qgd) - V_{GS}(2V_{GS} + V_M)Qgs]$$

For the power MOSFET used in the example of *Figure 29* (STP14NK60Z), the datasheet specifies: Qgs = 13.2 nC, Qgd = 38.6 nC, Qg = 75 nC @ V_{GS} = 10 V. Substituting these values and V_M = 5.8 V_{in} (*Equation 19*) to (*Equation 25*) we find: E_{ON_HS} = 305 nJ, E_{HS} = 750 nJ, E_{OFF_HS} = 445 nJ, Qg_Z = 55 nC, E_{ON_ZVS} = 276 nJ, E_{OFF_ZVS} = 331 nJ and E_{ZVS} = 607 nJ. Then, the total gate charge is decreased by 20 nC (-27%) and the total gate driving energy by 143 nJ (-19%).

Appendix B Resonant transitions of half-bridge midpoint

To analyze the transitions of the half-bridge midpoint node HB when either Q1 or Q2 is turned off, it is necessary to schematize the equivalent circuit during the transient. For simplicity only the turn-off of Q2 will be considered, being obvious that the turn-off of Q1 will be exactly mirror-symmetrical. Different circuits need to be considered, depending on whether the converter is operated in a DCM mode or a CCM mode. These equivalent circuits are shown in *Figure 30*.

Figure 30. Equivalent circuit to analyze the transitions of the half-bridge midpoint node when Q2 turns off



In fact, in the case of DCM operation, since the secondary windings are open, Lp is part of the circuit and is effectively in series to Ls to form a single inductor Ls+Lp. In CCM operation, instead, since the secondary windings are conducting there is a constant voltage equal to $\pm a \cdot (V_{out}+V_F)$ across Lp and then this can be replaced by a voltage generator (placed as shown in *Figure 30* in the case under consideration). In either circuit, Q2 is replaced by an ideal switch that opens at t=0.

Resonant tanks are again involved during the transitions, hence the denomination "resonant transitions" given to the swings of the node HB. Considering the operation of the LLC resonant converter in its entirety, then, there are four associated resonant frequencies.

C_{HB} is the total parasitic capacitance of the node HB already discussed in *Section 2.2: The switching mechanism* and illustrated in *Figure 8* and that will be the topic of the next section. Note that during the transient Cr and C_{HB} are effectively in series. However, since normally $Cr >> C_{HB}$ (typically, two orders of magnitude), the combined capacitance will be $\approx C_{HB}$ and the changes of the V_C voltage during the transient can be neglected, so that it is possible to assume $V_C = V_C(0)$ during the transient and replace Cr with a constant voltage generator $V_C(0)$.

The value of $V_C(0)$ can be determined on the basis of the following considerations. The value of at the end of the conduction cycle of Q1, $V_C(Ts/2)$, is given by:

Equation 26

$$V_C\left(\frac{Ts}{2}\right) = V_C(0) + \frac{1}{Cr}\int_0^{\frac{Ts}{2}} I_R(t)dt$$

Note that the integral in *Equation 26* is the total charge provided to Cr during the conduction time of Q1, when the converter draws current from the input source. This charge can be expressed also as the product of the DC input current Iin times the switching period, then:

Equation 27

$$V_C\left(\frac{Ts}{2}\right) = V_C(0) + \frac{Iin}{Cr}Ts$$

On the other hand, remembering that V_C has a DC value equal to $V_{in}/2$, for symmetry the following identity holds true:

Equation 28

$$V_C\left(\frac{Ts}{2}\right) - \frac{V_{in}}{2} = \frac{V_{in}}{2} - V_C(0)$$

By combination of (*Equation 39*) and (*28*) we find:

Equation 29

$$V_C(0) = \frac{1}{2}\left(V_{in} - \frac{Iin}{Cr}Ts\right)$$

$$V_C\left(\frac{Ts}{2}\right) = \frac{1}{2}\left(V_{in} + \frac{Iin}{Cr}Ts\right)$$

After some algebraic manipulations, it is possible to find that the equations governing the operation of the circuits in *Figure 30* are:

Equation 30

$$\begin{cases} \frac{d^2V_{HB}}{dt} + \frac{1}{C_{HB}(Ls+Lp)}V_{HB} = \frac{V_C(0)}{C_{HB}(Ls+Lp)} & \text{DCM} \\ \frac{d^2V_{HB}}{dt} + \frac{1}{C_{HB}Ls}V_{HB} = \frac{V_C(0) - a\cdot(V_{out}+V_F)}{C_{HB}Ls} & \text{CCM} \end{cases}$$

with the following initial conditions:

Equation 31

$$V_{HB}(0) = 0, \left.\frac{dV_{HB}}{dt}\right|_{t=0} = \frac{I_R(0)}{C_{HB}}$$

The solutions of these equations are:

Equation 32

$$V_{HB}(t) = \begin{cases} V_{DD}\sin(\omega_{DD}t - \varphi_{DD}) + V_C(0) & \text{DCM} \\ V_{CC}\sin(\omega_{CC}t - \varphi_{CC}) + V_C(0) - a\cdot(V_{out}+V_F) & \text{CCM} \end{cases}$$

with

Equation 33

$$\omega_{DD} = \frac{1}{\sqrt{(Ls+Lp)C_{HB}}}, \varphi_{DD} = \tan^{-1}\left(\frac{V_C(0)}{I_R(0)}\sqrt{\frac{C_{HB}}{Ls+Lp}}\right), V_{DD} = \frac{V_C(0)}{\sin\varphi_{DD}}, \omega_{CC} = \frac{1}{\sqrt{LsC_{HB}}},$$

$$\varphi_{CC} = \tan^{-1}\left(\frac{V_C(0) - a\cdot(V_{out}+V_F)}{I_R(0)}\sqrt{\frac{C_{HB}}{Ls}}\right), V_{CC} = \frac{V_C(0) - a\cdot(V_{out}+V_F)}{\sin\varphi_{CC}}$$

The expression of the tank current will be:

Equation 34

$$I_R(t) = C_{HB}\frac{dV_{HB}(t)}{dt} = \begin{cases} C_{HB}\cdot V_{DD}\cdot \omega_{DD}\cdot \cos(\omega_{DD}t-\omega_{DD}) = \dfrac{I_R(0)}{\cos\omega_{DD}}\cos(\omega_{DD}t-\varphi_{DD}) & \text{DCM} \\ C_{HB}\cdot V_{CC}\cdot \omega_{CC}\cdot \cos(\omega_{CC}t-\omega_{CC}) = \dfrac{I_R(0)}{\cos\omega_{CC}}\cos(\omega_{CC}t-\varphi_{CC}) & \text{CCM} \end{cases}$$

Equations (*Equation 30*) to (*34*) apply in the time interval (0, T_T), where T_T is the time needed for the voltage V_{HB} to reach V_{in}. T_T can be calculated from (*Equation 32*) taking (*33*) into account; the result is:

Equation 35

$$T_T = \begin{cases} \dfrac{1}{\omega_{DD}}\left[\varphi_{DD} + \sin^{-1}\left(\dfrac{V_{in}-V_C(0)}{V_{DD}}\right)\right] & \text{DCM} \\ \dfrac{1}{\omega_{CC}}\left[\varphi_{CC} + \sin^{-1}\left(\dfrac{V_{in}-V_C(0)+a\cdot(V_{out}+V_F)}{V_{CC}}\right)\right] & \text{CCM} \end{cases}$$

To achieve ZVS, the value of T_T given by (*Equation 35*) must not exceed the deadtime T_D to make sure that Q1 is turned on with zero drain-to-source voltage.

Note that in CCM operation there may be an additional constraint on the time interval where equations (*Equation 30*) to (*34*) are applicable. The current $I_R(t)$ will be described by *Equation 34* either until T_T or until it equals the current flowing through Lp (see *Figure 9*), whichever condition occurs first. We will assume that $I_R(t)=I(Lp)$ occurs after T_T.

With the usual values of all the involved quantities, the phase angles φ_{CC} and φ_{DD} are both considerably less than unity, then it is possible to use the approximation $\varphi \approx \sin\ \varphi \approx \tan\varphi$ for both of them. With this simplification (*Equation 35*) can be expressed as:

Equation 36

$$T_T = \frac{V_{in}}{I_R(0)}C_{HB}$$

for both CCM and DCM modes, which is equivalent to considering C_{HB} charged by a constant current $I_R(0)$.

Considering that in CCM operation above resonance it is $V_{in} > 2\cdot a\cdot(V_{out} + V_F)$ and, again, that $V_C(0) \le V_{in}/2$, φ_{CC} is always negative. As a result, $I_R(t)$ has its peak for negative t values and decays in (0, T_T). In DCM operation, if the input current is lower than a critical value, it is $V_C(0) > 0$ and, then, φ_{DD} positive. Thereby, $I_R(t)$ has its peak for positive t values, thus it initially increases and then decays in (0,T_T). In this case, which happens at light load and with no load, the approximation $I_R(t) = I_R(0)$ is excellent. Still in DCM operation, but with an input current exceeding that critical value, it is $V_C(0) < 0$ and, then, φ_{DD} negative, which happens below resonance at heavy load. However, as compared to what happens in CCM operation, the associated resonance period is longer, thus the change in $I_R(t)$ is lower and the approximation $I_R(t) = I_R(0)$ is still good. This is illustrated in *Figure 31* and *32*.

Figure 31. Voltage of HB node vs time (see *Equation 32*)

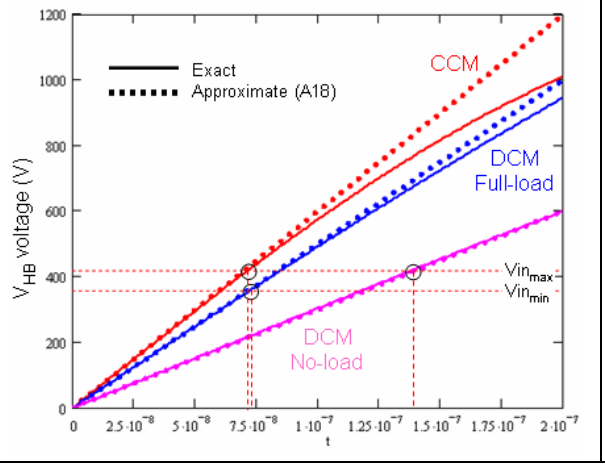
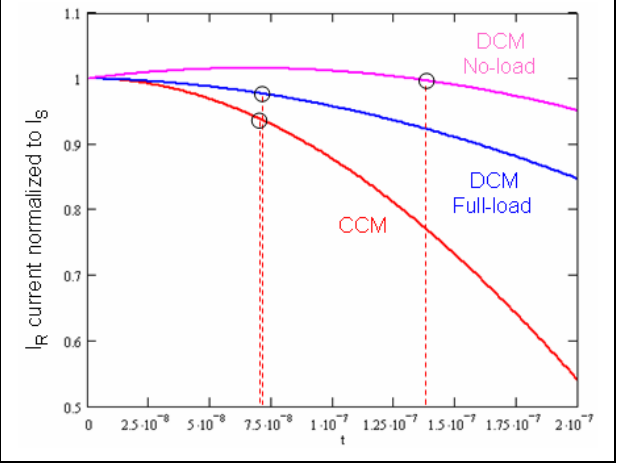


Figure 32. Resonant current vs time (see *Equation 34*)



In the end, the approximation (*Equation 36*) provides a relationship that is sufficiently accurate for design purposes under all operating conditions. Fortunately the conditions where accuracy is worst (CCM) are not critical as far as ZVS is concerned because the switched current $I_R(0)$ is greater than it is under all other conditions.

To achieve ZVS for both switches, a necessary condition is that $T_T \leq T_D$. An additional constraint comes from the condition that the tank current I_R has to keep its sign unchanged during the time interval $(0, T_D)$. Should the current become zero in that interval, the body diode of Q1 would not be forward biased any more and the voltage V_{HB}, no longer constrained to Vin, would experience oscillations at an angular frequency equal to either ω_{DD} or ω_{CC}. Q1 would then be turned on with a drain-to-source voltage in general greater then zero.

In practical cases, when the converter is operated at or above resonance the tank current crosses zero with a considerable delay after the end of the deadtime, especially in DCM modes, where the phase lag φ described by *Equation 5* or *8* or *11* or *13* tends to $\pi/2$; hence, this constraint can be disregarded. It becomes significant when working below resonance and close to the boundary between the capacitive and the inductive mode (CCMB mode).

Under the assumption $T_T < T_D$, in the time interval (T_T, T_D) *Equation 34* no longer apply and I_R is again a portion of sinusoid having frequency f_{R1}, which can be described by an equation of the type:

Equation 37

$$I_R(t) = I_{Rpk}\sin(2\pi f_{R1}t - \varphi)$$

In order for the tank current to keep the same sign during the remainder of the deadtime, the following condition must be fulfilled:

Equation 38

$$2\pi f_{R1}T_D - \varphi > 0$$

Appendix C Power MOSFET effective C_{oss} and half-bridge midpoint's transition times

Unlike linear capacitors, which have a capacitance value independent of the applied voltage, power MOSFET C_{oss} is a nonlinear capacitance, i.e. its value is a function of the drain-to-source voltage V_{DS}. Assuming a p-n step junction for the body-drain diode, with good approximation the C_{oss} vs. V_{DS} relationship can be expressed as:

Equation 39

$$\frac{C_{oss}(V_{DS1})}{C_{oss}(V_{DS2})} \approx \sqrt{\frac{V_{DS2}}{V_{DS1}}}$$

Power MOSFETs manufacturers usually specify the value of C_{oss} at V_{DS} = 25 V (with V_{GS}=0 at 1 MHZ), From (*Equation 39*) the C_{oss} at a given voltage V_{DS} will be:

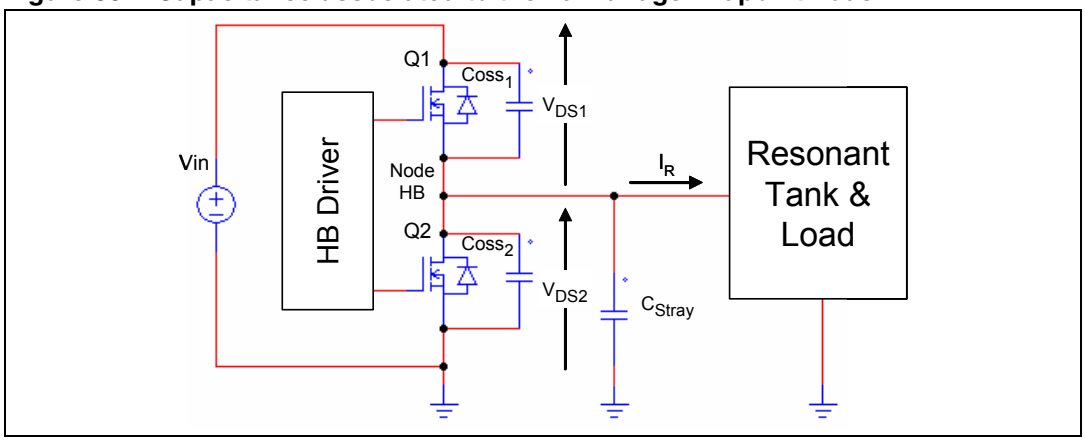
Equation 40

$$C_{oss}(V_{DS}) = C_{oss25}\sqrt{\frac{25}{V_{DS}}} = \frac{5}{\sqrt{V_{DS}}}C_{oss25}$$

Generally speaking, C_{oss} has a twofold role in switching losses mechanism in power MOSFET:

1. at turn-on C_{oss} is discharged and the energy stored in it is dissipated inside the MOSFET's $R_{DS(on)}$, thus giving origin to the so-called "capacitive losses". This is not significant in the LLC resonant converter because power MOSFETs are operated in ZVS and capacitive losses are zero, and then it will not be considered.
2. at turn-off the rate of rise of its voltage determines the voltage-current overlap that originates switching losses. This is significant in the LLC resonant converter.

Figure 33. Capacitance associated to the half-bridge midpoint node



It is worth noticing that, although the C_{oss} of the two power MOSFETs in the half-bridge are effectively connected in parallel, however they experience different V_{DS} voltages at any time. If V_{in} is the DC input voltage, and with reference to the circuit shown in *Figure 33*, the following relationship holds true:

Equation 41

$$V_{DS1} - V_{DS2} = V_{in}$$

Then, assuming that the two MOSFETs are identical to one another (so that $C_{oss25\text{-}1} = C_{oss25\text{-}2} = C_{oss25}$), and referring to the voltage of the half-bridge midpoint V_{HB} (= V_{DS2}), their individual C_{oss} will be:

Equation 42

$$C_{oss1} = \frac{5}{\sqrt{V_{DS1}}}C_{oss25} = \frac{5}{\sqrt{V_{in} - V_{HB}}}C_{oss25}$$

Equation 43

$$C_{oss2} = \frac{5}{\sqrt{V_{DS2}}}C_{oss25} = \frac{5}{\sqrt{V_{HB}}}C_{oss25}$$

and their instantaneous cumulative value will be:

Equation 44

$$Coss(V_{HB}) = C_{oss1} + C_{oss2} = 5\left(\frac{1}{\sqrt{V_{HB}}} + \frac{1}{\sqrt{V_{in} - V_{HB}}}\right)C_{oss25}$$

The diagram of equations (*Equation 43*) and (*Equation 44*) are shown in *Figure 34*. The branch-constitutive equation of the capacitor C_{oss}:

Equation 45

$$I_{C_{oss}}(t) = C_{oss}(V_{HB})\frac{dV_{HB}}{dt} \Rightarrow I_{C_{oss}}(t)dt = C_{oss}(V_{HB})dV_{HB}$$

can be integrated by variable separation.

Figure 34. C_{oss} capacitances vs. half-bridge midpoint's voltage

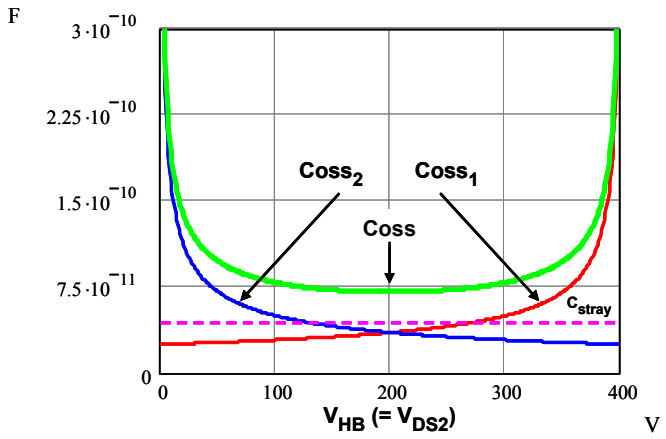
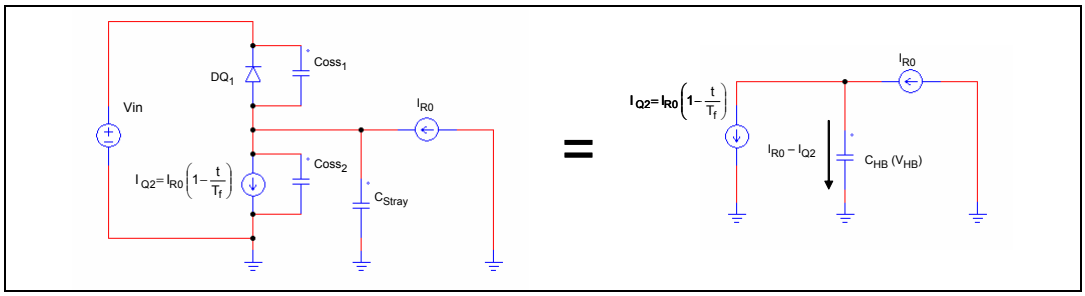


Figure 35. Simplified schematic to analyze transition times of the node HB when Q2 turns off



Assuming that $V_{HB}|_{t=0}$ it is possible to write:

Equation 46

$$\int_0^{tf} I_{C_{oss}}(\tau)d\tau = \int_0^{V_{HB}} C_{oss}(V)dV$$

Note that the left-hand side is the total charge $Q_{oss}(V_{HB})$ supplied to $C_{oss}(V_{HB})$ to raise its voltage up to the level V_{HB}. Substituting (*Equation 44*) in (*Equation 46*) and developing, it is possible to find:

Equation 47

$$Qoss(V_{HB}) = 10(\sqrt{V_{HB}} + \sqrt{V_{in}} - \sqrt{V_{in} - V_{HB}})C_{oss25}$$

Considering again the turn-off of Q2, as a consequence of the discussion of the previous section, the equivalent schematic of the circuit during the turn-off of Q2 is illustrated in *Figure 35*, where the tank circuit is then replaced by a constant current source equal to the switched current I_{R0}. Additionally, the turn-off of Q2 is assumed to be linear in time:

Equation 48

$$I_{Q2} = \begin{cases} I_{R0}\left(1 - \frac{t}{T_f}\right) & 0 \le t \le T_f \\ 0 & t > T_f \end{cases}$$

where T_f is the time the current I_{Q2} takes to become zero. The total capacitance of the node HB will be:

Equation 49

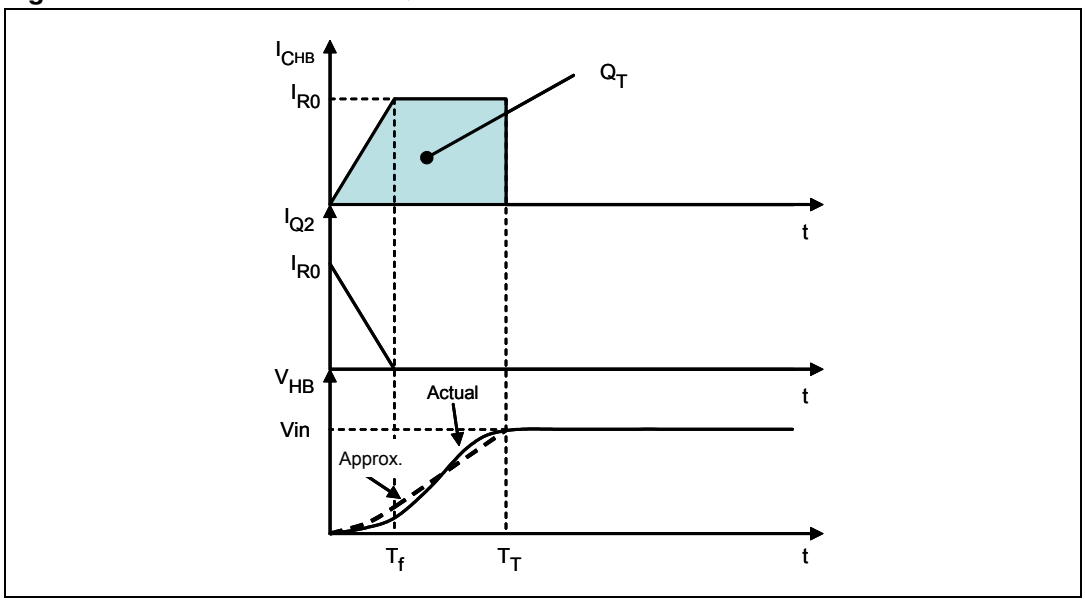
$$C_{HB}(V_{HB}) = C_{Stray} + C_{oss}(V_{HB})$$

C_{HB} will be charged by the current $I_{CHB} = I_{R0} - I_{Q2}$ until V_{HB} equals the input voltage V_{in} and DQ1 turns on, thus clamping V_{HB} at V_{in}. Let us assume that the time T_T needed for the voltage of the node HB to reach V_{in} is greater than T_f. The main quantities during the transient are illustrated in *Figure 36*. The total charge Q_T delivered to C_{HB} in the interval $(0, T_T)$ will be:

Equation 50

$$Q_T = \frac{1}{2}I_{R0}T_f + I_{R0}(T_T - T_f) = I_{R0}\left(T_T - \frac{T_f}{2}\right)$$

Figure 36. Schematization of Q2 turn-off transient



This charge will be partly stored in C_{Stray} and partly in C_{oss}. The charge in C_{Stray} will obviously be $C_{Stray} \cdot V_{in}$, then the one stored in C_{oss} will be given by (*Equation 47*) substituting V_{in} in V_{HB}:

Equation 51

$$Qoss(V_{in}) = 20\sqrt{V_{in}}C_{oss25}$$

A linear capacitance C_{HB} equivalent to $C_{HB}(V_{in})$ will have the same total charge Q_T stored in it when its voltage equals V_{in}. Then it is possible to write:

Equation 52

$$Q_T = C_{Stray}V_{in} + 20\sqrt{V_{in}}C_{oss25} = C_{HB}V_{in}$$

which yields:

Equation 53

$$C_{HB} = C_{Stray} + \frac{20}{\sqrt{V_{in}}}C_{oss25}$$

The capacitance value defined by (*Equation 53*) has to be used in calculations related to transition time of the node HB, as far as ZVS is concerned.

As previously stated, to achieve ZVS the transition of the node HB must be completed within the deadtime T_D inserted between the transitions from one state to the other of either switch, that is, $T_T \leq T_D$. Combining (*Equation 46*) and (*Equation 48*) and solving for T_T:

Equation 54

$$T_T = \frac{T_f}{2} + \frac{C_{Stray}V_{in} + 20\sqrt{V_{in}}C_{oss25}}{I_{R0}} = \frac{T_f}{2} + \frac{C_{HB}V_{in}}{I_{R0}} \leq T_D$$

Depending on the data available, (*Equation 54*) can be used for finding either the minimum value of I_{R0} (called I_{Rmin} in the text) or the maximum value of C_{HB} or the minimum value of T_D .

In datasheets of many power MOSFET manufacturers, it is customary to find an "equivalent output capacitance" denoted with C_{osseq} and defined as a constant equivalent capacitance giving the same charging time as C_{oss} when the drain-to-source voltage V_{DS} increases from 0 to 80% of the rated voltage V_{DSS}.

From the above discussion it is easy to recognize that the linear capacitance equivalent to the C_{oss} of a single MOSFET charged at a voltage V_{DS} is:

Equation 55

$$C_{osseq}(V_{DS}) = \frac{10}{\sqrt{V_{DS}}} C_{oss25}$$

then, as per the above definition:

Equation 56

$$C_{osseq} = \frac{10}{\sqrt{0.8 \cdot V_{DSS}}} \cdot C_{oss25} \approx \frac{11.2}{\sqrt{V_{DSS}}} C_{oss25}$$

The actual value provided in the datasheet can be different from the theoretical value given by (*Equation 56*), depending on the silicon cell design and density of the particular power MOSFET. For an assigned power MOSFET, whose C_{osseq} is specified, by combining with (*Equation 55*), equation (*Equation 53*) can be re-written as:

Equation 57

$$C_{HB} = C_{Stray} + 2\sqrt{\frac{V_{DSS}}{V_{in}}} C_{osseq}$$

Appendix D Power MOSFETs switching losses at turn-off

The nonlinearity of C_{oss} (refer to *Figure 34*) makes the voltage of the node HB increase slowly at its low values and its high values, and much faster when it is half way in its swing (see the solid V_{HB} waveform labeled "Actual" in *Figure 36*). Typically, the current through either Q1 or Q2 during their respective turn-off transients flows during the initial part of the transition of the node HB, i.e. when its value is changing more slowly. This reduces the voltage-current overlap and, consequently, the associated power loss with respect to a linear capacitor. However, the mathematical expression of the loss is extremely complex, therefore it is more useful to provide a conservative estimate using the equivalent linear capacitance C_{HB} defined by (*Equation 53*). The associated V_{HB} curve is the dotted one labeled "Approx." in *Figure 36* (under the assumption $T_f < T_T$).

Again with reference to the turn-off of Q2, the voltage on the node HB can be found by integration of the branch-constitutive equation of C_{HB}:

Equation 58

$$I_{C_{HB}}(t) = C_{HB}\frac{dV_{HB}}{dt} \Rightarrow V_{HB}(t) = \frac{1}{C_{HB}}\int_0^t I_{C_{HB}}(t)dt = \frac{1}{C_{HB}}\int_0^t [I_{R0} - I_{Q2}(t)]dt$$

Power loss due to voltage-current overlap (switching loss) will occur only during the time interval (0, T_f) where I_{Q2} is non-zero, then (*Equation 54*) will be considered in this interval only; substituting (*Equation 48*) in (*Equation 58*) we find:

Equation 59

$$V_{HB}(t) = \frac{1}{C_{HB}}\int_0^t \frac{I_{R0}}{T_f}tdt = \frac{I_{R0}}{2 \cdot C_{HB} \cdot T_f}t^2 \qquad t \in (0, T_f)$$

Note that in the remainder interval (T_f, T_T) the voltage V_{HB} will change linearly with time because charged by the constant current I_{R0}. The energy lost because of voltage-current overlap will be calculated by integration of the product of (*Equation 59*) times (*Equation 48*):

Equation 60

$$E_{off}(Q2) = \int_0^{T_f} I_{Q2}(t) \cdot V_{HB}(t)dt = \frac{I^2_{R0}}{2C_{HB} \cdot T_f}\int_0^{T_f} t^2\left(1 - \frac{t}{T_f}\right)dt = \frac{(I_{R0} \cdot T_f)^2}{24C_{HB}}$$

Power loss will be obtained multiplying the energy loss given by (*Equation 60*) by the operating frequency f_{sw}:

Equation 61

$$P_{off}(Q2) = E_{off}(Q2)f_{sw} = \frac{(I_{R0} \cdot T_f)^2}{24C_{HB}}$$

The same loss occurs to the high-side power MOSFET Q1 as well, thereby, the total switching loss will be:

Equation 62

$$P_{off_{TOT}} = \frac{(I_{R0} \cdot T_f)^2}{12C_{HB}} \cdot f_{sw}$$

A more accurate analysis could be done observing in *Figure 34* that C_{oss1} (C_{oss2} in case we consider Q1's turn-off) changes little during the first portion of the transient, so that it might be considered constant. With this approach, from (*Equation 44*) it is possible to assume:

Equation 63

$$C_{oss}(V_{HB}) \approx 5\left(\frac{1}{\sqrt{V_{HB}}} + \frac{1}{\sqrt{V_{in}}}\right)C_{oss25}$$

and, from (*Equation 49*), taking (*Equation 63*) into account:

Equation 64

$$C_{HB}(V_{HB}) \approx C_{Stray} + 5\left(\frac{1}{\sqrt{V_{HB}}} + \frac{1}{\sqrt{V_{in}}}\right)C_{oss25} = \left(C_{Stray} + \frac{5}{\sqrt{V_{in}}}Coss_{25}\right) + \frac{5}{\sqrt{V_{HB}}}C_{oss25}$$

Designating:

Equation 65

$$C_{HBF} = C_{Stray} + \frac{5}{\sqrt{V_{in}}}C_{oss25}$$

substituting (*Equation 64*) in (*Equation 46*), integrating both sides and solving for V_{HB} it is possible to find:

Equation 66

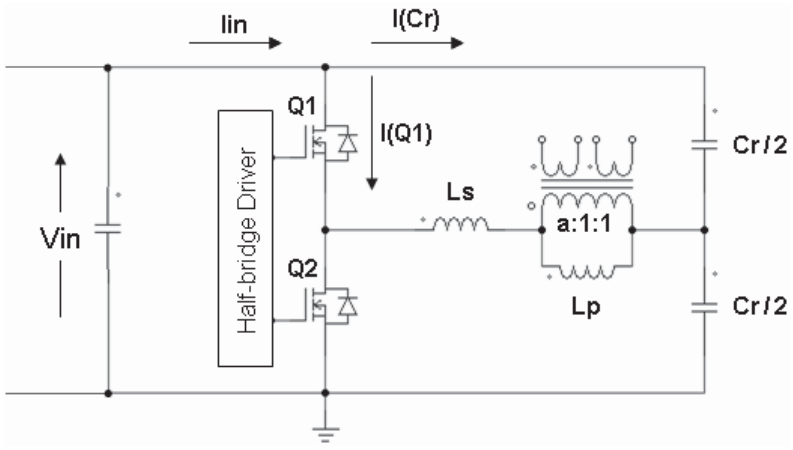
$$V_{HB}(t) = \frac{1}{C_{HBF}}\left[\frac{I_{R0}}{2 \cdot T_F}t^2 - 10\frac{C_{oss25}}{C_{HBF}}\left(\sqrt{25 \cdot C^2_{oss25} + \frac{C_{HBF}I_{R0}}{2 \cdot T_F}t^2} - 5C_{oss25}\right)\right]$$

Inserting this result in (*Equation 60*) and integrating would yield the turn-off energy, however the result is complex and of little practical use, hence it will not be provided.

Appendix E Input current in LLC resonant half-bridge with split resonant capacitors

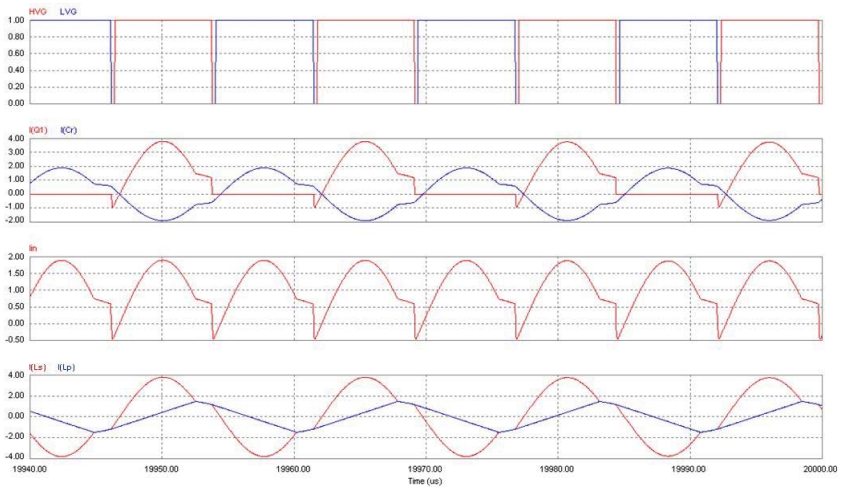
An interesting property of the LLC resonant half-bridge with split resonant capacitors is the shape of the input current. Unlike the single capacitor version, where the input current Iin equals the current through the high-side switch Q1, I(Q1), in this case Iin is given by the superposition of I(Q1) and the current through the high-side resonant capacitor I(Cr), as shown in *Figure 37*.

Figure 37. Input current components in a split-capacitor LLC resonant half-bridge



The current I(Cr) with the direction defined in *Figure 37* is in phase opposition to I(Q1) and to the current through the series resonant inductor I(Ls); also, its instantaneous amplitude is half that of I(Ls) since it is equally split between the two resonant capacitors. As a result, when Q1 is ON, I(Cr) is negative and Iin equals I(Q1) diminished by I(Cr); when Q1 is OFF and I(Q1)=0, Iin = I(Cr) is positive and provides a continuous input current flow. This is shown in the timing diagrams of *Figure 38*.

Figure 38. Timing diagram showing currents flow in the converter of *Figure 37*



Note that the input current is the same as in a full-bridge converter, where during each half switching period there is a conducting path drawing current from the input source.

With the same DC value of Iin, then, the split capacitor configuration makes its peak and squared rms values are cut in half. Unlike bridge converters, however, the currents I(Q1) and I(Q2) keep the same value as in the single capacitor half-bridge version.

It is then advantageous to use the split capacitor configuration to reduce not only the ac current requirements on the resonant capacitors but also the ac current in the input capacitor and the differential-mode conducted noise. It is then easy to find this solution at higher power levels but it is advisable to use it also when there is no front-end PFC pre-regulator. In this case, in fact, the differential-mode noise that the input EMI filter is required to mitigate is that generated by the resonant half-bridge converter (whereas, with a PFC front-end the noise generated by this stage would be largely dominant), thus it is possible to maximally benefit from the reduction of its differential-mode component.

Revision history

Table 2. Document revision history

Date	Revision	Changes
06-May-2008	1	Initial release
15-Sep-2008	2	Modified: *Section 2.1*, *2.2*, *Appendix B* Added: *Appendix E*

AN2450
Application note

LLC resonant half-bridge converter design guideline

Silvio De Simone

Introduction

The growing popularity of the LLC resonant converter in its half-bridge implementation (see *Figure 1 on page 4*) is due to its high-efficiency, low level of EMI emissions, and its ability to achieve high power density. Such features perfectly fit the power supply demand of many modern applications such as LCD and PDP TV or 80+ initiative compliant ATX silver box. One of the major difficulties that engineers are facing with this topology is the lack of information concerning the way the converter operates and, therefore, the way to design it in order to optimize its features.

The purpose of this application note is to provide a detailed quantitative analysis of the steady state operation of the topology that can be easily translated into a design procedure.

Exact analysis of LLC resonant converters (see *1.* of *Section 9: Reference on page 34*) leads to a complex model that cannot be easily used to derive a handy design procedure. R. L. Steigerwald (see *2.* of *Section 9: Reference*) has described a simplified method, applicable to any resonant topology, based on the assumption that input to output power transfer is essentially due to the fundamental Fourier series components of currents and voltages.

This is what is commonly known as the “first harmonic approximation” (FHA) technique, which enables the analysis of resonant converters by means of classical complex ac circuit analysis. This is the approach that has been used in this paper.

The same methodology has been used by T. Duerbaum (see *3.* of *Section 9*) who has highlighted the peculiarities of this topology stemming from its multi-resonant nature. Although it provides an analysis useful to set up a design procedure, the quantitative aspect is not fully complete since some practical design constraints, especially those related to soft-switching, are not addressed. In (see *4.* of *Section 9*) a design procedure that optimizes transformer's size is given but, again, many other significant aspects of the design are not considered.

The application note starts with a brief summary of the first harmonic approximation approach, giving its limitations and highlighting the aspects it cannot predict. Then, the LLC resonant converter is characterized as a two-port element, considering the input impedance, and the forward transfer characteristic. The analysis of the input impedance is useful to determine a necessary condition for Power MOSFETs' ZVS to occur and allows the designer to predict how conversion efficiency behaves when the load changes from the maximum to the minimum value. The forward transfer characteristic (see *Figure 3 on page 10*) is of great importance to determine the input to output voltage conversion ratio and provides considerable insight into the converter's operation over the entire range of input voltage and output load. In particular, it provides a simple graphical means to find the condition for the converter to regulate the output voltage down to zero load, which is one of the main benefits of the topology as compared to the traditional series resonant converter.

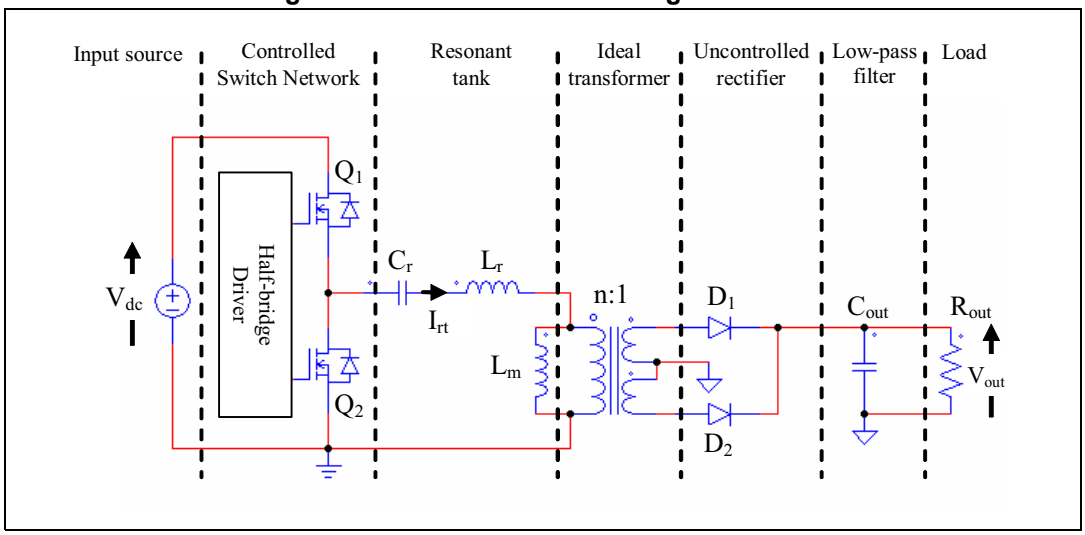
Contents

List of figures

1 FHA circuit model

The FHA approach is based on the assumption that the power transfer from the source to the load through the resonant tank is almost completely associated to the fundamental harmonic of the Fourier expansion of the currents and voltages involved. This is consistent with the selective nature of resonant tank circuits.

Figure 1. LLC resonant half-bridge converter



The harmonics of the switching frequency are then neglected and the tank waveforms are assumed to be purely sinusoidal at the fundamental frequency: this approach gives quite accurate results for operating points at and above the resonance frequency of the resonant tank (in the continuous conduction mode), while it is less accurate, but still valid, at frequencies below the resonance (in the discontinuous conduction mode).

It is worth pointing out also that many details of circuit operation on a cycle-to-cycle time base will be lost. In particular, FHA provides only a necessary condition for MOSFETs' zero-voltage switching (ZVS) and does not address secondary rectifiers' natural ability to work always in zero-current switching (ZCS). A sufficient condition for Power MOSFETs' ZVS will be determined in *Section 3: ZVS constraints on page 16* still in the frame of FHA approach.

Let us consider the simple case of ideal components, both active and passive.

The two Power MOSFETs of the half-bridge in *Figure 1* are driven on and off symmetrically with 50% duty cycle and no overlapping. Therefore the input voltage to the resonant tank $v_{sq}(t)$ is a square waveform of amplitude V_{dc}, with an average value of $V_{dc}/2$. In this case the capacitor C_r acts as both resonant and dc blocking capacitor. As a result, the alternate voltage across C_r is superimposed to a dc level equal to $V_{dc}/2$.

The input voltage waveform $v_{sq}(t)$ of the resonant tank in *Figure 1* can be expressed in Fourier series:

Equation 1

$$v_{sq}(t) = \frac{V_{dc}}{2} + \frac{2}{\pi}V_{dc}\sum_{n=1,3,5,\ldots}\frac{1}{n}\sin(n2\pi f_{sw}t)$$

whose fundamental component $v_{i.FHA}(t)$ (in phase with the original square waveform) is:

Equation 2

$$v_{iFHA}(t) = \frac{2}{\pi} V_{dc} \sin(2\pi f_{sw} t)$$

where f_{sw} is the switching frequency. The rms value $V_{i.FHA}$ of the input voltage fundamental component is:

Equation 3

$$v_{iFHA} = \frac{\sqrt{2}}{\pi} V_{dc}$$

As a consequence of the above mentioned assumptions, the resonant tank current $i_{rt}(t)$ will be also sinusoidal, with a certain rms value I_{rt} and a phase shift Φ with respect to the fundamental component of the input voltage:

Equation 4

$$i_{rt}(t) = \sqrt{2} I_{rt} \sin(2\pi f_{sw} t - \Phi) = \sqrt{2} I_{rt} \cos\Phi \bullet \sin(2\pi f_{sw} t) - \sqrt{2} I_{rt} \sin\Phi \bullet \cos(2\pi f_{sw} t)$$

This current lags or leads the voltage, depending on whether inductive reactance or capacitive reactance dominates in the behavior of the resonant tank in the frequency region of interest. Irrespective of that, $i_{rt}(t)$ can be obtained as the sum of two contributes, the first in phase with the voltage, the second with 90° phase-shift with respect to it.

The dc input current $I_{i.dc}$ from the dc source can also be found as the average value, along a complete switching period, of the sinusoidal tank current flowing during the high-side MOSFET conduction time, when the dc input voltage is applied to the resonant tank:

Equation 5

$$I_{idc} = \frac{1}{T_{sw}} \int_0^{\frac{T_{sw}}{2}} i_{rt}(t) dt = \frac{\sqrt{2}}{\pi} I_{rt} \cos\Phi$$

where T_{sw} is the time period at switching frequency.

The real power P_{in}, drawn from the dc input source (equal to the output power P_{out} in this ideal case) can now be calculated as both the product of the input dc voltage V_{dc} times the average input current $I_{i.dc}$ and the product of the rms values of the voltage and current's first harmonic, times $\cos\Phi$:

Equation 6

$$P_{in} = V_{dc} I_{idc} = V_{iFHA} I_{rt} \cos\Phi$$

the two expressions are obviously equivalent.

The expression of the apparent power P_{app} and the reactive power P_r are respectively:

Equation 7

$$P_{app} = V_{iFHA} I_{rt} \qquad P_r = V_{iFHA} I_{rt} \sin\Phi$$

Let us consider now the output rectifiers and filter part. In the real circuit, the rectifiers are driven by a quasi-sinusoidal current and the voltage reverses when this current becomes zero; therefore the voltage at the input of the rectifier block is an alternate square wave in phase with the rectifier current of amplitude V_{out}.

The expressions of the square wave output voltage $v_{o.sq}(t)$ is:

Equation 8

$$V_{osq}(t) = \frac{4}{\pi}V_{out}\sum_{n=1,3,5..}\frac{1}{n}\sin(n2\pi f_{sw}t - \Psi)$$

which has a fundamental component $v_{o.FHA}(t)$:

Equation 9

$$V_{oFHT}(t) = \frac{4}{\pi}V_{out}\sin(2\pi f_{sw}t - \Psi)$$

whose rms amplitude is:

Equation 10

$$V_{oFHA} = \frac{2\sqrt{2}}{\pi}V_{out}$$

where Ψ is the phase shift with respect to the input voltage. The fundamental component of the rectifier current $_{irect}(t)$ will be:

Equation 11

$$i_{rect}(t) = \sqrt{2}I_{rect}\sin(2\pi f_{sw}t - \Psi)$$

where I_{rect} is its rms value.

Also in this case we can relate the average output current to the load I_{out} and also derive the ac current $I_{c.ac}$ flowing into the filtering output capacitor:

Equation 12

$$I_{out} = \frac{2}{T_{sw}}\int_{0}^{\frac{T_{sw}}{2}}|i_{rect}(t)|dt = \frac{2\sqrt{2}}{\pi}I_{rect} = \frac{P_{out}}{V_{out}} = \frac{V_{out}}{R_{out}}$$

Equation 13

$$I_{cac} = \sqrt{I_{rect}^{2} - I_{out}^{2}}$$

where P_{out} is the output power associated to the output load resistance R_{out}.

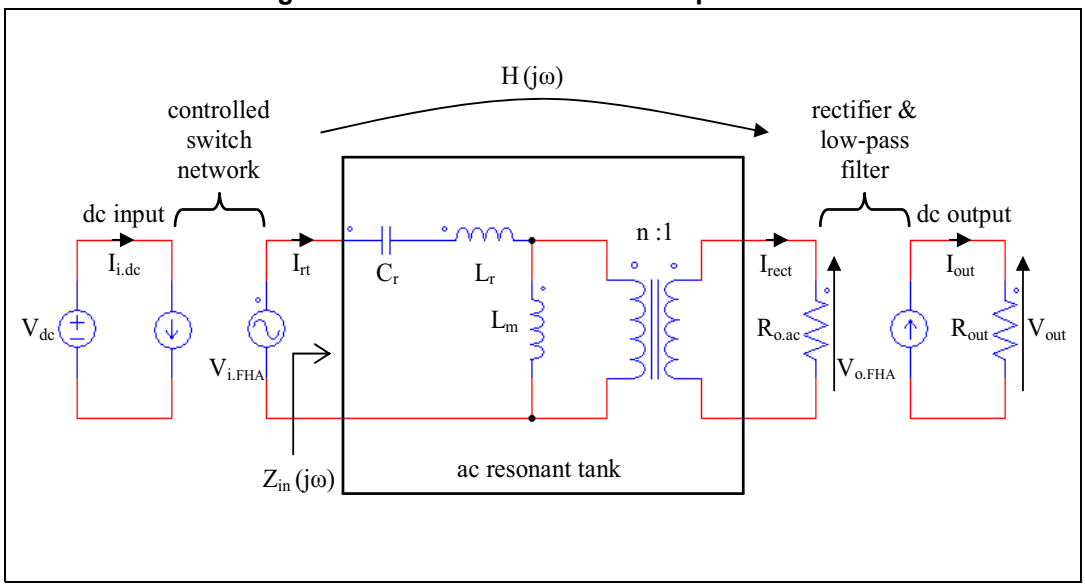
Since $v_{o.FHA}(t)$ and $i_{rect}(t)$ are in phase, the rectifier block presents an effective resistive load to the resonant tank circuit, $R_{o.ac}$, equal to the ratio of the instantaneous voltage and current:

Equation 14

$$R_{oac} = \frac{v_{oFHA}(t)}{i_{rect}(t)} = \frac{V_{oFHA}}{I_{rect}} = \frac{8}{\pi^2}\frac{V^2_{out}}{P_{out}} = \frac{8}{\pi^2}R_{out}$$

Thus, in the end, we have transformed the non linear circuit of *Figure 1* into the linear circuit of *Figure 2*, where the ac resonant tank is excited by an effective sinusoidal input source and drives an effective resistive load. This transformation allows the use of complex ac-analysis methods to study the circuit and, furthermore, to pass from ac to dc parameters (voltages and currents), since the relationships between them are well-defined and fixed (see *Equation 3*, *Equation 5*, *Equation 6*, *Equation 10* and *Equation 12* above).

Figure 2. FHA resonant circuit two port model



The ac resonant tank in the two-port model of *Figure 2* can be defined by its forward transfer function H(s) and input impedance $Z_{in}(s)$:

Equation 15

$$H(s) = \frac{V_{oFHA}(s)}{V_{iFHA}(s)} = \frac{1}{n}\frac{n^2 R_{oac} \parallel sL_m}{Z_{in}(s)}$$

Equation 16

$$Z_{in}(s) = \frac{V_{iFHA}(s)}{I_{rt}(s)} = \frac{1}{sC_r} + sL_r + n^2 R_{oac} \parallel sL_m$$

For the discussion that follows it is convenient to define the effective resistive load reflected to the primary side of the transformer R_{ac}:

Equation 17

$$R_{ac} = n^2 R_{oac}$$

And the so-called “normalized voltage conversion ratio” or “voltage gain” $M(f_{sw})$:

Equation 18

$$M(f_{sw}) = n\left\|H(j2\pi f_{sw})\right\| = n\frac{V_{oFHA}}{V_{iFHA}}$$

It can be demonstrated (by applying the relationships of *Equation 3*, *Equation 10* and *Equation 18* to the circuit in *Figure 2*) that the input to output dc-dc voltage conversion ratio is equal to:

Equation 19

$$\frac{V_{out}}{V_{dc}} = \frac{1}{2n}M(f_{sw})$$

In other words, the voltage conversion ratio is equal to one half the module of resonant tank's forward transfer function evaluated at the switching frequency.

2 Voltage gain and input impedance

Starting from *Equation 18* we can obtain the expression of the voltage gain:

Equation 20

$$M(f_n, \lambda, Q) = \frac{1}{\sqrt{\left(1 + \lambda - \frac{\lambda}{f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}}$$

with the following parameter definitions:

resonance frequency: $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$

characteristic impedance: $Z_o = \sqrt{\frac{L_r}{C_r}} = 2\pi f_r L_r = \frac{1}{2\pi f_r C_r}$

quality factor: $Q = \frac{Z_o}{R_{ac}} = \frac{Z_o}{n^2 R_{oac}} = \frac{\pi^2}{8}\frac{Z_0}{n^2}\frac{P_{out}}{V^2_{out}}$

inductance ratio: $\lambda = \frac{L_r}{L_m}$

normalized frequency: $f_n = \frac{f_{sw}}{f_r}$

Under no-load conditions, (i.e. Q = 0) the voltage gain assumes the following form:

Equation 21

$$M_{OL}(f_n, \lambda) = \frac{1}{\left|1 + \lambda - \frac{\lambda}{f_n^2}\right|}$$

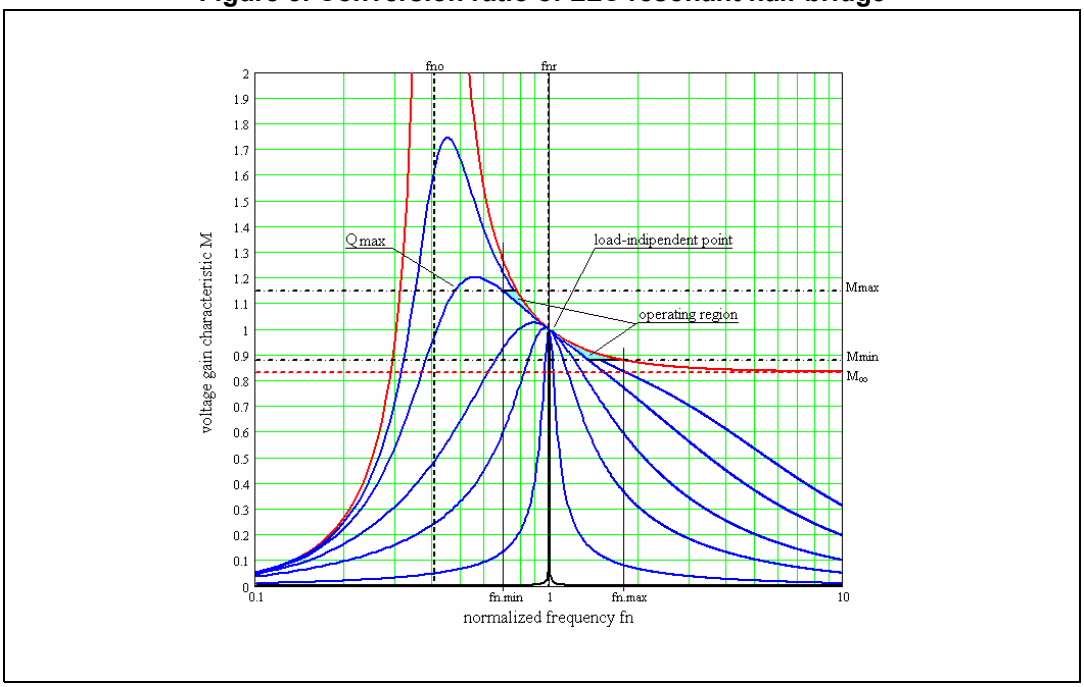
Figure 3 shows a family of plots of the voltage gain versus normalized frequency. For different values of Q, with $\lambda = 0.2$, it is clearly visible that the LLC resonant converter presents a load-independent operating point at the resonance frequency f_r ($f_n = 1$), with unity gain, where all the curves are tangent (and the tangent line has a slope -2λ). Fortunately, this load-independent point occurs in the inductive region of the voltage gain characteristic, where the resonant tank current lags the input voltage square waveform (which is a necessary condition for ZVS behavior).

The regulation of the converter output voltage is achieved by changing the switching frequency of the square waveform at the input of the resonant tank: since the working region is in the inductive part of the voltage gain characteristic, the frequency control circuit that keeps the output voltage regulated acts by increasing the frequency in response to a decrease of the output power demand or to an increase of the input dc voltage. Considering this, the output voltage can be regulated against wide loads variations with a relatively narrow switching frequency change, if the converter is operated close to the load-independent point. Looking at the curves in *Figure 3*, it is obvious that the wider the input dc voltage range is, the wider the operating frequency range will be, in which case it is difficult

to optimize the circuit. This is one of the main drawbacks common to all resonant topologies.

This is not the case, however, when there is a PFC pre-regulator in front of the LLC converter, even with a universal input mains voltage (85 V_{ac} - 264 V_{ac}). In this case, in fact, the input voltage of the resonant converter is a regulated high voltage bus of ~400 V_{dc} nominal, with narrow variations in normal operation, while the minimum and maximum operating voltages will depend, respectively, on the PFC pre-regulator hold-up capability during mains dips and on the threshold level of its overvoltage protection circuit (about 10 - 15% over the nominal value). Therefore, the resonant converter can be optimized to operate at the load-independent point when the input voltage is at nominal value, leaving to the step-up capability of the resonant tank (i.e. operation below resonance) the handling of the minimum input voltage during mains dips.

Figure 3. Conversion ratio of LLC resonant half-bridge



The red curve in *Figure 3* represents the no-load voltage gain curve M_{OL}; for normalized frequency going to infinity, it tends to an asymptotic value M_∞:

Equation 22

$$M_\infty = M_{OL}(f_n \to \infty, \lambda) = \frac{1}{1+\lambda}$$

Moreover, a second resonance frequency f_o can be found, which refers to the no-load condition or when the secondary side diodes are not conducting (i.e. the condition where the total primary inductance $L_r + L_m$ resonates with the capacitor C_r); $f_o$is defined as:

Equation 23

$$f_o = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} = f_r\sqrt{\frac{\lambda}{1+\lambda}}$$

or in normalized form:

Equation 24

$$f_{no} = \frac{f_o}{f_r} = \sqrt{\frac{\lambda}{1+\lambda}}$$

At this frequency the no-load gain curve M_{OL} tends to infinity.

By imposing that the minimum required gain M_{min} (at max. input dc voltage) is greater than the asymptotic value M_∞, it is possible to ensure that the converter can work down to no-load at a finite operating frequency (which will be the maximum operating frequency of the converter):

Equation 25

$$M_{min} = 2n\frac{V_{out}}{V_{dcmax}} > \frac{1}{1+\lambda}$$

The maximum required gain M_{max} (at min. input dc voltage) at max. output load (max. P_{out}), that is at max. Q, will define the min. operating frequency of the converter:

Equation 26

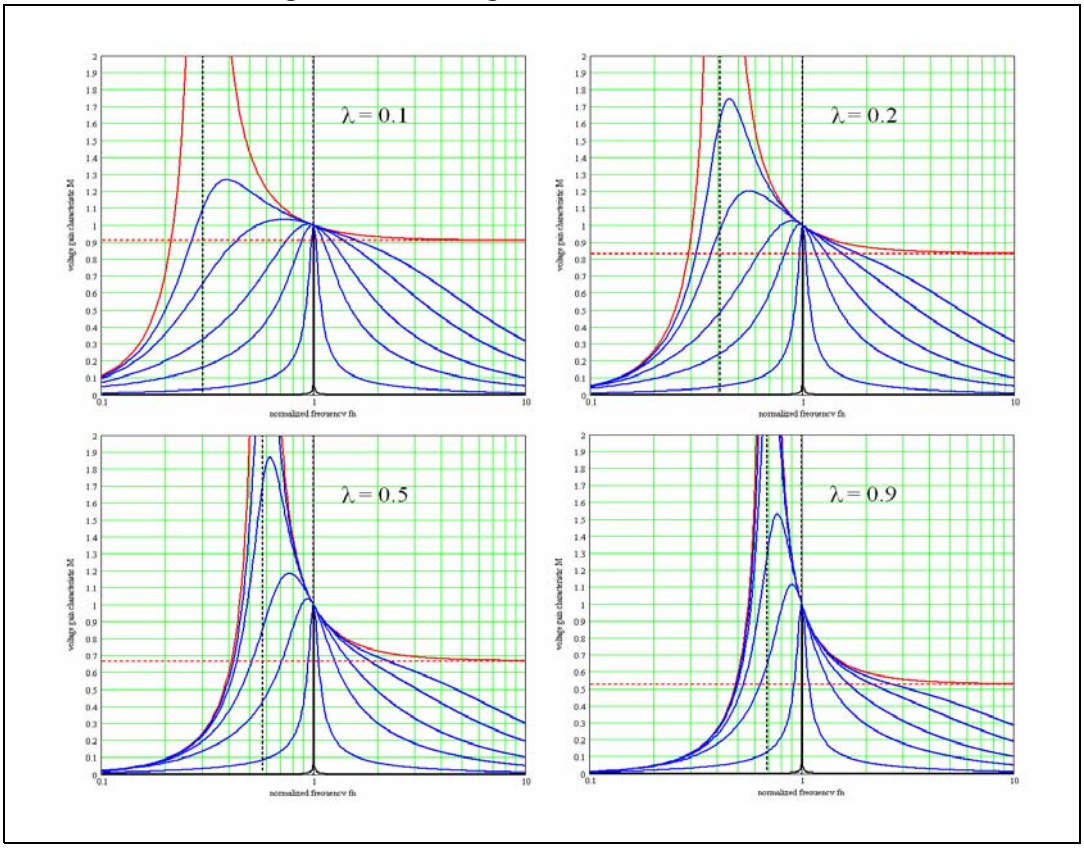
$$M_{max} = 2n\frac{V_{out}}{V_{dcmin}}$$

Given the input voltage range ($V_{dc.min}$ - $V_{dc.max}$), three types of operations are possible:

- always below resonance frequency (step-up operations)
- always above resonance frequency (step-down operations)
- across the resonance frequency (shown in *Figure 3*).

Looking at *Figure 4*, we can see that an increase of the inductance ratio value λ has the effect of shrinking the gain curves in the M - f_n plane toward the resonance frequency f_{nr} (which means the no-load resonance frequency f_{no} increases) and contemporaneously reduces the asymptotic level M_∞ of the no-load gain characteristic. At the same time the peak gain of each curve increases.

Figure 4. Shrinking effect of λ value increase



Starting from *Equation 16 on page 7* we can obtain the expression of the normalized input impedance Z_n of the resonant tank:

Equation 27

$$Z_n(f_n, \lambda, Q) = \frac{Z_{in}(f_n, \lambda, Q)}{Z_o} = \frac{jf_n}{\lambda + jf_nQ} + \frac{1 - f_n^2}{jf_n}$$

whose magnitude is plotted in *Figure 5*, at different Q values, with λ = 0.2.

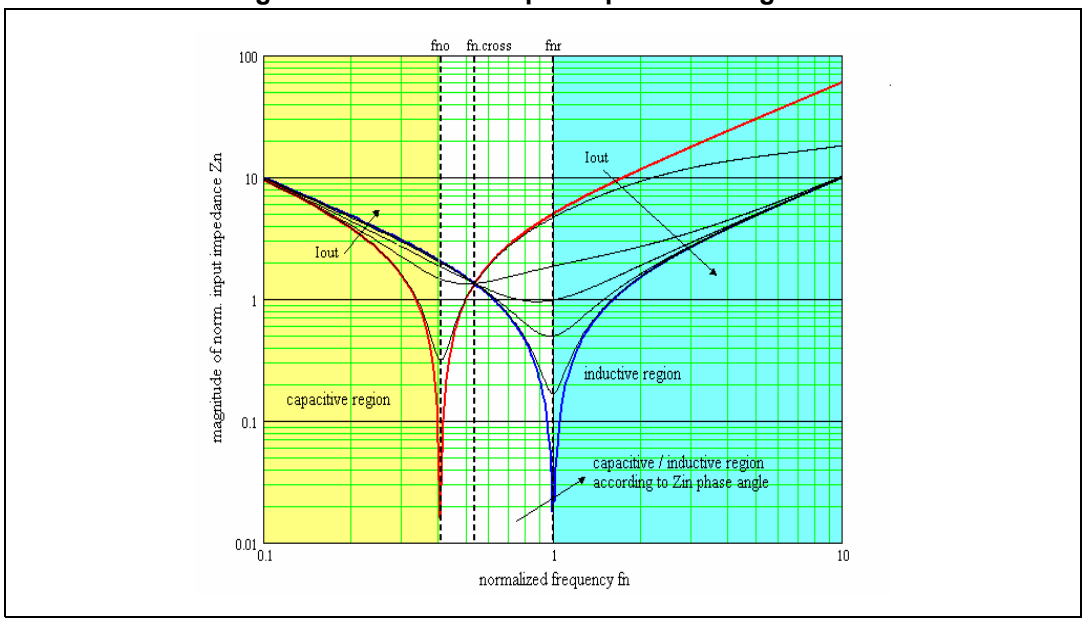
The red and blue curves in the above mentioned figure represent the no-load and short-circuit cases respectively, and are characterized by asymptotes at the two normalized resonance frequencies f_{no} and f_{nr} (= 1). All the curves at different values of Q intercept at normalized frequency $f_{n.cross}$:

Equation 28

$$f_{n.cross} = \sqrt{\frac{2\lambda}{1 + 2\lambda}}$$

At frequencies higher than the crossing frequency $f_{n.cross}$, the input impedance behaves such that at increasing output current I_{out} (that is at increasing P_{out} and Q) it decreases (coherently to the load resistance); the opposite happens at frequencies lower than $f_{n.cross}$, where the input impedance increases, while the output load resistance decreases.

Figure 5. Normalized input impedance magnitude



The ac analysis can also help to estimate converter's efficiency η and predict how this changes with the load. Considering the generic model similar to the one in *Figure 2 on page 7*, where the resonant tank includes also the dissipative elements (i.e. series resistors for magnetic components winding losses and capacitor's ESR, and parallel resistors for magnetic losses of inductors and transformer), we can compute the transfer function $H_{LOSS}(j\omega)$ and the input impedance $Z_{in.LOSS}(j\omega)$. By calculating input and output power in terms of H_{LOSS} and $Z_{in.LOSS}$, we get:

Equation 29

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\|H_{LOSS}(j\omega)\|^2}{R_{o.ac}Re[Y_{inLOSS}(j\omega)]}$$

where $Y_{in.LOSS}$ is the admittance (reciprocal of $Z_{in.LOSS}$) and the input and output power are expressed as:

Equation 30

$$P_{in} = V_{iFHA}I_{rt}\cos\Phi = V_{iFHA}^2 Re\left[\frac{1}{Z_{inLOSS}(j\omega)}\right]$$

Equation 31

$$P_{out} = V_{o\cdot FHA}I_{rect} = \frac{V^2_{o\cdot FHA}}{R_{o\cdot ac}} = \frac{V^2_{iFHA}}{R_{o\cdot ac}} \cdot \|H_{LOSS}(j\omega)\|^2$$

The region on the left-hand side of the diagram in *Figure 5*, i.e. for a normalized frequency lower than f_{no}, is the capacitive region, where the tank current leads the half-bridge square voltage; at normalized frequency higher than the resonance frequency f_{nr} (= 1), on the right-hand side region, the input impedance is inductive, and the resonant tank current lags the input voltage. In the region between the two resonance frequencies the impedance can be either capacitive or inductive, depending on the value of the impedance phase angle.

By imposing that the imaginary part of $Z_n(f_n, \lambda, Q)$ is zero (which means imposing that Z_{in} has zero phase angle, as Z_o is real and does not affect the phase), we can find the boundary condition between capacitive and inductive mode operation of the LLC resonant converter.

The analytical results are the following:

Equation 32

$$f_{nZ}(\lambda, Q) = \sqrt{\frac{Q^2 - \lambda(1+\lambda) + \sqrt{[Q^2 - \lambda(1+\lambda)]^2 + 4Q^2\lambda^2}}{2Q^2}}$$

Equation 33

$$Q_Z(f_n, \lambda) = \sqrt{\frac{\lambda}{1 - f_n^2} - \left(\frac{\lambda}{f_n}\right)^2}$$

where f_{nZ} represents the normalized frequency where, for a fixed couple (λ- Q), the input resonant tank impedance is real (and only real power is absorbed from the source); while Q_Z is the maximum value of the quality factor, below which, at a fixed normalized frequency and inductance ratio (f_n - λ) the tank impedance is inductive; hence, the maximum voltage gain available in that condition is also found:

Equation 34

$$M_{MAX}(\lambda, Q) = M(f_{nZ}(\lambda, Q), \lambda, Q)$$

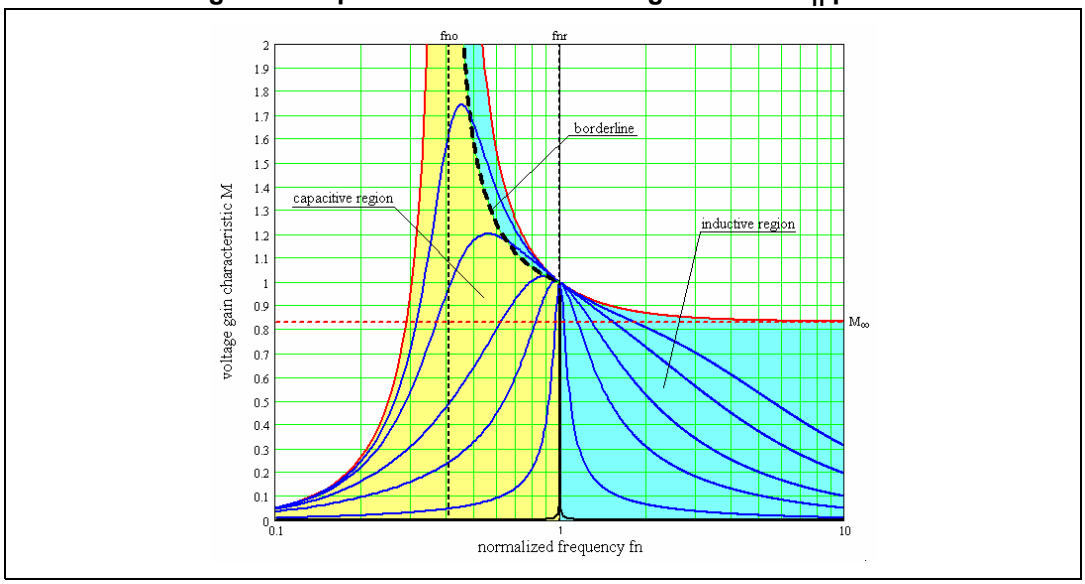
By plotting the locus of operating points [$M_{MAX}(\lambda, Q)$, $f_{nZ}(\lambda,Q)$], whose equation on M - f_n plane is the following:

Equation 35

$$M_Z(f_n, \lambda) = \frac{f_n}{\sqrt{f_n^2(1+\lambda) - \lambda}}$$

we can draw the borderline between capacitive and inductive mode in the region between the two resonance frequencies, shown in *Figure 6*. It is also evident that the peak value of the gain characteristics for a given quality factor Q value, already lies in the capacitive region.

Figure 6. Capacitive and inductive regions in M - f_n plane



Moreover, by equating the second term of (*Equation 35*) to the maximum required gain M_{max} (at minimum input voltage), and solving for f_n, we get the minimum operating frequency $f_{n.min}$ which allows the required maximum voltage gain at the boundary between capacitive and inductive mode:

Equation 36

$$f_{n.min} = \sqrt{\frac{1}{1+\frac{1}{\lambda}\left(1-\frac{1}{M_{max}^{2}}\right)}}$$

Furthermore, by substituting the minimum frequency (*Equation 36*) into the *Equation 33*, we get the maximum quality factor Q_{max} which allows the required maximum voltage gain at the boundary between capacitive and inductive mode:

Equation 37

$$Q_{max} = \frac{\lambda}{M_{max}}\sqrt{\frac{1}{\lambda}+\frac{M_{max}^{2}}{M_{max}^{2}-1}}$$

Finally, by equating the second term of the no-load transfer function (*Equation 21 on page 9*) to the minimum required voltage gain M_{min}, it is possible to find the expression of the maximum normalized frequency $f_{n.max}$:

Equation 38

$$f_{n.max} = \sqrt{\frac{1}{1+\frac{1}{\lambda}\left(1-\frac{1}{M_{min}}\right)}}$$

3 ZVS constraints

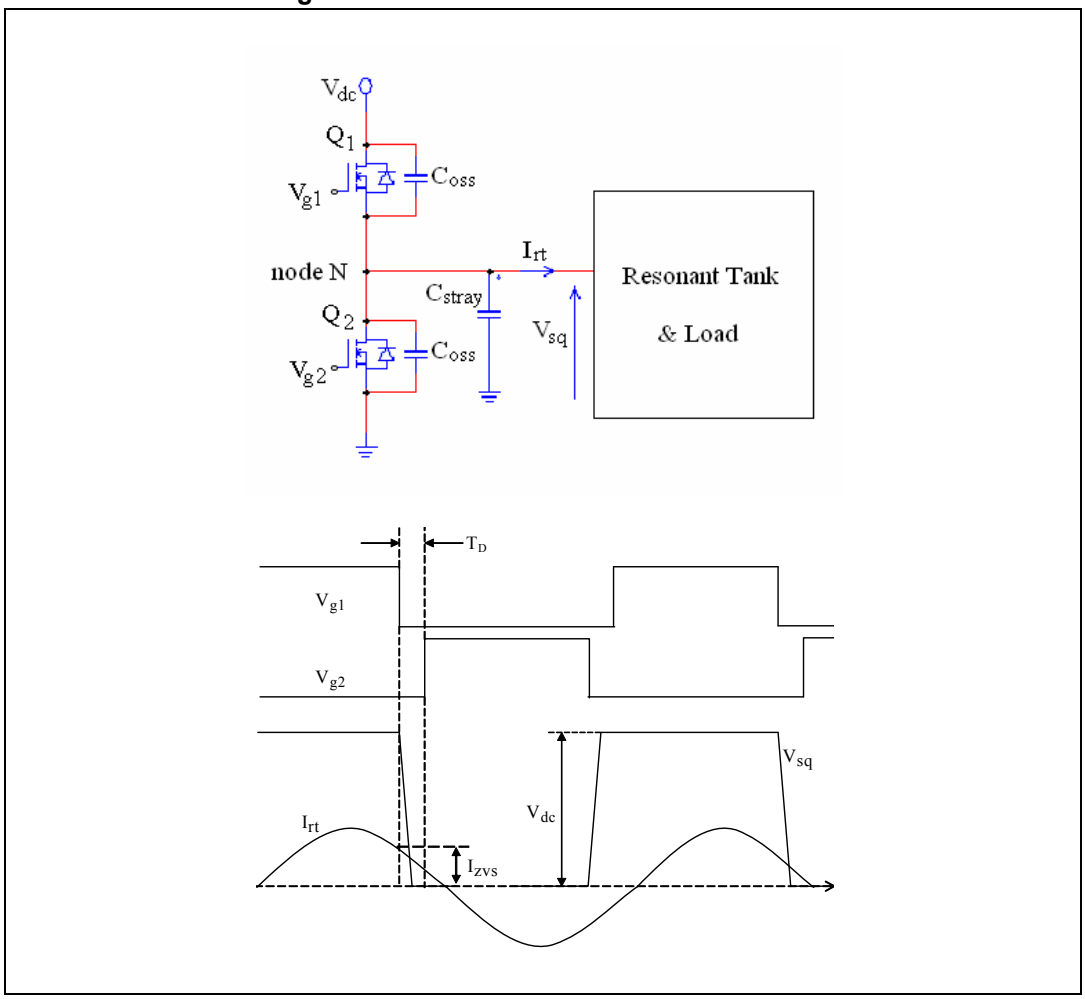
The assumption that the working region lies inside the inductive region of operation is only a necessary condition for the ZVS of the half-bridge MOSFETs, but not sufficient; this is because the parasitic capacitance of the half-bridge midpoint, neglected in the FHA analysis, needs energy to be charged and depleted during transitions. In order to understand ZVS behavior, refer to the half-bridge circuit in *Figure 7*, where the capacitors C_{oss} and C_{stray} are, respectively, the effective drain-source capacitance of the Power MOSFETs and the total stray capacitance present across the resonant tank impedance, so that the total capacitance C_{zvs} at node N is:

Equation 39

$$C_{zvs} = 2C_{OSS} + C_{stray}$$

which, during transitions, swings by $\Delta V = V_{dc}$. To allow ZVS, the MOSFET driving circuit is such that a dead time T_D is inserted between the end of the ON-time of either MOSFET and the beginning of the ON-time of the other one, so that both are not conducting during T_D.

Figure 7. Circuit behavior at ZVS transition



Due to the phase lag of the input current with respect to the input voltage, at the end of the first half cycle the inductor current I_{rt} is still flowing into the circuit and, therefore it can deplete C_{ZVS} so that its voltage swings from ΔV to zero (it will be vice versa during the second half cycle).

In order to guarantee ZVS, the tank current at the end of the first half cycle (considering the dead time negligible as compared to the switching period, so that the current change is negligible as well) must exceed the minimum value necessary to deplete C_{ZVS} within the dead time interval T_D, which means:

Equation 40

$$I_{zvs} = i_{rt}\left(\frac{T_{sw}}{2}\right) = C_{zvs}\frac{\Delta V}{T_D} = (2C_{OSS} + C_{stray})\frac{V_{dc}}{T_D}$$

This current equals, of course, the peak value of the reactive current flowing through the resonant tank (it is 90° out-of-phase); the one that determines the reactive power level into the circuit:

Equation 41

$$I_{zvs} = \sqrt{2} I_{rt} \sin\Phi$$

Moreover, as the rms component of the tank current associated to the active power is:

Equation 42

$$I_{act} = I_{rt}\cos\Phi = \frac{P_{in}}{V_{iFHA}}$$

we can derive also the rms value of the resonant tank current and the phase lag Φ between input voltage and current (that is the input impedance phase angle at that operating point):

Equation 43

$$I_{rt} = \sqrt{I_{rt}^2\cos(\Phi)^2 + I_{rt}^2\sin(\Phi)^2} = \sqrt{\left(\frac{P_{in}}{V_{iFHA}}\right)^2 + \frac{I_{zvs}}{2}^2}$$

Equation 44

$$\Phi = a\cos\left(\frac{P_{in}}{V_{iFHA} I_{rt}}\right)$$

Thus we can write the following analytic expression:

Equation 45

$$\tan(\Phi) = \frac{Im[Z_n(f_n, \lambda, Q)]}{Re[Z_n(f_n, \lambda, Q)]} \geq \frac{C_{zvs}}{\pi T_D}\frac{V_{dc}^2}{P_{in}}$$

which is the sufficient condition for ZVS of the half-bridge Power MOSFETs, to be applied to the whole operating range. The solution of *Equation 45* for the quality factor Q_{zvs} that ensures ZVS behavior at full load and minimum input voltage is not convenient.

Therefore, we can calculate the Q_{max} value (at max. output power and min. input voltage), where the input impedance has zero phase, and take some margin (5% - 10%) by choosing:

Equation 46

$$Q_{zvs.1} = 90\% \div 95\% \bullet Q_{max}$$

and check that the condition (*Equation 45*) is satisfied at the end of the process, once the resonant tank has been completely defined. The process will be iterated if necessary.

Of course the sufficient condition for ZVS needs to be satisfied also at no-load and maximum input voltage; in this operating condition it is still possible to find an additional constraint on the maximum quality factor at full load to guarantee ZVS. In fact the input impedance at no-load $Z_{in.OL}$ has the following expression:

Equation 47

$$Z_{inOL}(f_n) = jZ_o\left[f_n\left(1+\frac{1}{\lambda}\right)-\frac{1}{f_n}\right]$$

Taking into account that:

Equation 48

$$Z_o = R_{ac}Q$$

and writing the sufficient condition for ZVS in this operating condition, that is:

Equation 49

$$\frac{V_{iFHAmax}}{\left\|Z_{inOL}(f_{nmax})\right\|} \geq \frac{I_{zvs(Vdcmax)}}{\sqrt{2}}$$

we get the constraint on the quality factor for the ZVS at no-load and maximum input voltage:

Equation 50

$$Q_{zvs2} \leq \frac{2}{\pi}\frac{\lambda f_{nmax}}{(\lambda+1)f_{nmax}^{\ 2}-\lambda}\frac{T_D}{R_{ac}C_{zvs}}$$

Therefore, in order to guarantee ZVS over the whole operating range of the resonant converter, we have to choose a maximum quality factor value lower than the smaller of $Q_{zvs.1}$ and $Q_{zvs.2}$.

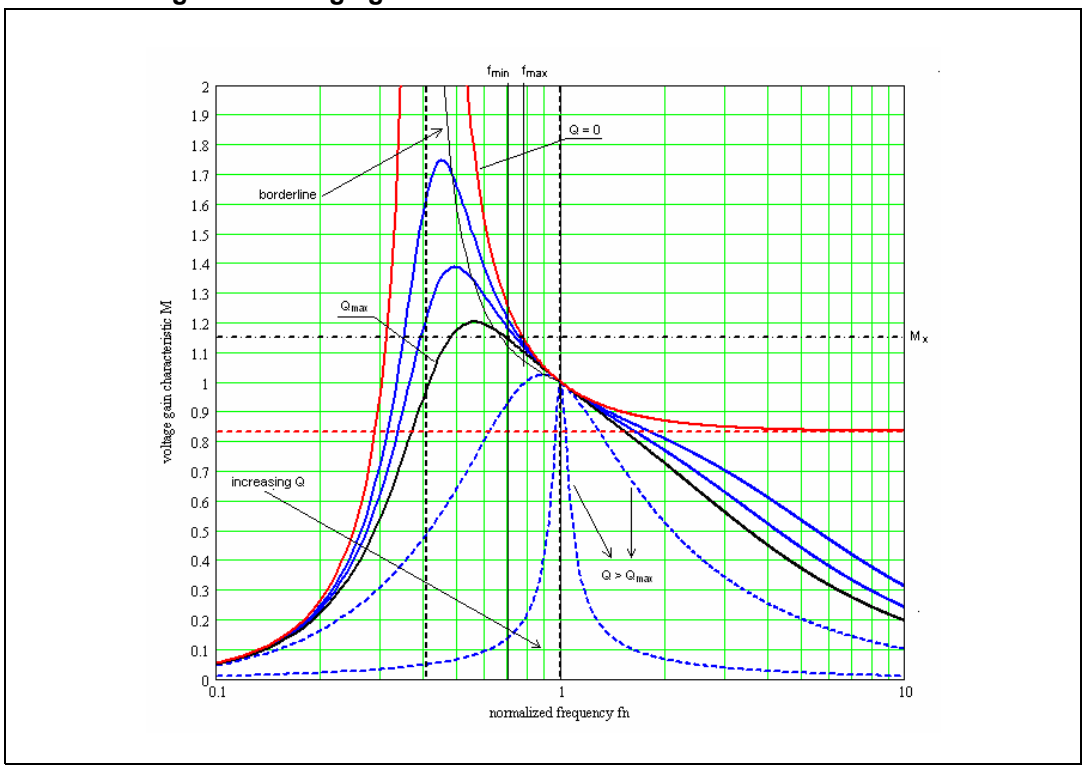
4 Operation under overload and short-circuit condition

An important aspect to analyze is the converter's behavior during output overload and/or short-circuit.

Referring to the voltage gain characteristics in *Figure 8*, let us suppose that the resonant tank has been designed to operate in the inductive region for a maximum output power $P_{out.max}$ (corresponding to the curve $Q = Q_{max}$) at a given output-to-input voltage ratio (corresponding to the horizontal line $M = M_x$) greater than 1.

When the output power is increased from zero to the maximum value, the gain characteristic relative to each power level changes progressively from the red curve (Q = 0) to the black one (Q_{max}). The control loop keeps the value of M equal to M_x, then the quiescent point moves along the horizontal line $M = M_x$ and the operating frequency at each load condition is given by the abscissa of the crossover between the horizontal line $M = M_x$ and the voltage gain characteristic relevant to the associated value of Q.

Figure 8. Voltage gain characteristics of the LLC resonant tank



If the load is increased over the maximum specified (associated to the curve $Q = Q_{max}$) eventually the converter's operating point will invariably enter the capacitive region, where hard switching of Power MOSFETs may cause device failures, if no corrective action is taken.

In fact, for values of Q sufficiently greater than Q_{max} the intersection with the $M = M_x$ line will take place on the left-hand side of the borderline curve and, then, in the capacitive region; moreover, if Q exceeds the value corresponding to the characteristic curve tangent to $M = M_x$ there will no longer be a possible operating point with $M = M_x$. This means that the

converter will no longer be able to keep the output voltage regulated and the output voltage will fall despite the reduction of the operating frequency (feedback reversal).

Limiting the minimum operating frequency (e.g. at the frequency value corresponding to the intersection of $M = M_x$ with $Q = Q_{max}$) is not enough to prevent the converter from entering the capacitive region of operation. In fact, as the minimum frequency is reached, from that point onwards a further load increase will make the operating point move along the vertical line $f = f_{min}$ and eventually cross the borderline.

Limiting the minimum operating frequency is effective in preventing capacitive mode operation only if the minimum (normalized) frequency value is greater than 1. This suggests that, in response to an overload/short-circuit condition at the output, the converter operating frequency must be pushed above the resonance frequency (it is better if well above it) in order to decrease power throughput.

It is worth noticing that, if the converter is specified to deliver a peak output power (where output voltage regulation is to be maintained) greater than the maximum continuous output power for a limited time, the resonant tank must be designed for peak output power to make sure that it will not run in capacitive mode. Of course, its thermal design will consider only the maximum continuous power.

In any case, whatever the converter specified, short-circuit conditions or, in general, overload conditions exceeding the maximum specified for the tank circuit, need to be handled with additional means, such as a current limitation circuit.

5 Magnetic integration

The LLC resonant half-bridge is well suited for magnetic integration, i.e. to combine the inductors as well as the transformer into a single magnetic device. This can be easily recognized looking at the transformer's physical model in *Figure 9*, where the topological analogy with the inductive part of the LLC tank circuit is apparent. However, the real transformer has leakage inductance on the secondary side as well, which is completely absent in the model considered so far. To include the effect of secondary leakage in the FHA analysis, we need a particular transformer model and a simplifying assumption.

It is well known that there are an infinite number of electrically equivalent models of a given transformer, depending on the choice of the turn ratio of the ideal transformer included in the model. With an appropriate choice of this “equivalent” turn ratio n (obviously different from the “physical” turn ratio n_t = N1/N2) all the elements related to leakage flux can be located on the primary side.

This is the APR (all primary referred) model shown in *Figure 10*, which fits the circuit considered in the FHA analysis. It is possible to show that the APR model is obtained with the following choice of *n*:

Equation 51

$$n = k\sqrt{\frac{L_1}{L_2}}$$

with *k* transformer's coupling coefficient, L_1 inductance of the primary winding and L_2 inductance of each secondary winding. Note that L_r still has physical meaning: it is the primary inductance measured with the secondary windings shorted. Note also that the primary inductance L_1 must be unchanged. It is only differently split in the 2 models of *Figure 9* and *Figure 10*, hence, L_m will be the difference between L_1 and L_r.

In the end, the analysis done so far is directly applicable to real-world transformers provided they are represented by their equivalent APR model. Vice versa, a design flow based on the FHA analysis will provide the parameters of the APR model; hence, an additional step is needed to determine those of the physical model. In particular this applies to the turn number n_t, since L_r and L_m still have a connection with the physical world ($L_r + L_m = L_{L1} + L_\mu = L_1$).

Figure 9. Transformer's physical model

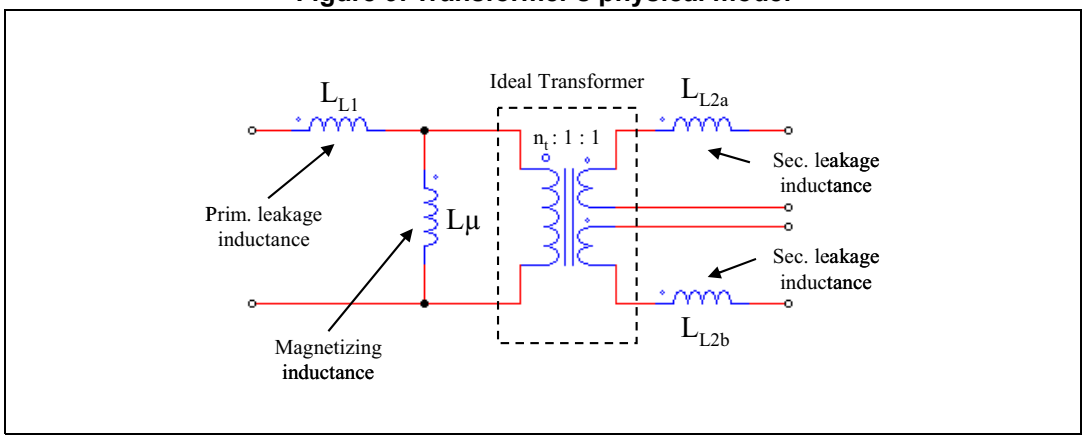
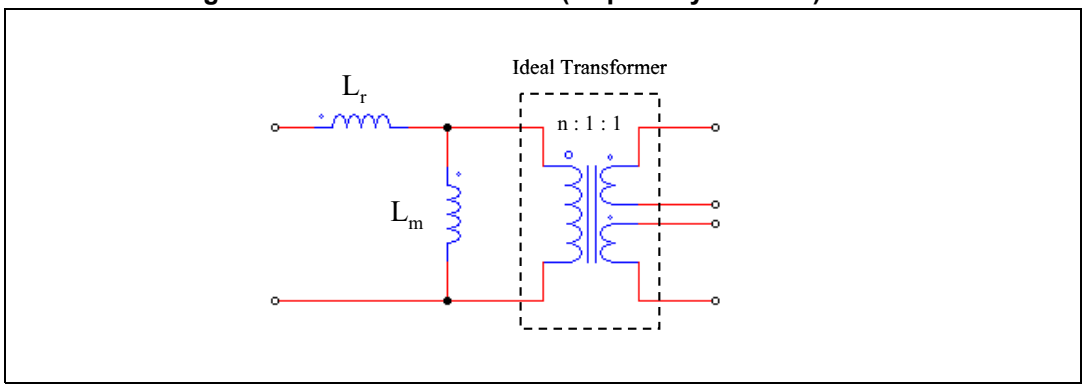


Figure 10. Transformer's APR (all primary referred) model



The problem is mathematically undetermined: there are 5 unknowns (L_{L1}, L_μ, n_t, and L_{L2a}, L_{L2b}) in the physical model and only three parameters in the APR model. The simplifying assumption that overcomes this issue is that of magnetic circuit symmetry: flux linkage is assumed to be exactly the same for both primary and secondary windings. This provides the two missing conditions:

Equation 52

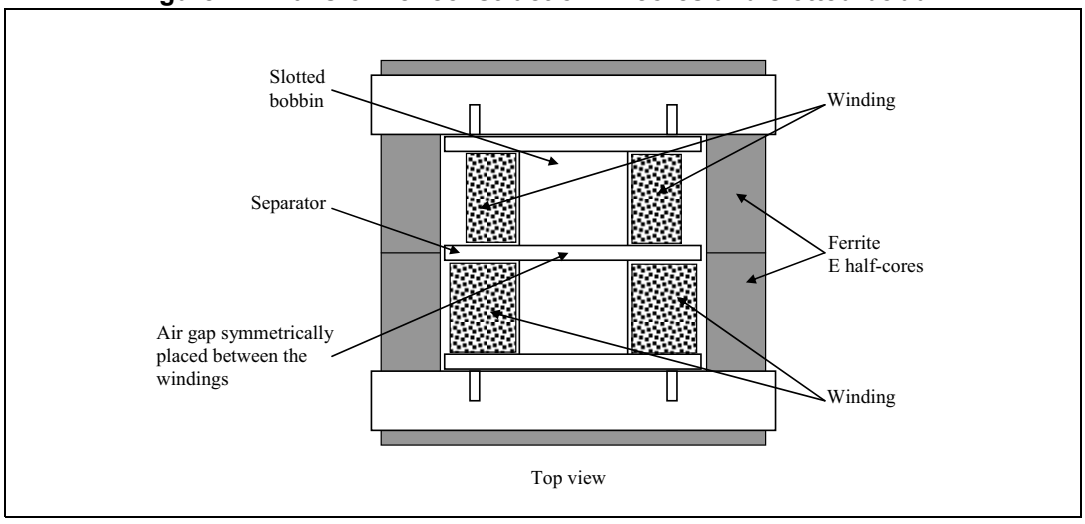
$$L_{L2a} = L_{L2b} = \frac{L_{L1}}{n_t^2}$$

With this assumption it is now possible to find the relationship between n and n_t:

Equation 53

$$n_t = n\sqrt{\frac{L_m + L_r}{L_m}} = n\sqrt{1+\lambda}$$

Figure 11. Transformer construction: E-cores and slotted bobbin



It is not difficult to find real-world structures where the condition of magnetic symmetry is quite close to reality. Consider for example the ferrite E-core plus slotted bobbin assembly, using side-by-side winding arrangement, shown in *Figure 11*.

6 Design procedure

Based on the analysis presented so far, a step-by-step design procedure of an LLC resonant converter is now proposed, which fulfills the following design specification and requires the additional information listed below:

- Design specification:
  - Input voltage range: $V_{dc.min}$ - $V_{dc.max}$
  - Nominal input voltage: $V_{dc.nom}$
  - Regulated output voltage: V_{out}
  - Maximum output power: P_{out}
  - Resonant frequency: f_r
  - Maximum operating frequency: f_{max}
- Additional info:
  - Parasitic capacitance at node N: C_{zvs}
  - Dead time of driving circuit: T_D
- General criteria for the design:
  - The converter will be designed to work at resonance at nominal input voltage.
  - The converter must be able to regulate down to zero load at maximum input voltage.
  - The converter will always work in ZVS in the whole operating range.
- 10 step procedure:
  - Step 1 - to fulfill the first criterion, impose that the required gain at nominal input voltage equals unity and calculate the transformer turn ratio:

Equation 54

$$M_{nom} = 2n\frac{V_{out}}{V_{dc.nom}} = 1 \quad \Rightarrow \quad n = \frac{1}{2}\frac{V_{dc.nom}}{V_{out}}$$

  - Step 2 - calculate the max. and min. required gain at the extreme values of the input voltage range:

Equation 55

$$M_{max} = 2n\frac{V_{out}}{V_{dc.min}}$$

Equation 56

$$M_{min} = 2n\frac{V_{out}}{V_{dc.max}}$$

– Step 3 - calculate the maximum normalized operating frequency (according to the definition):

Equation 57

$$f_{nmax} = \frac{f_{max}}{f_r}$$

– Step 4 - calculate the effective load resistance reflected at transformer primary side, from *Equation 14 on page 7* and *Equation 17 on page 7*:

Equation 58

$$R_{ac} = \frac{8}{\pi^2} n^2 \frac{V_{out}^2}{P_{out}}$$

– Step 5 - impose that the converter operates at maximum frequency at zero load and maximum input voltage, calculating the inductance ratio from *Equation 38 on page 15*:

Equation 59

$$\lambda = \frac{1 - M_{min}}{M_{min}} \frac{f_{nmax}^2}{f_{nmax}^2 - 1}$$

– Step 6 - calculate the max Q value to work in the ZVS operating region at minimum input voltage and full load condition, from *Equation 37 on page 15* and *Equation 46 on page 18*:

Equation 60

$$Q_{zvs1} = 95\% \bullet Q_{max} = 95\% \bullet \frac{\lambda}{M_{max}} \sqrt{\frac{1}{\lambda} + \frac{M_{max}^2}{M_{max}^2 - 1}}$$

– Step 7 - calculate the max Q value to work in the ZVS operating region at no-load condition and maximum input voltage, applying *Equation 50 on page 18*:

Equation 61

$$Q_{zvs2} = \frac{2}{\pi} \frac{\lambda f_{nmax}}{(\lambda + 1) f_{nmax}^2 - \lambda} \frac{T_D}{R_{ac} C_{zvs}}$$

– Step 8 - choose the max quality factor for ZVS in the whole operating range, such that:

Equation 62

$$Q_{zvs} \leq \min\{Q_{zvs1}, Q_{zvs2}\}$$

– Step 9 - calculate the minimum operating frequency at full load and minimum input voltage, according to the following approximate formula:

Equation 63

$$f_{min} = f_r \sqrt{\frac{1}{1 + \frac{1}{\lambda}\left(1 - \frac{1}{1 + \left(\frac{Q_{zvs}}{Q_{max}}\right)^4}\right)}}$$

$$M_{max}$$

– Step 10 - calculate the characteristic impedance of the resonant tank and all component values (from definition):

Equation 64

$$Z_o = Q_{zvs}R_{ac} \quad C_r = \frac{1}{2\pi f_r Z_o} \quad L_r = \frac{Z_o}{2\pi f_r} \quad L_m = \frac{L_r}{\lambda}$$

7 Design example

Here below, a design example follows for a 400 W resonant converter intended to be operated with a front-end PFC with a typical regulated bus voltage of about 400 V.

The STMicroelectronics® resonant controller L6599 is particularly suitable for this application. In fact it incorporates the necessary functions to properly drive the two half-bridge MOSFETs by a 50 percent fixed duty cycle with a fixed dead-time T_D, (between high-side and low-side MOSFET driving signals), changing the frequency according to the feedback signal in order to regulate the output voltages against load and input voltage variations. The main features of the L6599 are a non linear soft-start, a new current protection mode allowing to program the hiccup mode timing, a dedicated pin for sequencing or brown-out (pin LINE) and a standby pin (pin STBY) allowing for the burst mode operation at light load.

The converter specification data are the following:

- Nominal input DC voltage: 390 V
- Input DC voltage range: from 320 to 420 V
- Output voltages: 200 V at 1.6 A continuous current - 75 V at 1.0 A continuous current
- Resonance frequency: 120 kHz
- Max operating frequency: 150 kHz
- Delay time (L6599 datasheet): 270 ns
- Foreseen half-bridge total stray capacitance (at node N): 350 pF

The calculations have been done assuming that all power is delivered to the 200 V output voltage. Afterward, once the turn ratio has been defined, the transformer is designed to deliver the two output voltages, using the correct number of turns and the proper wire section.

The results of the 10 step procedure are summarized in *Table 1*:

Table 1. Design results

Step	Parameter
1	n = 0.975
2	M_{max} = 1.22 M_{min} = 0.93
3	$f_{n.max}$ = 1.25
4	R_{ac} = 77.05 Ω
5	λ = 0.21
6	$Q_{zvs.1}$ = 0.41
7	$Q_{zvs.2}$ = 1.01
8	Q_{zvs} = 0.41
9	f_{min} = 80.6 kHz
10	Z_o = 31.95 Ω C_r = 41.51 nF L_r = 42 µH L_m = 197 µH

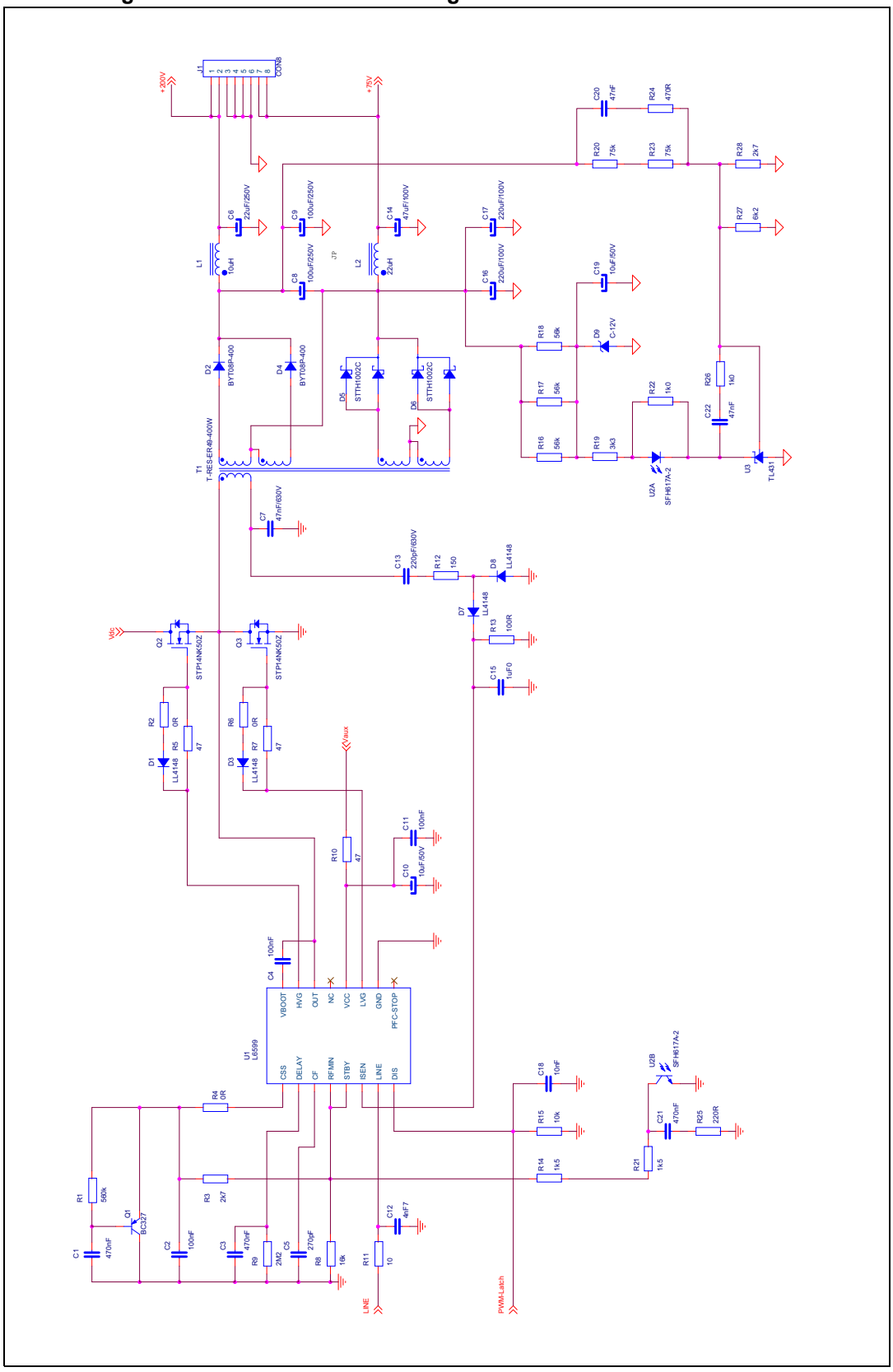
The chosen standard value of the resonant capacitor is 47 nF. The transformer has been designed using a two slot coil former and integrating both the series inductance L_r and the shunt inductance L_m, in order to obtain a magnetic component with the following parameters:

- $L_{p(SO)} = L_r + L_m = 240\ \mu H$ primary inductance (with secondary windings open)
- $L_{p(SS)} = L_r = 40\ \mu H$ primary inductance with secondary windings shorted
- $n_t = n \bullet \sqrt{1+\lambda} = 1.08$ transformer turn ratio

The number of primary turns has been found experimentally, by measuring the “specific leakage inductance” (i.e. the leakage inductance per square turns) of a few suitable ferrite cores, using a two slot winding configuration. The procedure consists of winding a few layers of turns on both slots of the coil former (same copper area for primary and secondary) and then measuring the inductance of one winding with the other one short-circuited. Dividing this measured value by the squared number of turns gives the specific leakage inductance of the core - coil former construction. The chosen ferrite core is a ER-49-27-17 type, material grade PC44, and the necessary number of primary turns to obtain the required leakage inductance is 19. Therefore, the total number of secondary turns for 200 V output is 18 (from the required turn ratio n_t).

The secondary side of the transformer consists of two center tap windings, one for each output, and the two output voltages (+75 V and +200 V) are obtained by series connecting the two secondary windings on the DC side (refer to the electrical schematic in *Figure 12* for better understanding of circuit configuration). The bottom winding (for +75 V output) has 7 turns, while the top winding consists of 11 (18 - 7) turns.

Figure 12. LLC resonant half-bridge converter electrical schematic



8 Electrical test results

8.1 Efficiency measurements

Table 2, *Table 3* and *Table 4* show the output voltage and current measurements at the various dc input voltage (nominal 390 Vdc, min 360 Vdc and max 420 Vdc) and several load conditions. For all measurements, both at full load and at light load operation, the input power has been measured by a digital power meter (Yokogawa WT-210). Particular attention has to be paid when measuring input power at full load in order to avoid measurement errors due to the voltage drop on cables and connections (connecting the WT-210 voltmeter termination to the board input connector). For the same reason, the measurements of the output voltages have been taken directly at the output connector, by using the remote sense option of the active load (Chroma 63108 and 63103) connected to the outputs.

Table 2. Efficiency measurements at V_{in} = 390 V_{dc}

+200 V	At load (A)	+75 (V)	At load (A)	P_{out} (W)	P_{in} (W)	Efficiency %
198.76	1.603	76.74	1.010	396.12	408.80	96.90%
198.75	1.300	76.80	0.811	320.66	330.81	96.93%
198.76	1.001	76.87	0.613	246.08	253.90	96.92%
198.79	0.751	76.95	0.414	181.15	187.54	96.59%
198.84	0.500	77.03	0.200	114.83	120.24	95.50%
198.87	0.151	77.06	0.107	38.27	42.70	89.64%

Table 3. Efficiency measurements at V_{in} = 360 V_{dc}

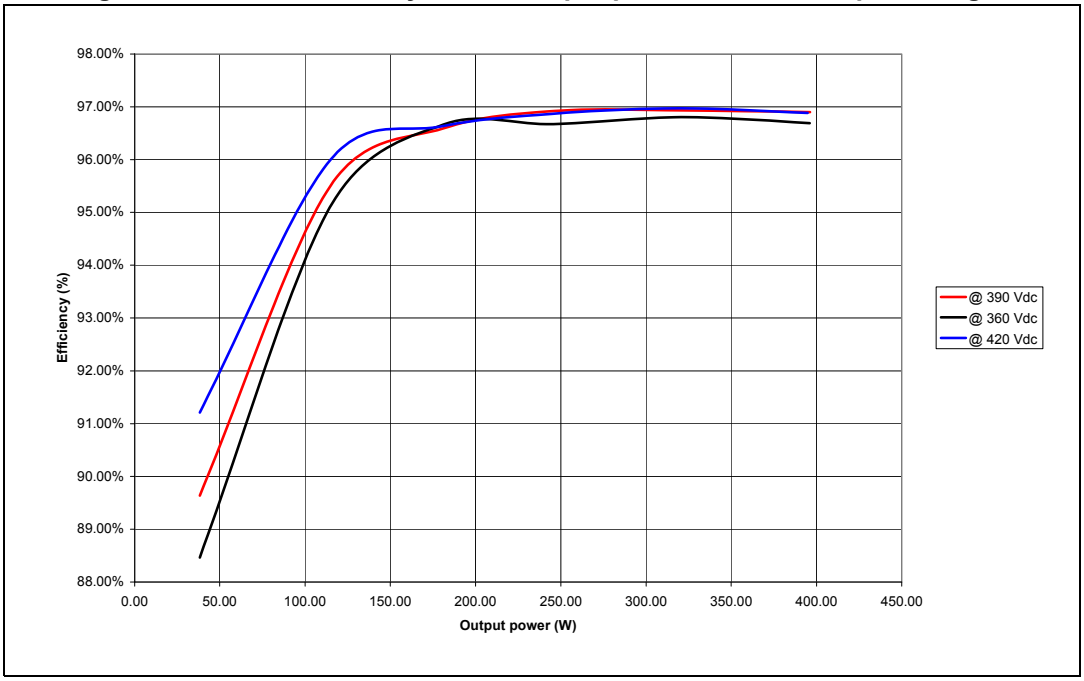
+200 V	At load (A)	+75 (V)	At load (A)	P_{out} (W)	P_{in} (W)	Efficiency %
198.68	1.603	76.68	1.010	395.93	409.47	96.69%
198.64	1.301	76.74	0.811	320.67	331.26	96.80%
198.62	1.000	76.81	0.613	245.70	254.17	96.67%
198.60	0.751	76.88	0.414	180.98	187.23	96.66%
198.57	0.500	76.94	0.198	114.52	120.43	95.09%
198.57	0.151	76.94	0.107	38.22	43.20	88.46%

Table 4. Efficiency measurements at V_{in} = 420V_{dc}

+200 V	At load (A)	+75 (V)	At load (A)	P_{out} (W)	P_{in} (W)	Efficiency %
198.35	1.601	76.57	1.008	394.74	407.45	96.88%
198.20	1.301	76.55	0.808	319.71	329.70	96.97%
197.87	1.001	76.47	0.609	244.64	252.55	96.87%
196.85	0.750	76.20	0.410	178.88	185.13	96.62%
198.01	0.504	76.74	0.198	114.99	119.78	96.00%
198.67	0.151	76.98	0.107	38.24	41.92	91.21%

The measurements have been done after 30 minutes of warm-up at maximum load. The circuit efficiency has been calculated at each load condition and input dc voltage and is plotted in *Figure 13*, showing very high values at maximum load level, higher than 96.5%. Also at light load, at an output power of about 10% of the maximum level, the converter efficiency is very good, reaching a value better than 88% in the whole DC input voltage range.

Figure 13. Circuit efficiency versus output power at various input voltages

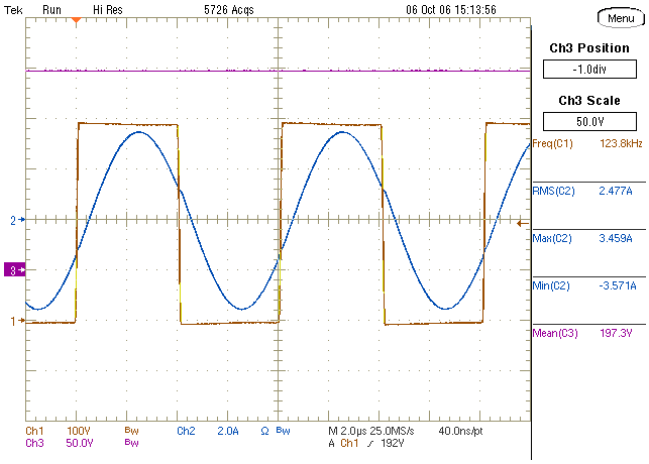


8.2 Resonant stage operating waveforms

Figure 14 shows some waveforms during steady state operation of the resonant circuit at nominal dc input voltage and full load. The Ch1 waveform is the half-bridge square voltage on pin 14 of the L6599, driving the resonant circuit. The trace Ch2 represents the transformer primary current flowing into the resonant tank. As shown, it is almost sinusoidal, because the operating frequency (about 123 kHz) is close to the resonance of the leakage inductance of the transformer and the resonant capacitor (C6). In this condition the circuit

has a good margin for ZVS operation, providing good efficiency, while the almost sinusoidal current waveform just allows for an extremely low EMI generation.

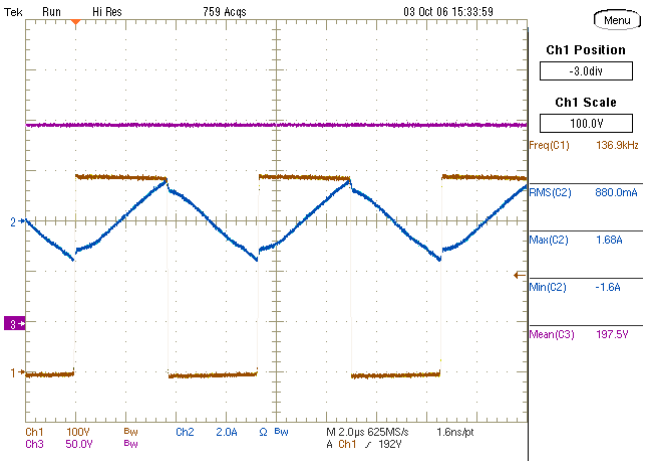
Figure 14. Resonant circuit primary side waveforms at nominal dc input voltage and full load



Ch1: half-bridge square voltage
Ch2: resonant tank current
Ch3: +200 V output voltage

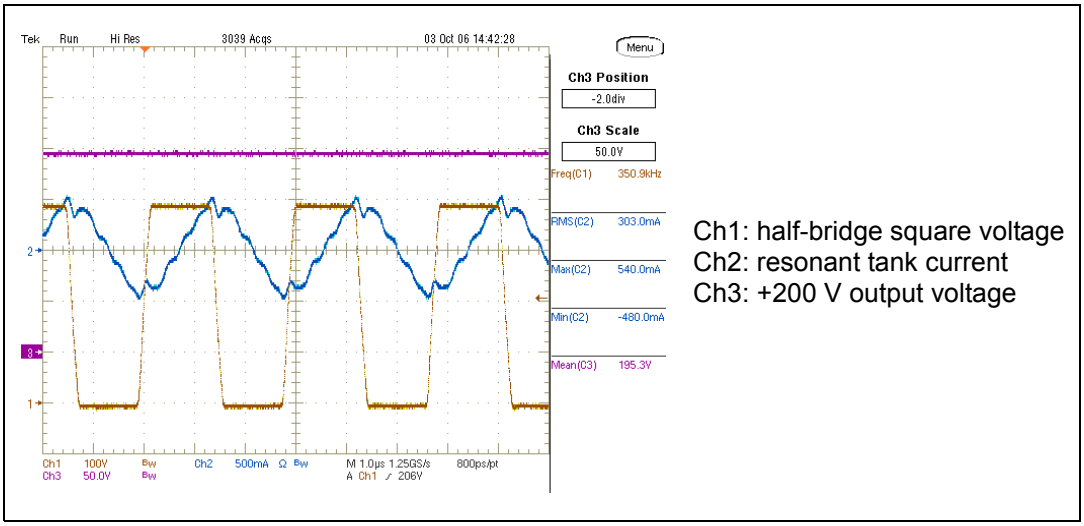
Figure 15 and *Figure 16* show the same waveforms as *Figure 14* with both outputs lightly loaded (50 mA each) and not loaded, respectively. These graphs demonstrate the ability of the converter to operate down to zero load, with the output voltages still within regulation limits (as can be seen looking at Ch3 waveform, representing the +200 V output voltage). The resonant tank current, in this load condition, assumes, obviously, an almost triangular shape and represents the magnetizing current flowing into the transformer primary side.

Figure 15. Resonant circuit primary side waveforms at nominal dc input voltage and light load



Ch1: half-bridge square voltage
Ch2: resonant tank current
Ch3: +200 V output voltage

Figure 16. Resonant circuit primary side waveforms at nominal dc input voltage and no-load



In *Figure 17*, the Ch1 waveform shows a detail of the half-bridge square voltage (directly taken across pin 14 and pin 10 of L6599 controller) to highlight the softness of voltage edge, without abrupt negative voltage spikes that would be generated in presence of large stray inductance of wiring. The layout is very critical in this respect and needs to be optimized in order to minimize this effect, which could damage the controller itself.

In *Figure 18* and *Figure 19*, waveforms relevant to the secondary side are represented. The rectifiers reverse voltage is measured by CH1 (for both +200 V and +75 V outputs) and the peak-to-peak value is indicated on the right of the graph. Waveform CH2 shows the current flowing into one of the two output diodes for each output voltage (respectively D6 and D8). Also this current shape is almost a sine wave, whose average value is one half the output current.

Figure 17. Resonant circuit primary side waveforms at nominal dc input voltage and light load

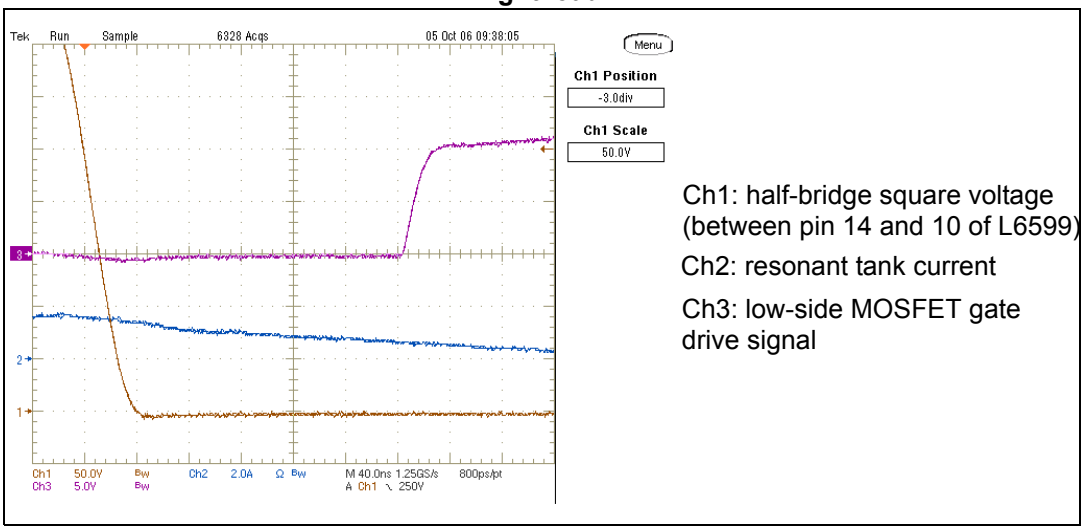
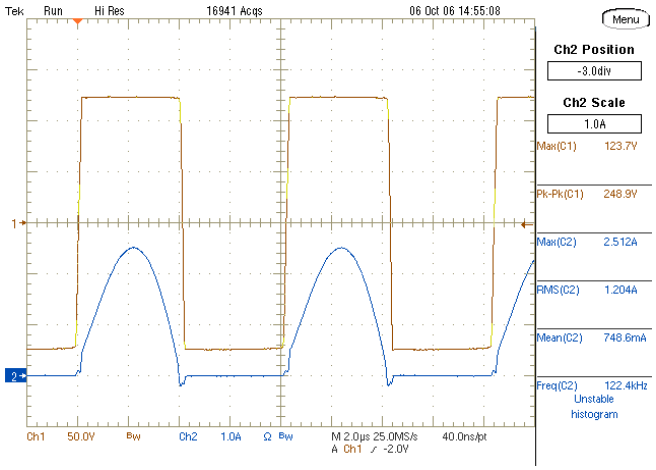
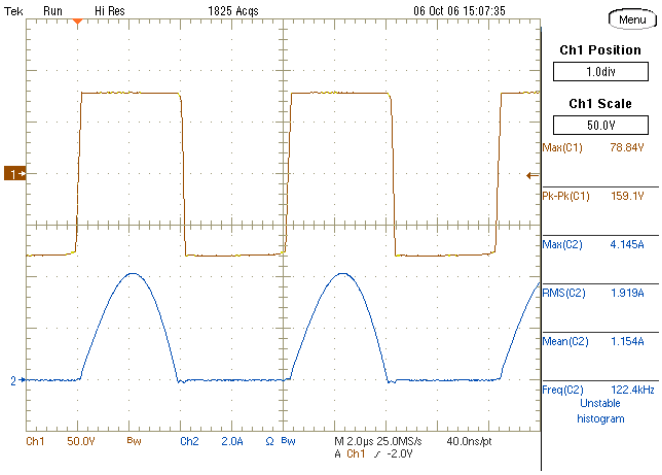


Figure 18. +200 V output diode voltage and current waveforms



+200 V output waveforms:
Ch1: +200 V diode reverse voltage
Ch2: diode D6 current

Figure 19. +75 V output diode voltage and current waveforms



+75 V output waveforms:
Ch1: resonant tank current
Ch2: diode D8 current

9 Reference

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2. A Comparison of Half Bridge Resonant Converter Topologies, IEEE Trans. on Power Electronics, 1988. Pages: 174 - 182.
3. First harmonic approximation including design constraints, Telecommunications Energy Conference, 1998. INTELEC. Pages: 321 - 328
4. Design Optimization for an LCL-Type Series Resonant Converter, see www.powerpulse.net.
5. L6599 High-voltage resonant controller datasheet, STMicroelectronics

10 Revision history

Table 5. Document revision history

Date	Revision	Changes
11-Jan-2007	1	First issue
06-Mar-2007	2	Minor text change
26-Mar-2007	3	*Equation 53* modified
24-Jul-2007	4	Quality factor (Q) modified
25-Oct-2007	5	Modified: *Equation 14* and *Equation 33*
17-Mar-2014	6	Updated *Equation 31 on page 13* (added "^{2}" to "$\|\|H_{LOSS}(j\omega)\|\|$"). Updated cross-references throughout document. Minor modifications throughout document.

Design Considerations for an LLC Resonant Converter

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Abstract: Recently, the LLC resonant converter has drawn a lot of attention due to its advantages over the conventional series resonant converter and parallel resonant converter: narrow frequency variation over wide load and input variation and Zero Voltage Switching (ZVS) of the switches for entire load range. This paper presents an analysis and reviews practical design considerations for the LLC-type resonant converter. It includes designing the transformer and selecting the components. The step-by-step design procedure explained with a design example will help engineers design the LLC resonant converter easily.

I. INTRODUCTION

The growing demand for higher power density and low profile in power converter designs has forced designers to increase switching frequencies. Operation at higher frequencies considerably reduces the size of passive components such as transformers and filters. However, switching losses have been an obstacle to high frequency operation. In order to reduce switching losses, allowing high frequency operation, resonant switching techniques have been developed [1-7]. These techniques process power in a sinusoidal manner and the switching devices are softly commutated. Therefore, the switching losses and noise can be dramatically reduced. Conventional resonant converters use an inductor in series with a capacitor as a resonant network. Two basic configurations are possible for the load connection; series connection and parallel connections.

For the series resonant converter (SRC), the rectifier-load network is placed in series with the L-C resonant network as depicted in Fig.1 [2-4]. From this configuration, the resonant network and the load act as a voltage divider. By changing the frequency of driving voltage V_d, the impedance of the resonant network changes. The input voltage will be split between this impedance and the reflected load. Since it is a voltage divider, the DC gain of an SRC is always lower than 1. At light load condition, the impedance of the load will be very large compared to the impedance of the resonant network; all the input voltage will be imposed on the load. This makes it difficult to regulate the output at light load. Theoretically, frequency should be infinite to regulate the output at no load.

For parallel resonant converter, the rectifier-load network is placed in parallel with the resonant capacitor as depicted in Fig. 2 [5-7]. Since the load is connected in parallel with the resonant network, there inevitably exists large amount of circulating current. This makes it difficult to apply parallel resonant topologies in high power applications.

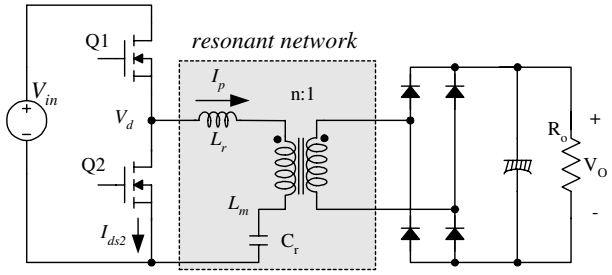

Fig.1. Half-bridge series resonant (SR) converter

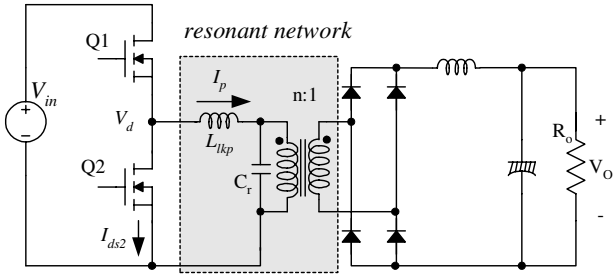

Fig.2. Half-bridge parallel resonant (PR) converter

In order to solve the limitations of the conventional resonant converters, the LLC resonant converter has been proposed [8-12]. The LLC-type resonant converter has many advantages over conventional resonant converters. First, it can regulate the output over wide line and load variations with a relatively small variation of switching frequency. Second, it can achieve zero voltage switching (ZVS) over the entire operating range. Finally, all essential parasitic elements, including junction capacitances of all semiconductor devices and the leakage inductance and magnetizing inductance of the transformer, are utilized to achieve ZVS.

This paper presents an analysis and design considerations for a half-bridge LLC resonant converter. Using the fundamental approximation, the voltage and current waveforms are analyzed and the gain equations are obtained. A design for DC/DC converter with 120W/24V output has been selected as a typical example for describing the design procedure.

II. OPERATION PRINCIPLES AND FUNDAMENTAL APPROXIMATION

Fig. 3 shows the simplified schematic of half-bridge LLC resonant converter and Fig. 4 shows its typical waveforms. In Fig. 3, L_m is the transformer magnetizing inductance and L_{lkp} and L_{lks} are the leakage inductances on the transformer primary and secondary sides respectively. Operation of the LLC resonant converter is similar to that of the conventional LC series resonant converter. The only difference is that the value of the magnetizing inductance is relatively small and therefore the resonance between L_m+L_{lkp} and C_r affects the converter operation. Since the magnetizing inductor is relatively small, there exists considerable amount of magnetizing current (I_m) as illustrated in Fig. 4.

In general, the LLC resonant topology consists of three stages as shown in Fig. 3; square wave generator, resonant network and rectifier network.

- The square wave generator produces a square wave voltage, V_d by driving switches, Q1 and Q2 with alternating 50% duty cycle for each switch. The square wave generator stage can be built as a full-bridge or half bridge type.
- The resonant network consists of a capacitor, leakage inductances and the magnetizing inductance of the transformer. The resonant network filters the higher harmonic currents. Thus, essentially only sinusoidal current is allowed to flow through the resonant network even though a square wave voltage is applied to the resonant network. The current (I_p) lags the voltage applied to the resonant network (that is, the fundamental component of the square wave voltage (V_d) applied to the half-bridge totem pole), which allows the MOSFET's to be turned on with zero voltage. As can be seen in Fig. 4, the MOSFET turns on while the current is flowing through the anti-parallel diode and the voltage across the MOSFET is zero.
- The rectifier network produces DC voltage by rectifying the AC current with rectifier diodes and capacitor. The rectifier network can be implemented as a full-wave bridge or center-tapped configuration with capacitive output filter.

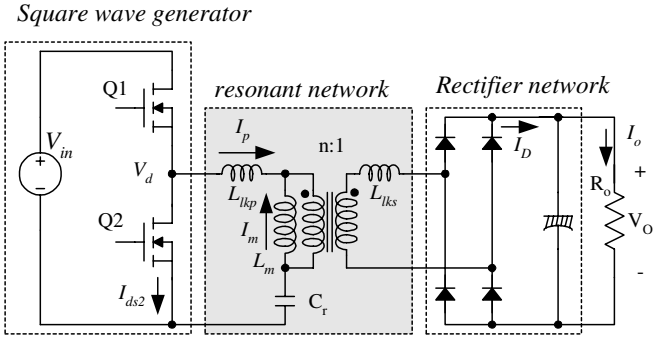

Fig. 3. A schematic of half-bridge LLC resonant converter

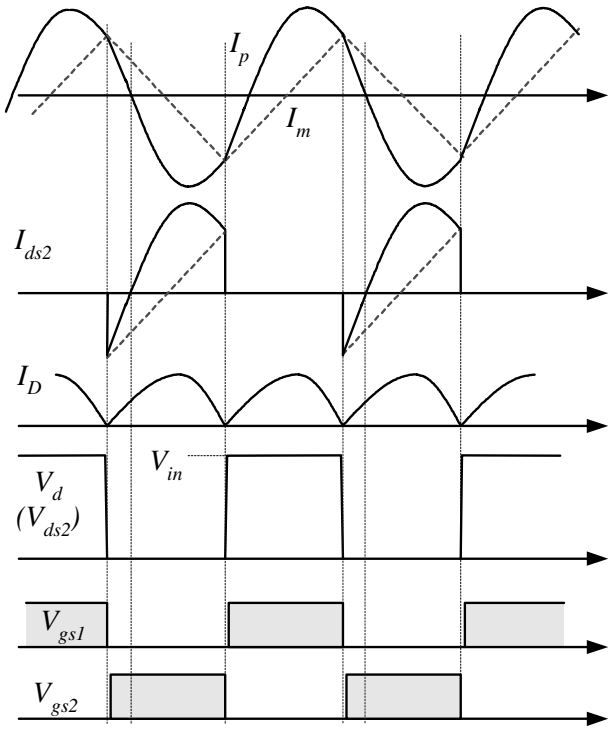

Fig. 4. Typical waveforms of half-bridge LLC resonant converter

The filtering action of the resonant network allows us to use the classical fundamental approximation to obtain the voltage gain of the resonant converter, which assumes that only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to the output. Because the rectifier circuit in the secondary side acts as an impedance transformer, the equivalent load resistance is different from actual load resistance. Fig. 5 shows how this equivalent load resistance is derived. The primary side circuit is replaced by a sinusoidal current source, I_{ac} and a square wave of voltage, V_{RI} appears at the input to the rectifier. Since the average of I_{ac} is the output current, I_o, I_{ac} is obtained as

$$I_{ac} = \frac{\pi \cdot I_o}{2}\sin(\omega t) \tag{1}$$

And V_{RI} is given as

$$\begin{aligned} V_{RI} &= +V_o \quad if\ \sin(\omega t) > 0 \\ V_{RI} &= -V_o \quad if\ \sin(\omega t) < 0 \end{aligned} \tag{2}$$

where V_o is the output voltage.

Then, the fundamental component of V_{RI} is given as

$$V_{RI}{}^F = \frac{4V_o}{\pi}\sin(\omega t) \tag{3}$$

Since harmonic components of V_{RI} are not involved in the power transfer, AC equivalent load resistance can be calculated by dividing $V_{RI}{}^F$ by I_{ac} as

$$R_{ac} = \frac{V_{RI}{}^F}{I_{ac}} = \frac{8}{\pi^2}\frac{V_o}{I_o} = \frac{8}{\pi^2}R_o \tag{4}$$

Considering the transformer turns ration ($n=N_p/N_s$), the equivalent load resistance shown in the primary side is obtained as

$$R_{ac} = \frac{8n^2}{\pi^2} R_o \tag{5}$$

By using the equivalent load resistance, the AC equivalent circuit is obtained as illustrated in Fig. 6, where V_d^F and V_{RO}^F are the fundamental components of the driving voltage, V_d and reflected output voltage, V_{RO} (nV_{RI}), respectively.

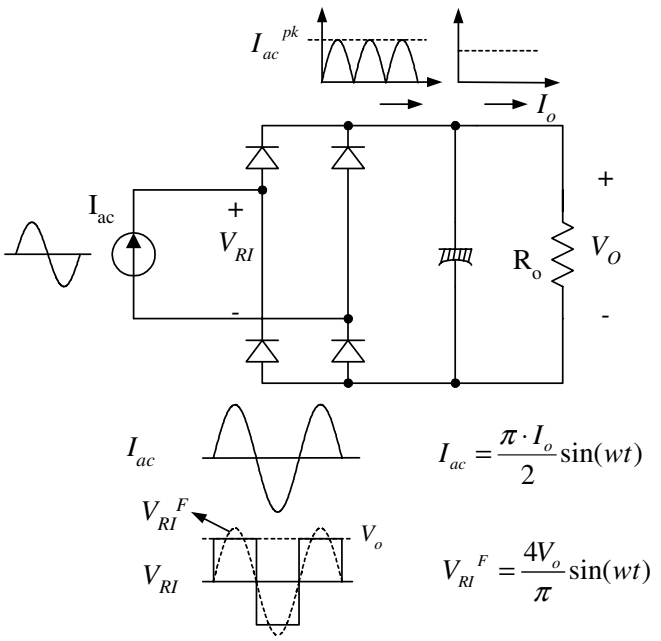

Fig. 5 Derivation of equivalent Load resistance R_{ac}

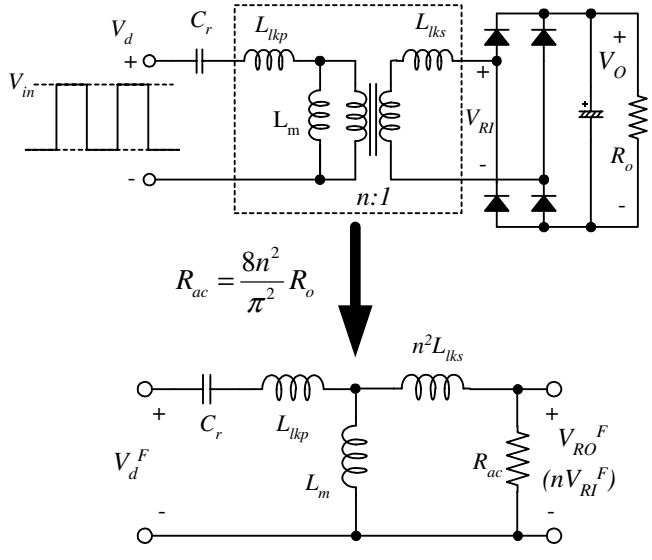

Fig. 6 AC equivalent circuit for LLC resonant converter

With the equivalent load resistance obtained in (5), the characteristics of the LLC resonant converter can be derived. Using the AC equivalent circuit of Fig. 6, the voltage gain, M is obtained as

$$M = \frac{V_{RO}^F}{V_d^F} = \frac{n \cdot V_{RI}^F}{V_d^F} = \frac{\frac{4n \cdot V_o}{\pi}\sin(\omega t)}{\frac{4}{\pi}\frac{V_{in}}{2}\sin(\omega t)} = \frac{2n \cdot V_o}{V_{in}} \tag{6}$$

$$= \left| \frac{\omega^2 L_m R_{ac} C_r}{j\omega \cdot (1-\frac{\omega^2}{\omega_o^2}) \cdot (L_m + n^2 L_{lks}) + R_{ac}(1-\frac{\omega^2}{\omega_p^2})} \right|$$

where

$$R_{ac} = \frac{8n^2}{\pi^2} R_o$$

$$\omega_o = \frac{1}{\sqrt{L_r C_r}} \ , \quad \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

$$L_p = L_m + L_{lkp} \ , \ L_r = L_{lkp} + L_m // (n^2 L_{lks})$$

As can be seen in (6), there are two resonant frequencies. One is determined by L_r and C_r while the other is determined by L_p and C_r. In actual transformer, L_p and L_r can be measured in the primary side with the secondary side winding open circuited and short circuited, respectively.

One important point that should be observed in (6) is that the gain is fixed at resonant frequency (ω_o) regardless of the load variation, which is given as

$$M_{@\omega=\omega_o} = \frac{L_m}{L_p - L_r} = \frac{L_m + n^2 L_{lks}}{L_m} \tag{7}$$

Without considering the leakage inductance in the transformer secondary side, the gain in (7) becomes unity. In previous research, the leakage inductance in the transformer secondary side was ignored to simplify the gain equation [8-12]. However, as observed, there exists considerable error when ignoring the leakage inductance in the transformer secondary side, which generally results in an incorrect design.

By assuming that $L_{lkp}=n^2L_{lks}$, the gain in (6) can be simplified as

$$M = \frac{2n \cdot V_O}{V_{in}} = \left| \frac{(\frac{\omega^2}{\omega_p^2})\frac{k}{k+1}}{j(\frac{\omega}{\omega_o}) \cdot (1-\frac{\omega^2}{\omega_o^2}) \cdot Q\frac{(k+1)^2}{2k+1} + (1-\frac{\omega^2}{\omega_p^2})} \right| \tag{8}$$

where

$$k = \frac{L_m}{L_{lkp}} \tag{9}$$

$$Q = \frac{\sqrt{L_r / C_r}}{R_{ac}} \tag{10}$$

The gain at the resonant frequency (ω_o) of (7) can be also simplified in terms of k as

$$M_{@\omega=\omega_o} = \frac{L_m + n^2 L_{lks}}{L_m} = \frac{L_m + L_{lkp}}{L_m} = \frac{k+1}{k} \tag{11}$$

While the gain is expressed in terms of k in (8), a gain expressed with L_p and L_r is preferred when handling an actual transformer since these values can be easily measured with a transformer. Expressing L_p and L_r in terms of k, we can obtain

$$L_p = L_m + L_{lkp} = (k+1)L_{lkp} \tag{12}$$

$$L_r = L_{lkp} + L_m // L_{lkp} = L_{lkp}(1 + \frac{k}{k+1}) \tag{13}$$

Using (12) and (13), (8) becomes

$$M = \frac{2n \cdot V_O}{V_{in}} = \left| \frac{(\frac{\omega^2}{\omega_p^{\,2}})\sqrt{\frac{L_p - L_r}{L_p}}}{j(\frac{\omega}{\omega_o}) \cdot (1 - \frac{\omega^2}{\omega_o^{\,2}}) \cdot Q\frac{L_p}{L_r} + (1 - \frac{\omega^2}{\omega_p^{\,2}})} \right| \tag{14}$$

(11) can be also expressed in terms of L_p and L_r as

$$M_{@\omega=\omega_o} = \frac{k+1}{k} = \sqrt{\frac{L_p}{L_p - L_r}} \tag{15}$$

By using the gain at the resonant frequency of (15) as a virtual gain of the transformer, the AC equivalent circuit of LLC resonant converter of Fig. 6 can be simplified in terms of L_p and L_r as shown in Fig. 7.

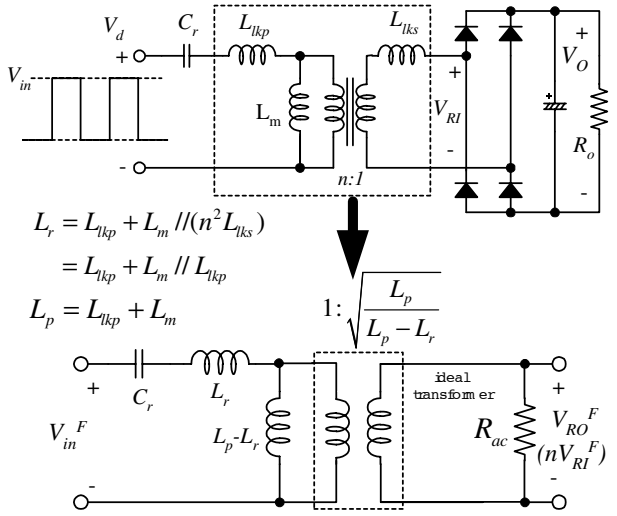

Fig. 7 Simplified AC equivalent circuit for LLC resonant converter

The gain of (8) is plotted in Fig. 8 for different Q values with k=5, f_o=100kHz and f_p=55kHz. As observed in Fig. 8, the LLC resonant converter shows characteristics which are almost independent of the load when the switching frequency is around the resonant frequency, f_o. This is a distinct advantage of LLC-type resonant converter over the conventional series-resonant converter. Therefore, it is natural to operate the converter around the resonant frequency to minimize the switching frequency variation at light load conditions.

The operating range of the LLC resonant converter is limited by the peak gain (attainable maximum gain), which is indicated with '*' in Fig. 8. It should be noticed that the peak voltage gain does not occur at f_o nor f_p. The peak gain frequency where the peak gain is obtained exists between f_p and f_o as shown in Fig. 8. As Q decreases (as load decreases), the peak gain frequency moves to f_p and higher peak gain is obtained. Meanwhile, as Q increases (as load increases), the peak gain frequency moves to f_o and the peak gain drops. Thus, the full load condition should be the worst case for the resonant network design.

Another important factor that determines the peak gain is the ratio between L_m and L_{lkp} which is defined as k in (9). Even though the peak gain at a given condition can be obtained by using the gain in (8), it is difficult to express the peak gain in explicit form. Moreover, the gain obtained from (8) has some error at frequencies below the resonant frequency (f_o) due to the fundamental approximation. In order to simplify the analysis and design, the peak gains are obtained using simulation tool and depicted in Fig. 9, which shows how the peak gain (attainable maximum gain) varies with Q for different k values. It appears that higher peak gain can be obtained by reducing k or Q values. With a given resonant frequency (f_o) and Q value, decreasing k means reducing the magnetizing inductance, which results in increased circulating current. Accordingly, there is a trade-off between the available gain range and conduction loss.

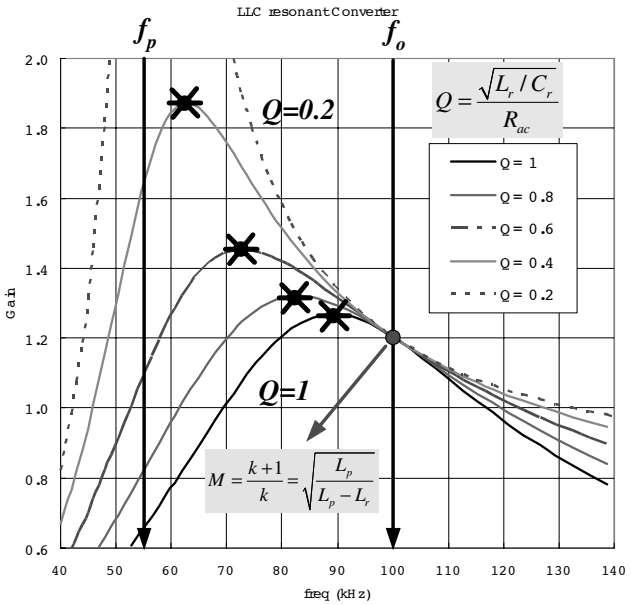

Fig. 8 Typical gain curves of LLC resonant converter (k=5 and f_o=100kHz)

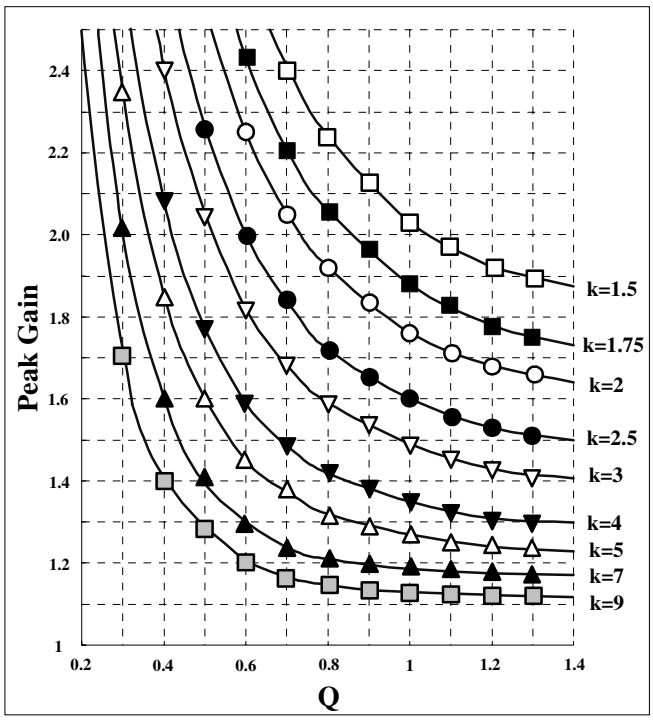

Fig. 9 peak gain (attainable maximum gain) versus Q for different k values

III. DESIGN PROCEDURE

In this section, a design procedure is presented using the schematic of Fig.10 as a reference. A dc/dc converter with 125W/24V output has been selected as a design example. The design specifications are as follows:

- Input voltage: 380Vdc (output of PFC stage)
- Output: 24V/5A (120W)
- Holdup time requirement: 17ms
- DC link capacitor of PFC output: 100uF

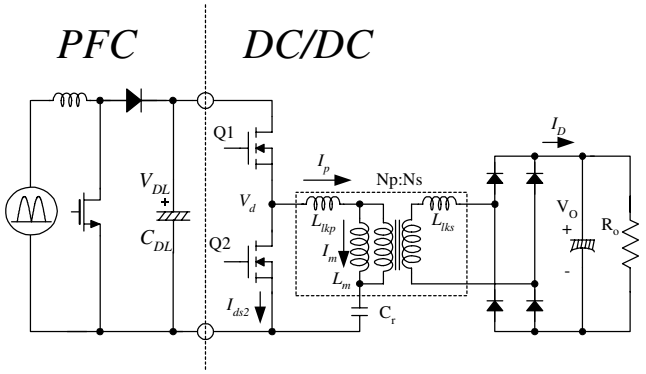

Fig.10 Schematic of half-bridge LLC resonant converter with power factor pre-regulator

[STEP-1] Define the system specifications

As a first step, the following specification should be defined.

-Estimated efficiency (E_{ff}): The power conversion efficiency must be estimated to calculate the maximum input power with a given maximum output power. If no reference data is available, use E_{ff} = 0.88~0.92 for low voltage output applications and E_{ff} = 0.92~0.96 for high voltage output applications. With the estimated efficiency, the maximum input power is given as

$$P_{in} = \frac{P_o}{E_{ff}} \tag{16}$$

-Input voltage range (V_{in}^{min} and V_{in}^{max}) : Typically, it is assumed that the input voltage is provided from Power Factor Correction (PFC) pre-regulator output. When the input voltage is supplied from PFC output, the minimum input voltage considering the hold-up time requirement is given as

$$V_{in}^{min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{DL}}} \tag{17}$$

where $V_{O.PFC}$ is the nominal PFC output voltage, T_{HU} is a hold up time and C_{DL} is the DC link bulk capacitor.
The maximum input voltage is given as

$$V_{in}^{max} = V_{O.PFC} \tag{18}$$

(Design Example) Assuming the efficiency is 95%,

$$P_{in} = \frac{P_o}{E_{ff}} = \frac{120}{0.95} = 126W$$

$$V_{in}^{min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{DL}}}$$

$$= \sqrt{380^2 - \frac{2 \cdot 126 \cdot 17 \times 10^{-3}}{100 \times 10^{-6}}} = 319V$$

$$V_{in}^{max} = V_{O.PFC} = 380V$$

[STEP-2] Determine the maximum and minimum voltage gains of the resonant network

As discussed in the previous section, it is typical to operate the LLC resonant converter around the resonant frequency (f_o) in normal operation to minimize switching frequency variation. When the input voltage is supplied from the PFC output, the input voltage has the maximum value (nominal PFC output voltage) in normal operation. Designing the converter to operate at f_o for the maximum input voltage condition, the minimum gain should occur at the resonant frequency (f_o). As observed in (11), the gain at f_o is a function of the ratio ($k=L_m/L_{lkp}$) between the magnetizing inductance and primary

side leakage inductance. Thus, the value of k should be chosen to obtain the minimum gain. While a higher peak gain can be obtained with a small k value, too small k value results in poor coupling of the transformer and deteriorates the efficiency. It is typical to set k to be 5~10, which results in a gain of 1.1~1.2 at the resonant frequency (f_o).

With the chosen k value, the minimum voltage gain for maximum input voltage (V_{in}^{max}) is obtained as

$$M^{\min} = \frac{V_{RO}}{\frac{V_{in}^{\max}}{2}} = \frac{L_m + n^2 L_{lks}}{L_m} = \frac{L_m + L_{lkp}}{L_m} = \frac{k+1}{k} \quad (19)$$

Then, the maximum voltage gain is given as

$$M^{\max} = \frac{V_{in}^{\max}}{V_{in}^{\min}} M^{\min} \quad (20)$$

(Design Example) The ratio (k) between L_m and L_{lkp} is chosen as 7, which results in the minimum and maximum gains as

$$M^{\min} = \frac{V_{RO}}{V_{in}^{\max}/2} = \frac{k+1}{k} = \frac{7+1}{7} = 1.14$$

$$M^{\max} = \frac{V_{in}^{\max}}{V_{in}^{\min}} M^{\min} = \frac{380}{319} \cdot 1.14 = 1.36$$

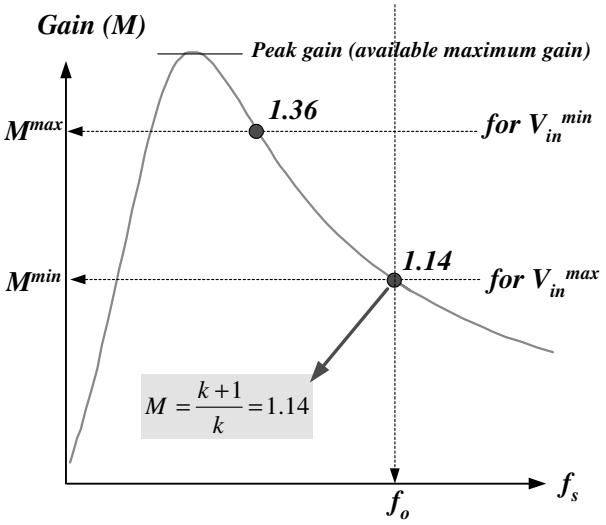

Fig. 11 Maximum gain and minimum gain

[STEP-3] Determine the transformer turns ratio ($n=N_p/N_s$)

Since the full-wave bridge rectifier is used for the rectifier network, the transformer turns ratio is given as

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{\max}}{2(V_o + 2V_F)} \cdot M^{\min} \quad (21)$$

where V_F is the secondary side rectifier diode voltage drop.

(Design Example)

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{\max}}{2(V_o + 2V_F)} \cdot M_{\min} = \frac{380}{2(24 + 2 \cdot 0.6)} \cdot 1.14 = 8.6$$

[STEP-4] Calculate the equivalent load resistance (R_{ac})

With the transformer turns ratio obtained from (21), the equivalent load resistance is obtained as

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{V_o^2}{P_o} E_{ff} \quad (22)$$

(Design Example)

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{V_o^2}{P_o} = \frac{8 \cdot 8.6^2 \cdot 24^2}{\pi^2 \cdot 120} = 288\Omega$$

[STEP-5] Design the resonant network

With k chosen in STEP-2, read proper Q value from the peak gain curves in Fig. 9 that results in enough peak gain. 10~15% margin on the peak gain is typical.
Then, the resonant parameters are obtained as

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} \quad (23)$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} \quad (24)$$

$$L_p = \frac{(k+1)^2}{(2k+1)} L_r \quad (25)$$

(Design Example)
As calculated in STEP-2, the maximum voltage gain (M^{max}) for the minimum input voltage (V_{in}^{min}) is 1.36. With 10% margin, a peak gain of 1.5 is required. k has been chosen as 7 in STEP-2 and Q is obtained as 0.43 from the peak gain curves in Fig. 12. By selecting the resonant frequency as 85kHz, the resonant components are determined as

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} = \frac{1}{2\pi \cdot 0.43 \cdot 85 \times 10^3 \cdot 288}$$
$$= 15nF$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} = \frac{1}{(2\pi \cdot 85 \times 10^3)^2 \cdot 15 \times 10^{-9}}$$
$$= 234uH$$

$$L_p = \frac{(k+1)^2}{(2k+1)} L_r = 998uH$$

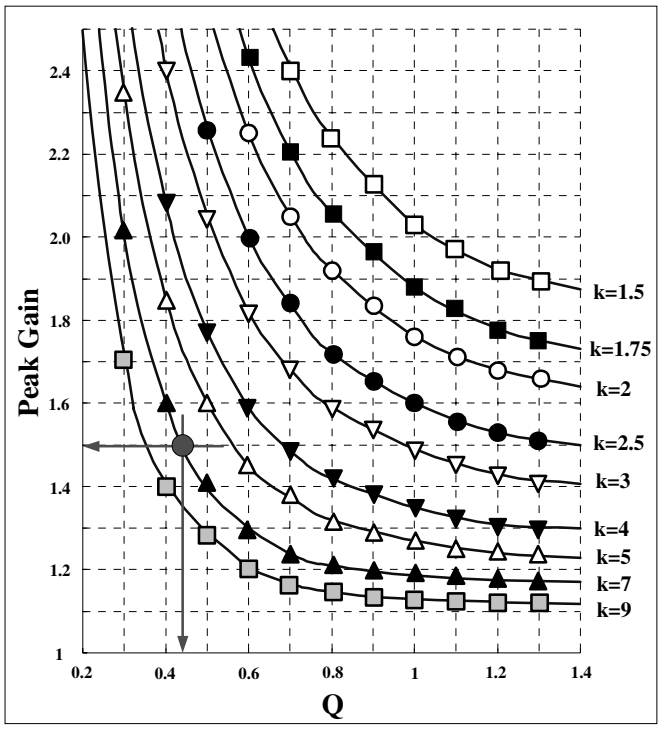

Fig. 12 Resonant network design using the peak gain (attainable maximum gain) curve for k=7

[STEP-6] Design the transformer

The worst case for the transformer design is the minimum switching frequency condition, which occurs at the minimum input voltage and full load condition. To obtain the minimum switching frequency, plot the gain curve using the gain equation of (8) and read the minimum switching frequency. Then, the minimum number of turns for the transformer primary side is obtained as

$$N_p^{\min} = \frac{n(V_o + 2V_F)}{2 f_s^{\min} \cdot \Delta B \cdot A_e} \tag{26}$$

where A_e is the cross-sectional area of the transformer core in m^2 and ΔB is the maximum flux density swing in Tesla. If there is no reference data, use ΔB =0.25~0.30 T.

Then, choose the proper number of turns for the secondary side that results in primary side turns larger than $N_p^{\min}$ as

$$N_p = n \cdot N_s > N_p^{\min} \tag{27}$$

(Design Example) EER3541 core (A_e=107mm^2) is selected for the transformer. From the gain curve of Fig .13, the minimum switching frequency is obtained as 66kHz. Then, the minimum primary side turns of the transformer is given as

$$N_p^{\min} = \frac{n(V_o + 2V_F)\times 10^6}{2 f_s^{\min} \Delta B \cdot A_e}$$

$$= \frac{8.6 \times 25.2}{2 \cdot 66 \times 10^3 \cdot 0.3 \cdot 107 \times 10^{-6}} = 51.1 \; turns$$

$$\therefore N_p = n \cdot N_s = 8.6 \times 6 = 51.6 > N_p^{\min}$$

Choosing N_s as 6 turns, N_p is given as

$$N_p = n \cdot N_s = 8.6 \times 6 = 51.6 \Rightarrow 52 > N_p^{\min}$$

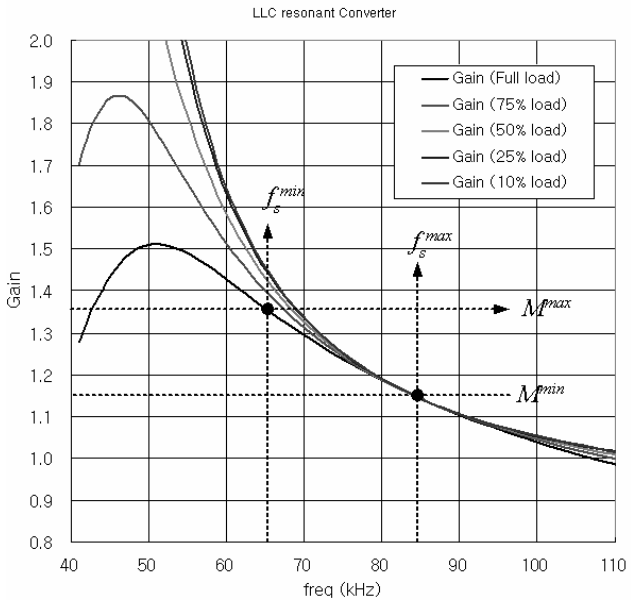

Fig. 13 Gain curve

[STEP-7] Transformer Construction

Parameters L_p and L_r of the transformer were determined in STEP-5. L_p and L_r can be measured in the primary side with the secondary side winding open circuited and short circuited, respectively. Since LLC converter design requires a relatively large L_r, a sectional bobbin is typically used as shown in Figure 14 to obtain the desired L_r value. For a sectional bobbin, the number of turns and winding configuration are the major factors determining the value of L_r, while the gap length of the core does not affect L_r much. Whereas, L_p can be easily controlled by adjusting the gap length. Table 1 shows measured L_p and L_r values with different gap lengths. With a gap length of 0.15mm, the desired L_p and L_r values are obtained.

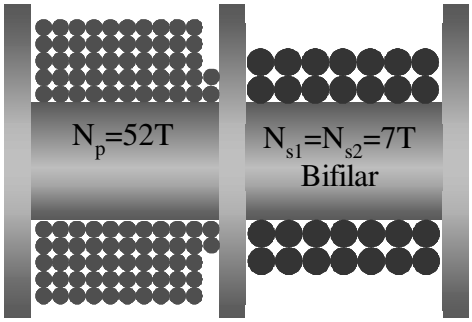

Fig. 14 Sectional bobbin

Table. 1 Measured Lp and Lr with different gap lengths

Gap length	L_p	L_r
0.0 mm	5,669 μH	237 μH
0.05 mm	2,105 μH	235 μH
0.10 mm	1,401 μH	233 μH
0.15 mm	**1,065 μH**	**230 μH**
0.20 mm	890 μH	225 μH
0.25 mm	788 μH	224 μH
0.30 mm	665 μH	223 μH
0.35 mm	623 μH	222 μH

Even though the integrated transformer approach in LLC resonant converter design can implement the magnetic components in a single core and save one magnetic component, the value of L_r is not easy to control in real transformer design. Thus, the resonant network design sometimes requires iteration with an actual L_r value after the transformer is actually built. Or, an additional resonant inductor can be added in series with the resonance capacitor to obtain the desired L_r value.

[STEP-8] Select the resonant capacitor

When choosing the resonant capacitor, the current rating should be considered since a considerable amount of current flows through the capacitor. The RMS current through the resonant capacitor is given as

$$I_{C_r}^{RMS} \cong \sqrt{[\frac{\pi I_o}{2\sqrt{2}n}]^2 + [\frac{n(V_o + 2\cdot V_F)}{4\sqrt{2} f_o L_m}]^2} \qquad (28)$$

Then, the maximum voltage of the resonant capacitor in normal operation is given as

$$V_{C_r}^{\max} \cong \frac{V_{in}^{\max}}{2} + \frac{\sqrt{2}\cdot I_{Cr}^{RMS}}{2\cdot\pi\cdot f_o \cdot C_r} \qquad (29)$$

(Design Example)

$$I_{C_r}^{RMS} \cong \sqrt{[\frac{\pi I_o}{2\sqrt{2}n}]^2 + [\frac{n(V_o + 2\cdot V_F)}{4\sqrt{2} f_o L_m}]^2}$$

$$= \sqrt{[\frac{\pi\cdot 5}{2\sqrt{2}\cdot 8.6}]^2 + [\frac{8.6\cdot(24+1.2)}{4\sqrt{2}\cdot 873\times10^{-6}\cdot 85\times10^{3}}]^2}$$

$$= 0.87A$$

$$V_{C_r}^{\max} \cong \frac{V_{in}^{\max}}{2} + \frac{\sqrt{2}\cdot I_{Cr}^{RMS}}{2\cdot\pi\cdot f_o\cdot C_r}$$

$$= \frac{380}{2} + \frac{\sqrt{2}\cdot 0.916}{2\cdot\pi\cdot 85\times10^{3}\cdot 15\times10^{-9}} = 343V$$

IV. CONCLUSION

This paper has presented the design of an LLC resonant converter utilizing the leakage inductance and magnetizing inductance of transformer as resonant components. The leakage inductance in the transformer secondary side was also considered in the gain equation.

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Design guideline for magnetic integration in LLC resonant converters

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***Abstract* -- The aim of this paper is to present a comprehensive design methodology for the magnetic integration of the series and shunt inductances of the resonant tank in an LLC resonant converter within the transformer.**

The design procedure applies to symmetrical core-bobbin structures with two separate slots for the primary and secondary windings. A specific leakage inductance A_σ (per square turn) that depends on geometrical parameters only is derived. This is used, together with the cross section and winding area of the core, to define two other core parameters that allow the designer to identify the minimum ferrite core size suitable for the application.

***Index Terms* – First harmonic approximation (FHA), LLC resonant converter, zero-voltage switching (ZVS), magnetic integration, transformer "all primary referred" (APR) model.**

I. Introduction

The interest in resonant topologies is continuously growing in the power conversion market, due to better efficiency and lower EMI pollution, with respect to traditional PWM solutions, inherent to these kinds of converters. This, in turn, allows for higher operating frequencies and consequently for a size reduction of the magnetic components and, generally, of the overall volume of the power supply.

One of the most popular resonant topologies nowadays is the multi-resonant LLC converter in its half-bridge implementation, which directly derives from the LC series resonant converter, by adding a shunt inductor in parallel to the load (see Fig. 1).

The LC series resonant converter suffers from a few drawbacks, which limit its use in several applications: in fact it only allows for buck operation (step-down) and cannot regulate the output voltage when unloaded; furthermore, at light load (when the resonant tank current is very low), the ZVS (zero voltage switching) behavior that minimizes power consumption is lost.

The LLC converter overcomes all of these problems, as shown in [1], where its behavior is analyzed, demonstrating that the resonant tank can be designed in order to always operate the half-bridge MOSFETs in ZVS condition, while regulating the output voltage down to zero-load. This operation is achieved essentially for free, as the additional shunt inductor can be implemented simply by introducing an air gap in the transformer core and, furthermore, the transformer leakage inductance can be used as the series resonant inductor.

The aim of this paper is to give guidelines for the magnetic integration of the series and shunt inductances of the resonant tank inside the transformer, in order to get a resonant circuit composed only of a capacitor and a resonant transformer.

The article starts illustrating the LLC resonant converter principle of operation, recalling the FHA (first harmonic approximation) approach used in [1] and the design procedures proposed in [1] and [2] to calculate the resonant tank. Then, we discuss various transformer models, including the APR (all-primary-referred) one, which better fits with the basic LLC resonant tank circuit. Afterwards, considering the case of a symmetrical two-slot coil-former, the specific leakage inductance of the core-bobbin structure is introduced, a parameter that only depends on the shape and size of the ferrite core.

Finally, we outline the proposed design process for the magnetic integration; and we define two core specific parameters, K_{GM} and K_{GW}, which allow the designer to choose the minimum ferrite core size that meets the electrical requirements and, at the same time, guarantee a maximum specified temperature rise of the transformer.

II. Circuit Description

A resonant converter basically applies a square voltage or current generated by a power switch network to a resonant circuit; the energy circulates in the resonant tank and part of it is delivered to the load. Fig. 1 shows a typical LLC resonant half-bridge converter: the half-bridge MOSFETs, driven on and off symmetrically with 50% duty cycle, generate a square waveform with peak-to-peak amplitude V_{dc}, and an average value of $V_{dc}/2$. This voltage is applied to the resonant tank, composed of the series capacitor C_r, the series inductor L_r and the shunt inductor L_m, so that energy can be transferred to the load, which is coupled to the resonant tank by the ideal transformer T. The capacitor C_r acts both as a resonant and a dc blocking capacitor: so, at the end, the alternate square voltage across the resonant tank has an amplitude of $\pm V_{dc}/2$. The transformer also provides insulation from the mains.

The design procedure of an LLC converter is not as straightforward as for a PWM converter; in [1] a design guideline is presented that is based on the FHA approach; this tremendously simplifies the circuit model, leading to

a linear circuit, which can be dealt with through the classical complex ac-circuit analysis. The FHA approach is based on the assumption, that the power transfer from the source to the load through the resonant tank is almost completely associated to the fundamental harmonic of the Fourier expansion of the currents and voltages involved, in accordance to the selective nature of a resonant circuit.

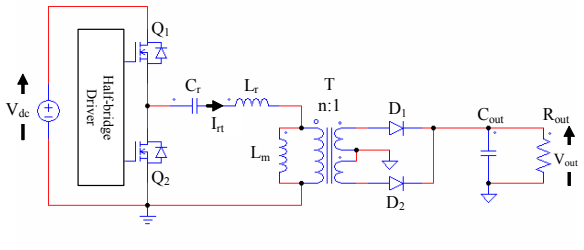

Figure 1. Half-bridge LLC resonant converter schematic

Fig. 2 shows the linear equivalent circuit, derived from the FHA assumption, where $V_{i.FHA}$ and $V_{o.FHA}$ are the first harmonic of the Fourier series expansion of the input and output square voltages of the resonant converter, respectively, while $R_{o.ac}$ is the ac equivalent resistance of the output load:

$$V_{i.FHA} = \frac{\sqrt{2}}{\pi} V_{dc} \qquad V_{o.FHA} = \frac{2\sqrt{2}}{\pi} V_{out} \qquad R_{o.ac} = \frac{8}{\pi^2}\frac{V_{out}^2}{P_o} = \frac{8}{\pi^2} R_{out}$$

The ten-step procedure proposed in [1], allows the designer to calculate the resonant-tank circuit parameters, C_r, L_r, L_m and n, which fulfill a set of input/output specifications, including the ZVS condition and the no-load operation, and assuming that the circuit operates at resonance frequency when the input voltage has the nominal value. The resonance frequency and the maximum operating frequency are input parameters, chosen by the designer.

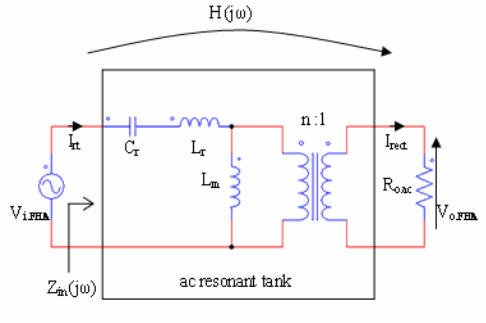

Figure 2. LLC resonant converter FHA equivalent model

The circuit in Fig. 2 is completely characterized by its input impedance $Z_{in}(j2\pi f_{sw})$ and forward transfer function $H(j2\pi f_{sw})$. These are used in [1] to identify all the relationships and conditions to solve for the unknowns of the circuit (C_r, L_r, L_m and n). Fig. 3 shows the resonant tank voltage gain M (M = n|H|) versus normalized frequency f_n, at different values of the circuit quality factor Q (which means, at different power levels). The red curve in this graph represents the no-load voltage gain. The load independent point, where all the curves touch, is the operating point at the resonance frequency ($f_n = 1$), where the required gain is unity: therefore, in the frame of the ten-step procedure, this is the operating point at nominal input voltage.

The regulation of the output voltage of the resonant converter is achieved by changing the switching frequency of the square waveform: as the working region is in the inductive part of the voltage gain characteristics of the resonant tank, the frequency control acts by increasing the frequency to lower the output power and by decreasing the frequency at decreasing input voltage (because the required voltage gain increases with decreasing input voltage).

Because the FHA model of an LLC resonant converter is not so accurate in the below-resonance region (where the current waveforms exhibit both the resonance frequency of C_r with L_r and the resonance frequency of C_r with the total inductance L_r+L_m), in [2] a further model is presented that is based on the inspection of the tank current in a particular operating mode. In this operating mode, the tank current, during the time interval when the output diodes are conducting, has a sinusoidal shape at resonance frequency (while the current in L_m is linear, because the voltage across it is clamped to the output voltage reflected at primary). In the time interval when diodes are not conducting, the tank current (and therefore the magnetizing current, too) is imposed to stay flat, equal to the value at the end of the previous time interval: in this way, the induction level B, which only depends on the current flowing in the magnetizing inductance, also does not increase, and the transformer can be designed as if it was operated at resonance frequency instead of the real operating frequency, below resonance. Also the nine-step procedure proposed in [2] allows the designer to calculate the values of the circuit parameters of Fig. 2, according to the same specification requirements as in [1].

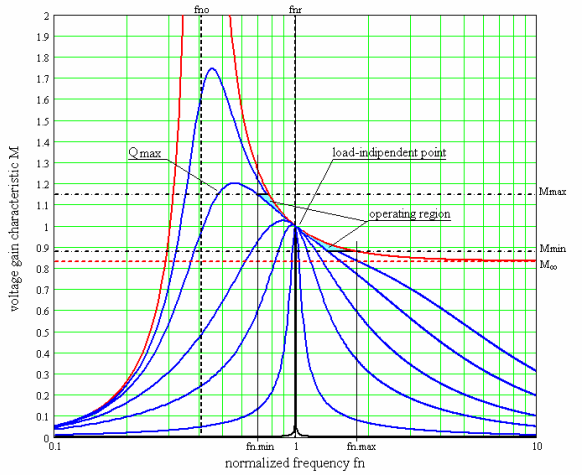

Figure 3. Voltage gain of an LLC resonant converter

Looking at Fig. 2, it is evident that the LLC resonant converter is well suited for the magnetic integration of the series and shunt inductances (L_r, L_m) as well as the transformer (T) into one magnetic component. In fact, the tank configuration recalls one of the most popular models

of a transformer: the APR one, where the series inductance L_r can be seen as the total leakage inductance, that is, the one measured on the primary side with the secondary windings short circuited.

III. Transformer Model

Fig. 4 shows a system of two coupled inductors (as a two winding transformer can be generally termed), with L_1 and L_2, respectively, primary and secondary self-inductance and M mutual inductance; we can derive an electrical-equivalent model of this magnetically coupled system, formed by the inductors L_a, L_b, L_μ and an ideal transformer with turn ratio N. By comparing the branch-constitutive equations of the two circuits:

$$\begin{vmatrix} V_1 \\ V_2 \end{vmatrix} = s \cdot \begin{vmatrix} L_1 & M \\ M & L_2 \end{vmatrix} \cdot \begin{vmatrix} I_1 \\ I_2 \end{vmatrix} \quad \Leftrightarrow \quad \begin{vmatrix} V_1 \\ V_2 \end{vmatrix} = s \cdot \begin{vmatrix} L_\mu + L_a & L_\mu / N \\ L_\mu / N & \dfrac{L_\mu}{N^2} + L_b \end{vmatrix} \cdot \begin{vmatrix} I_1 \\ I_2 \end{vmatrix}$$

we can find the relationships to pass from one model to the other:

$$\begin{cases} L_1 = L_\mu + L_a \\ M = \dfrac{L_\mu}{N} \\ L_2 = \dfrac{L_\mu}{N^2} + L_b \end{cases} \quad \Leftrightarrow \quad \begin{cases} L_a = L_1 - L_\mu = L_1 - N\,M \\ L_\mu = N\,M \\ L_b = L_2 - \dfrac{L_\mu}{N^2} = L_2 - \dfrac{M}{N} \end{cases}$$

The equivalent model presents one degree of freedom, as it has four unknowns (L_a, L_b, L_μ and N), while the coupled inductor has only three unknowns (L_1, L_2 and M); that means we can fix one of these arbitrarily and determine all the others: the logic choice is to fix N.

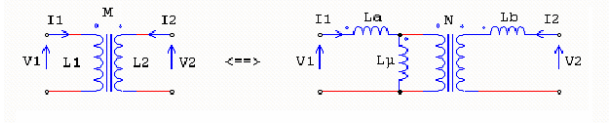

Figure 4. Coupled inductor equivalent model

In case N equals the real winding turns ratio $n_t = N_1/N_2$ (where N_1 and N_2 are the number of turns of the two windings), the model represents the real physical model of the coupled inductor (see Fig. 5), where L_M is the magnetizing inductance (associated to the flux that mutually links the two windings), while $L_{\sigma 1}$ and $L_{\sigma 2}$ are the primary and secondary leakage inductances (which are associated to the primary and secondary leakage fluxes). This physical model is exactly equal to that coming from the reluctance model approach. From a physical standpoint it must be verified that:

$$M \le \sqrt{L_1\,L_2}$$

where the equality sign means perfect coupling between the windings (which cannot be reached in reality, as leakage fluxes are always present, though they can be very small). A coupling coefficient k ($k < 1$) is therefore introduced, so that it is possible to write:

$$M = k\,\sqrt{L_1\,L_2}$$

and it can be demonstrated that k is the geometric mean of the primary and secondary coupling coefficients k_1 and k_2 (which represent the portions of flux generated by the primary and secondary windings, respectively, that link to the other winding):

$$k = \sqrt{k_1\,k_2}$$

In fact, by the definitions of the coupling coefficients, we have:

$$\frac{M}{L_1} = \frac{N_2}{N_1}\,k_1 \qquad \text{and} \qquad \frac{M}{L_2} = \frac{N_1}{N_2}\,k_2 \qquad (*)$$

By multiplying the two expressions above and solving for M, we get:

$$M = \sqrt{k_1\,k_2}\;\sqrt{L_1\,L_2} = k\,\sqrt{L_1\,L_2}$$

Therefore, for the physical model we find the following relationships:

$$n_t = \frac{N_1}{N_2} \qquad \begin{cases} L_M = k_1\,L_1 \\ L_{\sigma 1} = (1-k_1)\,L_1 \\ L_{\sigma 2} = (1-k_2)\,L_2 \end{cases} \qquad \text{where} \qquad \begin{cases} k_1 = \dfrac{M}{L_1}\,n_t \\ k_2 = \dfrac{M}{L_2}\,\dfrac{1}{n_t} \end{cases}$$

Another interesting transformer model comes out when N is chosen equal to the square root of primary to secondary inductance ratio (see Fig. 5) which leads to the following set of relationships:

$$n_e = \sqrt{\frac{L_1}{L_2}} \qquad \begin{cases} L_\mu = k\,L_1 \\ L_{S1} = (1-k)\,L_1 \\ L_{S2} = (1-k)\,L_2 = L_{S1}/n_e^2 \end{cases} \qquad k = \frac{M}{\sqrt{L_1\,L_2}}$$

where n_e is the effective turns ratio. In this case, L_μ, L_{S1} and L_{S2} do not have the physical meaning of magnetizing and leakage inductances, but they are only model parameters. Furthermore, it is worth noting that the secondary side series inductance reflected to the primary side equals the primary side series inductance:

$$L_{S1} = L_{S2.p} = n_e^2\,L_{S2}$$

Figure 5. Coupled inductor equivalent models for $N = n_t$ and $N = n_e$

The two models with $N = n_t$ and $N = n_e$ are perfectly identical in case that $k_1 = k_2$, which might happen when the system of coupled inductors is symmetrical, such as in a two-slot symmetrical bobbin, with each winding of equal number of turns wound in each slot. In fact, by dividing the two expressions above in (*) and root squaring, we get:

$$n_e = \sqrt{\frac{L_1}{L_2}} = \frac{N_1}{N_2}\,\sqrt{\frac{k_2}{k_1}} = n_t\,\sqrt{\frac{k_2}{k_1}}$$

Another very useful equivalent model of the coupled inductor is the APR one illustrated in Fig. 6, derived by imposing the secondary side series inductance L_b (in Fig. 4) is zero, which translates to:

$$N = \frac{M}{L_2} = \frac{M}{\sqrt{L_1 L_2}} \sqrt{\frac{L_1}{L_2}} = k\, n_e = n$$

The resulting relationships for this model (both in direct and inverse form) are:

$$\begin{cases} L_m = n\, M = k^2\, L_1 \\ L_r = L_1 - n\, M = (1-k^2)\, L_1 \end{cases} \qquad \begin{cases} L_1 = \dfrac{L_m}{k^2} \\ L_2 = \dfrac{L_m}{n^2} \end{cases} \qquad M = \frac{L_m}{n}$$

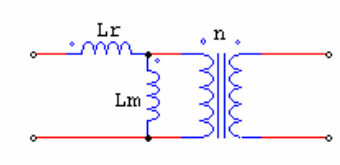

Figure 6. Transformer APR model

The transformer equivalent circuit (for N = n_e and for N = n = k n_e) can be completely identified through three measurements: the inductances L_1 and L_2 of the primary and secondary windings and the inductance L_{tot} of the series connection of the two windings (such that the current has the same flowing direction through both the dotted winding terminals), that is:

$$L_{tot} = L_1 + L_2 + 2\, M \qquad ==> \qquad M = \frac{L_{tot} - (L_1 + L_2)}{2}$$

Once L_1, L_2 and M are known, you can calculate the model parameters (n, L_m, L_r) and (n_e, k, L_{S1}, L_{S2}) through the above sets of equations. If the primary and secondary number of turns (or turns ratio) are also known, you can also completely define the physical model (for N = n_t) by calculating (k_1, k_2, L_M, $L_{\sigma 1}$, $L_{\sigma 2}$).

It is easy to recognize that the LLC resonant circuit is well suited for magnetic integration, i.e. to combine the inductors as well as the transformer in Fig. 2 into a single magnetic device; in fact, the magnetic part of the basic LLC resonant circuit is topologically identical to the APR model of a transformer.

The design flow based on the procedures proposed in [1] and [2] provides the parameters of the APR model L_r, L_m and n (together with the resonant capacitance C_r); hence, the further step is to determine the parameters of the physical model.

The problem is mathematically undetermined: there are four unknowns (n_t, L_μ, $L_{\sigma 1}$ and $L_{\sigma 2}$) in the physical model and only three parameters in the APR one. One simplifying assumption that overcomes this issue is the magnetic circuit symmetry: flux linkage is assumed to be exactly the same for both primary and secondary windings (that is $k_1 = k_2$). In this case, the physical model (N = n_t) and the model with N = n_e are the same, which provides the missing condition for solving the system ($L_{S1} = n_e^2\, L_{S2}$). The complete solution is the following:

$$\begin{cases} k = \sqrt{L_m / (L_r + L_m)} \\ n_e = n_t = n / k \end{cases} \qquad \begin{cases} L_1 = L_r + L_m \\ L_M = L_\mu = k\, L_1 \end{cases} \qquad \begin{cases} L_{S1} = (1-k)\, L_1 = L_{\sigma 1} \\ L_{S2} = L_{S1} / n_e^2 = L_{\sigma 2} \end{cases}$$

As previously mentioned, it is not difficult to find real-world structures where the condition of magnetic symmetry is quite close to reality: consider for example the ferrite E-core plus slotted bobbin assembly, using side-by-side winding arrangement, as shown in Fig. 7.

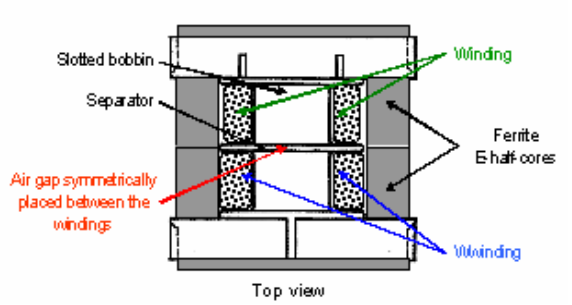

Figure 7. Transformer construction: E-cores and slotted bobbin

This type of transformer construction is well suited for this application, where the leakage inductance is used as the resonant-tank series inductance, and therefore needs to be well controlled and reliable for the circuit operation. Furthermore, the side-by-side winding technique allows for a wide range of values of leakage inductance, and hence coupling coefficient k, and is simpler and more effective than the layer winding arrangement.

Once the transformer model is completely defined, the next step is to find out the relationships to pass from the model parameters to the transformer construction parameters: N_1, N_2 and l_G, respectively, primary and secondary number of turns and thickness of the air gap. These parameters are the only ones that can be changed within a certain design to get the desired transformer, once the ferrite core and bobbin are chosen.

The inductance factor A_L (i.e. the inductance per square turn) can be alternatively used, instead of the air gap thickness l_G. Magnetic material suppliers usually specify A_L and l_G data in the form of a table in their ferrite core datasheets, or give the A_L values as a parameterised function of the air gap size.

IV. Specific Leakage Inductance

In this section we derive a semi-empirical formula based on the energy calculation approach. It allows the designer to estimate the leakage inductance of a two-winding transformer employing a two-section coil-former.

Fig. 8 shows a symmetrical two-slot bobbin with N1 turns primary winding (in red) and N2 turns secondary (in yellow). In the next discussion we will neglect the coil former thickness and dimensions, except the safety distance d_S between primary and secondary windings, and we will assume that the two windings are equally and evenly distributed inside their respective slots.

It is possible to derive the expression of the energy associated to the leakage flux, which is stored in the winding volume. If the secondary winding is short circuited, the current I_1 flowing into the primary winding causes a current $I_2 = I_1\, N_1/N_2$ flowing into the secondary, such that the flux inside the magnetic core is almost zero.

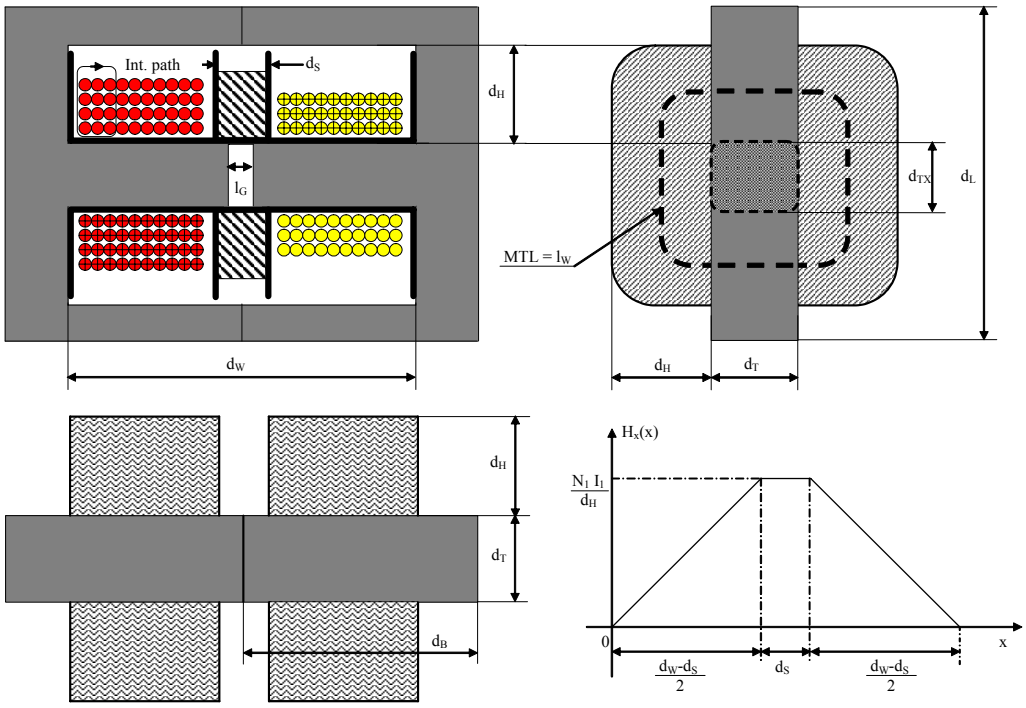

Figure 8. Two section slotted transformer and magnetic field distribution along winding section width direction

Due to the high permeability of ferrite materials, the field intensity, H, inside the magnetic core is negligible too; therefore, we can neglect the energy stored into the core and assert that the energy of the magnetic field, generated by the primary current I_1, is only dislocated within the winding volume. Referring to Fig. 6, we can also assert that this energy equals the one associated to the leakage inductances $L_{\sigma 1}$ and $L_{\sigma 2}$ of the transformer model, when the secondary is short circuited, that is (due to symmetry assumption) it is equal to twice the energy associated to $L_{\sigma 1}$:

$$E = \frac{1}{2} L_{\sigma 1} I_1^2 + \frac{1}{2} L_{\sigma 2} \left(\frac{N_1}{N_2} I_1 \right)^2 = L_{\sigma 1} I_1^2 = \frac{1}{2} \int_{Vol} B\, H\, dv = \frac{\mu_o}{2} \int_{Vol} H^2\, dv$$

The field intensity H (see Fig. 8), considered approximately uniform along the window height (d_H) direction, is derived through Ampere's law:

$$\oint H\, d\ell = N_1\, I_1 \;\Leftrightarrow\; H_x(x) = \frac{N_1\, I_1}{d_H} \frac{2\,x}{d_W - d_S} \qquad 0 \le x \le \frac{d_W - d_S}{2}$$

In fact, considering an integration path as indicated in Fig. 8, which encircles more and more current along the x direction, the H_x field increases linearly from zero to the maximum value ($N_1 I_1/d_H$) when all the turns are encircled, then it stays constant through the safety distance spacer and at last decreases linearly again down to zero, when all of the secondary turns are encircled.

The differential volume element dv is equal to the product of dx times the area A_x of the cross section of the winding area orthogonal to the x axis (see Fig. 8), which is a sort of ring surface, whose area is approximately the product of the mean turn length l_W times the window area height d_H; therefore the energy stored in the magnetic field is:

$$E = L_{\sigma 1}\, I_1^2 = \frac{\mu_o}{2} \int_0^{d_W} H_x^2(x)\, A_x\, dx = \frac{\mu_o}{2} \int_0^{d_W} H_x^2(x)\, l_W\, d_H\, dx =$$

$$= \frac{\mu_o}{2} (N_1 I_1)^2 \frac{l_W}{d_H} \left[2 \int_0^{\frac{d_W - d_S}{2}} \left(\frac{2\,x}{d_W - d_S} \right)^2 dx + \int_0^{d_S} dx \right] =$$

$$= \frac{\mu_o}{6} l_W \frac{d_W + 2\,d_S}{d_H} (N_1 I_1)^2$$

The average length of turn (l_W), in case of an E core type (square center leg), can be evaluated as follows:

$$l_W = \frac{A_{ext.T} - A_{CS}}{d_H} = \frac{2}{d_H} \left(d_H^2 + d_H (d_T + d_{TX}) \right) = d_H + d_T + d_{TX}$$

while in the case of an ETD core type (round center leg diameter D_{CL}) it can be approximated by the expression:

$$l_W = \frac{A_{ext.T} - A_{CS}}{d_H} = \frac{1}{d_H} \frac{\pi}{4} \left((d_H + D_{CL})^2 - D_{CL}^2 \right)$$

where A_{CS} is the area of the center leg cross section of the core, while $A_{ext.T}$ is the area of the most external winding turn. From the above calculated energy expression, we can obtain the series inductance L_r in the transformer APR model:

$$L_r = A_\sigma (1 + k)\, N_1^2 \qquad \text{where} \qquad A_\sigma = \frac{\mu_o}{6} l_W \frac{d_W + 2\,d_S}{d_H}$$

The term A_σ is the "specific leakage inductance per squared turn" associated with the core and winding construction: it depends only on the geometrical parameters of the chosen core and coil-former and, in

spite of all simplifying assumptions, its expression provides quite accurate results, within 10-15% of experimental measurements.

The above relationships have been found in the hypothesis in which the windings completely fill the available area, but they are still valid when the winding area is not completely used; they allow us to pass from the model parameters to the construction ones (once a magnetic core and bobbin have been chosen) according to the following expressions:

$$N_1 = \sqrt{\frac{L_r}{A_\sigma}\frac{1}{1+k}} \qquad N_2 = N_1\,\frac{k}{n} = \frac{N_1}{n_t} \qquad A_L = \frac{L_{tot}}{(N_1+N_2)^2} \tag{1}$$

where L_{tot} is the total inductance of the primary and secondary windings series connected (with the flowing current path entering the dotted terminals):

$$L_{tot} = L_1 + L_2 + 2\,M = L_1 + L_2 + 2\,k\,\sqrt{L_1\,L_2}$$

In literature there are several models and expressions for the A_L value of the core versus the air gap thickness l_G; the one proposed by McLyman [3] results in very good agreement with empirical data, and is suitable when the thickness of the air gap is larger than 0.1 mm. The expression below takes the fringing flux around the air gap into account, whose effect (increasing with l_G) is to increase the effective cross section of the magnetic path:

$$A_L = \mu_o\,\frac{A_{CS}}{l_G}\left[1 + \frac{l_G}{\sqrt{A_{CS}}}\ln\left(\frac{2\,d_W}{l_G}\right)\right]$$

where A_{CS} and d_W are the ferrite core cross section area and the winding area width, respectively: the above expression shows that A_L only depends on geometrical parameters (like the specific leakage inductance A_σ).

V. Derivation of the K_{GM} and K_{GW} Constants

In this section, a set of basic constraining equations is presented that, if combined together, allows selecting the minimum core size of the transformer that fulfills the electrical specifications and guarantees a maximum temperature rise. The first constraint is derived by Faraday's law applied on the transformer secondary side:

$$N_2\,\Delta\Phi = N_2\,\Delta B\,A_e = \int_0^{T_s/2} v_o(t)\,dt = \frac{V_{out}+V_F}{2\,f_{op}} = \frac{V_o}{2\,f_{op}}$$

where $\Delta\Phi$ is the flux generated by the magnetizing current that is linked to all primary and secondary turns; the corresponding peak value of the flux density $B_{pk}=\Delta B/2$ is responsible for the core losses. The worst condition occurs at the resonance frequency, when the resonant tank circuit design is made according to the procedure presented in [2], otherwise the minimum operating frequency has to be chosen, in which case the above equation overestimates the flux density: here we follow the $f_{op} = f_{res}$ option. Taking the primary to secondary turn ratio into account, the above relationship becomes:

$$N_1 = \frac{n\,V_o}{4\,k\,f_{res}\,B_{pk}\,A_e} \tag{2}$$

where A_e is the effective ferrite core cross section and V_o is the transformer output voltage, which includes the diode voltage drop V_F as well. Of course, the peak operating flux density B_{pk} must be lower than the saturation value B_{sat}.

The second constraint is represented by the modified Steinmetz equation that expresses the core losses as a function of the core volume V_e, the operating frequency f_{op} and the peak flux density B_{pk} (supposed sinusoidal):

$$P_{fe} = \left(\frac{8}{\pi}\right)^{\alpha-1} V_e\,K_m\,f_{op}^{\alpha}\,B_{pk}^{\beta} \tag{3}$$

The parameters K_m, α and β depend on the chosen material grade and can be derived from the data or loss charts provided by the ferrite manufacturers for the specific material. The numerical coefficient $(8/\pi^2)^{\alpha-1}$ is a form factor taking into account that the applied voltage (and hence induction) is a square waveform with 50% duty cycle.

A further constraint is that the temperature rise caused by the total losses should not exceed the maximum allowed by specification, that is:

$$\Delta T_{\max} \le R_{th}\,P_{diss} = R_{th}(P_{fe}+P_{cu}) \tag{4}$$

where P_{fe} and P_{cu} are respectively the core and copper losses; it is assumed that the temperature rise will be accordingly apportioned:

$$\begin{aligned}\Delta T_{cu} &= \frac{P_{cu}}{P_{diss}}\Delta T_{\max} = K_{cu}\,\Delta T_{\max}\\ \Delta T_{fe} &= \frac{P_{fe}}{P_{diss}}\Delta T_{\max} = (1-K_{cu})\,\Delta T_{\max}\end{aligned} \tag{5}$$

where ΔT_{cu} and ΔT_{fe} are the amount of temperature rise associated to the copper losses and to the ferrite core losses, respectively. The thermal resistance R_{th} of the magnetic structure is usually specified by the supplier: an empirical formula is also available, which estimates the thermal resistance as a function of the core area product AP (product of the cross section area A_e and the winding area A_w of the ferrite core):

$$R_{th} = 23\,AP^{-0.37}\ °C/W \qquad \text{(with AP in cm}^4\text{)}$$

Another constraint is constituted by a further empirical equation that relates the current density J (responsible for the temperature rise ΔT_{cu} inside the winding area) to the area product AP (expressed in cm^4):

$$J = J_{30}\sqrt{\frac{\Delta T_{cu}}{30°C}}\,AP^{-0.24} = J_{30}\sqrt{K_{cu}\frac{\Delta T_{\max}}{30°C}}\,AP^{-0.24} \tag{6}$$

where J_{30}=420 A/cm^2 is the current density that produces 30°C temperature rise in the windings; it is worth pointing out that AP in (6) is dimensionless: it just represents the number of cm^4 of core area product.

Considering that the primary ampere-turns equal the current density times the total primary conductor area, we can write:

$$N_1\,I_{p.rms} = K_{ut}\,A_w\,J \tag{7}$$

where $I_{p.rms}$ is the rms value of the resonant tank current

flowing in the transformer primary winding and K_{ut} is the window utilization factor (that is the ratio between the primary winding copper area to the winding area); this factor, in case Litz wire is used for windings (the real case in this application type, in order to reduce the copper losses due to skin and proximity effect), can be as low as 0.2.

The last constraint is the relationship, already found in the previous section, between the specific leakage inductance A_σ, the number of primary turns and the total leakage inductance, here rewritten for convenience:

$$L_r = A_\sigma (1+k)\, N_1^2 = \Lambda_\sigma\, \mu_o\, (1+k)\, N_1^2 \tag{8}$$

It is worth pointing out that the quantity $\Lambda_\sigma = A_\sigma/\mu_o$ is dimensionally a length and only depends on the core and coil-former geometry.

Combining the equations (2) to (5) with (8), it is possible to write the following expression:

$$\frac{A_e^2}{\Lambda_\sigma}\left(\frac{1}{V_e R_{th}}\right)^{\frac{2}{\beta}} = \frac{\mu_o L_r}{1-k}\left(\frac{n V_o}{4k f_{res}}\right)^2\left[\frac{K_m f_{res}^{\alpha}}{(1-K_{cu})\Delta T_{\max}}\left(\frac{8}{\pi^2}\right)^{\alpha-1}\right]^{\frac{2}{\beta}} \tag{9}$$

Combining the equations (5) to (8), a second expression can be found:

$$A_w^2\, \Lambda_\sigma A P^{-0.48} = \mu_o\left(\frac{I_{p.rms}}{K_{ut}\, J_{30}}\right)^2 \frac{1+k}{K_{cu}} \frac{30°C}{\Delta T_{\max}} \tag{10}$$

The terms on the left side of equations (8) and (9) depend on the core geometry (and β coefficient), while the terms on the right side depend on the circuit and application parameters and chosen material grade. Therefore the left side of above equations can be defined as the core geometrical constants K_{GM} and K_{GW}:

$$K_{GM} = \frac{A_e^2}{\Lambda_\sigma}\left(\frac{1}{V_e\, R_{th}}\right)^{\frac{2}{\beta}} \qquad K_{GW} = A_w^2\, \Lambda_\sigma A P^{-0.48} \tag{11}$$

Hence, to design a transformer which integrates the series and shunt inductances for the LLC resonant converter application, first the suitable material grade has to be chosen, depending on the operating frequency range of the application; then the second terms of equations (9) and (10) have to be calculated and finally, a core has to be selected, whose geometrical constants exceed these values:

$$K_{GM} \geq \mu_o\left(\frac{n V_o}{4\, k\, f_{res}}\right)^2 \frac{L_r}{1-k}\left[\frac{K_m f_{res}^{\alpha}}{(1-K_{cu})\Delta T_{\max}}\left(\frac{8}{\pi^2}\right)^{\alpha-1}\right]^{\frac{2}{\beta}} \tag{12}$$

$$K_{GW} \geq \mu_o\left(\frac{I_{p.rms}}{K_{ut}\, J_{30}}\right)^2 \frac{1+k}{K_{cu}} \frac{30°C}{\Delta T_{\max}}$$

The first core parameter, K_{GM}, is related to the capability of the chosen ferrite core to handle the losses into the magnetic material, while assuring the required leakage: therefore, in case the inequality related to this parameter is not verified with a chosen material grade, the designer can try to use a better one, if available, with lower specific losses, and check again if the first inequality in (12) is satisfied. The second core parameter, K_{GW}, is related to the core capability to dissipate the Joule losses generated inside the copper windings. In this procedure, the parameter K_{cu} (apportionment of copper to total losses) is arbitrarily chosen: it can be initially set to 50% and then, in case only one of the two inequalities above is verified, it can be changed in the attempt to get both of them verified for the chosen core. For example, in case the second inequality is not verified, it is possible to gradually increase K_{cu} and check if in the end both the relationships are true, that is, the ferrite core is suitable to manage the total amount of power dissipation without exceeding the maximum allowed temperature rise.

VI. Design Procedure

Based on the analysis presented so far, the following procedure is proposed to design the integrated transformer in Fig. 2. The input data are the values of parameters n, L_r, L_m, previously calculated according to [2] in order to fulfill the converter specifications. Further input data are the maximum allowed temperature rise ΔT_{max}, the output voltage V_o (including the output diode forward drop), the rms value of current flowing into the primary and secondary windings ($I_{p.rms}$ and $I_{s.rms}$), the resonance frequency f_r and the operating frequency range (f_{min} - f_{max}).

1- first, select a material grade suitable for the operating frequency range of the application, identifying the parameters K_m, α and β.

2- then, calculate the terms on the right side of expressions (12), considering that the coupling coefficient k is found through: $k = \sqrt{L_m/(L_r + L_m)}$

3- select a core-bobbin shape and size such that the core geometrical constants K_{GM} and K_{GW}, defined in (11), satisfy the inequalities in (12). The designer can initially set the copper to total losses apportionment K_{cu} = 50% and then play with it (+/- 15%) if needed, in order to get the inequalities verified. In case the inequalities are both satisfied, the designer can try to reduce the core size by using a better material grade, with lower losses in the application frequency range.

4- calculate the number of primary turns N_1, to get the required leakage inductance, by using the first equation of (1): this number is only the first attempt and may need to be fine tuned once the first sample is built and measured. Also, define the number of secondary turns N_2 and the A_L value through the other two equations of (1).

5- define the wire section for primary and secondary windings. High frequency copper losses must be particularly addressed, because eddy currents and proximity losses are considerable and, consequently, suggest the use of Litz wires or multi-strand wires for both primary and secondary windings. If the strand diameter and the number of strands are optimized (see [4]) to minimize the total copper losses (ohmic and eddy), usually this leads to select a wire cross section such that the losses due to eddy currents are one half of the ohmic

losses: this means that the ohmic losses $P_{cu.ohm}$ are 2/3 of the maximum allowed copper losses P_{cu}. From this consideration the designer can find out the required wire section of the primary and secondary windings: the last step is then to select the strand configuration (strand diameter and number of parallel strands with the calculated total cross section) that presents the lowest ac resistance.

Throughout the various sections presented so far, the transformer has been considered composed of one primary winding and one secondary winding (single ended), that is the case where the full-bridge rectification is used at converter output. In case of secondary center-tap windings and full-wave rectification (as in Fig. 1), the rms value of the current flowing into each secondary winding is $1/\sqrt{2}$ times the current flowing through the single-ended winding of the previous output configuration: therefore the wire section of each center-tap can be half the copper section, necessary for the single-ended secondary winding (while the number of secondary turns N_2 is obviously the same in both cases).

There is another important aspect to consider in case of a transformer with secondary center-tap: the two windings need to be tightly coupled to each other, so that the leakage inductance, measured on the primary side with either secondary winding short circuited, is almost the same. In fact, during each half cycle of operation, the resonant capacitor in Fig. 2 rings with the leakage inductance between the primary winding and the corresponding center-tap winding that is conducting current on the secondary side. Therefore, in case these two leakage inductances are substantially different, the tank current will be not symmetrical and the circuit will exhibit two different resonance frequencies during each half cycle, that can make it very difficult (or even impossible) to compensate the feedback loop of the converter. In order to get good coupling between the center-tap windings, a good practice is to wound them in parallel (in bifilar).

An integrated transformer with secondary center-tap for the LLC resonant converter specified in Table I has been designed, following the proposed procedure and a prototype has been built and tested on the bench. The resonant tank parameters, calculated through the procedure in [2], are summarized in Table II and used as input data for the transformer design. The chosen ferrite core is ETD49, grade 3F3 Ferroxcube (with α=1.6, β=2.5 K_m=0.25 W/m^3), for which the core parameters are: K_{GM}=829.3 cm^3(W/°C m^3)$^{2/\beta}$, K_{GW}=29.6 cm^5 (assuming R_{th}=8°C/W and Λ_σ=5.05 cm). The second terms of (9) and (10), calculated for K_{cu}=0.5 and ΔT_{max}=40°C, make the inequalities (12) verified according to:
$K_{GM} \geq$ 737.4 cm^3(W/°C m^3)$^{2/\beta}$ and $K_{GW} \geq$ 10.6 cm^5.
The prototype has been built with N_1=23 primary turns (calculated 21.4) of litz wire 30x0.2 mm, N_2=4 secondary turns of Litz wire 75x0.2 mm, for each cente-tap winding, and a gap of about 0.45mm. The coil-former has a spacer between the two slots, whose thickness is d_s=3 mm.

TABLE I
DESIGN SPECIFICATION OF THE EXEMPLARY LLC CONVERTER

Parameter	Symbol	Value	Unit
Input voltage range	Vin_{min} - Vin_{max}	320 - 430	V
Nominal input voltage	Vin_{nom}	390	V
Regulated output voltage	*Vout*	36	V
Maximum (peak) output current	*Iout*	8.35	A
Expected efficiency (@ Vin_{min})	η	95	%
Parasitic capacitance of node HB	C_{HB}	200	pF
Dead time of driver circuit	*Td*	200	ns

TABLE II
RESONANT TANK ELECTRICAL AND OPERATING PARAMETERS

Parameter	Symbol	Value	Unit
Resonance frequency	f_r	120	kHz
Turn ratio of transformer in Fig. 2	*n*	5.335	-
Shunt inductance (see Fig. 2)	L_m	305	µH
Series inductance (see Fig. 2)	L_r	56	µH
Coupling coefficient	*k*	0.92	-
Tank primary current (rms value)	$I_{p.rms}$	2.1	A
Total rectified output current (rms value)	$I_{s.rms}$	9.3	A

CONCLUSIONS

In this article a design procedure has been outlined to completely define the parameters of a transformer (N_1, N_2, l_G) that integrates all the magnetic parts of an LLC resonant converter (Fig. 2) into a single component. This procedure allows the designer to choose the minimum ferrite core size to satisfy the electrical specifications and guarantee a maximum temperature rise of the transformer, once a suitable ferrite material grade has been selected for the operating frequency range. For this purpose, the two constants K_{GM} and K_{GW} have been defined, related to the core and bobbin geometry, that estimate the capability of the core-bobbin assembly to handle the total losses, while assuring the required leakage inductance, necessary for the correct operation of the resonant tank. These two constants also depend on a further parameter of the core-bobbin set: the specific leakage inductance A_σ (or equivalently Λ_σ), that has been estimated (in section IV) using the energy calculation approach, that is, by evaluating the energy associated to the leakage flux in the winding volume.

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LED Application Design Guide Using Half-Bridge LLC Resonant Converter for 160W Street Lighting

Introduction

This application note describes the LED driving system using a half-bridge LLC resonant converter for high power LED lighting applications, such as outdoor or street lighting. Due to the existence of the non-isolation DC-DC converter to control the LED current and the light intensity, the conventional PWM DC-DC converter has the problem of low-power conversion efficiency. The half-bridge LLC converter can perform the LED current control and the efficiency can be significantly improved. Moreover, the cost and the volume of the whole LED driving system can be reduced.

Consideration of LED Drive

LED lighting is rapidly replacing conventional lighting sources like incandescent bulbs, fluorescent tubes, and halogens because LED lighting reduces energy consumption. LED lighting has greater longevity, contains no toxic materials, and emits no harmful UV rays, which are 5 ~ 20 times longer than fluorescent tubes and incandescent bulbs. All metal halide and fluorescent lamps, including CFLs, n contain mercury.

The amount of current through an LED determines the light it emits. The LED characteristics determine the forward voltage necessary to achieve the required level of current. Due to the variation in LED voltage versus current characteristics, controlling only the voltage across the LED leads to variability in light output. Therefore, most LED drivers use current regulation to support brightness control. Brightness can be controlled directly by changing the LED current.

Consideration of LLC Resonant Converter

The attempt to obtain ever-increasing power density of switched-mode power supplies has been limited by the size of passive components. Operation at higher frequencies considerably reduces the size of passive components, such as transformers and filters; however, switching losses have been an obstacle to high-frequency operation. To reduce switching losses and allow high-frequency operation, resonant switching techniques have been developed. These techniques process power in a sinusoidal manner and the switching devices are softly commutated. Therefore, the switching losses and noise can be dramatically reduced[1-7].

Among various kinds of resonant converters, the simplest and most popular is the LC series resonant converter, where the rectifier-load network is placed in series with the L-C resonant network, as depicted in Figure 1[2-4]. In this configuration, the resonant network and the load act as a voltage divider. By changing the frequency of driving voltage V_d, the impedance of the resonant network changes. The input voltage is split between this impedance and the reflected load. Since it is a voltage divider, the DC gain of a LC series resonant converter is always <1. At light-load condition, the impedance of the load is large compared to the impedance of the resonant network; all the input voltage is imposed on the load. This makes it difficult to regulate the output at light load. Theoretically, frequency should be infinite to regulate the output at no load.

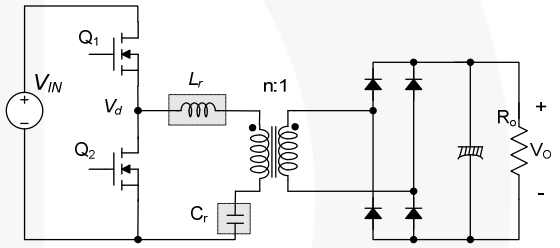

Figure 1. Half-Bridge, LC Series Resonant Converter

To overcome the limitation of series resonant converters, the LLC resonant converter has been proposed[8-12]. The LLC resonant converter is a modified LC series resonant converter implemented by placing a shunt inductor across the transformer primary winding, as depicted in Figure 2. When this topology was first presented, it did not receive much attention due to the counterintuitive concept that increasing the circulating current in the primary side with a shunt inductor can be beneficial to circuit operation. However, it can be very effective in improving efficiency for high-input voltage applications where the switching loss is more dominant than the conduction loss.

In most practical designs, this shunt inductor is realized using the magnetizing inductance of the transformer. The circuit diagram of LLC resonant converter looks much the same as the LC series resonant converter: the only difference is the value of the magnetizing inductor. While the series resonant converter has a magnetizing inductance larger than the LC series resonant inductor (L_r), the magnetizing inductance in an LLC resonant converter is just 3~8 times L_r, which is usually implemented by introducing an air gap in the transformer.

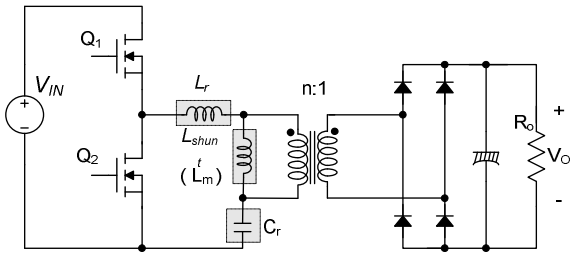

Figure 2. Half-Bridge LLC Resonant Converter

An LLC resonant converter has many advantages over a series resonant converter. It can regulate the output over wide line and load variations with a relatively small variation of switching frequency. It can achieve zero voltage switching (ZVS) over the entire operating range. All essential parasitic elements, including junction capacitances of all semiconductor devices and the leakage inductance and magnetizing inductance of the transformer, are utilized to achieve soft switching.

This application note presents design considerations of an LLC resonant half-bridge converter employing Fairchild's FLS-XS series. It includes explanation of the LLC resonant converter operation principles, designing the transformer and resonant network, and selecting the components. The step-by-step design procedure, explained with a design example, helps design the LLC resonant converter.

LLC Resonant Converter and Fundamental Approximation

Figure 3 shows a simplified schematic of a half-bridge LLC resonant converter, where L_m is the magnetizing inductance that acts as a shunt inductor, L_r is the series resonant inductor, and C_r is the resonant capacitor. Figure 4 illustrates the typical waveforms of the LLC resonant converter. It is assumed that the operation frequency is same as the resonance frequency, determined by the resonance between L_r and C_r. Since the magnetizing inductor is relatively small, a considerable amount of magnetizing current (I_m) exists, which freewheels in the primary side without being involved in the power transfer. The primary-side current (I_p) is sum of the magnetizing current and the secondary-side current referred to the primary.

In general, the LLC resonant topology consists of three stages shown in Figure 3; square-wave generator, resonant network, and rectifier network.

- The square-wave generator produces a square-wave voltage, V_d, by driving switches Q_1 and Q_2 alternately with 50% duty cycle for each switch. A small dead time is usually introduced between the consecutive transitions. The square-wave generator stage can be built as a full-bridge or half-bridge type.
- The resonant network consists of a capacitor, leakage inductances, and the magnetizing inductance of the transformer. The resonant network filters the higher harmonic currents. Essentially, only sinusoidal current is allowed to flow through the resonant network even though a square-wave voltage is applied to the resonant network. The current (I_p) lags the voltage applied to the resonant network (that is, the fundamental component of the square-wave voltage (V_d) applied to the half-bridge totem pole), which allows the MOSFETs to be turned on with zero voltage. As shown in Figure 4, the MOSFET turns on while the voltage across the MOSFET is zero by flowing current through the anti-parallel diode.
- The rectifier network produces DC voltage by rectifying the AC current with rectifier diodes and a capacitor. The rectifier network can be implemented as a full-wave bridge or center-tapped configuration with capacitive output filter.

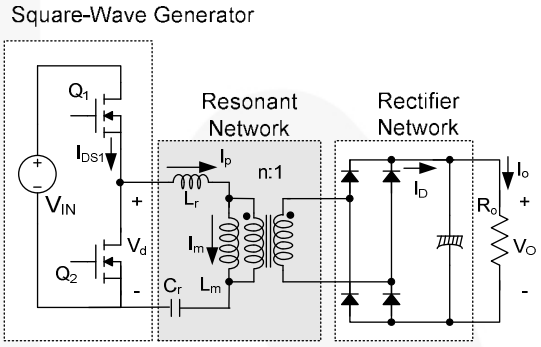

Figure 3. Schematic of Half-Bridge LLC Resonant Converter

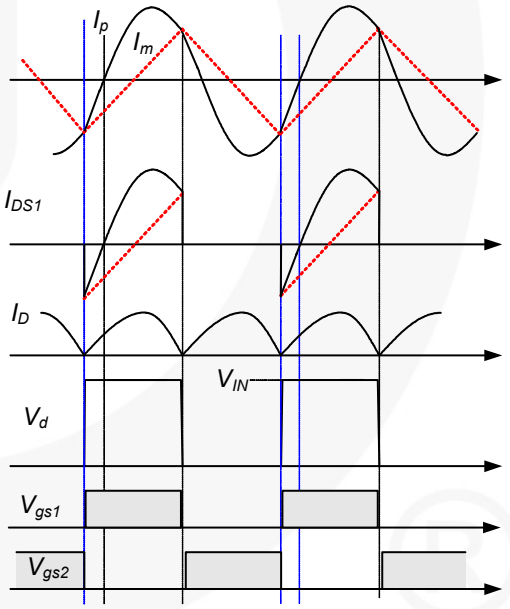

Figure 4. Typical Waveforms of Half-Bridge LLC Resonant Converter

The filtering action of the resonant network allows use of the fundamental approximation to obtain the voltage gain of the resonant converter, which assumes that only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to the output. Because the rectifier circuit in the secondary side acts as an impedance transformer, the equivalent load resistance is different from actual load resistance. Figure 5 shows how this equivalent load resistance is derived. The

primary-side circuit is replaced by a sinusoidal current source, I_{ac}, and a square wave of voltage, V_{RI}, appears at the input to the rectifier. Since the average of $|I_{ac}|$ is the output current, I_o, I_{ac}, is obtained as:

$$I_{ac} = \frac{\pi \cdot I_o}{2}\sin(\omega t) \tag{1}$$

and V_{RI} is given as:

$$\begin{aligned} V_{RI} &= +V_o \quad if\ \sin(\omega t) > 0 \\ V_{RI} &= -V_o \quad if\ \sin(\omega t) < 0 \end{aligned} \tag{2}$$

where V_o is the output voltage.

The fundamental component of V_{RI} is given as:

$$V_{RI}{}^F = \frac{4V_o}{\pi}\sin(\omega t) \tag{3}$$

Since harmonic components of V_{RI} are not involved in the power transfer, AC equivalent load resistance can be calculated by dividing $V_{RI}{}^F$ by I_{ac} as:

$$R_{ac} = \frac{V_{RI}{}^F}{I_{ac}} = \frac{8}{\pi^2}\frac{V_o}{I_o} = \frac{8}{\pi^2}R_o \tag{4}$$

Considering the transformer turns ratio ($n=N_p/N_s$), the equivalent load resistance shown in the primary side is obtained as:

$$R_{ac} = \frac{8n^2}{\pi^2}R_o \tag{5}$$

By using the equivalent load resistance, the AC equivalent circuit is obtained, as illustrated in Figure 6, where $V_d{}^F$ and $V_{RO}{}^F$ are the fundamental components of the driving voltage, V_d and reflected output voltage, V_{RO} (nV_{RI}), respectively.

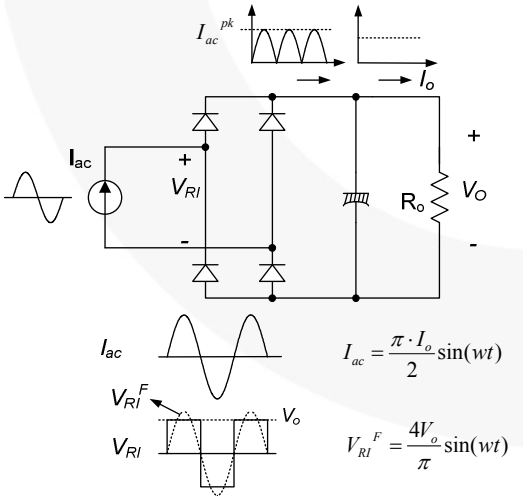

Figure 5. Derivation of Equivalent Load Resistance R_{ac}

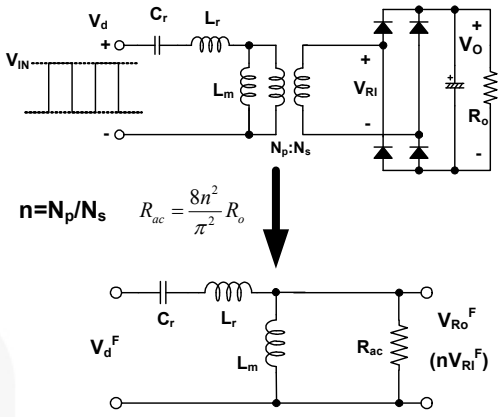

Figure 6. AC Equivalent Circuit for LLC Resonant Converter

With the equivalent load resistance obtained in Equation 5, the characteristics of the LLC resonant converter can be derived. Using the AC equivalent circuit of Figure 6, the voltage gain, M, is obtained as:

$$\begin{aligned} M = \frac{V_{RO}{}^F}{V_d{}^F} = \frac{n \cdot V_{RI}{}^F}{V_d{}^F} &= \frac{\frac{4n \cdot V_o}{\pi}\sin(\omega t)}{\frac{4}{\pi}\frac{V_{in}}{2}\sin(\omega t)} = \frac{2n \cdot V_o}{V_{in}} \\ &= \left| \frac{(\frac{\omega}{\omega_o})^2 (m-1)}{(\frac{\omega^2}{\omega_p{}^2}-1) + j\frac{\omega}{\omega_o}(\frac{\omega^2}{\omega_o{}^2}-1)(m-1)Q} \right| \end{aligned} \tag{6}$$

where:

$$L_p = L_m + L_r\ ,\ R_{ac} = \frac{8n^2}{\pi^2}R_o\ ,\ m = \frac{L_p}{L_r}$$

$$Q = \sqrt{\frac{L_r}{C_r}}\frac{1}{R_{ac}}\ ,\ \omega_o = \frac{1}{\sqrt{L_r C_r}}\ ,\ \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

As can be seen in Equation (6), there are two resonant frequencies. One is determined by L_r and C_r, while the other is determined by L_p and C_r.

Equation (6) shows the gain is unity at resonant frequency (ω_o), regardless of the load variation, which is given as:

$$M = \frac{2n \cdot V_o}{V_{in}} = \frac{(m-1)\cdot \omega_p{}^2}{\omega_o{}^2 - \omega_p{}^2} = 1 \quad at\ \omega = \omega_o \tag{7}$$

The gain of Equation (6) is plotted in Figure 7 for different Q values with m=3, f_o=100kHz, and f_p=57kHz. As observed in Figure 7, the LLC resonant converter shows gain characteristics that are almost independent of the load when the switching frequency is around the resonant frequency, f_o. This is a distinct advantage of LLC-type resonant converter over the conventional series resonant converter. Therefore, it is natural to operate the converter around the resonant frequency to minimize the switching frequency variation.

The operating range of the LLC resonant converter is limited by the peak gain (attainable maximum gain), which is indicated with ‘ ’ in Figure 7. Note that the peak voltage gain does not occur at f_o or f_p. The peak gain frequency where the peak gain is obtained exists between

f_p and f_o, as shown in Figure 7. As Q decreases (as load decreases), the peak gain frequency moves to f_p and higher peak gain is obtained. Meanwhile, as Q increases (as load increases), the peak gain frequency moves to f_o and the peak gain drops; the full load condition should be worst case for the resonant network design.

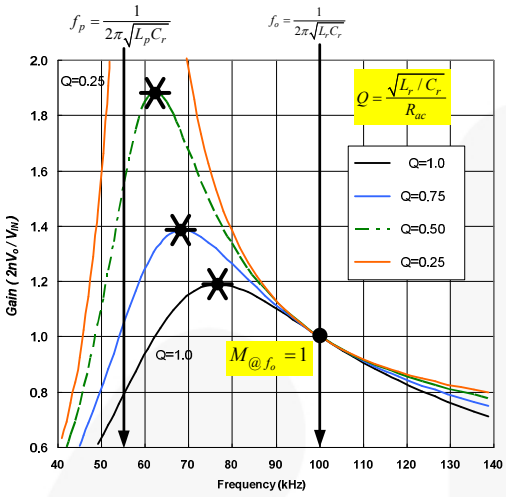

Figure 7. Typical Gain Curves of LLC Resonant Converter (*m*=3)

Consideration for Integrated Transformer

For practical design, it is common to implement the magnetic components (series inductor and shunt inductor) using an integrated transformer; where the leakage inductance is used as a series inductor, while the magnetizing inductor is used as a shunt inductor. When building the magnetizing components in this way, the equivalent circuit in Figure 6 should be modified as shown in Figure 8 because leakage inductance exists, not only in the primary side, but also in the secondary side. Not considering the leakage inductance in the transformer secondary side generally results in an ineffective design.

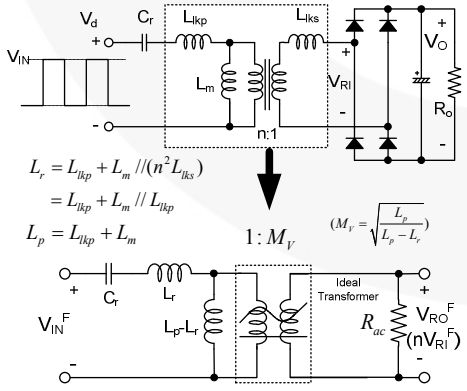

Figure 8. Modified Equivalent Circuit to Accommodate the Secondary-Side Leakage Inductance

In Figure 8, the effective series inductor (L_p) and shunt inductor (L_p-L_r) are obtained by assuming $n^2L_{lks}=L_{lkp}$ and referring the secondary-side leakage inductance to the primary side as:

$$L_p = L_m + L_{lkp}$$
$$L_r = L_{lkp} + L_m // (n^2 L_{lks}) = L_{lkp} + L_m // L_{lkp} \quad (8)$$

When handling an actual transformer, equivalent circuit with L_p and L_r is preferred since these values can be measured with a given transformer. In an actual transformer, L_p and L_r can be measured in the primary side with the secondary-side winding open circuited and short circuited, respectively.

In Figure 9, notice that a virtual gain M_V is introduced, which is caused by the secondary-side leakage inductance. By adjusting the gain equation of Equation (6) using the modified equivalent circuit of Figure 9, the gain equation for integrated transformer is obtained by:

$$M = \frac{2n \cdot V_O}{V_{in}} = \left| \frac{(\frac{\omega}{\omega_o})^2 \cdot (m-1) \cdot M_V}{(\frac{\omega^2}{\omega_p{}^2} - 1) + j(\frac{\omega}{\omega_o}) \cdot (\frac{\omega^2}{\omega_o{}^2} - 1) \cdot (m-1) Q^e} \right|$$
$$= \left| \frac{(\frac{\omega^2}{\omega_o{}^2}) \sqrt{m(m-1)}}{(\frac{\omega^2}{\omega_p{}^2} - 1) + j(\frac{\omega}{\omega_o}) \cdot (\frac{\omega^2}{\omega_o{}^2} - 1) \cdot (m-1) \cdot Q^e} \right| \quad (9)$$

where:

$$R_{ac}{}^e = \frac{8n^2}{\pi^2} \frac{R_o}{M_V{}^2}, \; m = \frac{L_p}{L_r}$$
$$Q^e = \sqrt{\frac{L_r}{C_r}} \frac{1}{R_{ac}{}^e}, \; \omega_o = \frac{1}{\sqrt{L_r C_r}}, \; \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

The gain at the resonant frequency (ω_o) is fixed regardless of the load variation, which is given as:

$$M = M_V = \sqrt{\frac{L_p}{L_p - L_r}} = \sqrt{\frac{m}{m-1}} \quad at\, \omega = \omega_o \quad (10)$$

The gain at the resonant frequency (ω_o) is unity when using individual core for series inductor, as shown in Equation 7. However, when implementing the magnetic components with integrated transformer, the gain at the resonant frequency (ω_o) is larger than unity due to the virtual gain caused by the leakage inductance in the transformer secondary side.

The gain of Equation (9) is plotted in Figure 10 for different Q^e values with m=3, f_o=100kHz, and f_p=57kHz. As observed in Figure 9, the LLC resonant converter shows gain characteristics almost independent of the load when the switching frequency is around the resonant frequency, f_o.

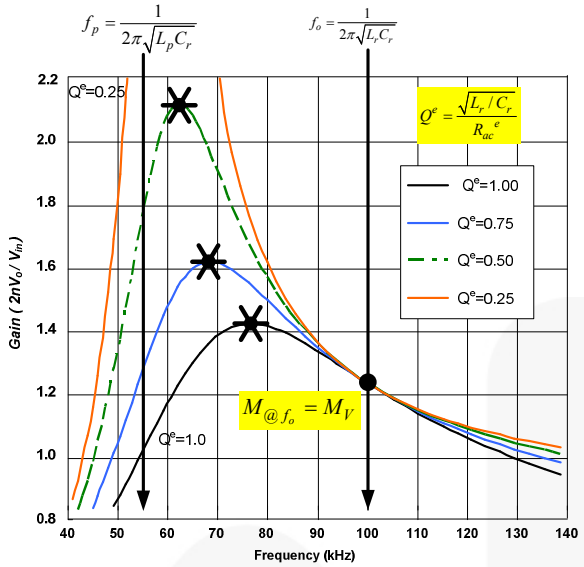

Figure 9. Typical Gain Curves of LLC Resonant Converter (*m*=3) Using an Integrated Transformer

Consideration of Operation Mode and Attainable Maximum Gain

Operation Mode

The LLC resonant converter can operate at frequency below or above the resonance frequency (f_o), as illustrated in Figure 10. Figure 11 shows the waveforms of the currents in the transformer primary side and secondary side for each operation mode. Operation below the resonant frequency (case I) allows the soft commutation of the rectifier diodes in the secondary side, while the circulating current is relatively large. The circulating current increases more as the operation frequency moves downward from the resonant frequency. Meanwhile, operation above the resonant frequency (case II) allows the circulating current to be minimized, but the rectifier diodes are not softly commutated. Below-resonance operation is preferred for high output voltage applications, such as street LED lighting systems where the reverse-recovery loss in the rectifier diode is severe. Below-resonance operation has a narrow frequency range with respect to the load variation since the frequency is limited below the resonance frequency even at no-load condition.

On the other hand, above-resonance operation has less conduction loss than the below-resonance operation. It can show better efficiency for low output voltage applications, such as Liquid Crystal Display (LCD) TV or laptop adaptor, where Schottky diodes are available for the secondary-side rectifiers and reverse-recovery problems are insignificant. However, operation above the resonant frequency may cause too much frequency increase at light-load condition. Above-frequency operation requires frequency skipping to prevent too much increase of the switching frequency.

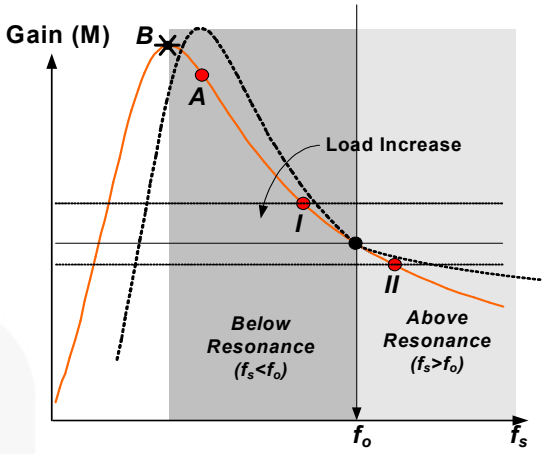

Figure 10. Operation Modes According to the Operation Frequency

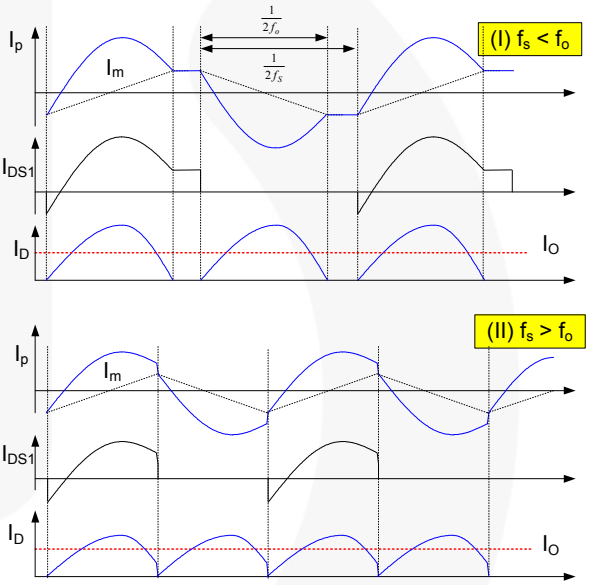

Figure 11. Waveforms of Each Operation Mode

Required Maximum Gain and Peak Gain

Above the peak gain frequency, the input impedance of the resonant network is inductive and the input current of the resonant network (I_p) lags the voltage applied to the resonant network (V_d). This permits the MOSFETs to turn on with zero voltage (ZVS), as illustrated in Figure 12. Meanwhile, the input impedance of the resonant network becomes capacitive and I_p leads V_d below the peak gain frequency. When operating in capacitive region, the MOSFET body diode is reverse recovered during the switching transition, which results in severe noise. Another problem of entering the capacitive region is that the output voltage becomes out of control since the slope of the gain is reversed. The minimum switching frequency should be limited above the peak gain frequency.

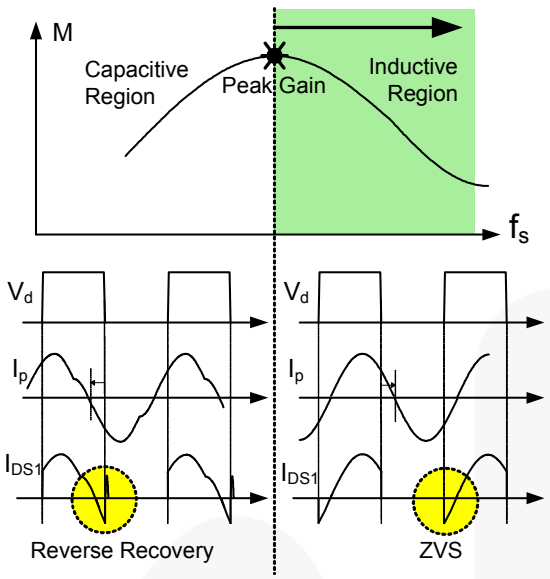

Figure 12. Operation Waveforms for Capacitive and Inductive Regions

The available input voltage range of the LLC resonant converter is determined by the peak voltage gain. Thus, the resonant network should be designed so that the gain curve has an enough peak gain to cover the input voltage range. However, ZVS condition is lost below the peak gain point, as depicted in Figure 12. Therefore, some margin is required when determining the maximum gain to guarantee stable ZVS operation during the load transient and startup. Typically 10~20% of the maximum gain is used as a margin, as shown in Figure 13.

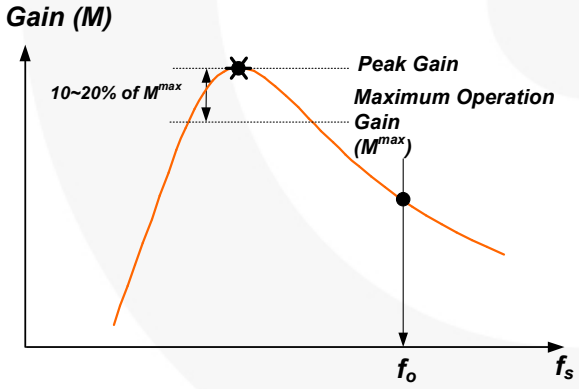

Figure 13. Determining the Maximum Gain

Even though the peak gain at a given condition can be obtained using the gain in Equation (6), it is difficult to express the peak gain in explicit form. To simplify the analysis and design, the peak gains are obtained using simulation tools and depicted in Figure 14, which shows how the peak gain (attainable maximum gain) varies with Q for different m values. It appears that higher peak gain can be obtained by reducing m or Q values. With a given resonant frequency (f_o) and Q value, decreasing m means reducing the magnetizing inductance, which results in increased circulating current. There is a trade-off between the available gain range and conduction loss.

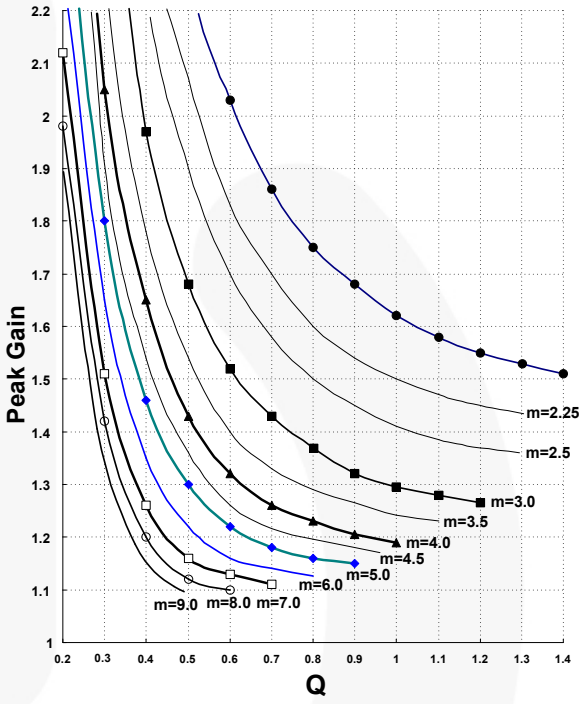

Figure 14. Peak Gain (Attainable Maximum Gain) vs. *Q* for Different *m* Values

Features of FLS-XS Series

FLS-XS series is an integrated Pulse Frequency Modulation (PFM) controller and MOSFETs specifically designed for Zero Voltage Switching (ZVS) half-bridge converters with minimal external components. The internal controller includes an under-voltage lockout, optimized high-side / low-side gate driver, temperature-compensated precise current controlled oscillator, and self-protection circuitry. Compared with discrete MOSFET and PWM controller solutions, FLS-XS series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability.

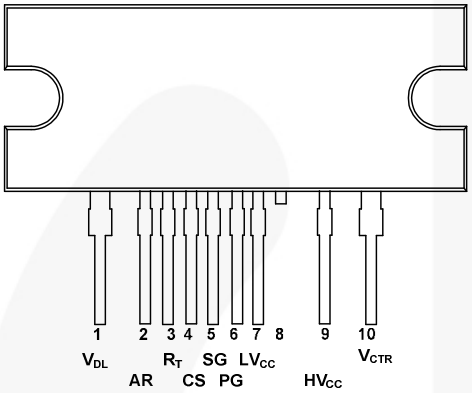

Figure 15. Package Diagram

Table 1. Pin Description

Pin#	Name	Description
1	V_{DL}	This pin is the drain of the high-side MOSFET, typically connected to the input DC link voltage.
2	AR	This pin is for discharging the external soft-start capacitor when any protections are triggered. When the voltage of this pin drops to 0.2V, all protections are reset and the controller starts to operate again.
3	R_T	This pin is to program the switching frequency. Typically, opto-coupler and resistor are connected to this pin to regulate the output voltage.
4	CS	This pin is to sense the current flowing through the low-side MOSFET. Typically negative voltage is applied on this pin.
5	SG	This pin is the control ground.
6	PG	This pin is the power ground. This pin is connected to the source of the low-side MOSFET.
7	LV_{CC}	This pin is the supply voltage of the control IC.
8	NC	No connection.
9	HV_{CC}	This pin is the supply voltage of the high-side drive circuit.
10	V_{CTR}	This pin is the drain of the low-side MOSFET. Typically transformer is connected to this pin.

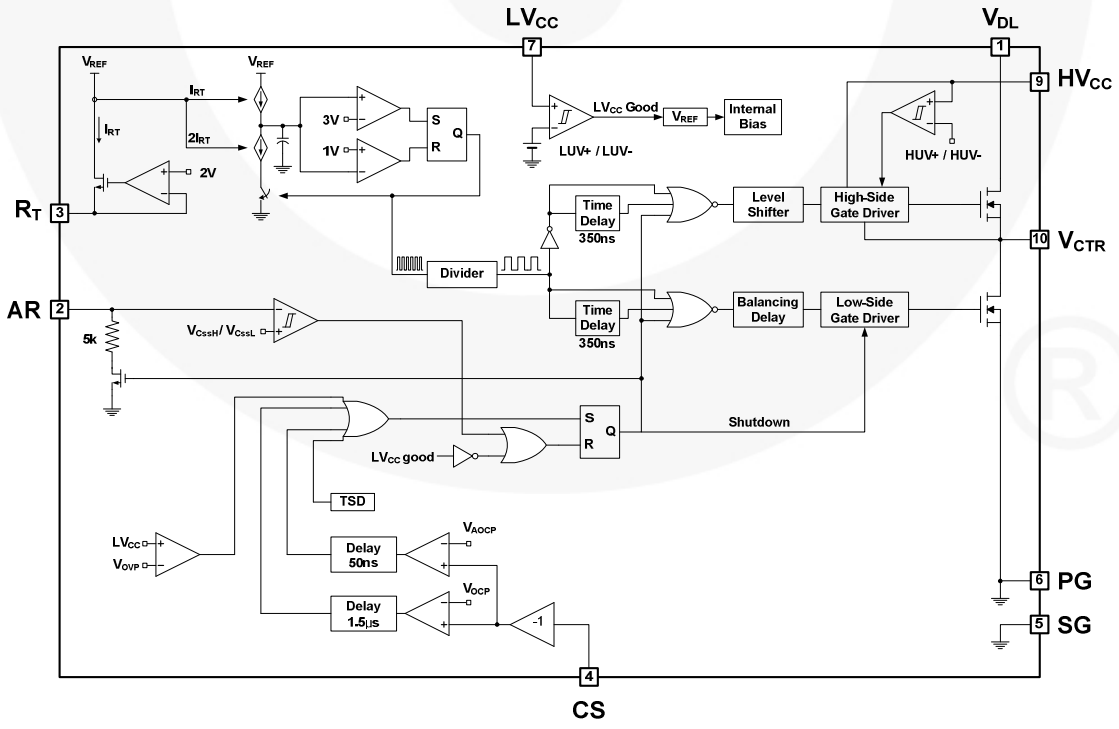

Figure 16. Functional Block Diagram of FSFR-Series

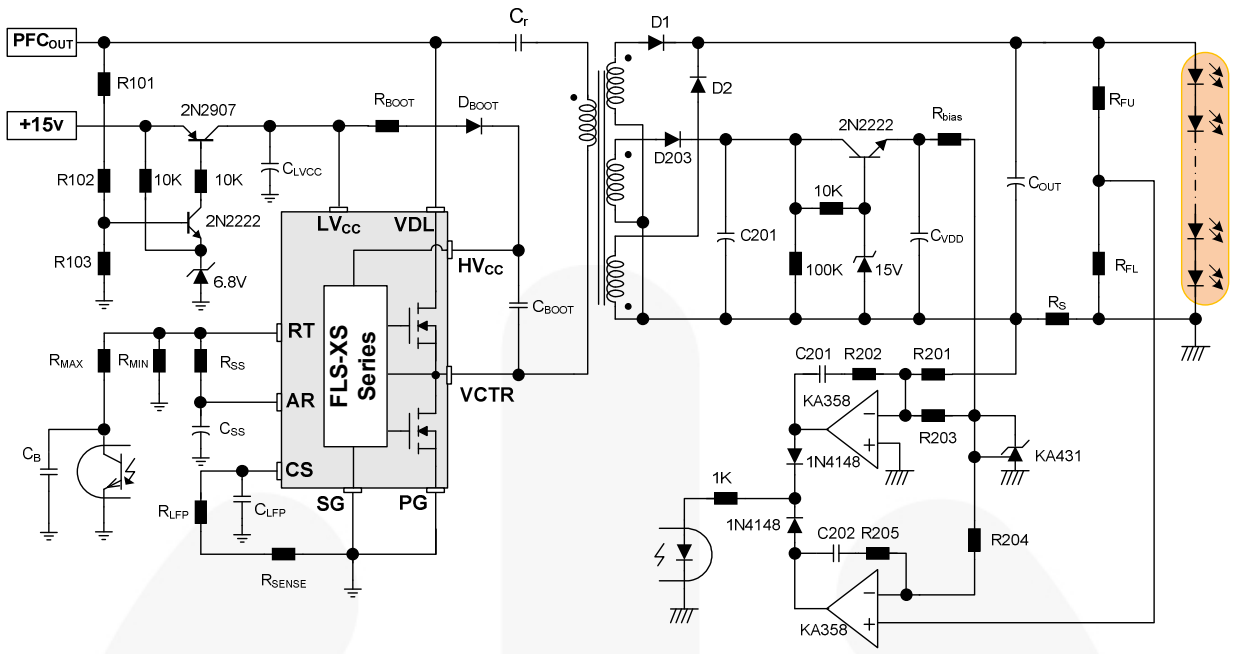

Figure 17. Reference Circuit for Design Example of LLC Resonant Half-Bridge Converter

Design Procedure

In this section, a design procedure is presented using the schematic in Figure 17 as a reference. An integrated transformer with center tap, secondary side is used and input is supplied from Power Factor Correction (PFC) pre-regulator. A DC-DC converter with 160W/115V output has been selected as a design example. The design specifications are as follows:

- Nominal input voltage: $400V_{DC}$ (output of PFC stage)
- Output: 115V/1.4A (160W)
- Hold-up time requirement: 30ms (50Hz line freq.)
- DC link capacitor of PFC output: 240µF

[STEP-1] Define System Specifications

Estimated Efficiency (E_{ff}): The power conversion efficiency must be estimated to calculate the maximum input power with a given maximum output power. If no reference data is available, use E_{ff} = 0.88~0.92 for low-voltage output applications and E_{ff} = 0.92~0.96 for high-voltage output applications. With the estimated efficiency, the maximum input power is given as:

$$P_{in} = \frac{P_o}{E_{ff}} \tag{11}$$

Input Voltage Range (V_{in}^{min} and V_{in}^{max}): The maximum input voltage would be the nominal PFC output voltage as:

$$V_{in}^{max} = V_{O.PFC} \tag{12}$$

Even though the input voltage is regulated as constant by PFC pre-regulator, it drops during the hold-up time. The minimum input voltage considering the hold-up time requirement is given as:

$$V_{in}^{min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{DL}}} \tag{13}$$

where $V_{O.PFC}$ is the nominal PFC output voltage, T_{HU} is a hold-up time, and C_{DL} is the DC link bulk capacitor.

(Design Example) Assuming the efficiency is 92%,

$$P_{in} = \frac{P_o}{E_{ff}} = \frac{161}{0.92} = 175W$$

$$V_{in}^{max} = V_{O.PFC} = 400V$$

$$V_{in}^{min} = \sqrt{V_{O.PFC}^{2} - \frac{2P_{in}T_{HU}}{C_{DL}}}$$

$$= \sqrt{400^2 - \frac{2 \cdot 175 \cdot 30 \times 10^{-3}}{240 \times 10^{-6}}} = 341V$$

[STEP-2] Determine Maximum and Minimum Voltage Gains of the Resonant Network

As discussed in the previous section, it is typical to operate the LLC resonant converter around the resonant frequency (f_o) to minimize switching frequency variation. Since the input of the LLC resonant converter is supplied from PFC output voltage, the converter should be designed to operate at f_o for the nominal PFC output voltage.

As observed in Equation (10), the gain at f_o is a function of m ($m=L_p/L_r$). The gain at f_o is determined by choosing that value of m. While a higher peak gain can be obtained with a small m value, too small m value results in poor coupling of the transformer and deteriorates the efficiency. It is typical to set m to be 3~7, which results in a voltage gain of 1.1~1.2 at the resonant frequency (f_o).

With the chosen m value, the voltage gain for the nominal PFC output voltage is obtained as:

$$M^{\min} = \sqrt{\frac{m}{m-1}} \quad @f=f_o \tag{14}$$

which would be the minimum gain because the nominal PFC output voltage is the maximum input voltage (V_{in}^{max}).

The maximum voltage gain is given as:

$$M^{\max} = \frac{V_{in}^{\max}}{V_{in}^{\min}} M^{\min} \tag{15}$$

(Design Example) The ratio (m) between L_p and L_r is chosen as 5. The minimum and maximum gains are obtained as:

$$M^{\min} = \frac{V_{RO}}{V_{in}^{\max}/2} = \sqrt{\frac{m}{m-1}} = \sqrt{\frac{5}{5-1}} = 1.12$$

$$M^{\max} = \frac{V_{in}^{\max}}{V_{in}^{\min}} m^{\min} = \frac{400}{341} \cdot 1.12 = 1.31$$

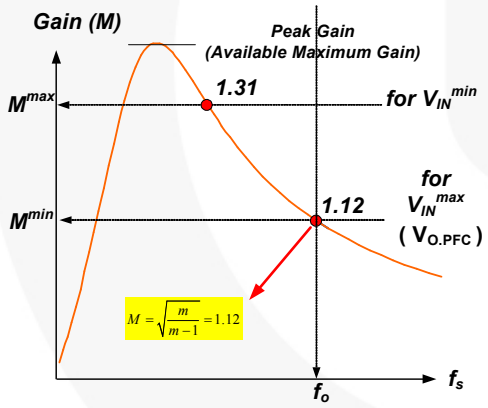

Figure 18. Maximum Gain / Minimum Gain

[STEP-3] Determine the Transformer Turns Ratio ($n=N_p/N_s$)

With the minimum gain (M^{min}) obtained in STEP-2, the transformer turns ratio is given as:

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{\max}}{2(V_o + V_F)} \cdot M^{\min} \tag{16}$$

where V_F is the secondary-side rectifier diode voltage drop.

(Design Example) assuming V_F is 0.9V,

$$n = \frac{N_p}{N_s} = \frac{V_{in}^{\max}}{2(V_O + V_F)} \cdot M_{\min} = \frac{400}{2(115+0.9)} \cdot 1.12 = 1.93$$

[STEP-4] Calculate Equivalent Load Resistance

With the transformer turns ratio obtained from Equation (16), the equivalent load resistance is obtained as:

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{V_o^2}{P_o} \tag{17}$$

(Design Example)

$$R_{ac} = \frac{8n^2}{\pi^2} \frac{(V_o + V_F)^2}{P_o} = \frac{8 \cdot 1.93^2 \cdot 115.9^2}{\pi^2 \cdot 161} = 252\Omega$$

[STEP-5] Design the Resonant Network

With m value chosen in STEP-2, read proper Q value from the peak gain curves in Figure 14 that allows enough peak gain. Considering the load transient and stable zero-voltage-switching (ZVS) operation, 10~20% margin should be introduced on the maximum gain when determining the peak gain. Once the Q value is determined, the resonant parameters are obtained as:

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} \tag{18}$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} \tag{19}$$

$$L_p = m \cdot L_r \tag{20}$$

(Design Example)

As calculated in STEP-2, the maximum voltage gain (M^{max}) for the minimum input voltage (V_{in}^{min}) is 1.31. With 15% margin, a peak gain of 1.51 is required. m has been chosen as 5 in STEP-2 and Q is obtained as 0.38 from the peak gain curves in Figure 19. By selecting the resonant frequency as 100kHz, the resonant components are determined as:

$$C_r = \frac{1}{2\pi Q \cdot f_o \cdot R_{ac}} = \frac{1}{2\pi \cdot 0.38 \cdot 100 \times 10^3 \cdot 252} = 16.64nF$$

$$L_r = \frac{1}{(2\pi f_o)^2 C_r} = \frac{1}{(2\pi \times 100 \times 10^3)^2 \cdot 16.64 \times 10^{-9}} = 152uH$$

$$L_p = m \cdot L_r = 760uH$$

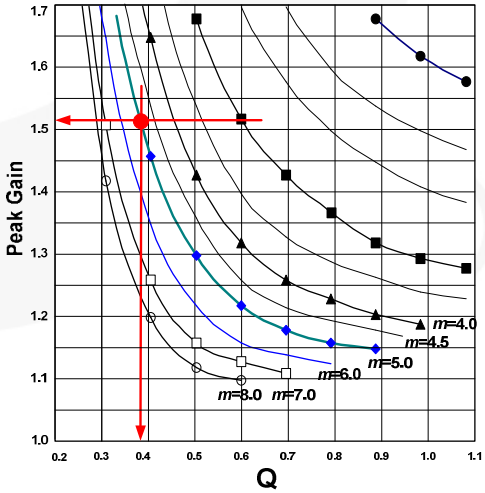

Figure 19. Resonant Network Design Using the Peak Gain (Attainable Maximum Gain) Curve for m=5

[STEP-6] Design the Transformer

The worst case for the transformer design is the minimum switching frequency condition, which occurs at the minimum input voltage and full-load condition. To obtain the minimum switching frequency, plot the gain curve using gain Equation 9 and read the minimum switching frequency. The minimum number of turns for the transformer primary-side is obtained as:

$$N_p^{\min} = \frac{n(V_o + V_F)}{2 f_s^{\min} \cdot M_V \cdot \Delta B \cdot A_e} \quad (21)$$

where A_e is the cross-sectional area of the transformer core in m^2 and ΔB is the maximum flux density swing in Tesla, as shown in Figure 20. If there is no reference data, use ΔB =0.3~0.4 T.

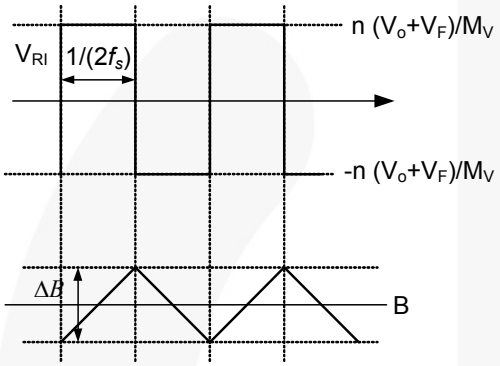

Figure 20. Flux Density Swing

Choose the proper number of turns for the secondary side that results in primary-side turns larger than $N_p^{\min}$ as:

$$N_p = n \cdot N_s > N_p^{\min} \quad (22)$$

(Design Example) EER3542 core (A_e=107mm^2) is selected for the transformer. From the gain curve of Figure 21, the minimum switching frequency is obtained as 82KHz. The minimum primary-side turns of the transformer is given as:

$$N_p^{\min} = \frac{n(V_o + V_F)}{2 f_s^{\min} \Delta B \cdot 1.11 \cdot A_e}$$

$$= \frac{1.93 \times 115.9}{2 \times 82 \times 10^3 \cdot 0.4 \cdot 1.11 \cdot 107 \times 10^{-6}} = 29\ turns$$

Choose N_s so that the resultant N_p is larger than $N_p^{\min}$:

$$N_p = n \cdot N_s = 1.93 \times 14 = 27 < N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 15 = 29 < N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 16 = 31 > N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 17 = 33 > N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 18 = 35 > N_p^{\min}$$

$$N_p = n \cdot N_s = 1.93 \times 19 = 37 > N_p^{\min}$$

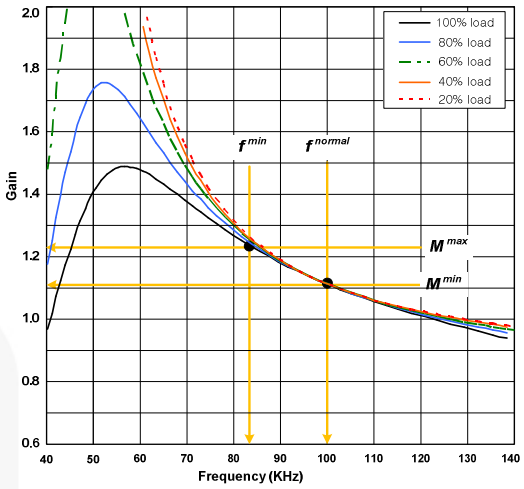

Figure 21. Gain Curve

[STEP-7] Transformer Construction

Parameters L_p and L_r of the transformer were determined in STEP-5. L_p and L_r can be measured in the primary side with the secondary-side winding open circuited and short circuited, respectively. Since LLC converter design requires a relatively large L_r, a sectional bobbin is typically used, as shown in Figure 22, to obtain the desired L_r value. For a sectional bobbin, the number of turns and winding configuration are the major factors determining the value of L_r, while the gap length of the core does not affect L_r much. L_p can be controlled by adjusting the gap length. Table 2 shows measured L_p and L_r values with different gap lengths. A gap length of 0.05mm obtains values for L_p and L_r closest to the designed parameters.

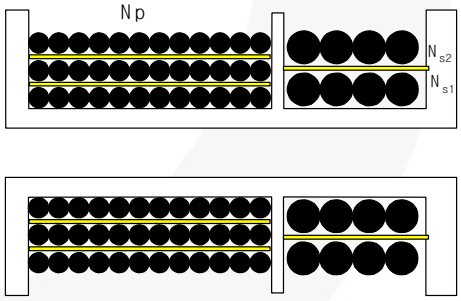

Figure 22. Sectional Bobbin

Table 2. Measured L_p and L_r with Different Gap Lengths

Gap Length	Lp	Lr
0.0mm	2,295μH	123μH
0.05mm	943μH	122μH
0.10mm	**630μH**	**118μH**
0.15mm	488μH	117μH
0.20mm	419μH	115μH
0.25mm	366μH	114μH

(Design Example)

Final Resonant Network Design

Even though the integrated transformer approach in LLC resonant converter design can implement the magnetic components in a single core and save one magnetic component, the value of L_r is not easy to control in real transformer design. Resonant network design sometimes requires iteration with a resultant L_r value after the transformer is built. The resonant capacitor value is also changed since it should be selected among off-the-shelf capacitors. The final resonant network design is summarized in Table 3 and the new gain curves are shown in Figure 23.

Table 3. Final Resonant Network Design Parameters

Parameters	Initial Design	Final Design
L_p	760μH	**625μH**
L_r	152H	**125μH**
C_r	16.64nF	**22nF**
f_o	100kHz	**96kHz**
m	5	**5**
Q	0.38	**0.3**
M@f_o	1.12	**1.12**
Minimum Frequency	75kHz	**74.4kHz**

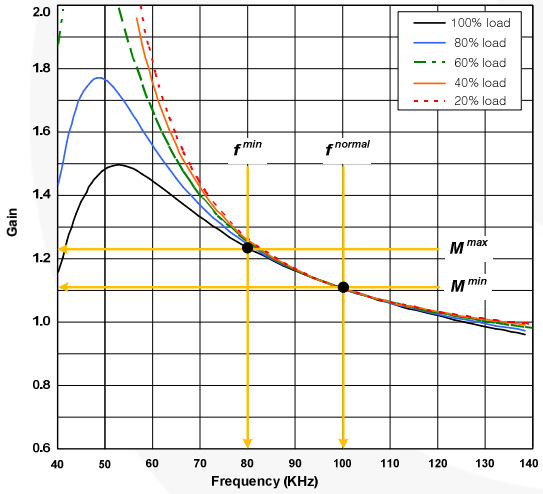

Figure 23. Gain Curve of the Final Resonant Network Design

[STEP-8] Select the Resonant Capacitor

When choosing the resonant capacitor, the current rating should be considered because a considerable amount of current flows through the capacitor. The RMS current through the resonant capacitor is given as:

$$I_{C_r}^{RMS} \cong \frac{1}{E_{ff}}\sqrt{\left[\frac{\pi I_o}{2\sqrt{2}n}\right]^2+\left[\frac{n(V_o+V_F)}{4\sqrt{2}f_o M_V(L_p-L_r)}\right]^2} \quad (23)$$

The nominal voltage of the resonant capacitor in normal operation is given as:

$$V_{C_r}^{nom} \cong \frac{V_{in}^{\max}}{2}+\frac{\sqrt{2}\cdot I_{Cr}^{RMS}}{2\cdot\pi\cdot f_o\cdot C_r} \quad (24)$$

However, the resonant capacitor voltage increases higher than this at overload condition or load transient. Actual capacitor selection should be based on the Over-Current Protection (OCP) trip point. With the OCP level, IOCP, the maximum resonant capacitor voltage is obtained as:

$$V_{C_r}^{nom} \cong \frac{V_{in}^{\max}}{2}+\frac{I_{OCP}}{2\cdot\pi\cdot f_o\cdot C_r} \quad (25)$$

(Design Example)

$$I_{C_r}^{RMS} \cong \frac{1}{E_{ff}}\sqrt{\left[\frac{\pi I_O}{2\sqrt{2}n}\right]^2+\left[\frac{n(V_o+V_F)}{4\sqrt{2}f_o M_v(L_p-L_r)}\right]^2}$$

$$=\frac{1}{0.92}\sqrt{\left[\frac{\pi\cdot 1.4}{2\sqrt{2}\cdot 1.93}\right]^2+\left[\frac{1.93(115+0.9)}{4\sqrt{2}\cdot 96\times 10^3\cdot 1.12\cdot 500\times 10^{-6}}\right]^2}$$

$=1.18A$

The peak current in the primary side in normal operation is:

$$I_{C_r}^{peak}=\sqrt{2}\cdot I_{C_r}^{rms}=1.67A$$

OCP level is set to 2.5A with 50% margin on I_{Cr}^{peak}:

$$V_{C_r}^{nom} \cong \frac{V_{in}^{\max}}{2}+\frac{\sqrt{2}\cdot I_{C_r}^{RMS}}{2\cdot\pi\cdot f_o\cdot C_r}$$

$$=\frac{400}{2}+\frac{\sqrt{2}\cdot 1.18}{2\cdot\pi\cdot 96\times 10^3\cdot 22\times 10^{-9}}=326V$$

$$V_{C_r}^{\max} \cong \frac{V_{in}^{\max}}{2}+\frac{I_{OCP}}{2\cdot\pi\cdot f_o\cdot C_r}$$

$$=\frac{400}{2}+\frac{2.5}{2\cdot\pi\cdot 96\times 10^3\cdot 22\times 10^{-9}}=388.5V$$

A 630V rated low-ESR film capacitor is selected for the resonant capacitor.

[STEP-9] Rectifier Network Design

When the center tap winding is used in the transformer secondary side, the diode voltage stress is twice of the output voltage expressed as:

$$V_D=2(V_o+V_F) \quad (26)$$

The RMS value of the current flowing through each rectifier diode is given as:

$$I_D^{RMS}=\frac{\pi}{4}I_o \quad (27)$$

Meanwhile, the ripple current flowing through output capacitor is given as:

$$I_{Co}^{RMS}=\sqrt{\left(\frac{\pi I_o}{2\sqrt{2}}\right)^2-I_o^2}=\sqrt{\frac{\pi^2-8}{8}}I_o \quad (28)$$

The voltage ripple of the output capacitor is:

$$\Delta V_o = \frac{\pi}{2} I_o \cdot R_C \tag{29}$$

where R_C is the effective series resistance (ESR) of the output capacitor and the power dissipation is the output capacitor is:

$$P_{Loss.Co} = (I_{Co}{}^{RMS})^2 \cdot R_C \tag{30}$$

(Design Example) The voltage stress and current stress of the rectifier diode are:

$$V_D = 2(V_o + V_F) = 2(115 + 0.9) = 231.8V$$

$$I_D{}^{RMS} = \frac{\pi}{4} I_o = 1.1A$$

The 600V/8A Ultra fast recovery diode is selected for the rectifier, considering the voltage overshoot caused by the stray inductance.

The RMS current of the output capacitor is:

$$I_{C_o}{}^{RMS} = \sqrt{(\frac{\pi I_o}{2\sqrt{2}})^2 - I_o{}^2} = \sqrt{\frac{\pi^2 - 8}{8}} I_o = 0.675A$$

When two electrolytic capacitors with ESR of 100mΩ are used in parallel, the output voltage ripple is given as:

$$\Delta V_o = \frac{\pi}{2} I_o \cdot R_C = \frac{\pi}{2} \cdot 1.4 \cdot (\frac{0.1}{2}) = 0.1V$$

The loss in electrolytic capacitors is:

$$P_{Loss,C_o} = (I_{C_o}{}^{RMS})^2 \cdot R_C = 0.675^2 \cdot 0.05 == 0.02W$$

[STEP-10] Control Circuit Configuration

Figure 24 shows the typical circuit configuration for the RT pin of FLS-XS series, where the opto-coupler transistor is connected to the RT pin to control the switching frequency. The minimum switching frequency occurs when the opto-coupler transistor is fully tuned off, which is given as:

$$f_{\min} = \frac{5.2k\Omega}{R_{\min}} \times 100(kHz) \tag{31}$$

Assuming the saturation voltage of opto-coupler transistor is 0.2V, the maximum switching frequency is determined as:

$$f_{\max} = (\frac{5.2k\Omega}{R_{\min}} + \frac{4.68k\Omega}{R_{\max}}) \times 100(kHz) \tag{32}$$

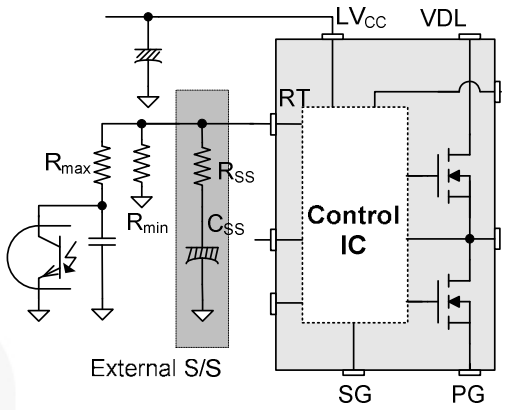

Figure 24. Typical Circuit Configuration for RT Pin

Soft-Start To prevent excessive inrush current and overshoot of output voltage during startup, increase the voltage gain of the resonant converter progressively. Since the voltage gain of the resonant converter is reversely proportional to the switching frequency, soft-start is implemented by sweeping down the switching frequency from an initial high frequency (f^{ISS}) until the output voltage is established, as illustrated in Figure 25. The soft-start circuit is made by connecting RC series network on the RT pin as shown in Figure 24. FLS-XS series also has an internal soft-start for 3ms to reduce the current overshoot during the initial cycles, which adds 40KHz to the initial frequency of the external soft-start circuit, as shown in Figure 25. The actual initial frequency of the soft-start is given as:

$$f^{ISS} = (\frac{5.2k\Omega}{R_{\min}} + \frac{5.2k\Omega}{R_{SS}}) \times 100 + 40\ (kHz) \tag{33}$$

It is typical to set the initial frequency of soft-start (f^{ISS}) as 2~3 times of the resonant frequency (f_o).

The soft-start time is determined by the RC time constant:

$$T_{SS} = 3 \sim 4\ times\ of\ R_{SS} \cdot C_{SS} \tag{34}$$

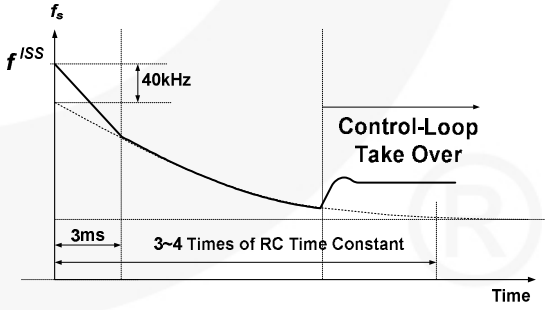

Figure 25. Frequency Sweep of the Soft-Start

(Design Example) The minimum frequency is 75kHz in STEP-6. R_{min} is determined as:

$$R_{\min} = \frac{100KHz}{f_{\min}} \times 5.2K\Omega = 6.93K\Omega$$

Considering the output voltage overshoot during transient (10%) and the controllability of the feedback loop, the maximum frequency is set as 140kHz. R_{max} is determined as:

$$R_{\max} = \frac{4.68K\Omega}{(\frac{f_o \times 1.40}{100KHz} - \frac{5.2K\Omega}{R_{\min}})}$$

$$= \frac{4.68K\Omega}{(\frac{96KHz \times 1.40}{100KHz} - \frac{5.2K\Omega}{6.93K\Omega})} = 7.88K\Omega$$

Setting the initial frequency of soft-start as 250kHz (2.5 times of the resonant frequency), the soft-start resistor R_{SS} is given as:

$$R_{SS} = \frac{5.2K\Omega}{(\frac{f_{ISS} - 40KHz}{100KHz} - \frac{5.2K\Omega}{R_{\min}})}$$

$$= \frac{5.2K\Omega}{(\frac{250KHz - 40KHz}{100KHz} - \frac{5.2K\Omega}{6.93K\Omega})} = 3.85K\Omega$$

[STEP-11] Current Sensing and Protection

FLS-XS series senses low-side MOSFET drain current as a negative voltage, as shown in Figure 26 and Figure 27. Half-wave sensing allows low-power dissipation in the sensing resistor, while full-wave sensing has less switching noise in the sensing signal. Typically, RC low-pass filter is used to filter out the switching noise in the sensing signal. The RC time constant of the low-pass filter should be 1/100~1/20 of the switching period.

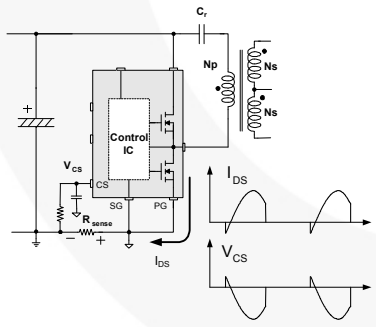

Figure 26. Half-Wave Sensing

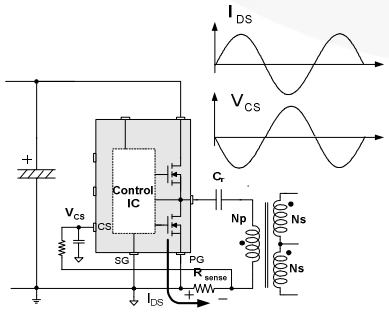

Figure 27. Full-Wave Sensing

(Design Example) Since the OCP level is determined as 2.5A in STEP-8 and the OCP threshold voltage is -0.6V, a sensing resistor of 0.24Ω is used. The RC time constant is set to 100ns (1/100 of switching period) with 1kΩ resistor and 100pF capacitor.

[STEP-12] Voltage and Current Feedback

Power supplies for LED lighting must be controlled by Constant Current (CC) Mode as well as a Constant Voltage (CV) Mode. Because the forward-voltage drop of LED varies with the junction temperature and the current also increases greatly consequently, devices can be damaged. Figure 28 shows an example of a CC and CV Mode feedback circuit for single output LED power supply. During normal operation, CC Mode is dominant and CV control circuit does not activate as long as the feedback voltage is lower than reference voltage, which means that CV control circuit only acts as OVP for abnormal modes.

(Design Example) The output voltage (V_O) is 115V in design target. V_O is determined as:

$$V_o = 2.5(1 + \frac{R_{FU}}{R_{FL}})$$

Set the upper-side feedback resistance (R_{FU}) as 330KΩ. R_{FL} is determined as:

$$R_{FL} = \frac{2.5 \times R_{FU}}{(V_o - 2.5)} = \frac{2.5 \times 330K\Omega}{(115 - 2.5)} = 7.33K\Omega$$

The output voltage of op-amp is given as:

$$0 = \frac{\frac{V_{sense}}{R201} + \frac{V_{REF}}{R203} + sC201 \cdot V_{OC}}{\frac{1}{R201} + \frac{1}{R203} + sC201}$$

$$V_{OC} = -\frac{1}{sC201}(\frac{V_{sense}}{R201} + \frac{V_{REF}}{R203})$$

Actually, the V_{sense} has a negative value and assume all resistors have the same value for simplification;

$$V_{OC} = -\frac{1}{sC201 \times R}(V_{sense} - V_{REF})$$

The output voltage of the op-amp for CC control keeps zero voltage as long as the sensing voltages are lower than the reference voltage.

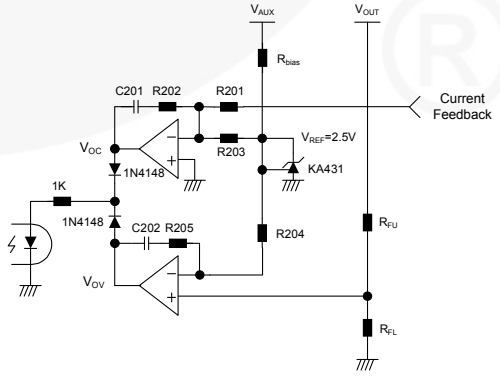

Figure 28. Example of CC and CV Feedback Circuit

Figure 29 shows another example of a CC and Over-Voltage Regulation (OVR) Mode feedback circuit for multi-output LED power supply. The FAN7346 is a LED current-balance controller that controls four LED arrays to maintain equal LED current. To prevent LED driving voltage being over the withstanding voltage of component, the FAN7346 controls LED driving voltage. The OVR control circuit activates when the ENA pin is in HIGH state. If OVR pin voltage is lower than 1.5V, the Feedback Control (FB) pin voltage follows headroom control to maintain minimum voltage of drain voltages as 1V. If OVR pin voltage is higher than 1.5V, the FAN7346 controls FB (FB is pulled LOW) through FB regulation so the OVR pin voltage is not over 1.5V.

LED current is controlled by FBx pin voltage. The external current balance switch is operating in linear region to control LED current. Sensed voltage at the FBx pin is compared with internal reference voltage and controller signals the gate (or base) for external current balance switch. Internal reference voltage is made from ADIM voltage. The LED current is determined as:

$$I_{LED} = \frac{V_{ADIM}}{10 \times R_{SENSE}} \quad (35)$$

ADIM voltage is clamped internally from 0.5V to 4V. The protections; such as open LED Protection (OLP), Short LED Protection (SLP), and Over-Current Protection (OCP); which increase system reliability, are applied in individual string protection method.

To sense a short LED condition, the FAN7346 senses drain voltage level. If LEDs are shorted, the LED forward voltage is lower than other LED strings, so its drain voltage of external balance switch is higher than other drain voltage. The SLP condition detection threshold voltage can be programmed by SLPR voltage. The internal short LED protection reference is determined as:

$$V_{SLP\_TH} = 10 \times V_{SLPR} \quad (36)$$

Minimum SLP threshold voltage is 0V and maximum SLP threshold voltage is 45V. If any string is in SLP condition, SLP string is turned off and other string is operated normally. If the sensed drain voltage (CHx voltage) is higher than the programmed threshold voltage for 20µs, CHx goes to short LED protection. As soon as encountering SLP, the corresponding channel is forced off.

To sense an open LED condition, the FAN7346 senses drain voltage level. If LED string is opened, its drain voltage of external balance switch is grounded, so the FAN7346 detects the open-LED condition. The detection threshold voltage is 0.3V. If CHx voltage is lower than 0.3V for 20µs, its drain voltage feedback is pulled up to 5V. This means the opened LED string is eliminated from drain feedback loop. Without OLP, minimum drain voltage is 0V, so drain voltage feedback forces the FB signal to increase output power. This can cause SLP or thermal stress problems in the other channel. OLP function has auto-recovery: As soon as drain voltage is higher than 0.3V, OLP is finished and drain voltage feedback system is restored.

To sense over-current condition, the FAN7346 monitors FBx pin voltage. If FBx voltage is higher than 1V for 20µs, CHx is considered in over-current condition. After sensing OCP condition, individual channel switch is latched off. So, even if a channel is in OCP condition, other channels keep operating. Any OCP channel is restarted after UVLO is reset.

(Design Example) The output voltage (V_O) is 115V in design target. V_O is determined as:

$$V_o = 1.5(1 + \frac{R8}{R10})$$

Set the upper-side feedback resistance (R8) as 1MΩ. R10 is determined as:

$$R10 = \frac{1.5 \times R8}{(V_o - 1.5)} = \frac{1.5 \times 1M\Omega}{(115 - 1.5)} = 13.2K\Omega$$

The output channel current (I_{LED}) is 350mA in design target. Setting the V_{ADIM} is above 4V, the current sense R_{SENSE} is determined as:

$$R_{SENSE} = \frac{V_{ADIM}}{10 \times I_{LED}} = \frac{4V}{10 \times 350mA} = 1.14\Omega$$

Choose the sense resistor (R29,R30,R31, and R32) is 1.2 Ω , the OCP level is determined as:

$$I_{OCP} = \frac{V_{OCP\_TH}}{R_{SENSE}} = \frac{1V}{1.5\Omega} = 833mA$$

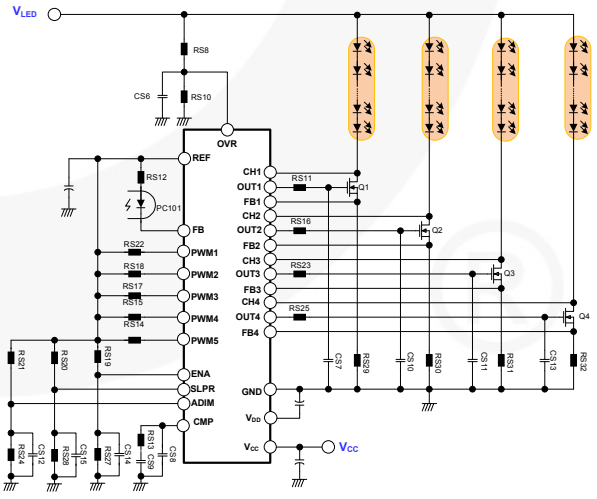

Figure 29. Example of CC and OVR Feedback Circuit

Design Summary

Figure 30 and Figure 31 show the final schematic of the LLC resonant half-bridge converter for LED lighting design example. EER3543 core with sectional bobbin is used for the transformer. Efficiency at full-load is around 94%.

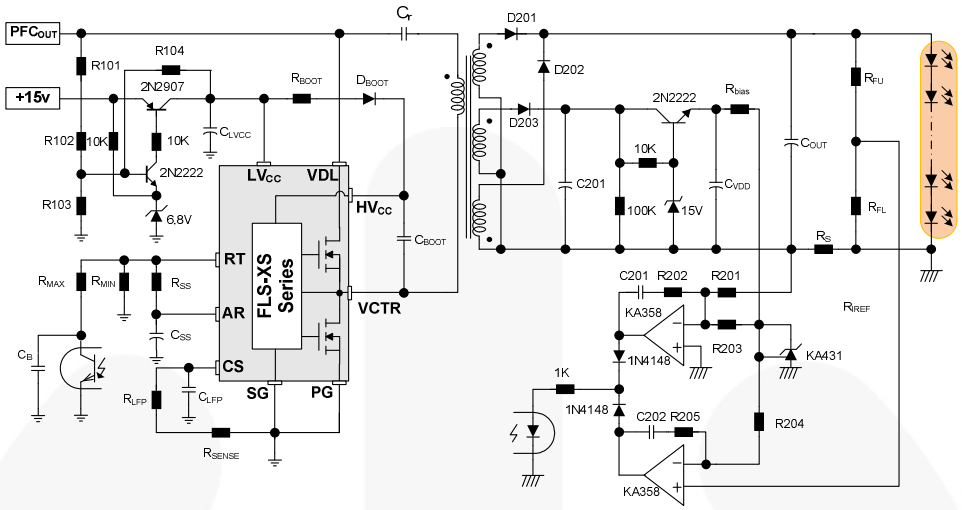

Figure 30. Final Schematic of Half-Bridge LLC Resonant Converter for Single Channel

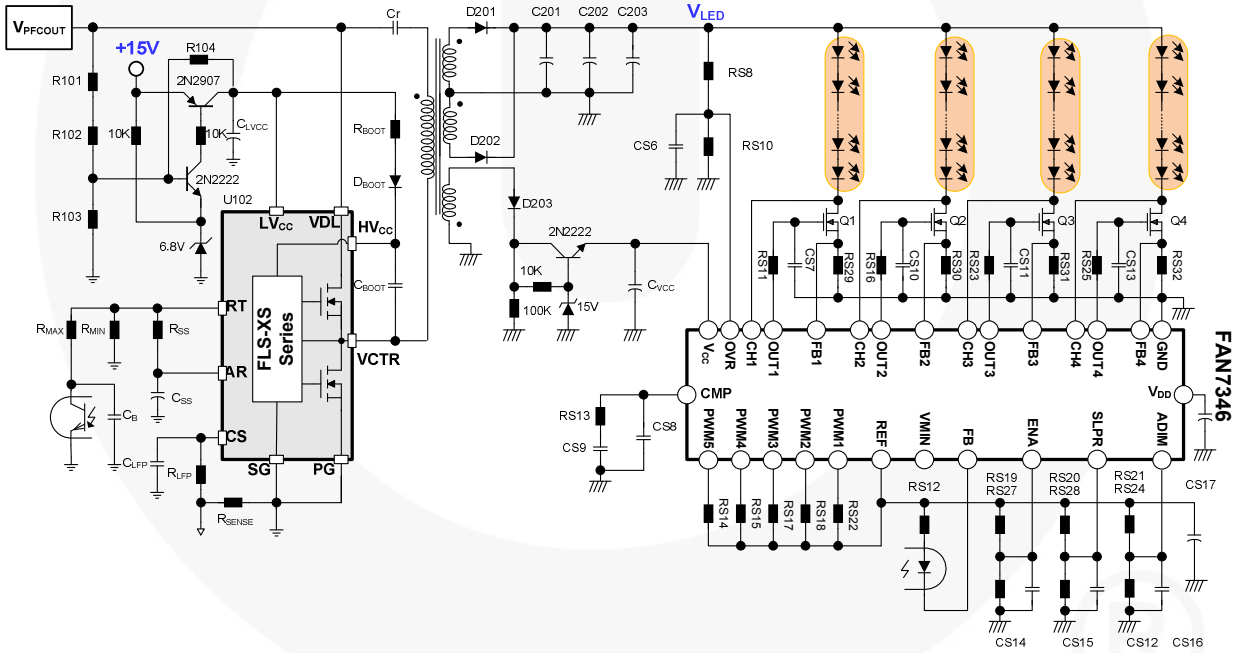

Figure 31. Final Schematic of Half-Bridge LLC Resonant Converter for Multi Channel

Experimental Verification

To show the validity of the design procedure presented in this application note, the converter of the design example was built and tested. All the circuit components are used as designed in the design example.

Figure 32 and Figure 33 show the operation waveforms at full-load and no-load conditions for nominal input voltage. As observed, the MOSFET drain-to-source voltage (V_{DS}) drops to zero by resonance before the MOSFET is turned on and zero voltage switching is achieved.

Figure 34 shows the waveforms of the resonant capacitor voltage and primary-side current at full-load condition. The peak values of the resonant capacitor voltage and primary-side current are 320V and 1.7A, respectively, which are well matched with the calculated values in STEP-8 of design procedure section.

Figure 35 shows the rectifier diode voltage and current waveforms at full-load condition. Due to the voltage overshoot caused by stray inductance, the voltage stress is a little bit higher than the value calculated in STEP-9.

Figure 36 shows the output load current and output voltage of op-amp waveforms for constant-current control when output load is step changed from 240mA to 1400mA at t_0.

Figure 37 shows the operation waveform when LED string is opened and restored condition

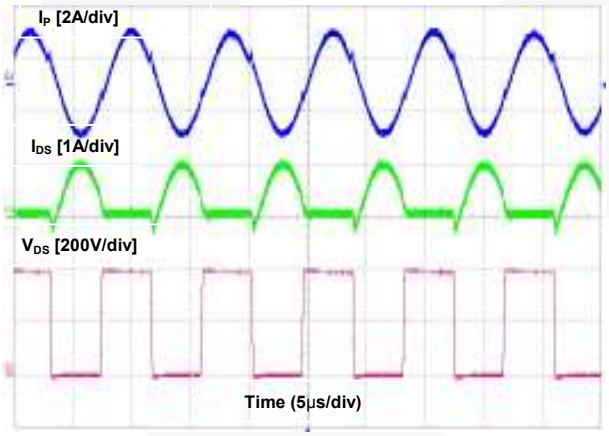

Figure 32. Operation Waveforms at Full-Load Condition

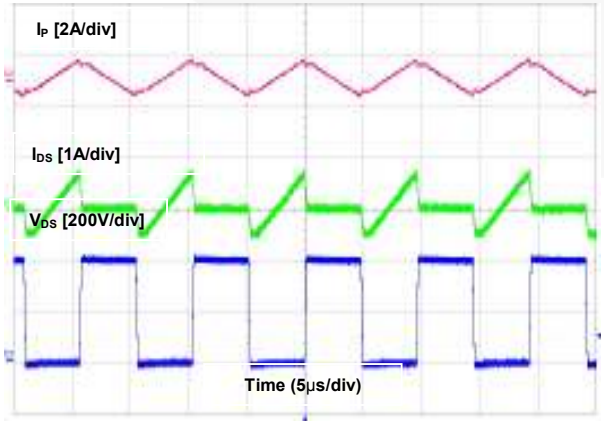

Figure 33. Operation Waveforms at No-Load Condition

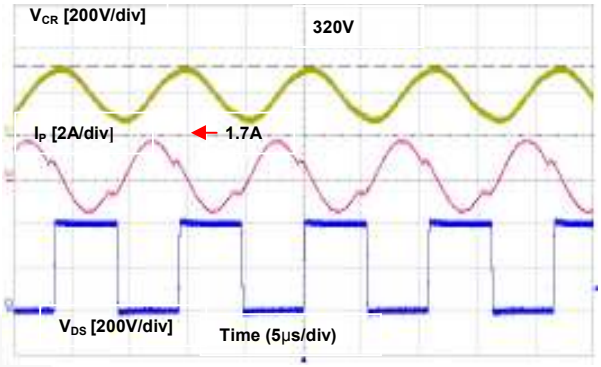

Figure 34. Resonant Capacitor Voltage and Primary-Side Current Waveforms at Full-Load Condition

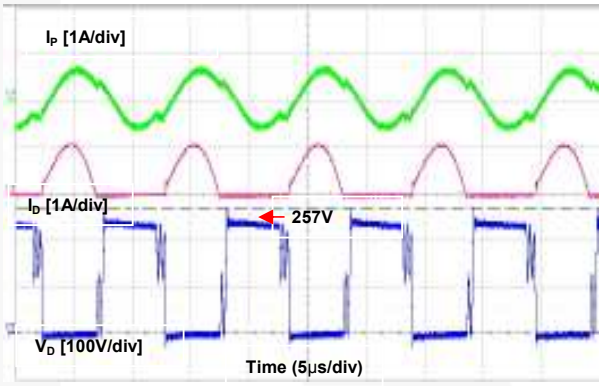

Figure 35. Rectifier Diode Voltage and Current Waveforms at Full-Load Condition

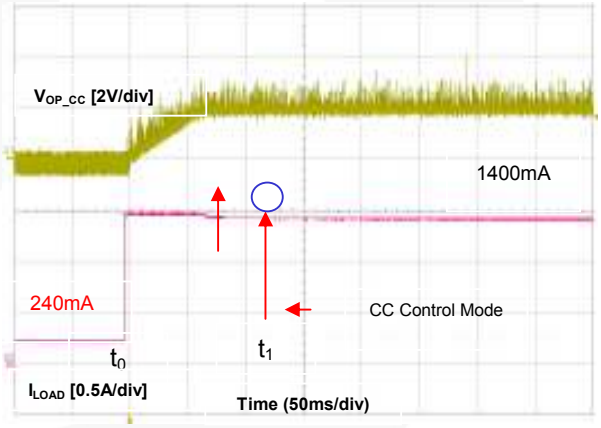

Figure 36. Constant-Current Control Waveforms

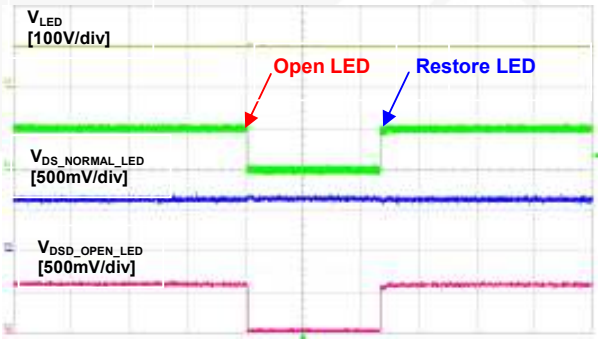

Figure 37. Open LED Protection Operation

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This application note written based on Fairchild Semiconductor Application Note AN-4137.

Related Datasheets

FLS1800XS — Half-Bridge LLC Resonant Control IC for Lighting

FLS2100XS — Half-Bridge LLC Resonant Control IC for Lighting

FAN7346 — 4-Channel LED Current Balance Control IC

Application Report
SLUA582A–October 2010–Revised November 2010

Feedback Loop Design of an LLC Resonant Power Converter

Hong Huang — *Power-Supply Control Products*

ABSTRACT

This application note describes an approach to design feedback loop compensation for an LLC resonant half-bridge power converter. The approach described here is based on the measured Bode plots of the modulator generated by a network analyzer. As we know, as long as the modulator Bode plots are obtained, the frequency domain poles and zeros in the feedback loop compensation can be analytically determined, then fine-tuned with a bench test. This measurement is necessary as part of feedback loop design because a practical small-signal model is not available for LLC resonant converters. This document uses the Texas Instruments' UCC25600 as the frequency controller. A detailed description of the UCC25600 and its associated example design fixture, the UCC25600EVM-341, can be found in the product data sheet and the evaluation module user's guide, respectively; both additional documents are available for download at www.ti.com.

Contents

List of Figures

1 Control Loop Description of an LLC Converter

NOTE: For complete details on the design of an LLC resonant power converter, the recommended reference is SEM1900 Topic 3, *Designing an LLC Resonant Half-Bridge Power Converter*. This application note will not repeat the discussion of these details.

Figure 1 shows a typical block diagram of an LLC resonant converter.

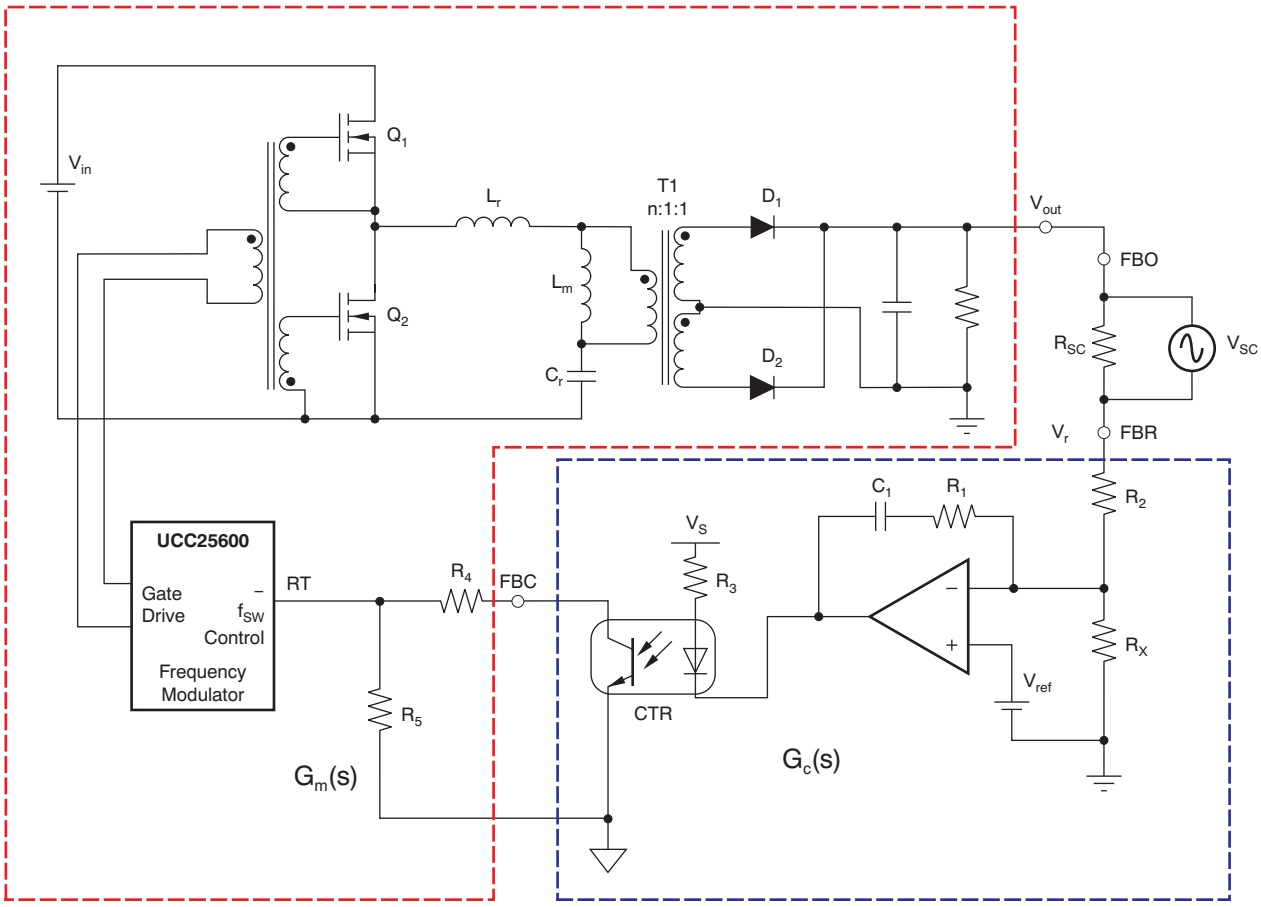

Figure 1. Block Diagram of a Typical LLC Resonant Half-Bridge Converter

This diagram consists of two blocks: the modulator and the compensator, expressed in the respective transfer functions of $G_m(s)$ and $G_c(s)$, or $G_m(j\omega)$ and $G_c(j\omega)$. In Figure 1, the red outline defines the $G_m(s)$ transfer function, and the blue outline defines the $G_c(s)$ transfer function.

$G_m(\omega)$ and $G_c(\omega)$ can be used to express $G_m(j\omega)$ and $G_c(j\omega)$ respectively in shorthand, where $j = \sqrt{-1}$ can be omitted without confusion. Then the loop gain transfer function $G_{lp}(s)$, or $G_{lp}(\omega)$, is expressed as Equation 1.

$$G_{lp}(s) = \frac{V_{out}(s)}{V_r(s)} = G_c(s) \bullet G_m(s) \quad (1)$$

or as Equation 2:

$$G_{lp}(\omega) = \frac{V_{out}(\omega)}{V_r(\omega)} = G_c(\omega) \bullet G_m(\omega) \quad (2)$$

Both $G_m(\omega)$ and $G_c(\omega)$ can be measured with a frequency sweeping signal applied on resistor R_{SC}, as these equations show:

$$G_m(\omega) = \frac{FBO}{FBC} \tag{3}$$

$$G_c(\omega) = \frac{FBC}{FBR} \tag{4}$$

The loop gain transfer function $G_{lp}(\omega)$ is measurable and obtained as Equation 5.

$$G_{lp}(\omega) = \frac{FBO}{FBR} \tag{5}$$

It is obvious that FBC can be assigned at different locations in the converter circuit. For example, it can be moved to the optocoupler input as Figure 2 illustrates. Here, the red area and the blue area represent the $G_m(\omega)$ and $G_c(\omega)$ functions, respectively, as they do in Figure 1.

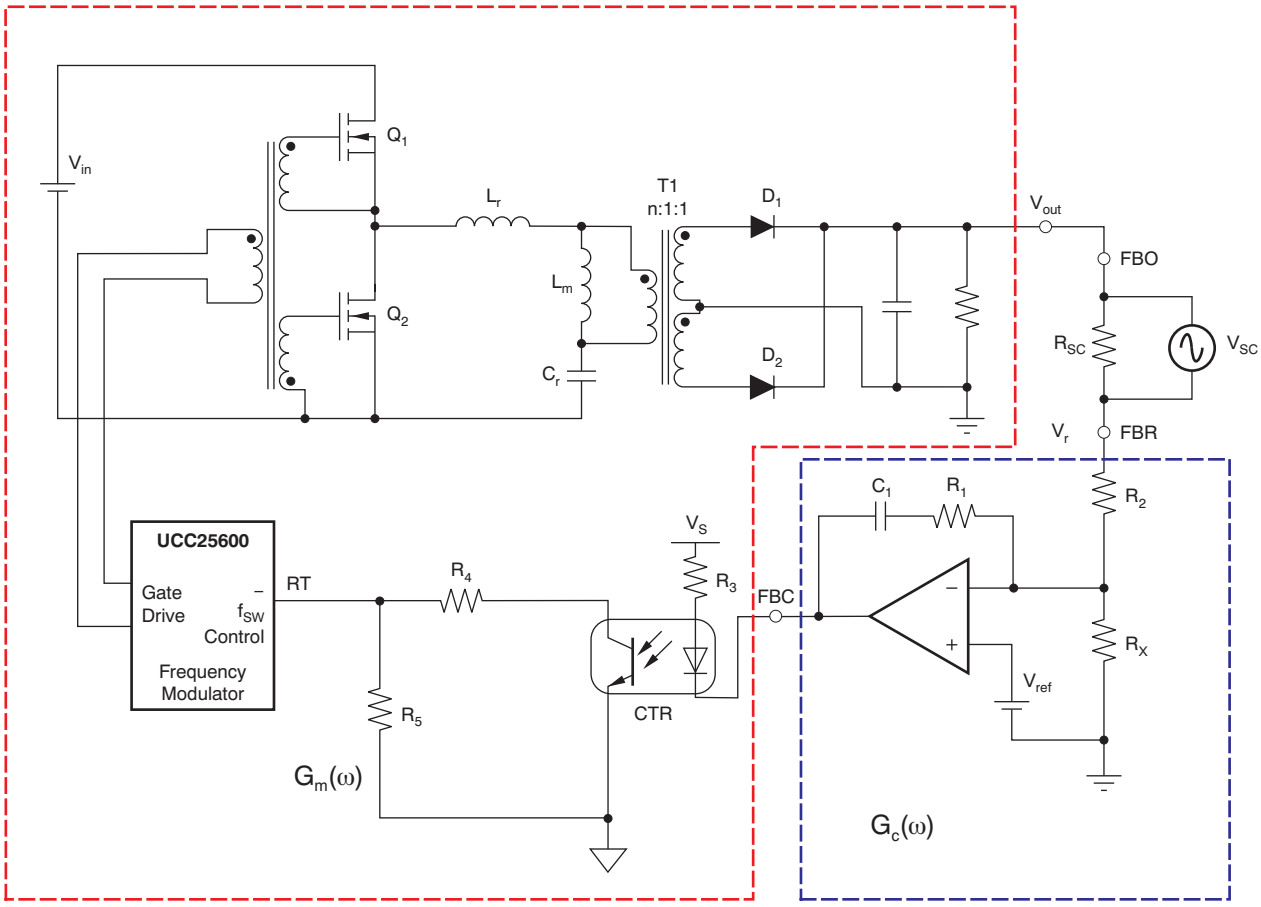

Figure 2. Another Way to Define $G_m(\omega)$ and $G_c(\omega)$

In this position, then, the measured $G_m(\omega)$ and $G_c(\omega)$ are different from those measured in Figure 1.

Note that it is possible to define $G_m(\omega)$ and $G_c(\omega)$ in several different ways. But $G_{lp}(\omega)$ will be the same, regardless of how $G_m(\omega)$ and $G_c(\omega)$ are defined. In this document, we use the definition as shown in Figure 1 to avoid confusion.

2 Loop Compensation Design Approach

Unlike $G_m(\omega)$, $G_c(\omega)$ can be expressed analytically. As shown in Figure 1, if we use Type I compensation, then $G_c(\omega)$ is expressed as Equation 6:

$$G_c(s) = \frac{\frac{s}{\frac{1}{R1 \bullet C1}} + 1}{\frac{s}{\omega_I} \bullet \left(\frac{s}{\omega_{p\_opto}} + 1\right)} \tag{6}$$

Where ω_{p_opto} is the angular frequency of the optocoupler frequency-domain pole. This value can be typically considered to be approximately $\omega_{p\_opto} = 2\pi \times 10$ kHz, although the value varies with the particular optocoupler in the circuit as well as with the bias point. *CTR* is the optocoupler current transfer ratio; the angular frequency ω_I is the gain of the frequency domain pole at origin; and therefore, we arrive at:

$$\omega_I = \frac{R_4 \bullet CTR}{R_3 \bullet R_2 \bullet C_1} \tag{7}$$

The angular frequency ω_I is the 0-dB crossover of $G_c(\omega)$ when we set $R_1 = 0$ and ignore ω_{p_opto} at a low-frequency range. In fact:

$$G_c(s) = \frac{\frac{j\omega}{\frac{1}{R1 \bullet C1}} + 1}{\frac{j\omega}{\omega_I} \bullet \left(\frac{j\omega}{\omega_{p\_opto}} + 1\right)} \quad \text{with: } R1 = 0,\ \omega << \omega_{p\_opto} \longrightarrow G_c(\omega) = \frac{1}{\frac{j\omega}{\omega_I}} = \frac{\omega_I}{j\omega} \tag{8}$$

If we let $|G_c(\omega)| = 1$, then:

$$|G_c(\omega)| = \left|\frac{\omega_I}{j\omega}\right| = 1 \rightarrow \omega = \omega_I \tag{9}$$

To compensate the LLC converter feedback loop, $G_m(\omega)$ must first be obtained by measurement. To make $G_m(\omega)$ measurable, the feedback loop must be stable, which is our design goal yet to be achieved. So we are now in a circle that we must break in order to achieve our design goal. To break this circle, one common technique is to use a large-value capacitor for C_1 in Figure 1 to push the loop bandwidth (that is, the gain crossover frequency) low enough in the expectation that the loop can be *stable* enough for initial measurement. This idea is workable and allows us to obtain initial $G_m(\omega)$ value. Sometimes, though, we may be confused about how large a capacitor is adequate for a specific application in order to make a stable $G_m(\omega)$ measurement. If an estimated C_1 value is not sufficient, we have a potential risk that the resulting loop may not be stable to measure $G_m(\omega)$, and potential circuit damage can occur.

To avoid these issues, we propose a more reliable approach that combines with the practice of using an initial low bandwidth measurement from a large value C_1. As we know, to maintain output voltage regulation in an LLC resonant converter, the input voltage must be great enough to achieve the desired output voltage. If the input voltage is not sufficient, the output voltage regulation cannot be achieved because the maximum gain has already reached its limit. However, even if output regulation is not achieved, the converter is stable, and this stability is not related to the feedback loop parameters. During such an operation, bench tests show a $G_m(\omega)$ can continue to be measured in the usual way. Although the measured $G_m(\omega)$ is not exactly the same as that obtained from an operation when the output comes into regulation, it is sufficient to give us an idea of how large the value of C_1 must be and how ω_I should be designed. Then, we will be able to complete the remaining design and avoid the risks noted earlier.

3 Methodology

To implement this approach, we first must make sure that all other segments of the converter work properly, especially the associated power stage. This operation is usually called an *open-loop test*, which must be passed to assure full functionality. Then we can close the feedback loop and measure $G_c(\omega)$ in this way:

- We first increase the input voltage slowly from zero and observe the output voltage.

  Because the input voltage is low, the controller in the feedback loop will generate the maximum gain to raise the output voltage as much to the point of regulation as it can.
- We then continue to increase the input voltage until the output voltage is close to the regulation (within 10%). At that point, we stop increasing the input voltage.

  The converter should now be stable and quite independent of the feedback loop compensation parameters.
- Then, we apply a frequency sweeping signal to R_{SC} and measure the Bode plots between FBO and FBC. This measurement gives us the initial $G_m(\omega)$ value.

We can make several more measurements by further increasing the input voltage in 1% increments if $G_m(\omega)$ does not show good measurement results. However, do ***not*** risk increasing the voltage to bring the output voltage into regulation yet.

Here, we offer an example to show how to make this type of initial $G_m(\omega)$ measurement, then how to design the subsequent feedback loop once the measurement is complete. We use the UCC25600EVM-341 as our example with the corresponding circuit diagram shown in Figure 1. Complete schematics for this device are found in the UCC25600EVM-341 User Guide.

This converter has these electrical specifications:

- Input voltage: 375 V_{DC} to 405 V_{DC}
- Output power (rated): 300 W
- Output voltage: 12 V_{DC}
- Output current (rated): 25 A
- Output voltage line regulation (with I_O = 1.0 A): ≤ 1%
- Output voltage load regulation (at V_{IN} = 390 V): ≤ 1%
- Output voltage peak-to-peak ripple (at V_{IN} = 390 V and I_O = 25 A): ≤ 120 mV
- Efficiency (at V_{IN} = 390 V and I_O = 25 A): ≥ 90%
- Switching frequency: 70 kHz to 150 kHz in normal operation
- Converter topology: LLC resonant half-bridge converter

3.1 Procedure and Results

Step 1. **$G_m(\omega)$ measurement; C_1 initial value.**

In the expression:

$$\omega_I = \frac{R_4 \bullet CTR}{R_3 \bullet R_2 \bullet C_1} \tag{10}$$

C_1 is only the parameter we must determine initially for a stable $G_m(\omega)$ measurement. The remaining parameters are determined by other design factors and generally have a limited adjustable range. For example, CTR is fixed after an optocoupler is selected. Additionally, R_3 and R_4 are determined by the requirements of the frequency range and the optocoupler configuration.

The value of C_1 is not critical from our proposed approach. For example, an initial C_1 value can be between 0.1 μF and 1 μF; this range is given only to show some commonly-used values. If C_1 is outside these values, the process should work. In this example, we use C_1 = 1.0 μF (note that it does not make much difference to use C_1 = 0.1 μF).

Step 2. **$G_m(\omega)$ measurement with output voltage not in regulation.**

As shown in Step 1, the output voltage regulation is 12 V with minimum input voltage 375 V. If we use a voltage much lower than 375 V, the output voltage is not able to enter regulation. A good rule of thumb is to use an input voltage low enough to keep the output voltage out of regulation, but close to

the regulation voltage; say, within 10%. This technique generally should give an acceptable measurement. If it does not, a value closer to regulation may be tested, using a 1% increment each time until a good measurement is obtained. In this example, when we slowly increase V_{IN} to 285 V with I_O = 1 A, the output voltage showed to be approximately 11 V, which is 8.3% below 12 V. Then we measured $G_m(\omega)$ with an acceptable result. A 25-mV frequency sweeping signal was used during this test. The $G_m(\omega)$ measurement is shown in Figure 3.

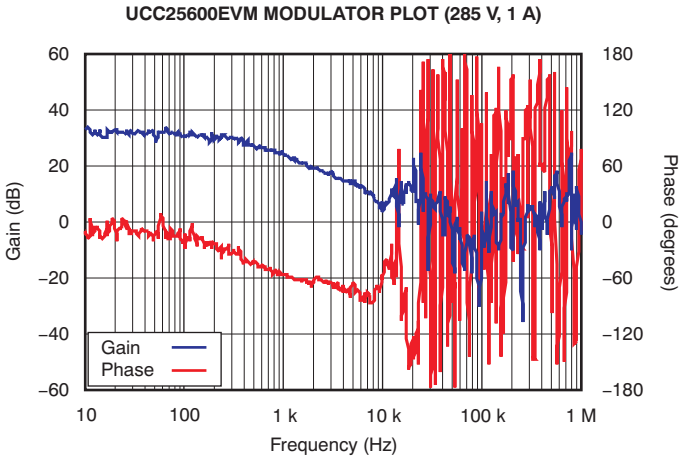

Figure 3. Initial $G_m(\omega)$ Measurement

Step 3. **Determine initial $G_c(\omega)$ based on $G_m(\omega)$ measurement.**

Now we need to design a proper $G_c(\omega)$ to allow the converter output to enter into regulation. The minimum switching frequency of the converter is specified at 70 kHz. As a rule of thumb, the gain crossover frequency should be below one-fifth of its minimum switching frequency. If we use one-tenth of its minimum switching frequency, that allows approximately 7 kHz to cover the entire operating range. Keep in mind, though, that we are only at the beginning stages and our primary purpose is to establish an initial operating point. The $G_m(\omega)$ obtained so far is also a very preliminary value. As such, we may want to make the target crossover frequency very conservative. Based on the measurement just obtained, it appears acceptable to set the crossover frequency somewhere around 100 Hz. One advantage to selecting 100 Hz is that it has a flat phase angle close to 0°; this response helps to achieve the desired stability as a 90° phase margin can be expected at 100 Hz. Notice, again, this target is only an initial design; the final desired value can be adjusted further.

At 100 Hz, $|G_m(\omega)|$ = 28 dB. Therefore, we would need to design $|G_c(\omega)|$ to have:

$$20\log(|G_c(\omega)|)_{\omega = 2\pi \times 100Hz} = -28\ dB$$

Because the crossover frequency of 100 Hz is a rough number to be used initially, we can simply do a quick design with only ω_I while leaving out the zero of R_1-C_1 by making R_1 = 0, such that the zero of R_1-C_1 is pushed beyond its effect to the 100-Hz crossover.

$$\omega_I = 10^{\frac{-28}{20}} \bullet 2\pi \bullet 100(Hz) = 25.0\ rad/s \tag{11}$$

$$\omega_I = \frac{R_4 \bullet CTR}{R_3 \bullet R_2 \bullet C_1} \tag{12}$$

If C_1 = 0.22 µF, we can obtain a ω_I =25.0 rad/s, or f_I = 3.98 Hz, with a given CTR = 120%, R_4 = 510 Ω, R_2 = 110 kΩ, and R_3 = 1.00 kΩ.

Step 4. **Re-measurement of $G_m(\omega)$.**

Now we are confident enough to increase the input voltage so the output is in regulation, and then make a stable measurement of $G_m(\omega)$. The measured $G_m(\omega)$ is shown in Figure 4, at 390-V input.

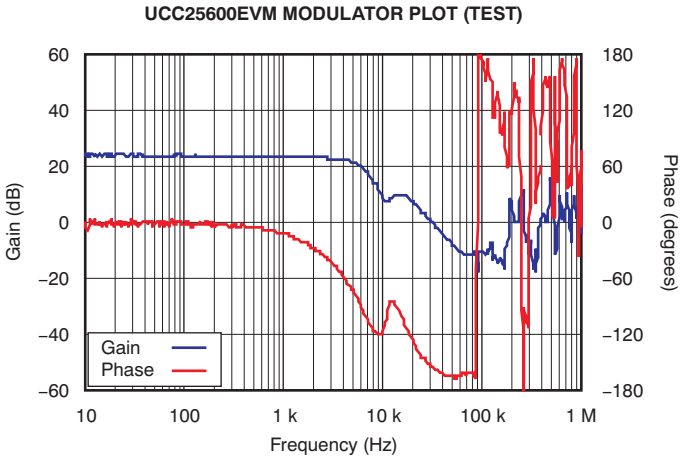

Figure 4. Re-Measurement of $G_m(\omega)$

Certainly, one can make additional measurements between 280 V and 390 V, say in 20-V increments, to gain confidence in what has already been obtained. An important note for test manipulation here is that the input voltage increase should progress slowly until the feedback loop compensation is complete. A slow increase of the input voltage can allow time for the designer to decide to stop if there is any sign that the feedback loop may become unstable.

Step 5. **Design $G_c(\omega)$ based on measured $G_m(\omega)$.**

To achieve the crossover frequency of 7 kHz with a minimum 45° phase margin, $G_c(\omega)$ would need to be designed to achieve the Bode plot responses shown in Figure 5. This result can be easily accomplished by arranging the pole and the zero shown in Equation 6. Below is one possible set of parameters to achieve the illustrated Bode plots:

- R_1 = 5.1 kΩ
- R_2 = 19.7 kΩ
- R_3 = 1.0 kΩ
- R_4 = 510 Ω
- C_1 = 0.22 µF
- CTR = 120%

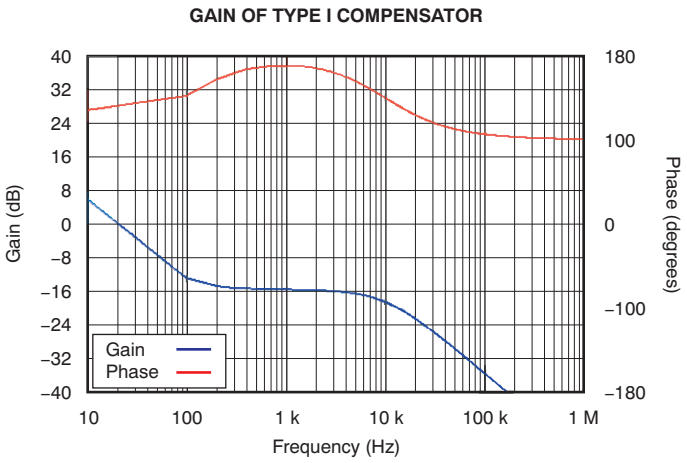

Figure 5. Design of $G_c(\omega)$

Step 6. **Bench testing and fine tuning.**

The last step is to plug in the obtained parameter values to perform a bench test. Usually, fine tuning is necessary to cover all operating conditions and to adapt to the parameters not modeled in the $G_c(\omega)$ for example parasitic variables.

The compensation values are finalized as R_1=17.8 kΩ, R_2 = 19.7 kΩ, R_3 = 1.0 kΩ, R_4 = 0.51 kΩ, and C_1 = 47 nF. Figure 6 shows the control loop Bode plots at V_{IN} = 390 V, V_o = 12 V, and a 25-A load.

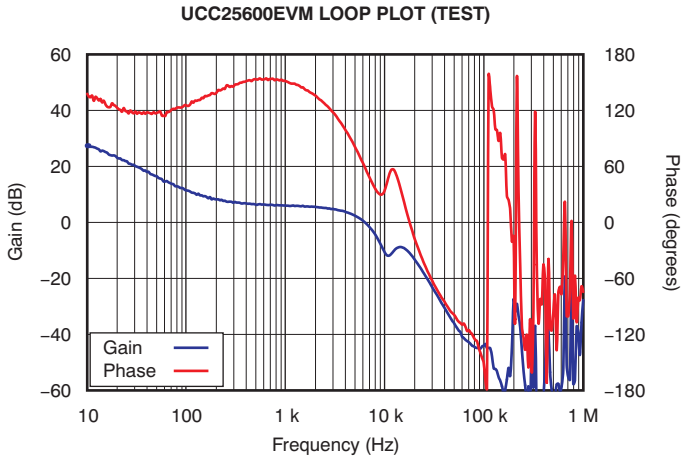

Figure 6. Feedback Loop Bode Plots After Final Values Set

4 References

Unless otherwise noted, these documents are available for download from the TI website (www.ti.com).

1. UCC25600 Product data sheet. Texas Instruments literature number SLUS846.
2. UCC25600EVM User guide. Texas Instruments literature number SLUU361.
3. TI Power Supply Design Seminar SEM1900 Topic 3, *Designing an LLC Resonant Half-Bridge Power Converter*. (2010-11). Texas Instruments literature number SLUP252.

Revision History

Changes from Original (October, 2010) to A Revision	Page
• Corrected Figure 1	2
• Updated Figure 2	3
• Replaced Figure 6	8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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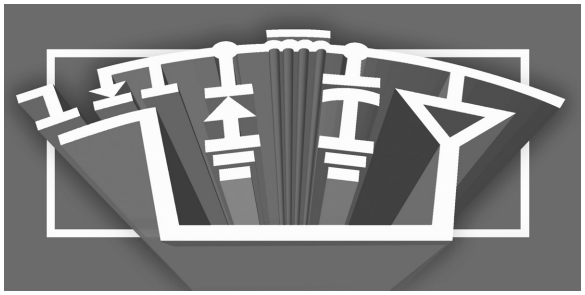

Power Supply Design Seminar

Designing an LLC Resonant Half-Bridge Power Converter

Topic Category:
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Designing an LLC Resonant Half-Bridge Power Converter

Hong Huang

ABSTRACT

While half-bridge power stages have commonly been used for isolated, medium-power applications, converters with high-voltage inputs are often designed with resonant switching to achieve higher efficiency, an improvement that comes with added complexity but that nevertheless offers several performance benefits. This topic provides detailed information on designing a resonant half-bridge converter that uses two inductors (LL) and a capacitor (C), known as an LLC configuration. This topic also introduces a unique analysis tool called first harmonic approximation (FHA) for controlling frequency modulation. FHA is used to define circuit parameters and predict performance, which is then verified through comprehensive laboratory measurements.

INTRODUCTION

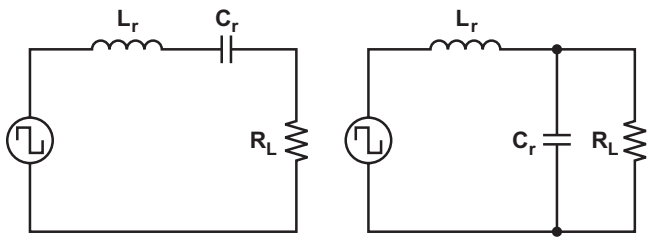
Higher efficiency, higher power density, and higher component density have become common in power-supply designs and their applications. Resonant power converters—especially those with an LLC half-bridge configuration—are receiving renewed interest because of this trend and the potential of these converters to achieve both higher switching frequencies and lower switching losses. However, designing such converters presents many challenges, among them the fact that the LLC resonant half-bridge converter performs power conversion with frequency modulation instead of pulse-width modulation, requiring a different design approach.

This topic presents a design procedure for the LLC resonant half-bridge converter, beginning with a brief review of basic resonant-converter operation and a description of the energy-transfer function as an essential requirement for the design process. This energy-transfer function, presented as a voltage ratio or voltage-gain function, is used along with resonant-circuit parameters to describe the relationship between input voltage and output voltage. Next, a method for determining parameter values is explained. To demonstrate how a design is created, a step-by-step example is then presented for a converter with 300 W of output power, a 390-VDC input, and a 12-VDC output. The topic concludes with the results of bench-tested performance measurements.

A. Brief Review of Resonant Converters

There are many resonant-converter topologies, and they all operate in essentially the same way: A square pulse of voltage or current generated by the power switches is applied to a resonant circuit. Energy circulates in the resonant circuit, and some or all of it is then tapped off to supply the output. More detailed descriptions and discussions can be found in this topic's references.

Among resonant converters, two basic types are the series resonant converter (SRC), shown in Fig. 1a, and the parallel resonant converter (PRC), shown in Fig. 1b. Both of these converters regulate their output voltage by changing the frequency of the driving voltage such that the impedance of the resonant circuit changes. The input voltage is split between this impedance and the load. Since the SRC works as a voltage divider between the input and the load, the DC gain of an SRC is always



a. Series resonant converter. *b. Parallel resonant converter.*

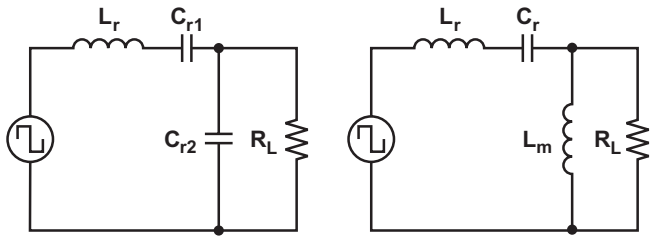
Fig. 1. Basic resonant-converter configurations.

lower than 1. Under light-load conditions, the impedance of the load is very large compared to the impedance of the resonant circuit; so it becomes difficult to regulate the output, since this requires the frequency to approach infinity as the load approaches zero. Even at nominal loads, wide frequency variation is required to regulate the output when there is a large input-voltage range.

In the PRC shown in Fig. 1b, the load is connected in parallel with the resonant circuit, inevitability requiring large amounts of circulating current. This makes it difficult to apply parallel resonant topologies in applications with high power density or large load variations.

B. LCC and LLC Resonant Converters

To solve these limitations, a converter combining the series and parallel configurations, called a series-parallel resonant converter (SPRC), has been proposed. One version of this structure uses one inductor and two capacitors, or an LCC configuration, as shown in Fig. 2a. Although this combination overcomes the drawbacks of a simple SRC or PRC by embedding more resonant frequencies, it requires two independent physical capacitors that are both large and expensive because of the high AC currents. To get similar characteristics without changing the physical component count, the SPRC can be altered to use two inductors and one capacitor, forming an LLC resonant converter (Fig. 2b). An advantage of the LLC over the LCC topology is that the two physical inductors can often be integrated into one physical component, including both the series resonant



a. LCC configuration. *b. LLC configuration.*

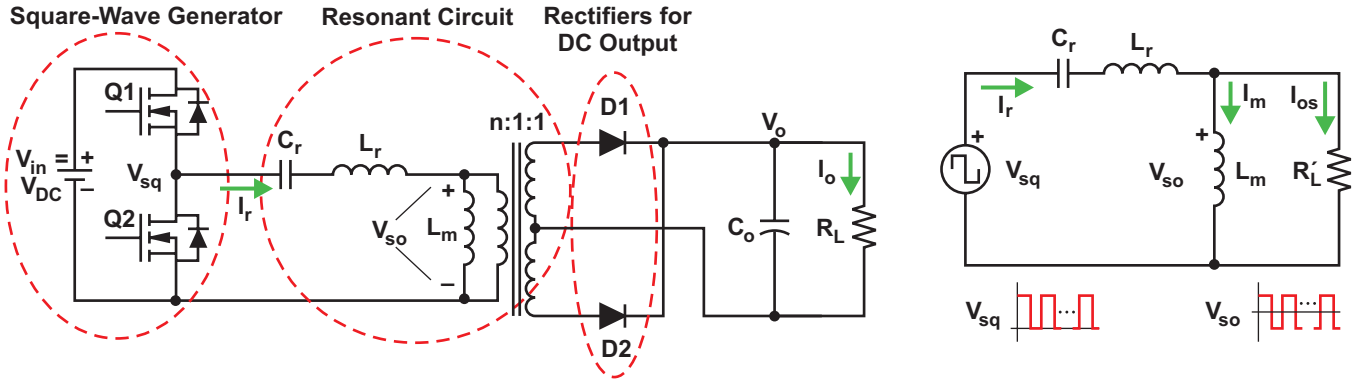
Fig. 2. Two types of SPRC.

inductance, L_r, and the transformer's magnetizing inductance, L_m.

The LLC resonant converter has many additional benefits over conventional resonant converters. For example, it can regulate the output over wide line and load variations with a relatively small variation of switching frequency, while maintaining excellent efficiency. It can also achieve zero-voltage switching (ZVS) over the entire operating range. Using the LLC resonant configuration in an isolated half-bridge topology will be described next, followed by the procedure for designing this topology.

II. LLC Resonant Half-Bridge Converter

This section describes a typical isolated LLC resonant half-bridge converter; its operation; its circuit modeling with simplifications; and the relationship between the input and output voltages, called the voltage-gain function. This voltage-gain function forms the basis for the design procedure described in this topic.



a. Typical configuration. *b. Simplified converter circuit.*

Fig. 3. LLC resonant half-bridge converter.

A. Configuration

Fig. 3a shows a typical topology of an LLC resonant half-bridge converter. This circuit is very similar to that in Fig. 2b. For convenience, Fig. 2b is copied as Fig. 3b with the series elements interchanged, so that a side-by-side comparison with Fig. 3a can be made. The converter configuration in Fig. 3a has three main parts:

1. Power switches Q1 and Q2, which are usually MOSFETs, are configured to form a square-wave generator. This generator produces a unipolar square-wave voltage, V_{sq}, by driving switches Q1 and Q2, with alternating 50% duty cycles for each switch. A small dead time is needed between the consecutive transitions, both to prevent the possibility of cross-conduction and to allow time for ZVS to be achieved.
2. The resonant circuit, also called a resonant network, consists of the resonant capacitance, C_r, and two inductances—the series resonant inductance, L_r, and the transformer's magnetizing inductance, L_m. The transformer turns ratio is n. The resonant network circulates the electric current and, as a result, the energy is circulated and delivered to the load through the transformer. The transformer's primary winding receives a bipolar square-wave voltage, V_{so}. This voltage is transferred to the secondary side, with the transformer providing both electrical isolation and the turns ratio to deliver the required voltage level to the output. In Fig. 3b, the load R_L' includes the load R_L of Fig. 3a together with the losses from the transformer and output rectifiers.
3. On the converter's secondary side, two diodes constitute a full-wave rectifier to convert AC input to DC output and supply the load R_L. The output capacitor smooths the rectified voltage and current. The rectifier network can be implemented as a full-wave bridge or center-tapped configuration, with a capacitive output filter. The rectifiers can also be implemented with MOSFETs forming synchronous rectification to reduce conduction losses, especially beneficial in low-voltage and high-current applications.

B. Operation

This section provides a review of LLC resonant-converter operation, starting with series resonance.

Resonant Frequencies in an SRC

Fundamentally, the resonant network of an SRC presents a minimum impedance to the sinusoidal current at the resonant frequency, regardless of the frequency of the square-wave voltage applied at the input. This is sometimes called the resonant circuit's selective property. Away from resonance, the circuit presents higher impedance levels. The amount of current, or associated energy, to be circulated and delivered to the load is then mainly dependent upon the value of the resonant circuit's impedance at that frequency for a given load impedance. As the frequency of the square-wave generator is varied,

the resonant circuit's impedance varies to control that portion of energy delivered to the load.

An SRC has only one resonance, the series resonant frequency, denoted as

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}. \quad (1)$$

The circuit's frequency at peak resonance, f_{c0}, is always equal to its f_0. Because of this, an SRC requires a wide frequency variation in order to accommodate input and output variations.

f_{c0}, f_0, and f_p in an LLC Circuit

However, the LLC circuit is different. After the second inductance (L_m) is added, the LLC circuit's frequency at peak resonance (f_{c0}) becomes a function of load, moving within the range of $f_p \le f_{c0} \le f_0$ as the load changes. f_0 is still described by Equation (1), and the pole frequency is described by

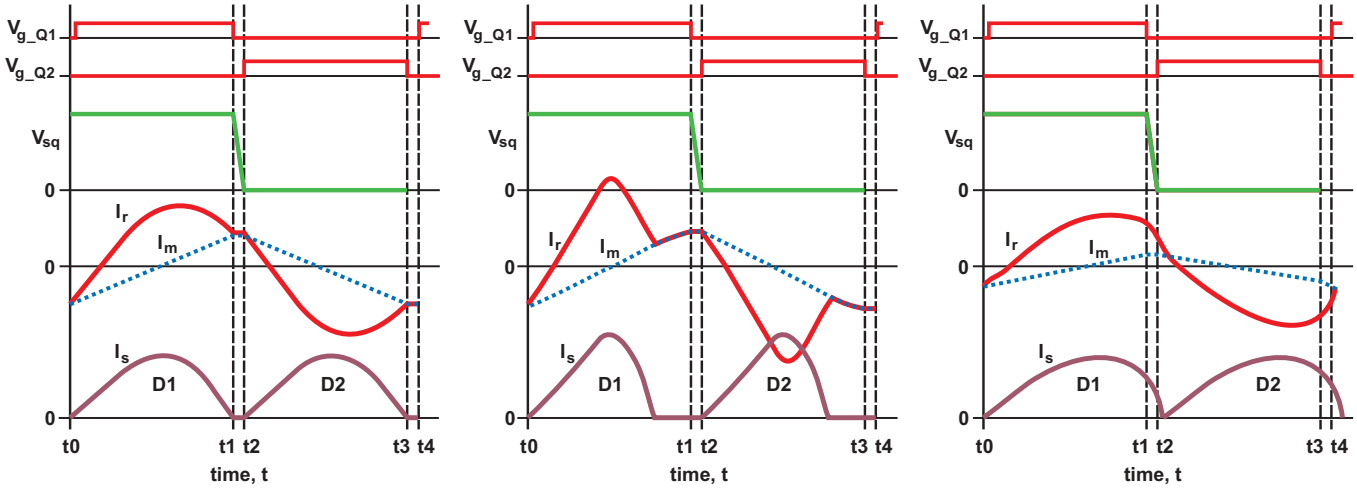
$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}. \quad (2)$$

At no load, $f_{c0} = f_p$. As the load increases, f_{c0} moves towards f_0. At a load short circuit, $f_{c0} = f_0$. Hence, LLC impedance adjustment follows a family of curves with $f_p \le f_{c0} \le f_0$, unlike that in SRC, where a single curve defines $f_{c0} = f_0$. This helps to reduce the frequency range required from an LLC resonant converter but complicates the circuit analysis.

It is apparent from Fig. 3b that f_0 as described by Equation (1) is always true regardless of the load, but f_p described by Equation (2) is true only at no load. Later it will be shown that most of the time an LLC converter is designed to operate in the vicinity of f_0. For this reason and others yet to be explained, f_0 is a critical factor for the converter's operation and design.

Operation At, Below, and Above f_0

The operation of an LLC resonant converter may be characterized by the relationship of the switching frequency, denoted as f_{sw}, to the series resonant frequency (f_0). Fig. 4 illustrates the typical waveforms of an LLC resonant converter with the switching frequency at, below, or above the series resonant frequency. The graphs show, from top to bottom, the Q1 gate (V_{g_Q1}), the Q2 gate (V_{g_Q2}), the switch-node voltage (V_{sq}), the resonant circuit's current (I_r), the magnetizing current (I_m), and the secondary-side diode current (I_s). Note that the primary-side current is the sum of the magnetizing current and the secondary-side current referred to the primary; but, since the magnetizing current flows only in the primary side, it does not contribute to the power transferred from the primary-side source to the secondary-side load.



a. At f_0. *b. Below f_0.* *c. Above f_0.*

Fig. 4. Operation of LLC resonant converter.

Operation at Resonance (Fig. 4a)

In this mode the switching frequency is the same as the series resonant frequency. When switch Q1 turns off, the resonant current falls to the value of the magnetizing current, and there is no further transfer of power to the secondary side. By delaying the turn-on time of switch Q2, the circuit achieves primary-side ZVS and obtains a soft commutation of the rectifier diodes on the secondary side. The design conditions for achieving ZVS will be discussed later. However, it is obvious that operation at series resonance produces only a single point of operation. To cover both input and output variations, the switching frequency will have to be adjusted away from resonance.

Operation Below Resonance (Fig. 4b)

Here the resonant current has fallen to the value of the magnetizing current before the end of the driving pulse width, causing the power transfer to cease even though the magnetizing current continues. Operation below the series resonant frequency can still achieve primary ZVS and obtain the soft commutation of the rectifier diodes on the secondary side. The secondary-side diodes are in discontinuous current mode and require more circulating current in the resonant circuit to deliver the same amount of energy to the load. This additional current results in higher conduction losses in both the primary and the secondary sides. However, one characteristic that should be noted is that the primary ZVS may be lost if the switching frequency becomes too low. This will result in high switching losses and several associated issues. This will be explained further later.

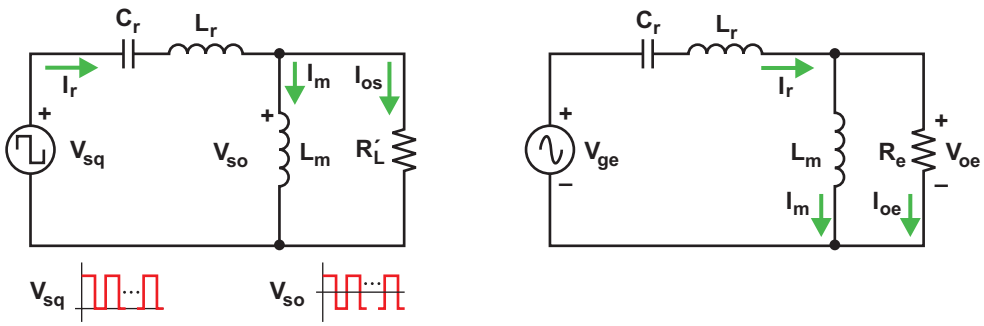
Operation Above Resonance (Fig. 4c)

In this mode the primary side presents a smaller circulating current in the resonant circuit. This reduces conduction loss because the resonant circuit's current is in continuous-current mode, resulting in less RMS current for the same amount of load. The rectifier diodes are not softly commutated and reverse recovery losses exist, but operation above the resonant frequency can still achieve primary ZVS. Operation above the resonant frequency may cause significant frequency increases under light-load conditions.

The foregoing discussion has shown that the converter can be designed by using either $f_{sw} \geq f_0$ or $f_{sw} \leq f_0$, or by varying f_{sw} on either side around f_0. Further discussion will show that the best operation exists in the vicinity of the series resonant frequency, where the benefits of the LLC converter are maximized. This will be the design goal.

C. Modeling an LLC Half-Bridge Converter

To design a converter for variable-energy transfer and output-voltage regulation, a voltage-transfer function is a must. This transfer function, which in this topic is also called the input-to-output voltage gain, is the mathematical relationship between the input and output voltages. This section will show how the gain formula is developed and what the characteristics of the gain are. Later the gain formula obtained will be used to describe the design procedure for the LLC resonant half-bridge converter.



a. Nonlinear nonsinusoidal circuit. *b. Linear sinusoidal circuit.*

Fig. 5. Model of LLC resonant half-bridge converter.

Traditional Modeling Methods Do Not Work Well

To develop a transfer function, all variables should be defined by equations governed by the LLC converter topology shown in Fig. 5a. These equations are then solved to get the transfer function. Conventional methods such as state-space averaging have been successfully used in modeling pulse-width-modulated switching converters, but from a practical viewpoint they have proved unsuccessful with resonant converters, forcing designers to seek different approaches.

Modeling with Approximations

As already mentioned, the LLC converter is operated in the vicinity of series resonance. This means that the main composite of circulating current in the resonant network is at or close to the series resonant frequency. This provides a hint that the circulating current consists mainly of a single frequency and is a pure sinusoidal current. Although this assumption is not completely accurate, it is close—especially when the square wave's switching cycle corresponds to the series resonant frequency. But what about the errors?

If the square wave is different from the series resonance, then in reality more frequency components are included; but an approximation using the single fundamental harmonic of the square wave can be made while ignoring all higher-order harmonics and setting possible accuracy issues aside for the moment. This is the so-called first harmonic approximation (FHA) method, now widely used for resonant-converter design. This method produces acceptable design results as long as the converter operates at or close to the series resonance.

The FHA method can be used to develop the gain, or the input-to-output voltage-transfer function. The first steps in this process are as follows:

- Represent the primary-input unipolar square-wave voltage and current with their fundamental components, ignoring all higher-order harmonics.
- Ignore the effect from the output capacitor and the transformer's secondary-side leakage inductance.
- Refer the obtained secondary-side variables to the primary side.
- Represent the referred secondary voltage, which is the bipolar square-wave voltage (V_{so}), and the referred secondary current with only their fundamental components, again ignoring all higher-order harmonics.

With these steps accomplished, a circuit model of the LLC resonant half-bridge converter in Fig. 5a can be obtained (Fig. 5b). In Fig. 5b, V_{ge} is the fundamental component of V_{sq}, and V_{oe} is the fundamental component of V_{so}. Thus, the nonlinear and nonsinusoidal circuit in Fig. 5a is approximately transformed into the linear circuit of Fig. 5b, where the AC resonant circuit is excited by an effective sinusoidal input source and drives an equivalent resistive load. In this circuit model, both input voltage V_{ge} and output voltage V_{oe} are in sinusoidal form with the same single frequency—i.e., the fundamental component of the square-wave voltage (V_{sq}), generated by the switching operation of Q1 and Q2.

This model is called the resonant converter's FHA circuit model. It forms the basis for the

design example presented in this topic. The voltage-transfer function, or the voltage gain, is also derived from this model, and the next section will show how. Before that, however, the electrical variables and their relationships as used in Fig. 5b need to be obtained.

Relationship of Electrical Variables

On the input side, the fundamental voltage of the square-wave voltage (V_{sq}) is

$$v_{ge}(t) = \frac{2}{\pi} \times V_{DC} \times \sin(2\pi f_{sw} t), \quad (3)$$

and its RMS value is

$$V_{ge} = \frac{\sqrt{2}}{\pi} \times V_{DC}. \quad (4)$$

On the output side, since V_{so} is approximated as a square wave, the fundamental voltage is

$$v_{oe}(t) = \frac{4}{\pi} \times n \times V_o \times \sin(2\pi f_{sw} t - \varphi_V), \quad (5)$$

where φ_V is the phase angle between V_{oe} and V_{ge}, and the RMS output voltage is

$$V_{oe} = \frac{2\sqrt{2}}{\pi} \times n \times V_o. \quad (6)$$

The fundamental component of current corresponding to V_{oe} and I_{oe} is

$$i_{oe}(t) = \frac{\pi}{2} \times \frac{1}{n} \times I_o \times \sin(2\pi f_{sw} t - \varphi_i), \quad (7)$$

where φ_i is the phase angle between i_{oe} and v_{oe}, and the RMS output current is

$$I_{oe} = \frac{\pi}{2\sqrt{2}} \times \frac{1}{n} \times I_o. \quad (8)$$

Then the AC equivalent load resistance, R_e, can be calculated as

$$R_e = \frac{V_{oe}}{I_{oe}} = \frac{8 \times n^2}{\pi^2} \times \frac{V_o}{I_o} = \frac{8 \times n^2}{\pi^2} \times R_L. \quad (9)$$

Since the circuit in Fig. 5b is a single-frequency, sinusoidal AC circuit, the calculations can be made in the same way as for all sinusoidal circuits. The angular frequency is

$$\omega_{sw} = 2\pi f_{sw}, \quad (10)$$

which can be simplified as

$$\omega = \omega_{sw} = 2\pi f_{sw}. \quad (11)$$

The capacitive and inductive reactances of C_r, L_r, and L_m, respectively, are

$$X_{C_r} = \frac{1}{\omega C_r}, \; X_{L_r} = \omega L_r, \text{ and } X_{L_m} = \omega L_m. \quad (12)$$

The RMS magnetizing current is

$$I_m = \frac{V_{oe}}{\omega L_m} = \frac{2\sqrt{2}}{\pi} \times \frac{n \times V_o}{\omega L_m}. \quad (13)$$

The circulating current in the series resonant circuit is

$$I_r = \sqrt{I_m^2 + I_{oe}^2}. \quad (14)$$

With the relationships of the electrical variables established, the next step is to develop the voltage-gain function.

D. Voltage-Gain Function

Naturally, the relationship between the input voltage and output voltage can be described by their ratio or gain:

$$M_{g\_DC} = \frac{n \times V_o}{V_{in}/2} = \frac{n \times V_o}{V_{DC}/2} \quad (15)$$

As described earlier, the DC input voltage and output voltage are converted into switching mode, and then Equation (15) can be approximated as the ratio of the bipolar square-wave voltage (V_{so}) to the unipolar square-wave voltage (V_{sq}):

$$M_{g\_DC} \approx M_{g\_sw} = \frac{V_{so}}{V_{sq}} \quad (16)$$

The AC voltage ratio, M_{g_AC}, can be approximated by using the fundamental components, V_{ge} and V_{oe}, to respectively replace V_{sq} and V_{so} in Equation (16):

$$\begin{aligned} M_{g\_DC} &= \frac{n \times V_o}{V_{in}/2} \approx M_{g\_sw} \\ &= \frac{V_{so}}{V_{sq}} \approx M_{g\_AC} = \frac{V_{oe}}{V_{ge}} \end{aligned} \quad (17)$$

To simplify notation, M_g will be used here in place of M_{g_AC}. From Fig. 5b, the relationship between V_{oe} and V_{ge} can be expressed with the electrical parameters L_r, L_m, C_r, and R_e. Then the input-to-output voltage-gain or voltage-transfer function becomes

$$M_g = \frac{V_{oe}}{V_{ge}} = \left| \frac{jX_{L_m} \parallel R_e}{(jX_{L_m} \parallel R_e) + j(X_{L_r} - X_{C_r})} \right| = \left| \frac{(j\omega L_m) \parallel R_e}{(j\omega L_m) \parallel R_e + j\omega L_r + \frac{1}{j\omega C_r}} \right|, \quad (18)$$

where $j = \sqrt{-1}$.

Equation (18) depicts a connection from the input voltage (V_{in}) to the output voltage (V_o) established in relation to M_g with LLC-circuit parameters. Although this expression is only approximately correct, in practice it is close enough to the vicinity of series resonance. Accepting the approximation as accurate allows Equation (19) to be written:

$$V_o = M_g \times \frac{1}{n} \times \frac{V_{in}}{2}. \quad (19)$$

In other words, output voltage can be determined after M_g, n, and V_{in} are known.

Normalized Format of Voltage-Gain Function

The voltage-gain function described by Equation (18) is expressed in a format with absolute values. It is difficult to give a general description of design issues with such a format. It would be better to express it in a normalized format. To do this, the series resonant frequency (f_0) can be selected as the base for normalization. Then the normalized frequency is expressed as

$$f_n = \frac{f_{sw}}{f_0}. \quad (20)$$

Further, to combine two inductances into one, an inductance ratio can be defined as

$$L_n = \frac{L_m}{L_r}. \quad (21)$$

The quality factor of the series resonant circuit is defined as

$$Q_e = \frac{\sqrt{L_r / C_r}}{R_e}. \quad (22)$$

Notice that f_n, L_n, and Q_e are no-unit variables.

With the help of these definitions, the voltage-gain function can then be normalized and expressed as

$$M_g = \left| \frac{L_n \times f_n^2}{[(L_n + 1) \times f_n^2 - 1] + j[(f_n^2 - 1) \times f_n \times Q_e \times L_n]} \right|. \quad (23)$$

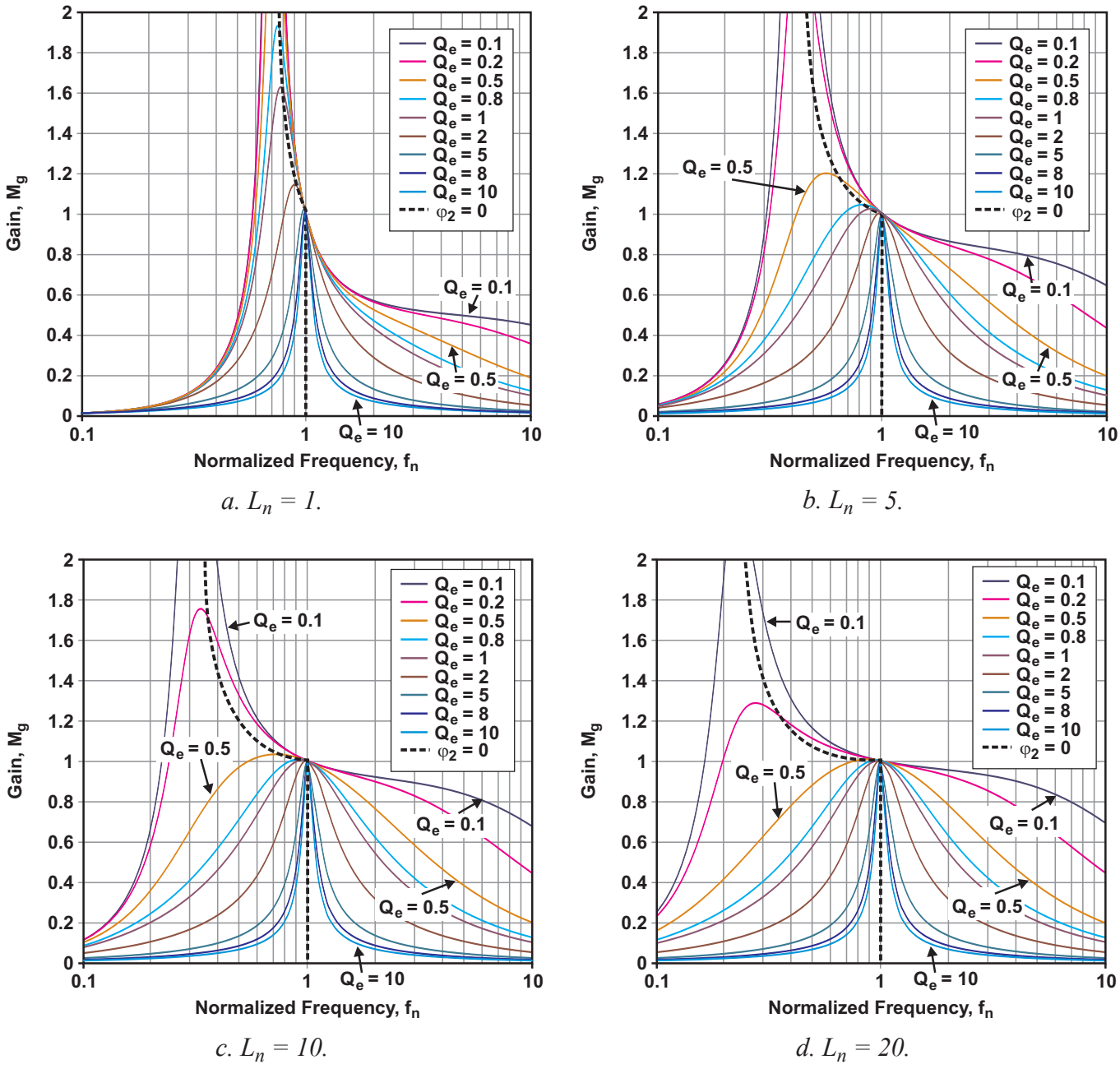
The relationship between input and output voltages can also be obtained from Equation (23):

$$V_o = M_g \times \frac{1}{n} \times \frac{V_{in}}{2} = M_g(f_n, L_n, Q_e) \times \frac{1}{n} \times \frac{V_{DC}}{2}, \quad (24)$$

where $V_{in} = V_{DC}$.

Behavior of the Voltage-Gain Function

The voltage-gain function expressed by Equation (23) and the circuit model in Fig. 5b form the basis for the design method described in this topic; therefore it is necessary to understand how M_g behaves as a function of the three factors f_n, L_n, and Q_e. In the gain function, frequency f_n is the control variable. L_n and Q_e are dummy variables, since they are fixed after their physical parameters are determined. M_g is adjusted by f_n after a design is complete. As such, a good way to explain how the gain function behaves is to plot M_g with respect to f_n at given conditions from a family of values for L_n and Q_e.



a. L_n = 1. *b. L_n = 5.*

c. L_n = 10. *d. L_n = 20.*

Fig. 6. Plots of voltage-gain function (M_g) with different values of L_n.

Figs. 6a to 6d illustrate several possible relationships. Each plot is defined by a fixed value for L_n (L_n = 1, 5, 10, or 20) and shows a family of curves with nine values, from 0.1 to 10, for the variable Q_e. From these plots, several observations can be made.

The value of M_g is not less than zero. This is obvious since M_g is from the modulus operator, which depicts a complex expression containing both real and imaginary numbers. These numbers represent both magnitude and phase angle, but only the magnitude is useful in this case.

Within a given L_n and Q_e, M_g presents a convex curve shape in the vicinity of the circuit's resonant frequency. This is a typical curve that shows the shape of the gain from a resonant converter. The normalized frequency corresponding to the resonant peak (f_{n_c0}, or $f_{sw} = f_{c0}$) is moving with respect to a change in load and thus to a change in Q_e for a given L_n.

Changing L_n and Q_e will reshape the M_g curve and make it different with respect to f_n. As Q_e is a function of load described by Equations (9) and (22), M_g presents a family of curves relating frequency modulation to variations in load.

Regardless of which combination of L_n and Q_e is used, all curves converge and go through the point of $(f_n, M_g) = (1, 1)$. This point is at $f_n = 1$, or $f_{sw} = f_0$ from Equation (20). By definition of series resonance, $X_{L_r} - X_{C_r} = 0$ at f_0. In other words, the voltage drop across L_r and C_r is zero, so that the input voltage is applied directly to the output load, resulting in a unity voltage gain of $M_g = 1$.

Notice that the operating point $(f_n, M_g) = (1, 1)$ is independent of the load; i.e., as long as the gain (M_g) can be kept as unity, the switching frequency will be at the series resonant frequency (f_0) no matter what the load current is. In other words, in a design whose operating point is at $(f_n, M_g) = (1, 1)$ or its vicinity, the frequency variation is narrowed down to minimal. At $(f_n, M_g) = (1, 1)$, the impedance of the series resonant circuit is zero, assuming there are no parasitic power losses. The entire input voltage is then applied to the output load no matter how much the load current varies. However, away from $(f_n, M_g) = (1, 1)$, the impedance of the series resonant circuit becomes nonzero, the voltage gain changes with different load impedances, and the corresponding operation becomes load-dependent.

For a fixed L_n, increasing Q_e shrinks the curve, resulting in a narrower frequency-control band, which is expected since Q_e is the quality factor of the series resonant circuit. In addition, as the whole curve shifts lower, the corresponding peak value of M_g becomes smaller, and the f_n corresponding to that value moves towards the right and closer to $f_n = 1$. This frequency shift with increasing Q_e is due to an increased load. It is apparent from reviewing Equations (9) and (22) that an increase in Q_e may come from a reduction in R_L, as both L_m and L_r are fixed. For the same series resonant frequency, C_r is fixed as well. R_L is in parallel with L_m, so reducing R_L will reduce the effect of L_m and shift f_{c0} towards f_0. As a simple illustration, it is helpful to examine two extremes:

1. If R_L is open, then $Q_e = 0$, and $f_{c0} = f_p$ as described by Equation (2). f_{c0} sits to the far left of f_0, and the corresponding gain peak is very high and can be infinite in theory.
2. If R_L is shorted, then $Q_e = \infty$ and L_m is completely bypassed or shorted, making the effect of L_m on the gain disappear. The corresponding peak gain value from the L_m effect then becomes zero, and f_{c0} moves all the way to the right, overlapping f_0.

   Therefore, if R_L changes from infinite to zero, the resonant peak gain changes from infinite to unity, and the corresponding frequency at peak resonance (f_{c0}) moves from f_p to the series resonant frequency (f_0).

For a fixed Q_e, a decrease in L_n shrinks the curve; the whole curve is squeezed, and f_{c0} moves towards f_0. This results in a better frequency-control band with a higher peak gain. There are two reasons for this. First, as L_n decreases due to the decrease in L_m, f_p gets closer to f_0, which squeezes the curves from f_p to f_0. Second, a decreased L_n increases L_r, resulting in a higher Q_e. A higher Q_e shrinks the curve as just described.

At first glance, it appears that any combination of L_n and Q_e would work for a converter design and that the design could be made with f_n operating on either side of $f_n = 1$. However, as explained in the following section, there are many more considerations.

III. Design Considerations

As discussed earlier, f_n is the control variable in frequency modulation. Therefore the output voltage can be regulated by M_g through controlling f_n, as indicated by Fig. 6 and Equation (24), which can be rearranged as

$$V_o = M_g(f_n, L_n, Q_e) \times \frac{1}{n} \times \frac{V_{in}}{2}. \qquad (25)$$

Although this discussion has so far determined that the design should operate in the vicinity of the series resonance, or near $f_n = 1$, it is recommended that the optimum design be restricted to the area described by a1 through a4 in Fig. 7, for reasons to be explained.

A. What Does "In the Vicinity" Mean?

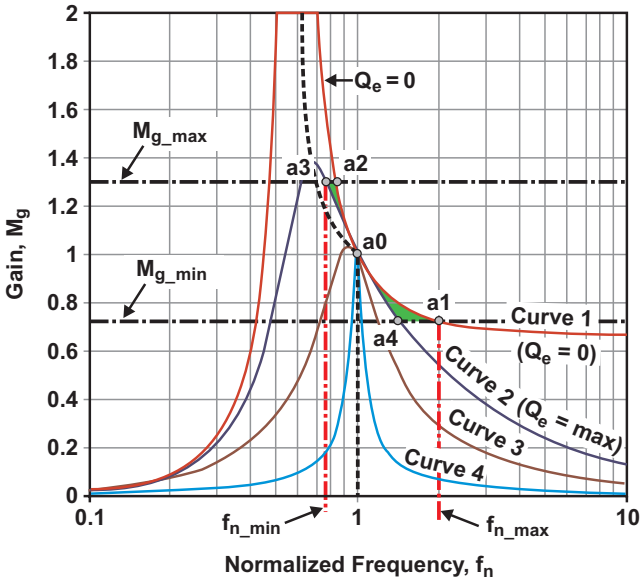
Obviously, "in the vicinity" is a loose designation; but, as stated before in the discussion of the FHA concept, if a pure sinusoidal current flowing through the resonant circuit is assumed, and if the circuit is made to operate at the exact location of f_0, then the design result is accurate. This can also be verified easily by a bench test or a computer simulation, but so far there is no verification in theory. A potential insight into such verification can be made through Equation (19). Assigning a value of 1 to M_g in Equation (19) as an indication of operation at $f_n = 1$ will remove the approximations made to Equation (17). A precise relationship is then achieved between the DC input and DC output as described by Equation (15).

A design that operates only at f_0 certainly cannot be made, but when it includes operating frequencies away from f_0, it starts to show errors when compared with bench-test measurements. So the common understanding in an FHA design approach is that it can help to create an initial design, with all design variables retaining their clear physical concepts and meanings, which is important in order for designers to understand the behavior of the LLC converter. However, it should be expected that some bench testing to optimize and finalize the design may be necessary. This could be an iterative process, but computer-based circuit simulation will save iteration cycles. As a matter of fact, computer simulation plays an important role in LLC-converter design after an initial design is made with the FHA approach.

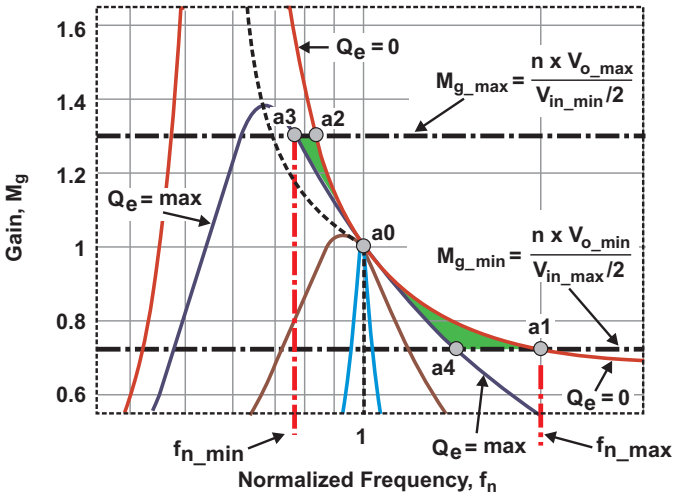
B. Basic Design Requirements

For a typical design of a power-supply converter, as is well-known, three basic requirements are almost always considered first—line regulation, load regulation, and efficiency.

Line regulation is defined as the maximum output-voltage variation caused by an input-voltage variation over a specified range, at a given output load current.



a. In the vicinity of series resonance (near $f_n = 1$).



b. Operation boundary set by a1 through a4.

Fig. 7. Recommended design area.

Load regulation is defined as the maximum output-voltage variation caused by a change in load over a stated range, usually from no load to maximum.

These two types of regulation are actually achieved through the voltage-gain adjustment—and in an LLC converter, the gain adjustment is made through frequency modulation. The recommended area of operation described in Fig. 7 shows a

relatively steep slope for the gain, which can narrow the range of the frequency modulation. As such, a design has to make the gain adequately adjustable in a range that meets the required regulating specifications.

Efficiency is one big benefit of using an LLC converter. The converter's switching losses can be reduced significantly by ensuring that primary-side ZVS is maintained over the whole operating range. As will be explained, ZVS cannot be achieved everywhere in the gain-plot area, but keeping the design within the recommended region will ensure ZVS.

Line Regulation

Achieving line regulation for the design of a power-supply converter can be based on Equation (25) and the recommended design areas in Fig. 7. A minimum and maximum output voltage, V_{o_min} and V_{o_max}, respectively, will be assumed. To simplify the discussion, it will also be assumed that all parasitic voltage drops—for example, from PCB traces, the MOSFET's R_{ds_on}, the diode's forward voltage, etc.—are already converted or lumped into a part of the output-voltage range. It will also be assumed that the design requires a maximum switching-frequency range; i.e., that it is limited within $f_{n\_min} \le f_n \le f_{n\_max}$. In reality, the frequency limits may need adjustment in order to adapt the line- and load-regulation requirements, or vice versa.

With these conditions and assumptions, to achieve line regulation (and load regulation as discussed later), M_g should be designed to meet the conditions described by Equation (26), which says that all possible M_g values must contain the value of both M_{g_min} and M_{g_max} within the f_n limits. For $I_o = 0$,

$$\{M_g \,|\, M_g > M_{g\_\infty}\} \supset \{M_{g\_min}, M_{g\_max}\}, \quad (26a)$$

and for $I_o > 0$,

$$\{M_g \,|\, M_g \ge 0\} \supset \{M_{g\_min}, M_{g\_max}\}, \quad (26b)$$

where

$$M_{g\_min} = \frac{n \times V_{o\_min}}{V_{in\_max}/2}, \quad (27)$$

$$M_{g\_max} = \frac{n \times V_{o\_max}}{V_{in\_min}/2}, \quad (28)$$

and

$$M_{g\_\infty} = \left|\frac{L_n}{L_n + 1}\right|. \quad (29)$$

M_{g_∞} is a special value of M_g that presents the gain value at no load when f_n is approaching infinity. In other words, at no load, the gain curve (M_g) is approaching an asymptotic horizontal line with its value described by Equation (29), which can be easily obtained from Equation (23) when the value of f_n approaches infinity.

M_{g_min} and M_{g_max} each form a horizontal line in Fig. 7. For the no-load condition ($I_o = 0$), the quality factor (Q_e) equals zero, shown in Fig. 7a as Curve 1. Since the gain curves are determined by L_n and Q_e, and $Q_e = 0$, L_n is the sole design factor at this stage. As such, a value for L_n needs to be selected that will provide a gain curve that meets the conditions of Equation (26). In other words, the value of L_n needs to make Curve 1 cross over the two horizontal lines defined by Equations (27) and (28) inside the frequency limits. This is depicted in Fig. 7 by design points a1 and a2.

Similarly, if the load condition is not zero ($I_o > 0$), then an appropriate curve can be selected by making Q_e correspond to the required maximum load and following the same process.

Load Regulation

Normal Load Operation

As illustrated in Fig. 7, the gain presents a family of curves. For a fixed L_n, each value for Q_e generates a different gain curve. A bigger Q_e makes the gain curve shift lower with a lower peak. As such, when load current increases, the gain curve moves away from its no-load shape (Curve 1) to a lower representation. In Fig. 7, Curve 2 corresponds to the maximum load current (Q_e = max) while still meeting the conditions of Equation (26) with the same L_n. This yields design points a3 and a4 in the recommended design area.

If the load is increased further, Curve 2 will be reshaped towards Curve 3. Horizontal line M_{g_max} will not be able to cross over with the gain curve,

so the conditions of Equation (26) cannot be met. Output-voltage regulation is then lost. When this happens, a design modification will be needed, such as adjusting L_n or the switching-frequency limits to reshape the gain curve.

Since Q_e is associated with the load current, it is appropriate to extend this discussion to include the possibility of overload and short-circuit conditions.

Overload Current

In the example, the recommended design area in Fig. 7 includes an overload because Q_{e_max} was defined to include a value for it. As stated earlier, any further increase in load causes Curve 2 to move towards Curve 3 or beyond, which places the design outside of the design area and towards the condition of a short circuit.

Load Short Circuit

Since a load short circuit causes a potentially excessive amount of current in the converter circuit, it is necessary to examine the gain plot of a load short circuit to know what happens and how to deal with it. The corresponding gain plot is shown by Curve 4 in Fig. 7a. f_{c0} will become f_0 when L_m is bypassed by a load short circuit, and this defines Curve 4 as the gain shape with a shorted output.

Curve 4 provides insight into possible solutions for protecting the LLC converter. One possibility is to increase the switching frequency to reduce the gain. Based on Figs. 6 and 7, if the switching frequency is increased to more than two times the series resonant frequency (f_0), the gain will be reduced to below 10%. If the frequency can be pulled up to ten times f_0, the gain becomes practically zero. From Equation (25) it can be seen that a zero gain transfers a zero percentage of input voltage to the load short circuit. In this way, the converter can be protected from a load short-circuit fault.

However, it is worth noting that the effectiveness of such a protection method depends on how quickly the short-circuit signal can be sent to the controller to activate the frequency increase. In the recommended design area, the gain will inevitably be forced to the left side of the resonant peak for some time until it eventually reaches Curve 4. This could cause several severe issues, including the possibility of a polarity reversal of the feedback control. Considering this, an independent overcurrent shutdown may be a preferable solution. However, if a frequency increase is still preferred, two other possible solutions are recommended. Either (1) add a separate high-speed control loop to rapidly initiate the frequency shift, or (2) shift the recommended design area to where the minimum switching frequency (f_{n_min}) is never less than the series resonant frequency (f_0)—i.e., to where $f_{n\_min} \geq 1$.

Zero-Voltage Switching (ZVS)

A major benefit of the LLC converter topology is its potential for significantly reduced switching losses, primarily achieved through primary-side ZVS; however, as stated earlier, it is ZVS considerations that drive the recommended design area to be only on the right side of the resonant gain curves in Fig. 7. This section discusses how ZVS is achieved and why it affects the design area.

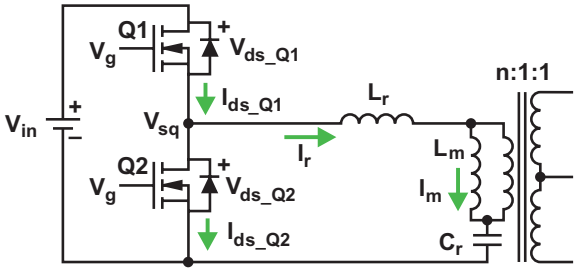
Achieving ZVS

To achieve ZVS, a MOSFET is turned on only after its source voltage, V_{ds}, has been reduced to zero by external means. One way of ensuring this

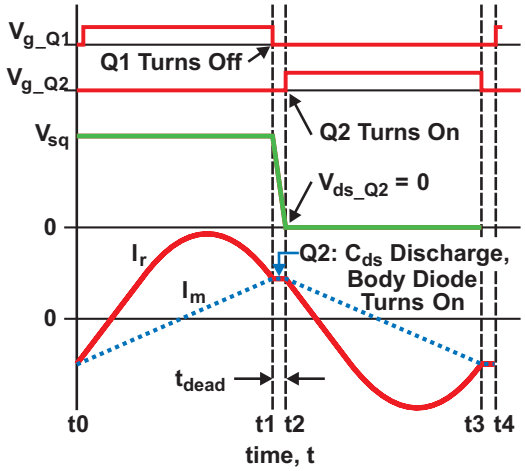
is to force a reversal of the current flowing through the MOSFET's body diode while a gate-drive turn-on signal is applied (see Fig. 8).

As shown in Fig. 8, when Q1 turns off at t1, the Q2 gate's turn-on drive signal is not applied until t2, such that there exists a dead time, t_{dead}, from t1 to t2. During t_{dead}, the current in the resonant circuit (I_r) is diverted from Q1 to Q2, first discharging Q2's drain-to-source capacitance, C_{ds}, to make its voltage zero, and then forward biasing Q2's body diode. At t2, conduction through the Q2 body diode maintains zero V_{ds_Q2} (ignoring the Q2 body diode's forward-voltage drop) until the Q2 gate's turn-on drive signal is applied. So the critical condition is when Q1 turns off. A nonzero current (I_r) should still continue in its same direction as when Q1 was on, normally accomplished by external circuit inductance. And, of course, the same conditions are necessary for a Q1 ZVS turn-on.

Since there is inductive impedance, the circuit's current lags behind its applied voltage. To achieve ZVS, the designer must determine the conditions



a. LLC resonant circuit.



b. ZVS timing waveform.

Fig. 8. ZVS operation.

where the input impedance, Z_{in} (shown in Fig. 9a), can be inductive, making the circuit's I_r lag behind its V_{ge}.

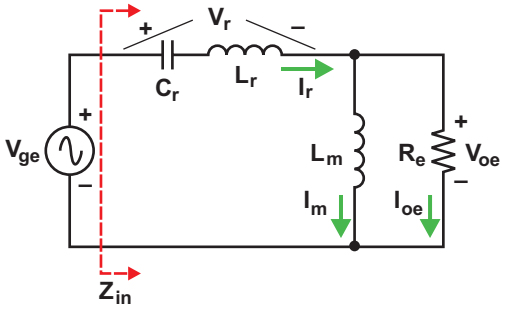
Z_{in} can be expressed in its polar form:

$$Z_{in} = |Z_{in}| e^{j\varphi_z}, \tag{30a}$$

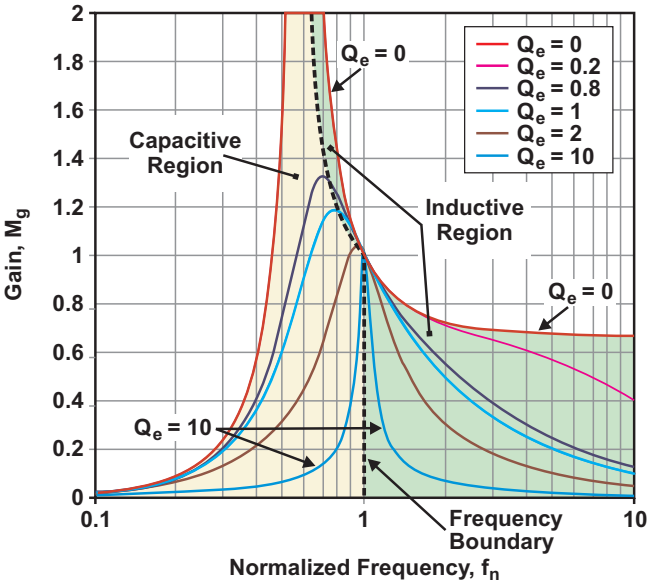
where φ_z is the phase angle between I_r and V_{ge}. From Equation (30a), it is apparent that Z_{in} varies in relation to φ_z ($-\pi/2 \le \varphi_z \le \pi/2$):

- When $\varphi_z > 0$, the impedance is inductive.
- When $\varphi_z < 0$, the impedance is capacitive.
- When $\varphi_z = 0$, the impedance is resistive.

The φ_z angle is a function of frequency, or switching frequency in this case. As such, a frequency boundary formed by the locus of the resonant peaks corresponds to $\varphi_z = 0$ and is the dividing line between the capacitive and inductive regions (see Fig. 9b). Therefore, ZVS can be

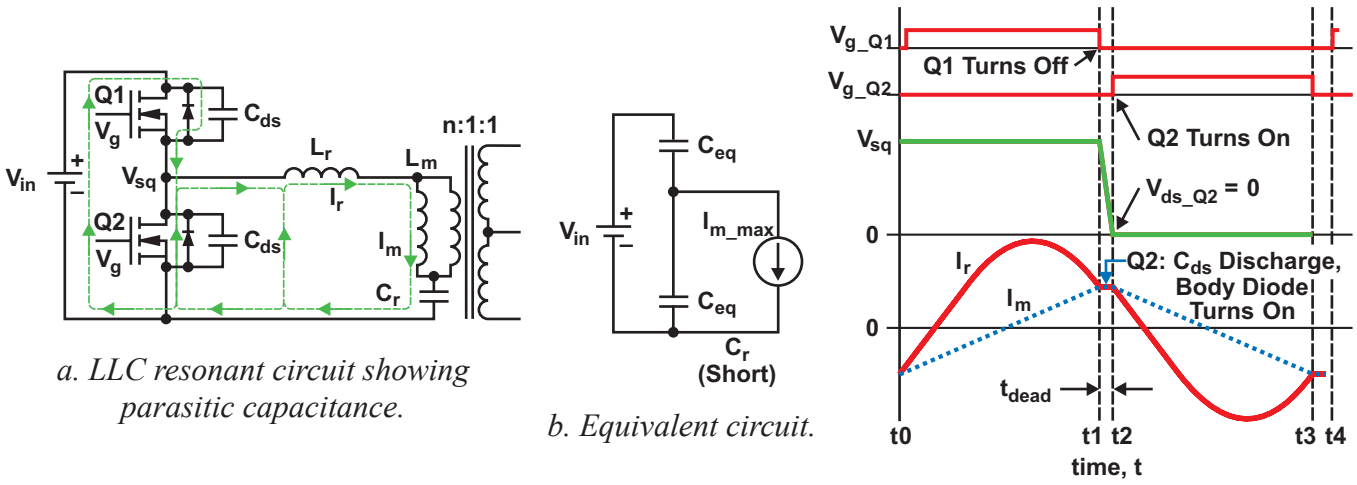


a. Input impedance.



b. Gain regions.

Fig. 9. LLC resonant circuit.



a. LLC resonant circuit showing parasitic capacitance.

b. Equivalent circuit.

c. ZVS timing waveform.

Fig. 10. Obtaining sufficient inductive energy for ZVS.

achieved only when the converter's input phase angle is greater than zero:

$$\varphi_z = \angle(|Z_{in}|e^{j\varphi_z}) > 0 \tag{30b}$$

All resonant peaks corresponding to f_{c0} are in the capacitive region, although the boundary line is very close to the peaks. To distinguish resonant peaks from the gain values on the resonant boundary, the gain values on the frequency boundary are defined as attainable peak-gain values, denoted as M_{g_ap}. Practically, though, M_{g_ap} is usually very close to M_{g_peak}, where

$$M_{g\_peak} = M_g\big|_{f=f_{c0}} \tag{31}$$

and f_{c0} is the frequency when the maximum value of M_g is achieved from Equation (18) or (23) during a frequency sweep from zero to infinity with a given L_m, L_r, C_r, and R_e.

From Fig. 7, it is clear that the recommended operating area, a1 through a4, is in the inductive region; so the design example should achieve ZVS. Although this is true, it is worth pointing out that the recommendation is only a condition necessary to ensure ZVS. There must also be sufficient inductive energy for the converter to operate with ZVS.

Ensuring Sufficient Inductive Energy

To realize sufficient inductive energy for ZVS, it is necessary to understand how ZVS is achieved in the inductive region. Fig. 10 can be used to describe the ZVS mechanism. During the dead-time interval between t1 and t2 (t_{dead}), the resonant circuit's current (I_r) equals the magnetizing current (I_m). I_m is by nature sinusoidal. In t_{dead}, I_m is circulating through the capacitances (C_{ds}) of Q1 and Q2 before Q2's body diode begins to conduct. In t_{dead}, the magnetic-field energy associated with I_m converts into the electric-field energy of the two capacitances; i.e., it charges up the C_{ds} of Q1 and discharges the C_{ds} of Q2 before Q2's body diode can turn on. C_r is much larger than $C_{ds} \times 2$, so any energy-conversion effect from C_r can be ignored. An equivalent circuit in t_{dead} can then be derived as shown in Fig. 10b. C_{eq} is used since parasitic capacitances exist in addition to $C_{ds} \times 2$. Hence, in order for the body diode of Q2 to be turned on within t_{dead}, the conditions in Equations (32a) and (32b) must be met:

$$\frac{1}{2}(L_m + L_r) \times I_{m\_peak}^2 \geq \frac{1}{2}(2C_{eq}) \times V_{in}^2 \tag{32a}$$

$$t_{dead} \geq 16 \times C_{eq} \times f_{sw} \times L_m \tag{32b}$$

Why the Capacitive Region Is Not Used

As already discussed, ZVS cannot be achieved in the capacitive region; and, without it, switching losses become high and the efficiency benefit of using an LLC converter is lost. Several additional issues arise if operation is allowed in the capacitive region:

- This region yields hard switching on the primary side, since ZVS is lost.
- Because of hard switching and a capacitive current, the primary-side MOSFET's body diodes present reverse-recovery losses, and these diodes are usually of a type with slow reverse recovery. The slow reverse recovery may allow severe shoot-through of the two primary MOSFETs, resulting in high current and causing the MOSFETs to fail.
- Even if the MOSFETs can be selected to tolerate shoot-through current caused by power dissipation from the reverse recovery, high current spikes are still present, leading to high EMI noise.
- The frequency relationship is reversed, which changes the feedback control to positive.

C. Selecting Design Parameters f_{sw}, n, L_n, and Q_e

With a better understanding of the gain behavior, it is now possible to move ahead and create the design. Thus far, all discussion has been based on knowing the values of f_{sw}, n, L_n, and Q_e and their potential effect on circuit operation; but, at the beginning of a design, nothing is known about these variables, so where does the designer start?

Selecting the Switching Frequency (f_{sw})

Acceptable switching frequency is usually defined for particular applications. For example, most off-line AC/DC applications require a switching frequency below 150 kHz for normal operation, and usually between 100 and 150 kHz as a rule of thumb. This is usually because conduction EMI testing starts at 150 kHz. Maintaining the switching frequency below the EMI test's lower boundary helps the application to pass the test. Therefore, circuit components corresponding to such a frequency range are usually well-developed, more available, and less expensive.

If a different frequency range is required for unique applications, there are several factors that may need consideration. As is well-known, the lower the switching frequency is, the bulkier the converter, and the less important switching losses and ZVS efficiency become. Conduction losses become dominant, making the LLC converter less attractive. A higher switching frequency makes the benefits of the LLC converter more pronounced, particularly in comparison with hard-switched converters. If the switching frequency is very high, additional factors may have to be considered, such as component availability and the associated additional cost; additional board-layout concerns; and additional switching losses despite MOSFET ZVS, such as magnetic-core losses. Also, the parasitic capacitance, C_w, of the transformer windings may begin to change the nature of the resonant gain curves, as shown in Fig. 11.

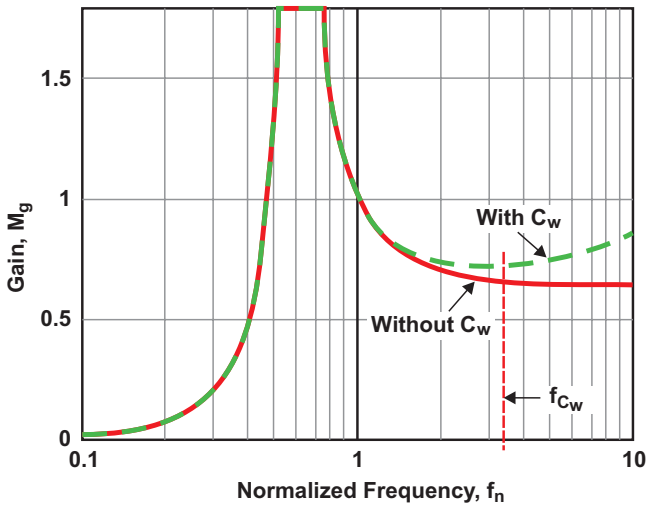


Fig. 11. Effect of transformer windings' parasitic capacitance (C_w) on gain function at high frequency.

Selecting the Transformer Turns Ratio (n)

As shown in Fig. 7, the gain magnitude in the recommended design area can be greater or smaller than unity. This provides flexibility in selecting the transformer turns ratio. Initially the gain can be set at unity ($M_g = 1$) for the output voltage at its middle value between V_{o_min} and V_{o_max}. This middle value can be called the output voltage's nominal value, V_{o_nom}, although the middle value may not necessarily always be the nominal value. Similarly, the input voltage's nominal value can be called V_{in_nom}. Then the transformer turns ratio

may be initially designed based on Equation (25):

$$n = M_g \times \frac{V_{in}/2}{V_o} = \frac{V_{in\_nom}/2}{V_{o\_nom}}\Bigg|_{M_g=1} \quad (33)$$

Selecting L_n and Q_e

Recall that in order to achieve line and load regulation across the operation range, the design must meet the conditions of Equation (26), which defines two horizontal lines crossing over two gain curves within frequency limits. Designing circuit parameters to select L_n and Q_e values that satisfy Equation (26) will be discussed next.

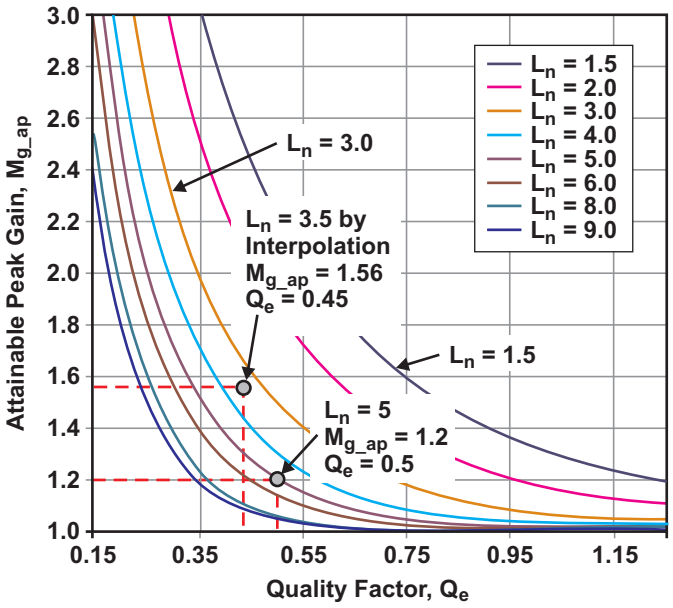
How Are the Proper L_n and Q_e Selected?

First, recall the discussion on Fig. 7. The most critical point for normal operation is the point a3. This point corresponds to Q_{e_max}, determined by the maximum load current. This point should be designed to avoid operation that would enter the capacitive region. Since a required maximum gain (M_{g_max}) can be determined from Equation (28), M_{g_max} can be plotted to the gain curves to obtain point a3 by finding the cross point between the M_{g_max} line and the gain curves. Because the gain curves are dependent on L_n and Q_e, several gain curves may need to be drawn to find a proper point a3. This is certainly one way to make the initial selection of L_n and Q_e, but it is a difficult way and most likely will require some wild guess.

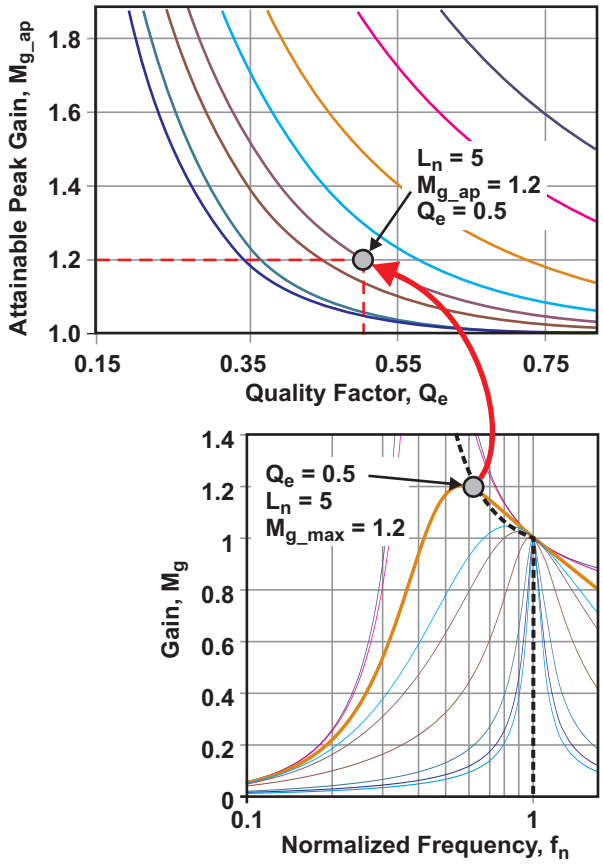
A more desirable approach is to create a common tool to represent the gain curves that can be shared and reused by different designs. Since the attainable peak gain (M_{g_ap}) corresponding to Q_{e_max} is the highest gain of concern for a design, gain-curve plots can be created beforehand to show M_{g_ap} with different values of L_n and Q_e. Then L_n and Q_e can be selected to achieve $M_{g\_ap} > M_{g\_max}$ based on a common tool—the M_{g_ap} curves. How this method is used will be described after a discussion of how the M_{g_ap} curves are obtained.

How Are the M_{g_ap} Curves Obtained?

The created M_{g_ap} curves are shown in Fig. 12a. The horizontal axis is Q_e and the vertical axis is M_{g_ap} with respect to a family of fixed values for L_n. Fig. 12b is used to illustrate how Fig. 12a is formed.



a. Peak-gain curves.



b. Obtaining peak-gain curves.

Fig. 12. Using peak-gain curves in a design.

From a plot of gain curves, for example from Fig. 6b, which is partially copied to the lower half of Fig. 12b, one attainable peak-gain value, M_{g_ap} = 1.2, can be located at the curve with (L_n, Q_e) = (5, 0.5). This point can be plotted to Fig. 12a at (M_{g_ap}, Q_e) = (1.2, 0.5). (Note that L_n = 5 at this point.) Because all curves in Fig. 6b have a fixed L_n = 5, that figure can be used to repeat the process with different Q_e values. Then a peak-gain curve can be formed as a function of Q_e with a fixed L_n = 5, shown in Fig. 12a. The process can be repeated for different L_n values of interest, producing the results in Fig. 12a.

How Are M_{g_ap} Curves Used in a Design?

With M_{g_max} already determined for a particular design from Equation (28), M_{g_max} can be plotted as a horizontal line on Fig. 12a. Any M_{g_ap} values above this line are greater than M_{g_max}, so the designed converter should operate in the inductive region. For example, for M_{g_max} = 1.2, any values of M_{g_ap} can be selected that are greater than 1.2, as shown in Fig. 12a. Then the selected value meets the maximum-gain requirement. From the selected M_{g_ap} value, L_n and Q_e values can then be selected. For example, selecting a value from the curve of L_n = 5 provides the L_n value right away. Since a gain value greater than M_{g_max} needs to be selected, Q_e would have to be less than 0.5, based on Fig. 12a. Similarly, a smaller L_n provides more gain and L_n can be selected by interpolating as shown in Fig. 12a. For example, if a value of 0.45 is selected for Q_e, the corresponding M_{g_ap} value with L_n = 3.5 would be 1.56 > M_{g_max} = 1.2, which satisfies the design requirements.

What L_n and Q_e Values Are Best if They Are All Greater than M_{g_max}?

Different applications may require the selection of unique values for L_n and Q_e to achieve an optimal design. However, LLC converters have some things in common that can be used to guide the selection:

- A smaller L_n can make the peak gain higher for a fixed Q_e, keeping the design's operation out of the capacitive region. Since L_n is a ratio of the magnetizing inductance (L_m) to the series resonant inductance (L_r), a smaller L_n usually results from a smaller L_m, and vice versa. Equation (13) indicates that a smaller L_m will introduce higher magnetizing current. This can help ZVS but will increase conduction losses.
- A smaller Q_e makes the peak gain higher while associated gain curves have a larger frequency variation for a given gain adjustment. A large Q_e results in a very low peak gain, which may not meet the design requirements.
- With these considerations in mind and from design practice, a good start is to select a value for L_n around 5 and for Q_e around 0.5 so that the corresponding gain curves will be neither too flat nor too steep.
- Reiteration is usually needed after an initial selection.

D. Peak-Gain Curves from a Bench Test

The attainable peak-gain curves shown in Fig. 12a were made from the gain function described by Equation (23), but Equation (23) was developed with approximations. These approximations allow errors in the peak-gain curves, causing accuracy concerns. To test the accuracy, a comparison was made between the gain function of Equation (23) and a bench test with a 135-kHz series resonant frequency. The peak-gain values were found to differ from those shown in Fig. 12a and from the gain curves shown in Fig. 6.

The comparison results are plotted in Fig. 13a. The solid line shows the result based on Equation (23), and the discrete points (▼) show the results from the bench test. This comparison supports the argument that the FHA-based gain function of Equation (23), while diverging for frequencies away from resonance, is accurate enough and acceptable in the vicinity of series resonance.

One other interesting observation is that the peak gain and attainable peak gain from the test are much larger than those obtained from the FHA-based gain function. Certainly this is good for a design, as it yields more design margin before operation enters the capacitive region. From this viewpoint, computer-based circuit simulation should be conducted to supplement an FHA design if more accuracy is desired prior to hardware implementation.

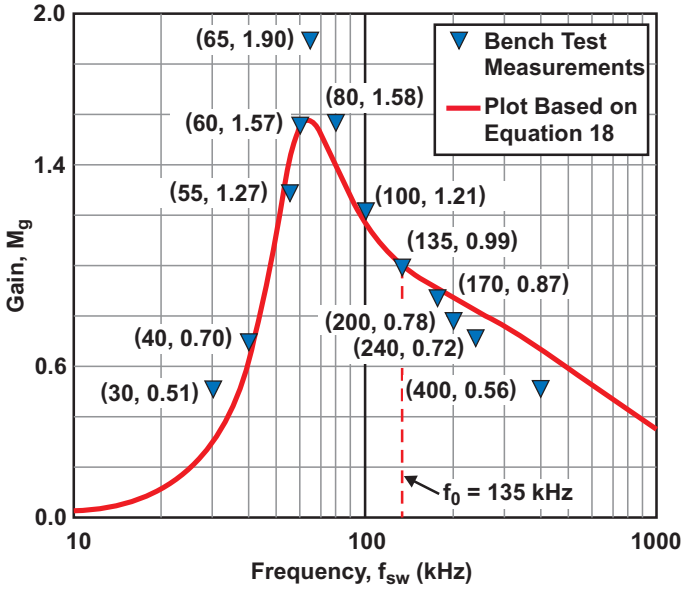
In practice, to reduce the potential effect of inaccuracy, peak-gain curves may be regenerated by experiment and/or by computer-based circuit simulation to replace the curves from Equation (23). Fig. 13b shows the peak-gain curves resulting from the experiment. Compared to Fig. 12a, Fig. 13b presents higher gain values. For example, for $L_n = 5$ and $Q_e = 0.5$, the attainable peak gain from Fig. 13b is $M_{g\_ap} = 1.65$, versus 1.2 from Fig. 12a.

E. Resonant-Network Design Flow

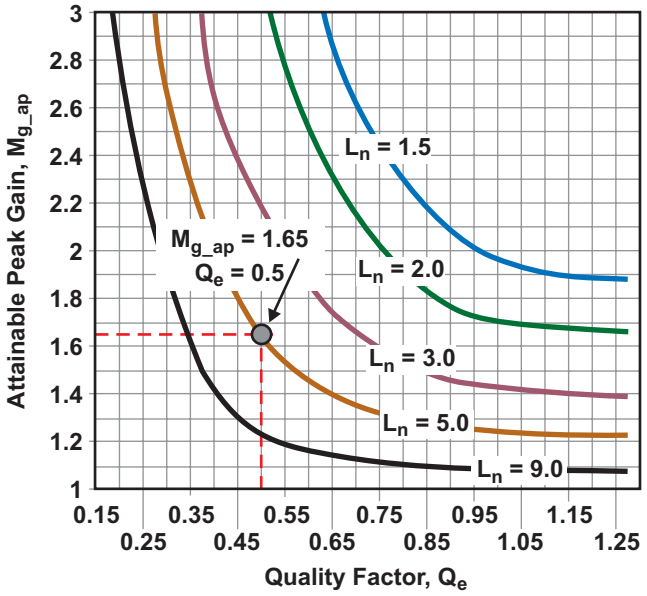
The design procedure that has been described can be summarized as follows:

- First, terminal voltages V_{o_min} and V_{in_max}, used in Equation (27), and V_{o_max} and V_{in_min}, used in Equation (28), must be taken from the converter specifications.
- Second, the transformer turns ratio (n) can be obtained from Equation (33). Then the two horizontal lines represented by M_{g_min} and M_{g_max} can be calculated. From the converter's load specifications, the load current with its corresponding resistance (R_L) can be obtained at any specified load condition. Then the AC equivalent load resistance (R_e) in the FHA circuit model can be determined from Equation (9).
- Third, two proper gain curves must be found that will cross over the two horizontal lines represented by M_{g_min} and M_{g_max} within selected or specified frequency limits. It is obvious that this can be done by selecting proper values for L_n and Q_e. After L_n and Q_e are obtained, the resonant circuit's parameters (C_r, L_r, and L_m) can be calculated based on Equations (22), (1), and (21), respectively:

$$C_r = \frac{1}{2\pi f_{sw} R_e Q_e}\Bigg|_{f_{sw} = f_0} \tag{34}$$



a. Comparison of FHA-based gain function and bench test.



b. Peak-gain curves from test.

Fig. 13. Peak-gain curves from experiment.

$$L_r = \left.\frac{1}{(2\pi f_{sw})^2 C_r}\right|_{f_{sw}=f_0} \quad (35)$$

$$L_m = L_n L_r \quad (36)$$

The design method can also be summarized with the flowchart shown in Fig. 14.

IV. Design Example

This section will demonstrate step-by-step how to use the described method to design an LLC resonant half-bridge converter. The design is oriented to applications with low output voltage, such as the ATX12 power supplies used in computers and servers, where energy conservation is important.

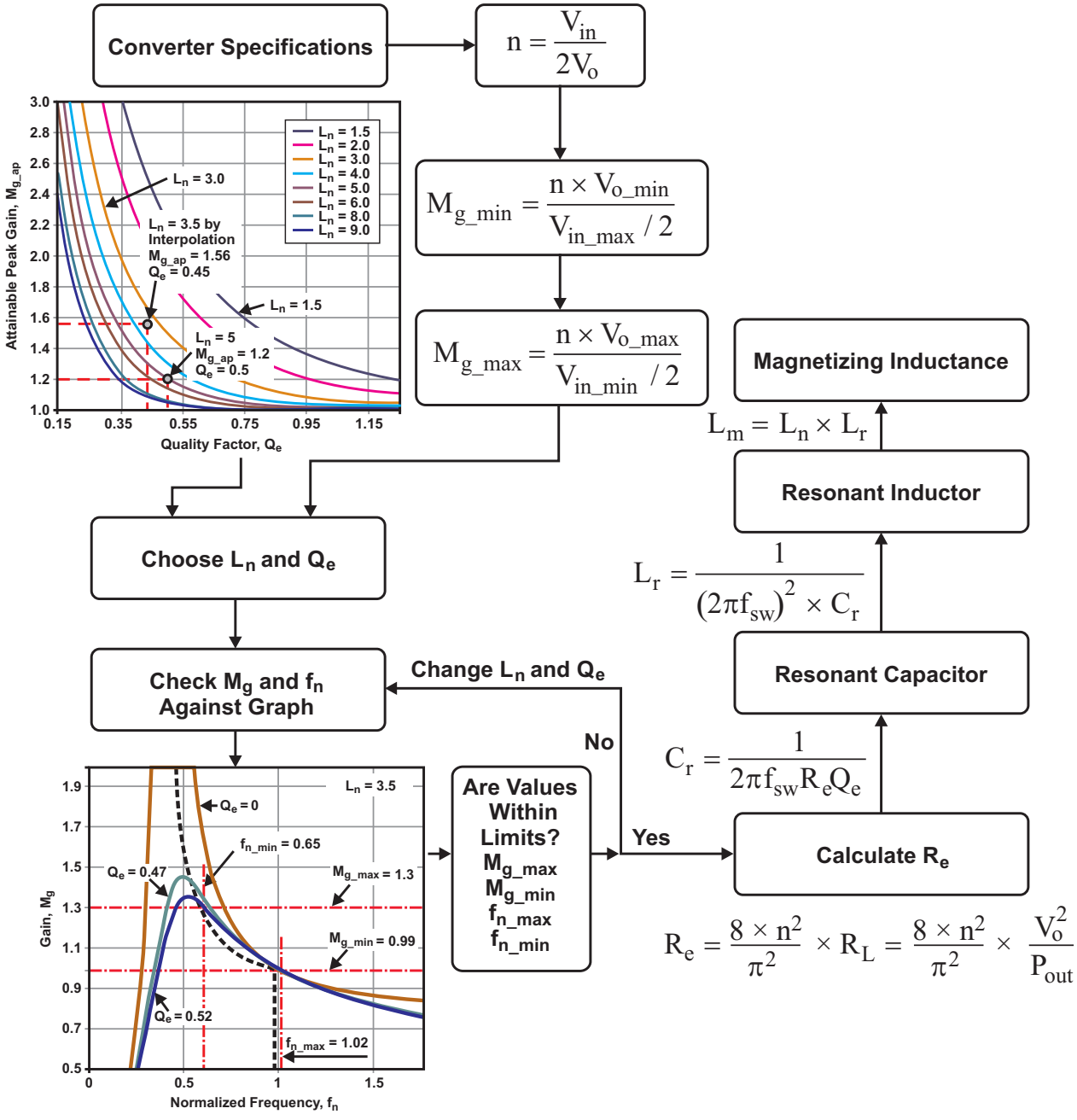


Fig. 14. Flowchart of resonant-network design.

The converter's electrical specifications are as follows:

- Input voltage: 375 to 405 VDC
- Rated output power: 300 W
- Output voltage: 12 VDC
- Rated output current: 25 A
- Output-voltage line regulation (I_o = 1.0 A): ≤ 1%
- Output-voltage load regulation (V_{in} = 390 V): ≤ 1%
- Output-voltage peak-to-peak ripple (V_{in} = 390 V and I_o = 25 A): ≤ 120 mV
- Efficiency (V_{in} = 390 V and I_o = 25 A): ≥ 90%
- Switching frequency (normal operation): 70 to 150 kHz

A. Block Diagram of Proposed Converter Circuit

A block diagram of the proposed circuit is shown in Fig. 15. For clarity, some auxiliary functions are not included. For the LLC resonant-mode controller, the UCC25600 can be a good choice. This eight-pin device has built-in, state-of-the-art, efficiency-boosting features and high-level protection features that provide a cost-effective solution. The step-by-step design demonstration will focus mainly on the power stage. For those interested in how to use and program the UCC25600, please refer to its data sheet (Reference [1]).

B. Design Steps

1. Determine Transformer Turns Ratio (n)

The transformer turns ratio is determined by Equation (33):

$$n = M_g \times \frac{V_{in}/2}{V_o} = \frac{V_{in\_nom}/2}{V_{o\_nom}}\bigg|_{M_g=1}$$

From the specifications, the nominal values for input voltage and output voltage are 390 V and 12 V, respectively, so the turns ratio can be calculated as

$$n = \frac{V_{in\_nom}/2}{V_{o\_nom}} = \frac{(390\ \text{V})/2}{12\ \text{V}} = 16.25 \Rightarrow 16.$$

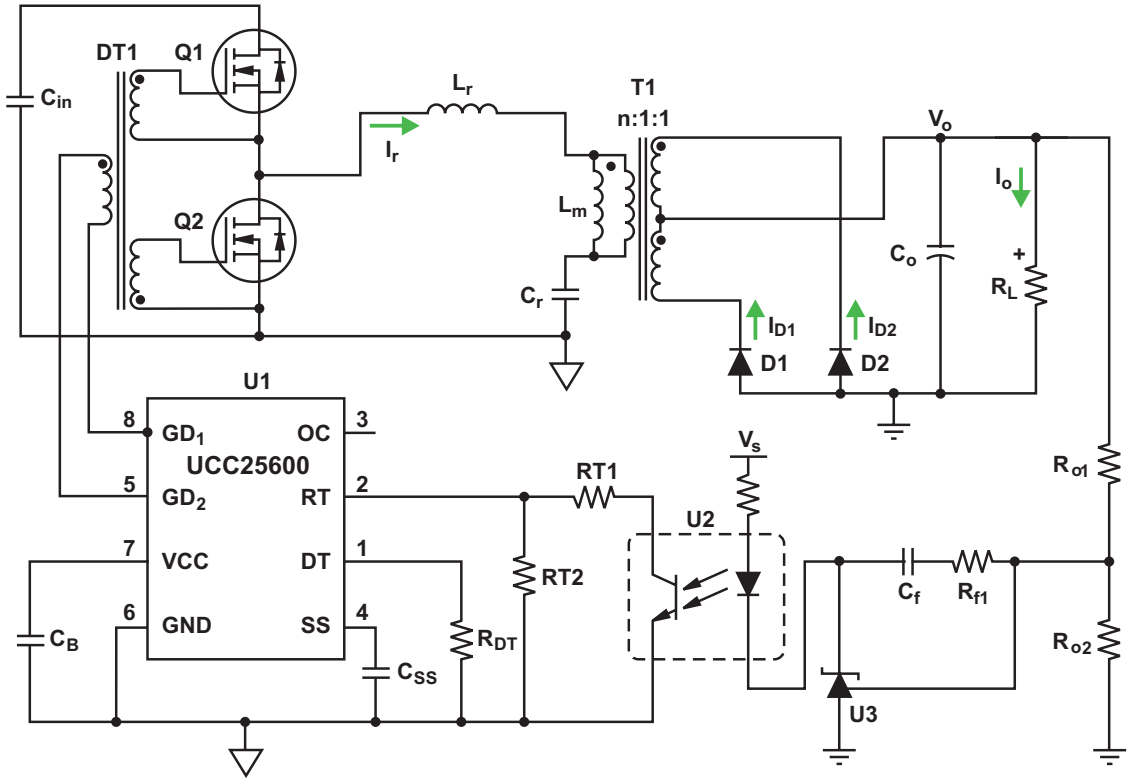


Fig. 15. Proposed circuit for the design example.

2. Determine M_{g_min} and M_{g_max}

M_{g_min} and M_{g_max} can be determined by using Equations (27) and (28), respectively:

$$M_{g\_min} = \frac{n \times (V_{o\_min} + V_F)}{V_{in\_max}/2}$$

$$= \frac{16 \times [12\ V \times (1-1\%) + 0.7\ V]}{(405\ V)/2} = 0.99$$

$$M_{g\_max} = \frac{n \times (V_{o\_max} + V_F + V_{loss})}{V_{in\_min}/2}$$

$$= \frac{16 \times [12\ V \times (1+1\%) + 0.7\ V + 1.05\ V]}{375/2}$$

$$= 1.18$$

In these calculations, 1% is used to adjust output voltage from the line and load regulation. V_F = 0.7 V is assumed for the secondary-side diode's forward-voltage drop. V_{loss} = 1.05 V is assumed for the voltage drop due to power losses. If the efficiency is assumed to be 92% (> 90% as required by the specifications), then 8% of the total power would be power losses. If all losses are referred to the output voltage, then 8% loss at 25 A would drop the output voltage to

$$\frac{\frac{300\ W}{92\%} \times 8\%}{25\ A} = 1.05\ V.$$

This is added to M_{g_max} to maintain voltage-load regulation.

To keep operation within the inductive region with an overload-current capability of 110%, M_{g_max} is increased from 1.18 to 1.18 × 110% = 1.30.

3. Select L_n and Q_e

From Fig. 12a, if the values L_n = 3.5 and Q_e = 0.45 are selected, the corresponding M_{g_ap} = 1.56, which is greater than M_{g_max} = 1.30. A curve for L_n = 3.5 is not shown in Fig. 12a, but it can be obtained by interpolating the curves of L_n = 3 and L_n = 4.

4. Determine the Equivalent Load Resistance (R_e) in Fig. 5b

R_e is determined from Equation (9). At full load,

$$R_e = \frac{8 \times n^2}{\pi^2} \times \frac{V_o}{I_o} = \frac{8 \times 16^2}{\pi^2} \times \frac{12\ V}{25\ A} = 99.7\ \Omega.$$

At 110% overload,

$$R_e = \frac{8 \times n^2}{\pi^2} \times \frac{V_o}{I_o} = \frac{8 \times 16^2}{\pi^2} \times \frac{12\ V}{25\ A \times 110\%} = 90.6\ \Omega.$$

5. Design Resonant Circuit's Parameters

The resonant circuit's parameters are determined from Equations (34), (35), and (36). A switching frequency of 130 kHz may be selected initially for the series resonant frequency, and then the resonant circuit's parameters can be calculated at full load:

$$C_r = \frac{1}{2\pi \times Q_e \times f_0 \times R_e}$$

$$= \frac{1}{2\pi \times 0.45 \times 130 \times 10^3\ Hz \times 99.7\ \Omega}$$

$$= 27.3\ nF \Rightarrow 12\ nF \times 2 + 3.3\ nF$$

$$L_r = \frac{1}{(2\pi \times f_0)^2 C_r}$$

$$= \frac{1}{(2\pi \times 130 \times 10^3\ Hz)^2 \times 27.3 \times 10^{-9}\ F}$$

$$= 54.9\ \mu H \Rightarrow 60\ \mu H$$

$$L_m = L_n \times L_r = 3.5 \times 60 = 210\ \mu H$$

6. Verify the Resonant-Circuit Design

The design parameters are as follows:

- Series resonant frequency:

$$f_0 = \frac{1}{2\pi \times \sqrt{L_r \times C_r}}$$

$$= \frac{1}{2\pi \times \sqrt{60 \times 10^{-6}\ H \times 27.3 \times 10^{-9}\ F}}$$

$$= 124.4\ kHz$$

- Inductance ratio:

$$L_n = \frac{L_m}{L_r} = \frac{210\ \mu H}{60\ \mu H} = 3.5$$

- Quality factor at full load:

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e}$$

$$= \frac{\sqrt{(60\times10^{-6}\ H)/(27.3\times10^{-9}\ F)}}{99.7\ \Omega} = 0.47$$

- Quality factor at 110% overload:

$$Q_e = \frac{\sqrt{L_r/C_r}}{R_e}$$

$$= \frac{\sqrt{(60\times10^{-6}\ H)/(27.3\times10^{-9}\ F)}}{90.6\ \Omega} = 0.52$$

Plot the gain curves corresponding to the design parameters (Fig. 16). The plot shows that the initial design meets the requirements of both Equation (26) and the following frequency specifications:

- The frequency at series resonance is f_0 = 124.4 kHz.
- The frequency at (M_{g_min}, f_{sw_max}) is $f_{n\_max} \times f_0$ = 1.02 × 124.4 kHz = 126.9 kHz.
- The frequency at (M_{g_max}, f_{sw_min}) with an overload (Q_e = 0.52) is $f_{n\_min} \times f_0$ = 0.65 × 124.4 kHz = 80.7 kHz.

7. Determine the Primary-Side Currents

The primary-side RMS load current (I_{oe}) with a 110% overload is determined from Equation (8):

$$I_{oe} = \frac{\pi}{2\sqrt{2}} \times \frac{I_o}{n} = 1.11 \times \frac{25\ A \times 110\%}{16} = 1.91\ A$$

The RMS magnetizing current (I_m) at f_{sw_min} = 80.7 kHz is determined from Equation (13):

$$I_m = 0.901 \times \frac{nV_o}{\omega L_m}$$

$$= 0.901 \times \frac{16 \times 12\ V}{2\pi \times 80.7 \times 10^3\ Hz \times 210 \times 10^{-6}\ H}$$

$$= 1.63\ A$$

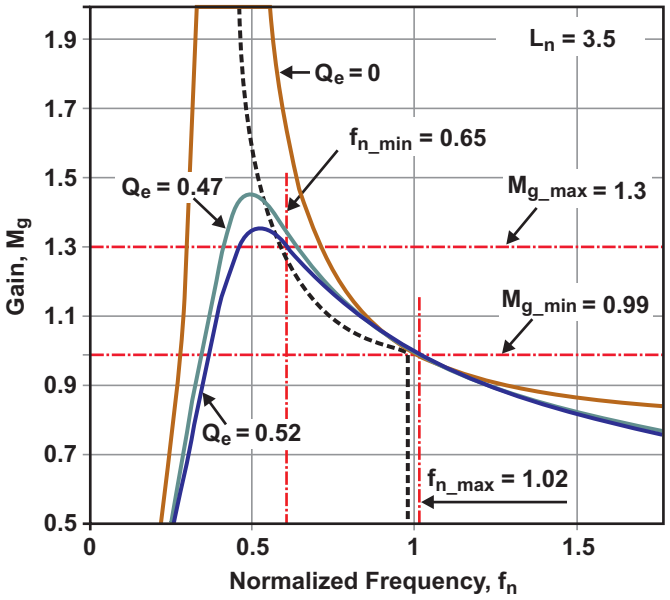


Fig. 16. Verification of resonant-circuit design.

The resonant circuit's current (I_r) is determined from Equation (14):

$$I_r = \sqrt{I_m^2 + I_{oe}^2} = \sqrt{(1.63\ A)^2 + (1.91\ A)^2} = 2.51\ A$$

This is also the transformer's primary winding current at f_{sw_min}.

8. Determine the Secondary-Side Currents

The total secondary-side RMS load current is the current referred from the primary-side current (I_{oe}) to the secondary side:

$$I_{oe\_s} = n \times I_{oe} = 16 \times 1.91\ A = 30.6\ A$$

Since the transformer's secondary side has a center-tapped configuration, this current is equally split into two transformer windings on the secondary side. The current of each winding is then calculated as

$$I_{sw} = \frac{\sqrt{2} \times I_{oe\_s}}{2} = \frac{\sqrt{2} \times 30.6\ A}{2} = 21.6\ A.$$

The corresponding half-wave average current is

$$I_{sav} = \frac{\sqrt{2} \times I_{oe\_s}}{\pi} = \frac{\sqrt{2} \times 30.6\ A}{\pi} = 13.8\ A.$$

9. Select the Transformer

The transformer can be built or purchased from a catalog. The specifications for this example are:

- Turns ratio (n): 16
- Primary terminal voltage: 450 VAC
- Primary winding's rated current, I_{wp}: 2.6 A
- Secondary terminal voltage: 36 VAC
- Secondary winding's rated current, I_{ws}: 21.6 A (center-tapped configuration)
- Frequency at no load: 127 kHz
- Frequency at full load: 80 kHz
- Insulation between primary and secondary sides: IEC60950 reinforced insulation

10. Select the Resonant Inductor

The inductor can be built or purchased from a catalog, with these specifications:

- Series resonant inductance, L_r: 60 µH
- Rated current, I_{L_r}: 2.6 A
- Terminal AC voltage:

$$V_{L_r} = \omega L_r \times I_r = 2\pi \times 80.7 \times 10^3 \times 60 \times 10^{-6} \times 2.6$$

$$= 75.7 \text{ V} \Rightarrow 100 \text{ V}$$

- Frequency range: 80 to 127 kHz

11. Select the Resonant Capacitor

The resonant capacitor (C_r) must have a low dissipation factor (DF) due to its high-frequency, high-magnitude current. Capacitors such as electrolytic and multilayer X7R ceramic types usually have high DF and therefore are not preferred. NP0 capacitors can be used due to their low DF, but their capacitance range presents limitations. Capacitors often used for LLC converters are made with metalized polypropylene film. These capacitors present very low DF and are capable of handling high-frequency current.

Before a capacitor is selected, its voltage rating has to be derated with regard to the switching frequency in use. Fig. 17 shows an example where a 12-nF capacitor rated at 600 V_{RMS} can be used only up to 300 V_{RMS} with a 100-kHz switching frequency.

The selected capacitor (C_r) must meet these additional specifications:

- Rated current, I_{C_r}: 2.6 A
- AC voltage, calculated from the circuit in Fig. 9a:

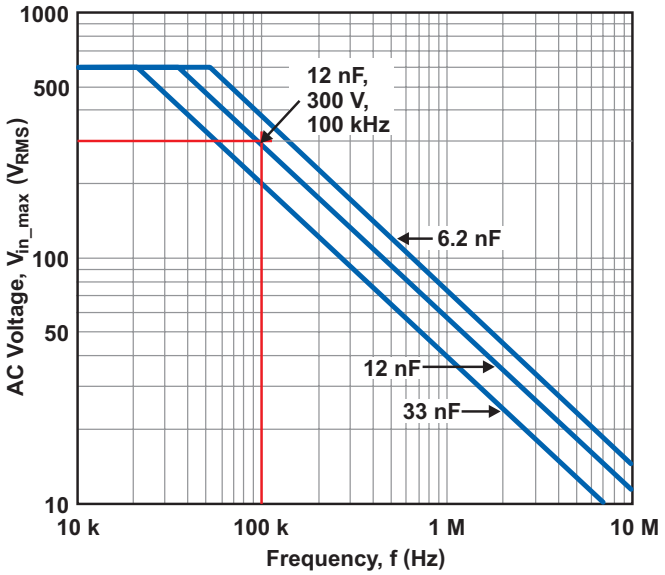


Fig. 17. Voltage derating from frequency.

$$V_{C_r} = X_{C_r} \times I_r = \frac{I_r}{\omega \times C_r}$$

$$= \frac{2.6 \text{ A}}{2\pi \times 80.7 \times 10^3 \text{ Hz} \times 27.3 \times 10^{-9} \text{ F}} = 187.9 \text{ V}$$

- RMS voltage:

$$V_{C_r\_RMS} = \sqrt{\left(\frac{V_{in\_max}}{2}\right)^2 + V_{C_r}^2}$$

$$= \sqrt{\left(\frac{405 \text{ V}}{2}\right)^2 + (187.9 \text{ V})^2} = 276.3 \text{ V}$$

- Corresponding peak voltage:

$$V_{C_r\_peak} = \frac{V_{in\_max}}{2} + \sqrt{2} \times V_{C_r}$$

$$= \frac{405 \text{ V}}{2} + \sqrt{2} \times 187.9 \text{ V} = 467.4 \text{ V}$$

12. Select the Primary-Side MOSFETs

Specify the MOSFET parameters required for the converter. Each MOSFET sees the input voltage as its maximum applied voltage:

$$V_{Q1\_peak} = V_{Q2\_peak} = V_{in} = 405 \text{ V} \Rightarrow 500 \text{ V}$$

Each MOSFET conducts half of the resonant network's current in steady state after the resonant capacitor's voltage has been established. However, during the initial start-up and transient, the current in each MOSFET can be as high as the resonant current (I_r) with a 110% overload:

$$I_{Q1\_RMS} = I_{Q2\_RMS} = I_r = 2.51\ A$$

MOSFET switching losses are minimized by ZVS; therefore, the MOSFETs' conduction losses may become the main concern for the design. This suggests that MOSFETs with a low R_{ds_on} should be used, but with the recognition that there is usually a trade-off between R_{ds_on} and C_{ds}.

13. Design for ZVS

The converter's input phase angle must be greater than zero, as described by Equation (30b). Based on Step 6, this requirement has been met.

The conditions under which the converter has sufficient inductive energy and sufficient switching dead time for ZVS are described by Equations (32a) and (32b), respectively. To check these conditions, it can be assumed that C_{eq} is mainly from the MOSFETs' C_{ds}. For typical 500-V MOSFETs, C_{ds} is around 200 pF. If it is assumed that C_{eq} = 200 pF and that the worst-case minimum magnetizing current (I_{m_min}) is

$$I_{m\_min} = 0.901 \times \left.\frac{n \times V_o}{2\pi \times f_{sw} \times L_m}\right|_{\substack{f_{sw} = \\ 127\ kHz}}$$

$$= 0.901 \times \frac{16 \times 12\ V}{2\pi \times 127 \times 10^3 \times 210 \times 10^{-6}}$$

$$= 1.03\ A,$$

then, to verify Equation (32a),

$$\frac{1}{2}(L_m + L_r) \times I_{m\_peak}^2$$

$$= \frac{1}{2}(210 \times 10^{-6}\ H + 60 \times 10^{-6}\ H) \times (\sqrt{2} \times 1.03\ A)^2$$

$$= 286.5 \times 10^{-6}\ \text{joules},$$

and

$$\frac{1}{2}(2C_{eq}) \times V_{in}^2 = 200 \times 10^{-12}\ F \times (405\ V)^2$$

$$= 32.8 \times 10^{-6}\ \text{joules}.$$

These calculations verify that Equation (32a) is true:

$$\frac{1}{2}(L_m + L_r) \times I_{m\_peak}^2 \geq \frac{1}{2}(2C_{eq}) \times V_{in}^2$$

To meet the requirements of Equation (32b), the dead time should be designed as

$$t_{dead} \geq 16 \times 200 \times 10^{-12}\ F \times 127 \times 10^3\ Hz$$

$$\times 210 \times 10^{-6}\ H = 85.0 \times 10^{-9}\ s.$$

A t_{dead} of 100 ns will meet the requirement.

14. Select the Rectifier Diodes

The diodes' voltage rating is determined as

$$V_{DB} = \frac{V_{in\_max}/2}{n} \times 2$$

$$= \frac{(405\ V)/2}{16} \times 2 = 25\ V \Rightarrow 30\ V.$$

The diodes' current rating is determined as

$$I_{sav} = \frac{\sqrt{2} \times I_{oe\_s}}{\pi} = \frac{\sqrt{2} \times 30.6\ A}{\pi} = 13.8\ A.$$

15. Select the Type of Output Filter and Specify the Capacitors

In an LLC converter, the output filter may consist of capacitors alone instead of the LC filter seen in most pulse-width-modulated converters, although a small second-stage LC filter can be an option. If the filter has only capacitors, they should be chosen to allow conduction of the rectifier current through all AC components.

The rectifier's full-wave output current is expressed as

$$I_{rect} = I_{sw} = \frac{\pi}{2\sqrt{2}} \times I_o.$$

Then, for the load current (I_o), the capacitor's RMS current rating at about 100 kHz is calculated as

$$I_{C_o} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times I_o\right)^2 - I_o^2} = \sqrt{\frac{\pi^2}{8} - 1} \times I_o$$

$$= 0.482 \times I_o = 0.482 \times 25\ A = 12.1\ A.$$

Usually a single capacitor will not allow such a high RMS current, so several capacitors connected in

parallel are often used and may offer a lower profile. Aluminum solid capacitors with conductive-polymer technology have a high current rating and a low equivalent series resistance (ESR), making them a good choice.

The ripple voltage is a function of the amount of AC current that flows in and out of the capacitors with each switching cycle, multiplied by the capacitors' ESR. Since all electric current, including the load's DC current, can be assumed to flow in and out of the filter capacitors, this is a very good estimate of the ripple voltage. To meet the specification for a 120-mV ripple voltage, the maximum ESR should be

$$ESR_{max} = \frac{V_{o\_pk\text{-}pk}}{I_{rect\_peak}} = \frac{V_{o\_pk\text{-}pk}}{\left(\frac{\pi}{4} \times I_o\right) \times 2}$$

$$= \frac{0.12\ V}{\frac{\pi}{2} \times 25\ A} = 3.05\ m\Omega.$$

Any capacitance value can be used as long as combined capacitors meet the following specifications:

- Voltage rating: 16 V
- Ripple-current rating: 12.1 A at 100 kHz
- ESR: < 3 mΩ

16. Verify the Design with a Bench Test

To verify the design's performance, a physical converter needs to be built and bench tested. Generally, one or more design iterations may be needed to meet all specifications and to optimize the design. The final design used the following parameters:

- Transformer turns ratio: n = 17:1:1
- Resonant network's parameters: L_m = 280 μH, L_r = 60 μH, and C_r = 24 nF

Detailed design files and test results can be found in Reference [2]. Physical EVM boards are also available from TI. Several critical test waveforms are shown in Fig. 18 for immediate reference.

V. Computer Simulation and FHA

For designing an LLC resonant half-bridge converter, it is strongly recommended that a computer-based circuit-simulation method be used along with the FHA method. Using the two methods together is effective and provides a good balance. The FHA method is very effective for initiating a design because it provides a functional connection between a frequency-modulated switching-mode converter and established sinusoidal AC circuit design and analysis, giving designers insight into the converter's operation. Computer-based circuit simulation, on the other hand, compensates the FHA method with accurate design values. The combined design approach can significantly reduce the number of design iterations, shortening the time from starting a design to realizing its final product.

VI. Conclusion

This topic has presented comprehensive considerations for designing an isolated LLC resonant half-bridge converter. It has been shown that the FHA method is especially effective for initiating a new design of this type. A step-by-step design example has also been presented to demonstrate how to use this method.

VII. Acknowledgments

The author would like to express sincere gratitude to Richard Garvey, Bob Mammano, Bing Lu, and Bob Neidorff for their valuable discussions during the preparation of this topic.

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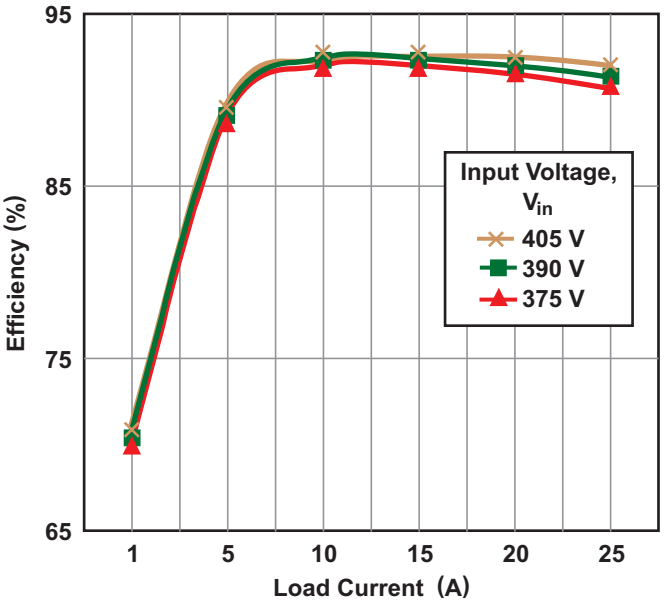
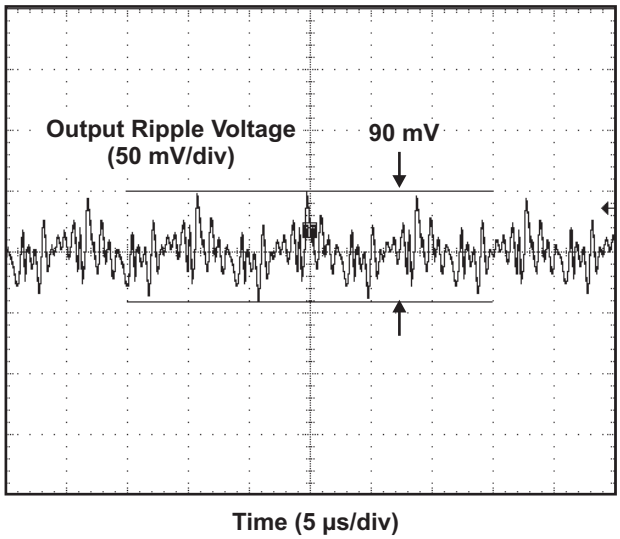
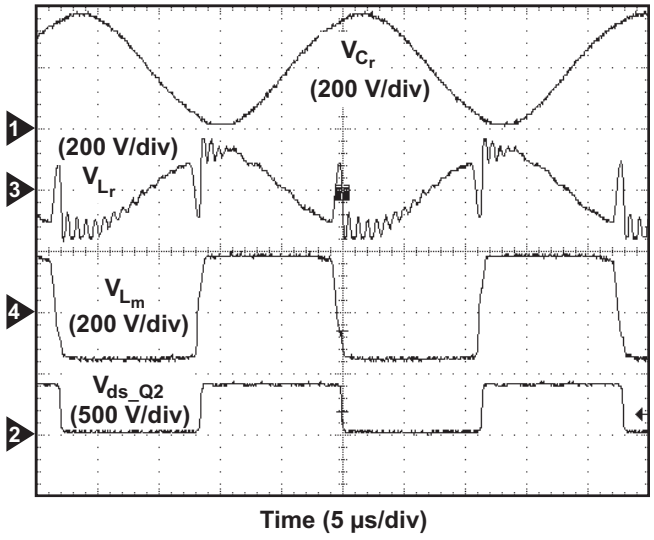


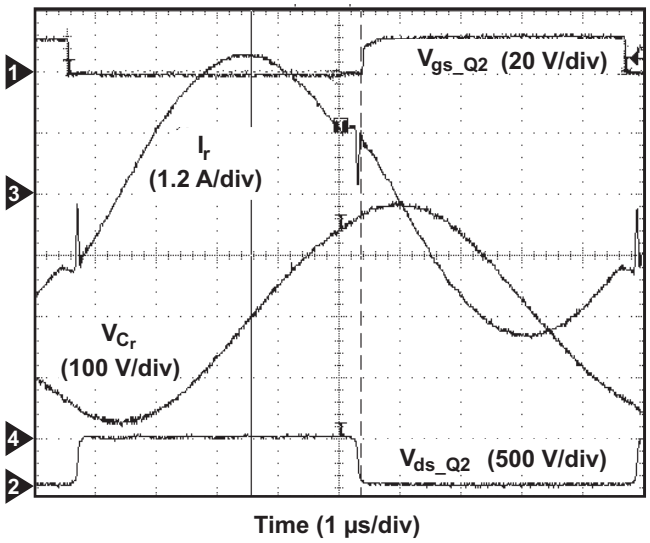
a. Efficiency.



b. Output ripple voltage (full load).



c. Voltage waveforms in resonant network (full load).



d. Resonant network's current and voltage (full load).

Fig. 18. Critical test waveforms of the design.

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Sanjaya Maniktala, 2013

Understanding and using LLC Converters to Great Advantage

PART 1: Overview of the Transition from Conventional PWM Power Conversion to Resonant Topologies

Introduction

At an early moment during the development of conventional "square-wave" switching power conversion, it was said that nature abhors any attempt to suddenly turn OFF the current passing through an inductor. That fear prompted early attempts at creating "resonant topologies". But for various reasons, in particular a very wide, almost uncontrolled switching frequency and resulting EMI spread, resonant topologies did not become mainstream, and *still aren't*. But nowadays there is a sudden resurgence of interest, primarily through the "LLC topology". This unique combination of two inductors and one capacitor ("L-L-C"), offers a relatively narrow range of switching frequencies, which are much easier to design a standard EMI filter for, combined with the capability of producing zero-voltage switching (soft-switching) through careful design which can significantly improve EMI and efficiency over a wide load range. But the overall topic and analysis is still considered complex, almost mystical, and is poorly understood. A majority of successful LLC designs are simply based on trial and error, i.e. the art of tweaking, both in a real lab environment, and in a virtual lab using Spice-based simulators. This has significantly hindered their adoption in a modern design-and-development, flowchart-based, commercial product environment.

To tackle the underlying "fear of resonance", in these pages, emphasis is laid on first understanding the guiding principles of resonance and soft-switching. Only after acquiring the underlying intuition and analytical depth, do we start to build the LLC converter, and we do that in steps: assembling the building-blocks one by one, at each stage analyzing the performance, providing the necessary simplified math, and validating each step via Mathcad and Simplis (Spice). In the process, a very unique method is being proposed on these pages perhaps for the very first time.

Soft and Hard Switching

To close loose ends, we need to revisit some of the originally expressed anxiety against interrupting inductor current in "square-wave" switching power conversion. That fear too is admittedly somewhat true, because energy is stored in an inductor as $\frac{1}{2} \times L \times I^2$, which depends on the current passing through it at any given moment. Since by the Law of Conservation of Energy, energy cannot just be "willed away" in an instant, we should never try to interrupt the inductor current by simply placing a switch (or FET) in series with it and turning that OFF. That attempt *will* destroy the switch --- on account of a huge voltage spike (induced voltage) which will suddenly appear. But there is a way out as people soon discovered: *we can consciously provide an alternate "freewheeling" path for the inductor current --- to keep it flowing smoothly (without any discontinuity) once the switch turns OFF*. That led to the "catch diode" seen in conventional switching power conversion. The provision of this diversionary diode path, a detour in effect for inductor current, is a much wiser option than trying to contain the current in a cul-de-sac of sorts, leaving it no way out. And that diode is the reason we can, by now, manage to get away turning the switch (FET) of any conventional power converter, ON and OFF, repetitively,

hundreds of thousands of times every second, and reliably so. Nature is clearly not complaining. But there *was a price to pay* for this inductor-driven brinksmanship of sorts. Diverting the current at the very last moment, and we mean *very last moment* here, does create *penalties*. Because whenever we try to turn OFF inductor current, by say dragging the Gate of the series FET to ground (or to its Source terminal as applicable), we do *not* manage to *instantaneously* reduce the current in the FET as we had perhaps hoped to do. On closer analysis we see that there needs to be a full rail-to-rail *voltage swing completed* (across the FET), just to be able to forward-bias the catch diode, to get it to even *start* taking up some of the current away from the FET. But before that happens, we cannot afford to somehow force the FET to relinquish its current, for fear of the induced voltage effect. In other words, there is a transitory moment where there is a full voltage swing taking place across the FET. Though the average value of this voltage swing is half its peak-to-peak value, this is present with the *full* pre-existing inductor current continuing to pass through the FET. There is *no* reduction in FET current *yet*, because the diode is still in the process of being "set up" to *start* taking up slack. And that does not even happen till the *entire* voltage swing is *completed* and the diode gets *forward-biased*. Geometrically speaking, we see an "overlap" of voltage and current across the FET as shown in Figure 1, and that constitutes "crossover" (switching) losses in the FET. Mathematically speaking, there is a non-zero V x I product across the FET during the switch transition. Yes, there are other subtle contributors to this crossover loss component too, such as the forcible discharging (burning up of energy) of the parasitic capacitance across the FET, and also the Drain to Gate "Miller effect" causing an increase in switching (transition) time and causing even more V-I crossover energy to be wasted, etc. Therefore, as we go to higher and higher switching frequencies, this useless "work" done by the input source (in the form of dissipation), leads to several percentage points of degradation in overall efficiency. It is for these reasons that the small, but extremely significant moment of switch transition, is garnering a lot of attention today, piquing renewed interest in resonant topologies which offer hope in this regard.

The reduction of switching losses during the few nanoseconds of switch state-transition (crossover of the FET), is critical to improving conversion efficiency. But we are also hoping to reduce EMI by the softer "resonant transitions", since we know that conventional "hard transitions" are the main source of most of the EMI in conventional converters. We are almost intuitively expecting that by using resonant topologies, the voltage will be softly reduced by self-resonant action, so that the V-I "overlap" will be likely reduced, or become *almost zero*, as also displayed in Figure 1. If so, that should help reduce EMI too.

Note: Another way out, suitable for low power applications, is to use discontinuous conduction mode (DCM), because we can thereby ensure the current is zero whenever we turn the FET ON. We can implement this using the well-known "ringing choke converter" (RCC) principle, which basically senses the ringing voltage of the inductor/transformer, to gauge when there is no residual current left (i.e. core is de-energized), and turns the FET ON at that moment. This is variable frequency PWM, in the form of boundary-conduction mode (BCM). It was actually used on a very wide scale in the 1980s in the form of the ubiquitous and historic Television Power Supply flyback controller IC, the TDA4601, originally from Philips, and still available from Infineon. The modern iPhone charger uses the L6565 from ST microelectronics, which though based on the same old ringing choke principle of the TDA4601, prefers to call itself a QR (quasi-resonant), ZVS (zero voltage switching) topology SMPS controller chip, in keeping with the times. But there are switching losses when we turn OFF the FET!

Keep in mind however, that the resonant soft-switching sketched intuitively in Figure 1, is only a "wish list" so far. It is all much easier said than done. On deeper examination, *all* resonant topologies are not similar or identical in all respects. Not all "naturally" offer soft-switching for example. In the well-known words of Bob Mammano (quoted from his presentation titled "Resonant Mode Converter Topologies", Topic 6, in the 1988/89 series of Unitrode Power Supply Design Seminars): *"While basically simple, this principle can be applied in a wide variety of ways, creating a bewildering array of possible circuits and operating modes".* In fact not all resonant topologies and modes are necessarily even conducive to the task of reducing switching losses, reducing stresses, improving efficiency, or even reducing EMI. In fact, some do not even lend themselves to a proper *control strategy* as we will see. This last aspect is extremely important but often overlooked in a virtual lab. The entire topic of resonant power conversion turns out to be an extremely complex one: to a) understand, and b) implement effectively.

But do we at least fully understand *conventional* power conversion well-enough? We may realize we need to do better in that regard, because some *critical hints for the successful analysis and implementation of resonant topologies are contained in conventional power conversion*. We may have missed the signs. For example, a potentially puzzling question in a conventional converter is: Why do we ***not*** have any overlap of voltage and current *across the catch diode*? As indicated in Figure 1, there is in fact no significant V-I overlap across the diode, which is the reason we typically assume almost zero switching losses for the diode in an efficiency calculation. This does remain a valid assumption to make, even when we move to synchronous topologies ---- in which we replace (or supplement) the catch diode with *another FET*. So now, consider this puzzle: We now *have a totem pole of near identical FETs (in a synchronous Buck for example), yet we somehow still disregard the switching losses in the lower FET, but not in the upper FET*. How come? In what way is the *location* of the lower FET so different from that of the upper FET? Why does nature seem to favor the top location from the bottom one?

Even more surprisingly, if we delve deeper we will learn that in one particular operating mode, for just *part of the cycle*, even the synchronous Buck exhibits almost no crossover loss in the top (control) FET, and actually shifts those losses to the lower (synchronous) FET! How did this role-reversal happen? *Once we understand all this, we will understand the intuitive direction we need to take in designing good resonant topologies too.*

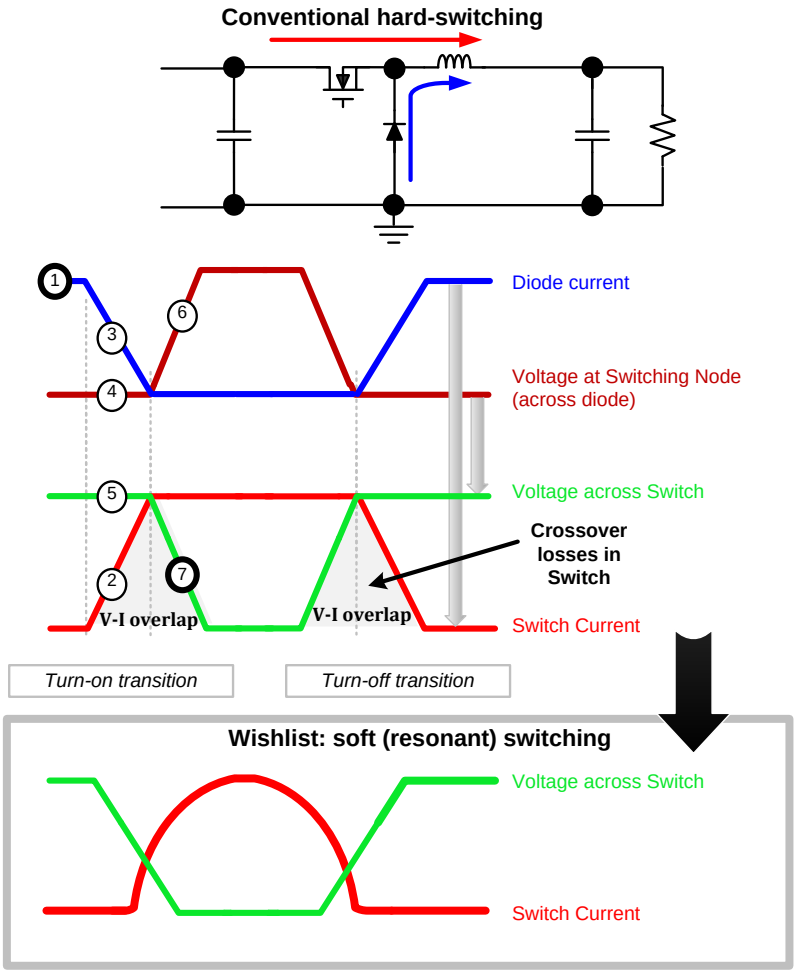

Figure 1: Hard switching compared to resonant (soft) switching

Two Key Concerns (Guiding Criteria)

These form our guiding criteria towards identifying suitable resonant topologies. The most basic questions we need to ask of any proposed circuit are:

Question 1: Does it really reduce switching losses? If so, in which *region of its operation* (or operating mode)? We need to know the line and load boundaries of any such soft-switching region, and thus try to ensure that at least at max load we can significantly reduce switching losses (and preferably continue to do so at light loads too). Finally, we hope we can do this, without asking for, or somehow creating, too wide a variation in the switching frequency. Because, though we may have soft- switching, if we have a very wide variation in switching frequency, that too cannot be good from the viewpoint of either the economics or the size of the EMI filtering

stage. We do not gain by simply shifting the cost and dissipation, from one circuit block to another: the EMI stage in this case.

Question 2: The simplest, seemingly most obvious, question can in fact become the hardest to answer: how do we "regulate" the output voltage (of a resonant converter)? Do we do pulse width modulation (PWM) or do something else? And is there a simple way to implement an unambiguous, almost "knee-jerk" (rapid) response to disturbances, *analogous to what we do in conventional power conversion?* We remember that in conventional converters, we pretty much blindly *increase* the duty cycle in response to a *fall* in the output below a set/reference level, for *any reason whatsoever*. Similarly, we decrease the duty cycle if the output rises. That is the heart of basic PWM implementation. We also know that, luckily, for all conventional topologies, a *falling input rail*, or an *increasing load*, *both* tend to cause the output to *fall*, both therefore demanding an *increase* in duty cycle (pulse width) to correct. Though that rapid response does in effect, lead to the complicated area of loop stability, the good news is that we do have a *simple, immediate, and unambiguous response to line/load disturbances*, one which is guaranteed to always be in the *right "direction" for achieving correction*. We do not for example have a complicated control scenario which asks of us something like this: "increase the duty cycle if the input rail falls to 80% of its set value, but thereafter *decrease* the duty cycle (to correctly regulate the output)". This algorithm would be impossible to implement practically. But unfortunately, *in resonant topologies, we can get exactly this odd situation*. If we do not define a very clear region of operation (the allowable/expected line and load variation, related to component selection), we will end up in an area of operation where we are expecting the output to get corrected by our response, but in fact the output veers away in the opposite direction, hopefully collapsing, not overshooting. This becomes another additional, and very tricky, part of the resonant topology puzzle that we seek to uncover in these pages.

Above we have listed the two key concerns or guiding criteria which will be addressed as we go along. But before we do that, as mentioned, first we need to understand a little more about *conventional converters*, and understand in particular, why the switching losses are "lop-sided" --- i.e. losses in one FET, not in the other, in a synchronous Buck converter for example. That will take us to the next step of development of resonant topologies.

Switching Losses in a Synchronous Buck and Lessons Learned

In Figure 1, we first consider the *turn-on* transition (on the left side). Prior to this, the diode is observed carrying the full inductor current (circled "1"). It is obviously forward-biased. But then the switch starts to turn ON, trying to take away the inductor current (circled "2"). Correspondingly, the diode current starts to fall (circled "3"). However, the important point is that while the switch current is still changing, and has not yet taken over the full inductor current, the diode needs to continue to conduct whatever remaining current, i.e. the difference between the inductor current and the switch current, at any given moment. However, to conduct even *some* current, the diode must remain *fully* forward-biased. So, there is no change in the voltage across the diode (circled "4"), or therefore, across the FET (circled "5") as the current through the FET swings from zero to max,

and in the diode from max to zero (crossover). Finally, only when the *entire* inductor current has shifted over to the switch, does the diode "let go" of the voltage. The switching node is released, and it flies up very close (a little higher) to the input voltage rail (circled "6") --- and so now, the voltage across the switch is allowed to fall (circled "7") by Kirchhoff's voltage law.

We therefore see that *at turn-on, the voltage across the switch does not change till the current waveform has **completed** its transition*. We thus get a significant V-I overlap in the switch (FET). That is "hard-switching" by definition.

If we do a similar analysis for the turn-off transition (right side of Figure 1), we will see that for the switch current to start decreasing by even a small amount, the diode must *first* be "positioned" (in terms of voltage) to take up *any* current coming its way (relinquished by the switch). So the voltage at the switching node must *first* fall close to zero (a little below ground), so as to forward-bias the diode. That also means the voltage across the switch must first transition *fully*, *before* the switch current is even allowed to decrease.
We therefore see that at turn-off, the current through the switch does not change till the voltage waveform has **completed** its transition. We thus get a significant V-I overlap in the switch (FET).

But in neither transition, turn-on or turn-off, is there any significant V-I overlap across the diode. We therefore typically assume that there are negligible switching losses in the diode in a conventional topology --- it is the switch (FET) that gets hard-switched during *both* transitions.

Note: In a Boost topology, despite no measurable V-I overlap term present across the diode, the diode can surprisingly cause significant additional switching losses to appear in the FET rather than in itself. For example, we can get losses *in the FET due to* shoot-through (poor reverse recovery characteristics of the catch diode, or the relatively "poor" body diode of a synchronous boost converter's synchronous FET). In other words, the diode may technically never "see" any significant V-I crossover loss across itself, but can certainly cause, or instigate, the switch (FET) to experience significant, perhaps even externally invisible, losses. This particular situation is often tackled by trying to achieve zero-current switching (ZCS), rather than the more common ZVS (zero-voltage switching) which are focusing on in these pages. One simple way out, especially for low-power applications, is to run the converter in DCM, because if the boost diode is no longer carrying current, it has no reverse recovery issues either (it has already recovered when the switch tries to turn ON).

However, now let us look at the synchronous Buck in Figure 2 more closely, at what really happens when the inductor current is *momentarily negative* (below zero, i.e. flowing from top to bottom, through the lower FET). Suppose during this negative current phase, the lower FET turns OFF, while the top FET is forced ON. It turns out we have to pay close attention to what happens *during the deadtime*, i.e. during the small interval between one FET turning OFF and the other turning ON. Most engineers are aware that the primary purpose of deadtime is to avoid any brief possibility of both top and bottom FETS being ON at the very same moment, which would cause efficiency loss due to cross-conduction/shoot-through, and possible destruction of the FETs too. But there is another, subtle advantage that deadtime provides, as explained in Figure 2.

From Figure 2 we can conclude that if the current is momentarily *negative*, and we turn OFF the lower FET at that moment, the inductor will in effect resonate with the Drain-Source parasitic capacitances of the FETs, causing the voltage at the switching node to rise, eventually causing a flow of current back into the input rail via the body-diode of the top FET. Keep in mind that to cause the body diode to conduct, it must be forward-biased. So the voltage on the switching node must swing. Now when the top FET turns ON, it does so with near-zero voltage across it (a forward-biased body diode drop across it). That is "ZVS" by definition. We see the Top-FET being "soft-switched" for a change. Though this effect is occurring only during part of the switching cycle, it is exactly the way it can be made to happen in both (or more) FETs in resonant power conversion too.

Note: Hypothetically, if the average of the inductor current of the Buck falls *completely* below zero (no part of it positive), we would be now constantly drawing current from the "output" (now really an input), and delivering it to the "input" (now really an output). We would have in effect a full-fledged Boost topology, not a Buck anymore. And we also know that in a Boost, it is the *lower* FET that is the "control FET" and the upper FET is the synchronous FET. We therefore intuitively expect to see only the lower (control) FET to have switching losses in a Boost. And, quite expectedly, all the crossover losses of this reversed Buck (which actually makes it a Boost), will now shift to the lower FET over the entire switching cycle. We will have no crossover loss anymore in the top FET. So the role-reversal now makes sense. When only part of the inductor current is negative (in a synchronous Buck), a switch transition during that negative-current time will produce switching losses in the synchronous (bottom) FET, not in the upper (control) FET. When a transition occurs during the positive-current part of the cycle, the switch loss is in the control (top) FET as usual.

We have learned that if we can achieve ZVS for whichever FET has current flowing through its body diode (or an anti-parallel diode placed externally across it) during the preceding dead time (just before transition). So, the *direction* of inductor current at the moment of transition is the key that identifies (or distinguishes) which FET position receives soft-switching and which one gets hard-switched. Keep in mind that what constitutes a "positive" or a "negative" current depends completely on what we are calling the "input" and what is the "output", and which direction we consider "normal" energy flow.

Note that in either scenario above, we ***certainly need current passing through an inductance to try and "force matters"***. And of course, we also need to leave a small (but not too small) an intervening deadtime for the induced voltage to be able to act. We also need enough inductance to force a *full* voltage swing. Very similarly, in resonant topologies too, whatever the type of simple or complex L-C network being switched, we learn that ***the tank circuit needs to appear "inductive" to the input source, for being able to achieve ZVS***.

Summarizing, the two basic prerequisites for achieving ZVS are:

We need the current to "slosh" *back and forth* --- something that occurs naturally in *resonant* topologies, but is also enforced in conventional half-bridge, full-bridge wave and push-pull topologies. All these are suitable candidates for ZVS, subject to the following stated condition.

The tank circuit (network) impedance must appear *inductive* to the input voltage source, because that is what is responsible, eventually, for trying to brute-force the current through (using induced voltage), in the process creating zero voltage switching across the FETs --- though as mentioned, we also must have *enough inductance*

(vis-à-vis available deadtime and parasitic FET output capacitances), so that the voltage on the swinging node can be forced to swing in a *timely* manner (before deadtime runs out), so to reduce the voltage across the FET *before* the FET is turned ON.

Note: Even in ZVS-eligible conventional topologies such as the full-bridge, we can *enforce the second requirement* above, and produce "quasi-resonant (QR) ZVS". These topologies are all based on the Forward converter topology using a transformer. We need to add a small Primary-side inductance (often just the transformer leakage) for this purpose.

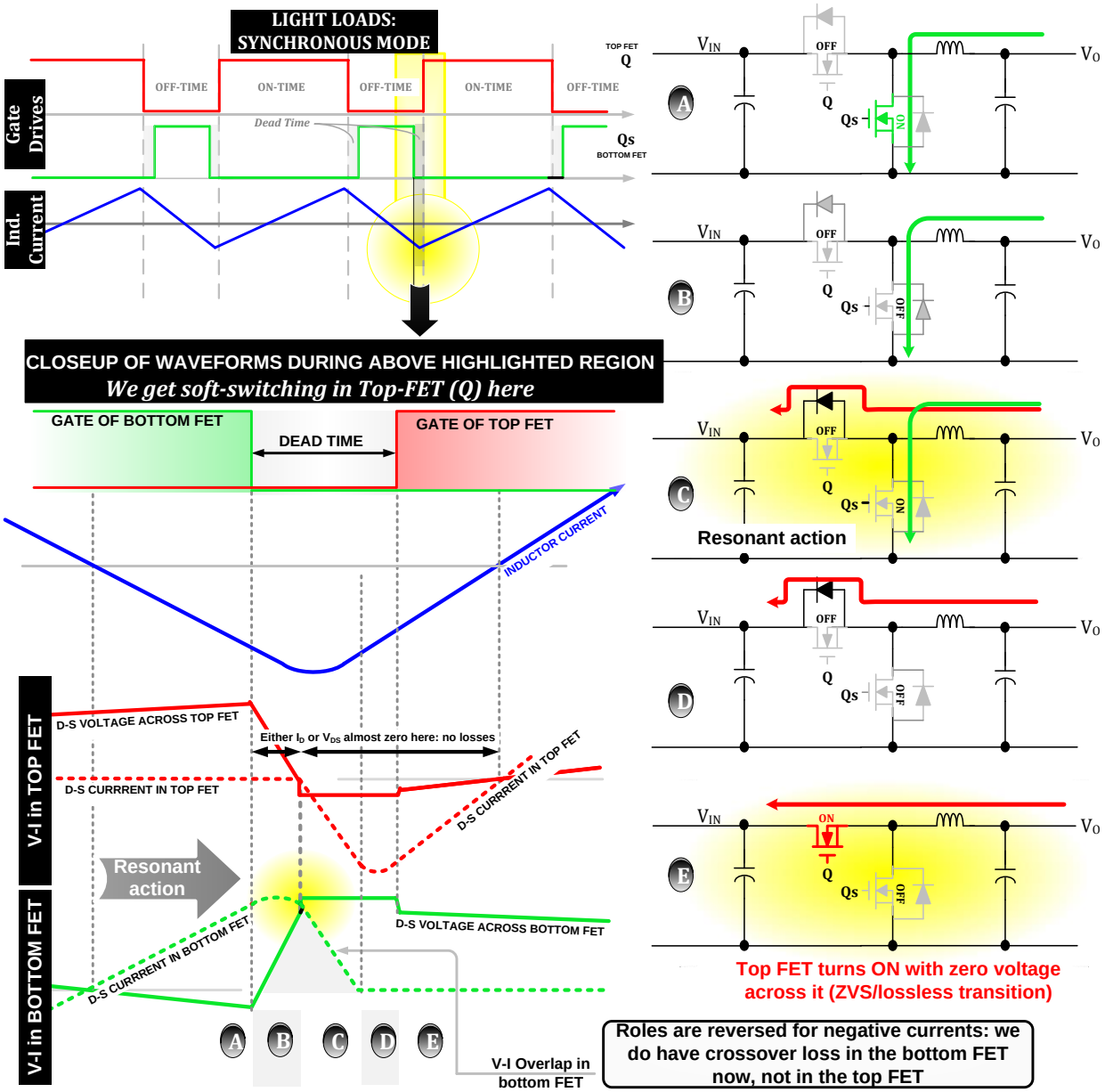

Figure 2: We do get ZVS naturally, in some cases/modes of the synchronous Buck too

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Building Basic Resonant Circuits from Components: the "PRC"

In resonant topologies, just as in conventional switching power conversion, we try to pick *reactive* components (inductors and capacitors). Because we know that ideally, they store energy, but cannot dissipate any. We always require *resistance*, either in the form of intervening parasitics, or in the form of the load itself, to dissipate any energy, either usefully or wastefully. But in addition, the L and C can pass energy back and forth *between each other* on account of their *complementary phase angles*. We can try to use that useful property to transport energy on their shoulders, from the input (source) to the output (load), somehow creating *DC regulation too along the way if possible,* which is a fundamental requirement of any type of practical power converter.

That is the general direction for implementing any "lossless" (high-efficiency) power conversion methodology. The key difference between resonant topologies and conventional switching topologies is primarily related to the actual "values" of the L and C components used. In conventional power conversion, we use relatively "large" capacitors at the input and output, so the natural LC frequency happens to be very large relative to the switching frequency. We just do not "see" resonant effects anymore, because *we do not wait that long* before we switch. But if we reduce the L and C values significantly, we will start to see resonant effects even in conventional power conversion. Keep in mind though, that just because they are "resonant", doesn't make them *acceptable* or useful. Their eventual usefulness is judged mainly on the basis of the two "guiding criteria" described previously.

Note: Modifying conventional topologies by reducing their L and C values is usually that is not the best way to go in creating resonance, except for example in the "ZVS phase-modulated full-bridge", which is best described as a "crossover converter" (in the sense of a crossover-vehicle category), literally bridging conventional power conversion with resonant effects (but resonance occurring only *during* the transition deadtimes). This maintains the desirable characteristics of constant clock frequency of conventional PWM topologies, but uses resonance during deadtime for inducing soft-switching (in all the FETs).

To create proper resonant circuits, let us start with a simple inductance and a simple capacitance. But they are *not connected to each other yet*. To make this "real", let us pick some numerical values. We choose L = 100mH and C= 10µF. These may seem rather big, but as a result, our switching frequency is also going to be low, and that is quite helpful initially at least, for ease-of-discussion, and for cleaner and faster circuit simulations etc. So, everything is initially being scaled to a lower switching frequency just for convenience.

Let us connect each separated L and C component to *identical* AC sources, of 30V (amplitude, or half peak-to-peak value) with a frequency of 300Hz, and just see the currents through each. We run this through a Simplis simulator. The results are presented in Figure 3.

As expected the input and output voltages on either component are the same, at 30V. The currents are different. We expect the corresponding current amplitudes to be:

$Z_C = 1/(2\times\pi\times f\times C) = 1/(2\times\pi\times 300\times 10^{-5}) = 53.05\Omega$. So $I_C = V/Z_C = 30/53.05 =$ **0.565 A**.
$Z_L = (2\times\pi\times f\times L) = (2\times\pi\times 300\times 0.1) = 188.5\ \Omega$. So $I_L = V/Z_L = 30/188.5 =$ **0.159 A**.

This is exactly what we got through the simulations shown in Figure 3. But via that figure, we see another possibility, one that we can hopefully exploit: the peak of the inductor current comes a little *later* (exactly $1/4^{th}$ of a cycle) after the peak of the inductor voltage (which is the same as input voltage in this case). That is why we usually say that the *current lags the voltage in an inductor by 90°*. We can confirm from conventional switching power conversion too, that when we apply a voltage across an inductor, the current ramps up slowly. So current does lag the voltage in that sense, though unfortunately, we can't really visualize or define what the "lag" is for non-sinusoidal waveforms as in conventional power conversion. Now, looking at Figure 3 once again, we see that the cap voltage peak *lags* the cap current peak by exactly the same amount, i.e. 90°. In other words, the ***capacitor and inductor currents are relatively exactly 180° out of phase.*** They are "complementary", because 180° is *just a change of sign* or direction (with respect to each other). Note that we have implicitly chosen/assumed the convention that current *into* the component (L or C) is "positive", whereas current coming out of it is "negative". So a 180° relative phase shift simply means that when 159 mA is coming *out* of the inductor, *exactly at that moment*, 565 mA is going *into* the capacitor. We can confirm this from Figure 3.

The preceding logic also leads us to the following thought process: Could we have "X" mA coming out of the inductor and exactly "X" mA going into the capacitor at the same moment? Yes, by varying the frequency we can always do that --- because in one case (inductor) the impedance increases with frequency whereas in the other case (capacitor) it decreases with frequency. So certainly, we can get the two values to converge at some "intersection" point, at which point their impedances would be equal *in magnitude* (opposite in sign, though). See Figure 4. That intersection then forms a "natural (or resonant) frequency" for the chosen L and C. The only question is: at what frequency? That is just the point at which the inductor's impedance $2\pi f\times L$, equals the capacitor's impedance $1/(2\pi f \times C)$. Equating the two, we solve to get the well-known equation for "resonant frequency": $f_{RES} = 1/\{2\pi\times\sqrt{(LC)}\}$. We will describe resonance more clearly now, based on the above observations. We could connect the two components (L and C) in parallel across each other, inject some energy into the "tank", say by tuning the applied AC source to the natural frequency of the two. Thereafter, *theoretically speaking*, once injected into this tank, energy could just slosh back and forth forever between the L and the C. It would be self-sustaining. See Figure 4. See also Figure 5 for a more detailed explanation of the phenomenon.

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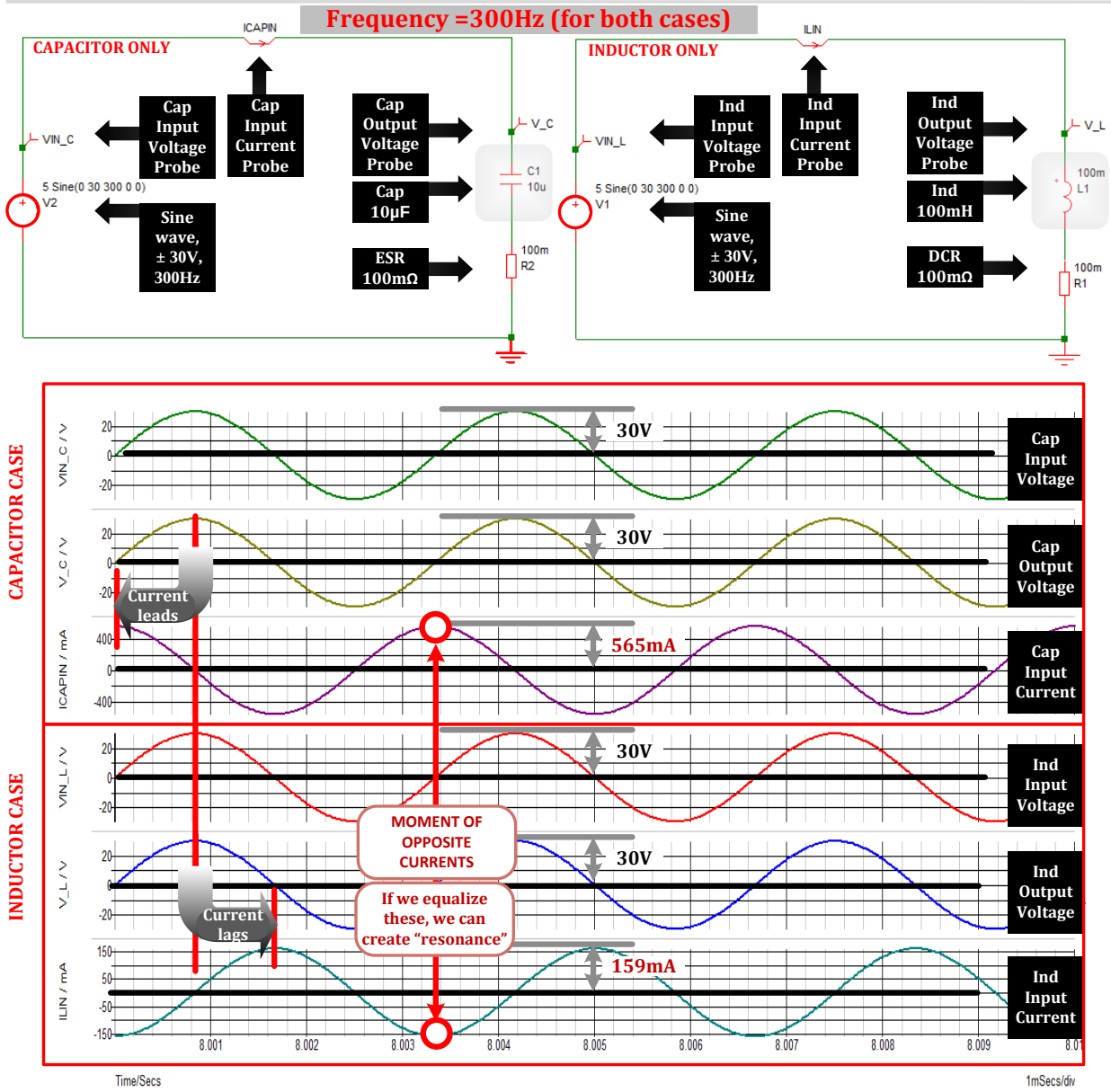

Figure 3: Response of a 100mH inductor and a 10µF capacitor to identical 30V/300Hz AC sources

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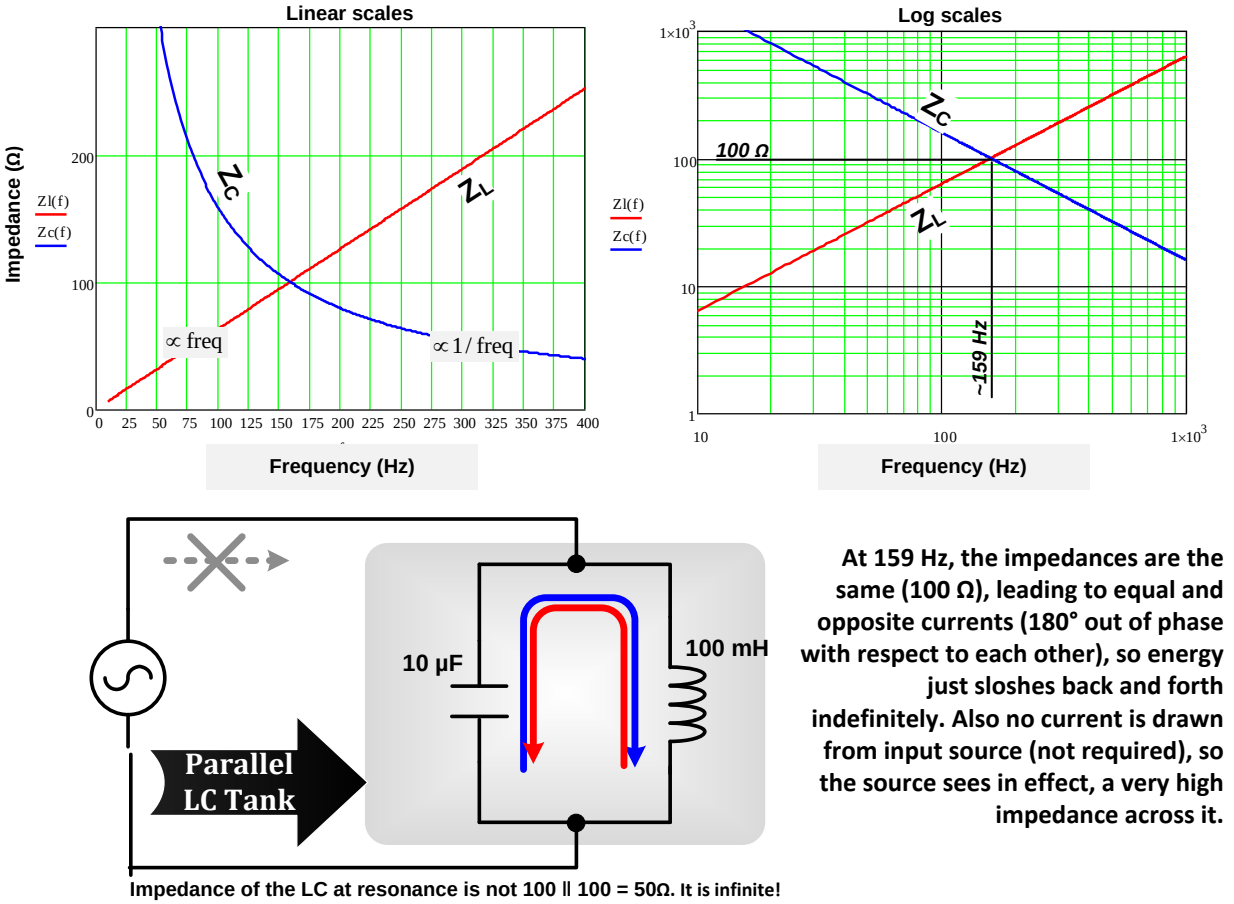

Figure 4: Explaining the energy storage capabilities of the parallel resonance tank circuit when driven at its resonant (natural) frequency

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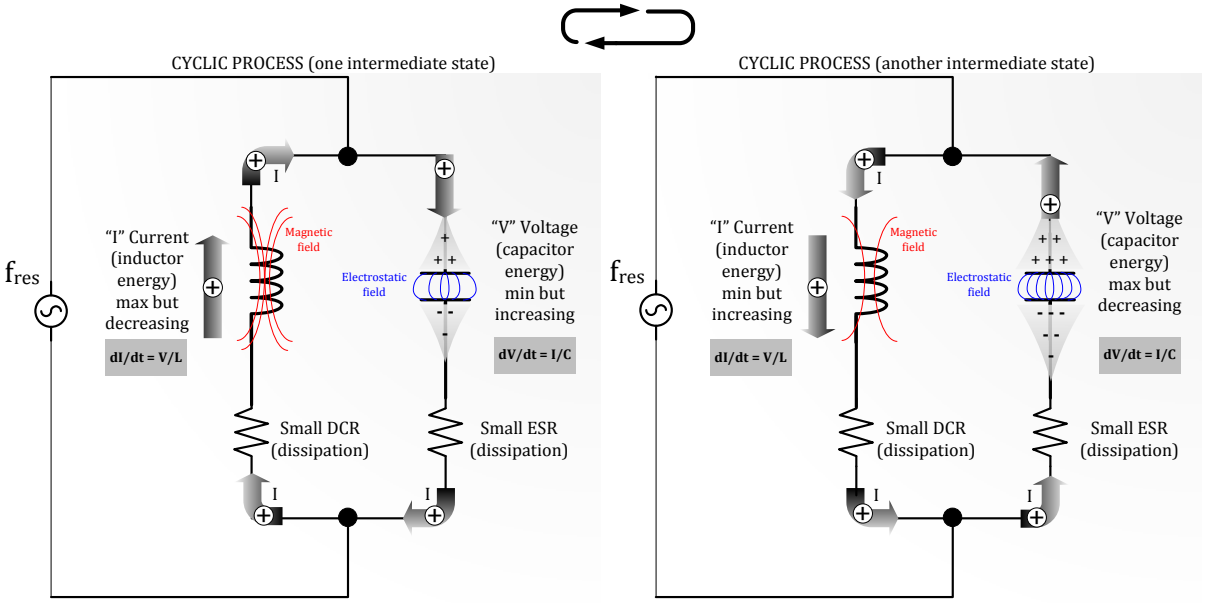

By physically paralleling the two components, L and C both are forced to have the same magnitude of voltage across them at any instant. At resonance, both have the same impedance too. So their **currents**, though equal, have a 180° *relative* phase shift --- i.e., the instantaneous current *out* of either one, almost exactly equals the current *into* the other (difference is due to non-idealities). So, during "resonance", energy (current) sloshes back and forth between inductor and capacitor as shown above. When current is peaking (i.e., inductor energy is max), its rate of rise (i.e. voltage, and therefore cap stored energy) is very small. When the voltage is peaking (i.e., max cap energy), its rate of rise (i.e., current, and therefore inductor stored energy) is very small. That leads to the back-and-forth energy sloshing. **Huge out-of-phase <u>currents</u> can be generated in the L and the C separately, but they almost cancel out, so the voltage source does not "see" those huge currents.**

This sloshing can go on forever, were it not for real-world parasitic resistances such as ESR and DCR. So, a small amount of energy is constantly dissipated during the sloshing, and the same gets pulled in from the voltage source to compensate for this loss and to maintain a steady state (provided that a voltage source is present, because otherwise the LC oscillations will decay exponentially). But being a parallel circuit, the voltage across the L and the C equals that of the voltage source, with a relatively small current (from the voltage source) passing through the LC combination . Since this small input current is only drawn for compensating a small purely resistive loss, the input current is in phase with the input voltage at resonance. To the input voltage source, the parallel-LCR network appears as a simple resistance (of a typically ***large value***, producing ***very small input currents***), at the resonant frequency.

Since the current drawn from the voltage source is very small, we can say that the **parallel LC circuit offers a very high net impedance at resonance**.

A small (large) resistance in series with the L for example, can be treated as a high (low) resistance across an ideal L. Though the transformation (equivalent parallel resistance) is frequency dependent. Similarly, a small (large) resistance in series with the C for example, can also be treated as a high (low) resistance across an ideal C. Though the transformation (equivalent parallel resistance) is frequency dependent again.

Figure 5: Explaining the energy storage of the parallel LC in more detail

Note that once the LC "tank" has been excited and "set in motion", we could even remove the AC source completely, and the oscillations would continue indefinitely (ideally). But note that if we had continued to keep the AC source connected to this tank circuit, it would make no difference at all really (unless of course the AC source tried to drive the tank circuit at some frequency *other* than its natural frequency). At the resonant (natural) frequency, provided the LC circuit has reached the voltage level of the AC source, the AC source does *not* need to replenish the energy in the tank (assuming no parasitic series resistances present). In other words, the AC source will thereafter provide *no* current at all, even if connected --- simply because it does *not need to*. But we also know from our usual electrical definitions, that if the current drawn from the input source is zero, then the *impedance (of the LC tank connected across the source), i.e., as seen by the source, is infinite (just like an open circuit, though only true at that specific frequency)*.

Above we have created our first resonant circuit: a pure "LC" parallel circuit (with no parasitic resistances). It is our first building block. We have intuitively also just learned that this pure parallel LC tank circuit has an infinite impedance at its resonant frequency "f_{RES}".

As mentioned, we have the result: $f_{RES} = 1/\{2\pi \times \sqrt{(LC)}\}$.

It is interesting to point out that at resonance, the overall impedance of the tank circuit is not half the impedance of each equal limb as we expect in the case of paralleled resistors. That is because of the complementary phase angles between voltage and current in the paralleled components, that the net impedance becomes infinite in magnitude, at the resonant frequency.

In reality, any small resistances in series with the C and the L (such as ESR and DCR), will cause the oscillations to decay exponentially. And in that case, to "replenish" the tank, the AC source will need to provide a small amount of current, *even at resonance*. Which implies that though the impedance is still very high, it is not "infinite" anymore, not even at the resonant frequency.

We have simulated an (almost unloaded) parallel LC circuit --- with a 30V AC source set exactly to the natural (computed) frequency of 159.155 Hz for the selected components (10µF and 100mH). The results are presented in Figure 6. Compare that with Figure 3 where we still had "unmarried" and separate components. If we had not loaded the circuit a bit, the Simplis simulator would have complained due to infinite numbers.

The impedance of the parallel LC falls off on either side of the resonant frequency, irrespective of parasitics being present or not. At very low frequencies, we can assume the inductor is just a short (piece of wire), and so the AC source too will see a short (zero impedance), whereas at very high frequencies, the capacitor becomes a short (high frequency bypass), so again, the AC source will see almost zero impedance.

Understanding and using LLC Converters to Great Advantage

We sum this up by saying that to the ***left of the resonant frequency of a parallel LC circuit, the LC network appears "inductive"*** (current lagging the voltage, but not necessarily by a full 90°). Whereas to the right of the resonant peak, the network appears "capacitive" (voltage lagging the current, but not necessarily by a full 90°). Since we have learned in the previous sections that a resonant network or circuit should appear "inductive" to the source, to be able to create ZVS, we realize that ***the parallel LC circuit is useful to us only provided we operate to the left of its resonant peak***.

Any small resistances in series with the L and C (their typical parasitics like ESR and DCR) can be transformed, or modeled, into an equivalent large resistance placed in parallel to the paralleled (pure) L and C. In any proposed resonant converter based on this type of tank circuit, the load too will be connected in parallel to the paralleled L and C. So the effect of all resistances is to cause a eventual decay of the stored energy if the AC source is suddenly disconnected. If the AC source continues to be connected, it now has to constantly provide current and energy into the system to keep it "topped up" --- in the form of a) useful energy delivered to the load, and b) wasted energy dissipated in the series parasitics (or the equivalent parallel resistance).

Note: The "series to parallel equivalent transformation" indicated above, in effect, makes the parallel resistance a function of the AC frequency. For any given frequency we have to recalculate it.

Finally, keep in mind that though the AC source may be providing only a tiny current at resonance, the current sloshing back and forth in the parallel LC can be *very high*. It is limited only by the impedances of the individual L and C, as we can see from Figure 6. The AC source may never "know" about these high currents since it is only delivering a very small current, but in a practical converter, where we would have transistors in the path of the circulating current, we are in danger of damaging our PRC (parallel resonant converter based on this building block tank circuit). That is one limitation. Another limitation of this very basic PRC is that there is no obvious way to regulate the output! The load is connected in parallel to the input source, so it has exactly the *same* voltage as the incoming rail. What use is that if we can't offer load and line regulation? Yes, we can add other L and C's to try to get this to work, but at this point we prefer to move on to another, more promising resonant converter variation, which was in fact quite popular in older resonant converters: the SRC (series resonant converter). It is based on the series resonant LC cell, discussed next.

Note: We can prove that the real-world actually depends on their being "parasitics" present almost everywhere. Very strange things would happen in our "real-world" if there were no *resistive* parasitics present in particular. It turns out, it is also a very good idea to include small resistive parasitics during simulation, just as we have done in Figure 6. To avoid mysterious simulation stalls, we should also try putting in initial conditions for the L and C, for the voltage across the cap or the initial current through the inductor.

Understanding and using LLC Converters to Great Advantage

PARALLEL LC AT RESONANT FREQUENCY (159.2Hz)

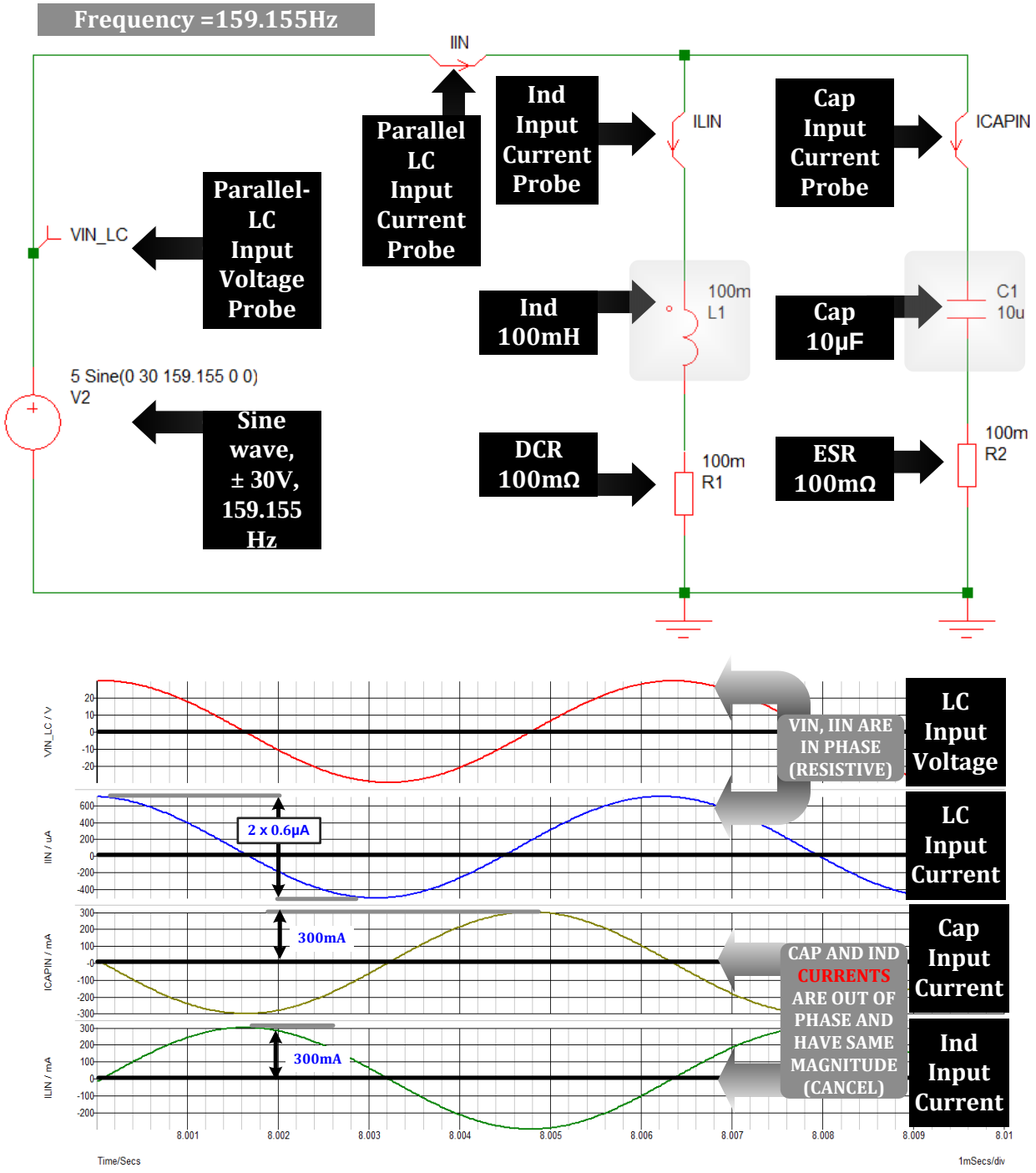

Figure 6: The (almost unloaded) parallel LC at resonance, showing the high circulating currents in L and C

Understanding and using LLC Converters to Great Advantage

PART 2: Building Resonant Tank Circuits for Future Converters

After having completed the initial transition from "PWM-thinking" to a better understanding of resonant behavior, we now start putting the LC components together to create some "trial balloons" first. Eventually we will then understand the best direction to take for practical converters.

Series Resonant Tank Circuit

This formed the basis of several commercial resonant converters. Let us get familiar with its pros and cons.
In Figure 7, we have simulated the series resonant tank, driven at its resonant frequency, almost fully unloaded (i.e. small parasitic resistances too). We see very *high currents* at resonance, clearly *limited only by the parasitics*. Then using V=I×Z, because of the very high currents, we also get *very high voltages* across the L and C. However, these high voltages are out of phase, and almost fully cancel out from the viewpoint of the input source. So we are just left with 30V (AC amplitude) to satisfy Kirchhoff's voltage law. The AC source does not "see" the high voltages, but does see the very high currents because they pass through it.

In a practical converter based on this series LC principle, we would typically connect the load across the L. Now we can use a "parallel to series equivalent (frequency dependent) transformation" and visualize this parallel load resistor as appearing in series with the L and C, just like the resistive parasitics (ESR and DCR) do. Or we could, in fact, really place the load in series with the L and C as shown in Figure 8. Whatever way, the load helps significantly reduce the high voltages and currents of the series LC (in any proposed SRC, i.e., series resonant converter). This is called "damping". It does make the series LC tank a possible practical choice, *provided we do not try to run it with no load across L*--- because damping would be lost in that case, and we could easily damage it due to the high peaking at resonance of the series LC . That is one limitation of the SRC (based on this tank circuit).

Can we at least use the SRC to provide a regulated output rail, something we couldn't do easily with a proposed PRC? As shown in Figure 8, we in fact use the basic voltage divider principle we use in setting the output voltage of a typical conventional PWM regulator, to produce a voltage rail (always) lower than the input. Nom we have to *vary the impedance of the LC* appropriately to produce whatever output we want. In other words, ***in a series resonant circuit (in general many types of resonant circuits), we need to vary the "switching" (driving) frequency to create output regulation, just as in a conventional converter we need to vary the pulse width to create regulation.***

Can we ensure ZVS in a series LC based converter? For that we need the tank circuit to appear *inductive* to the AC source as explained. So, without bothering to plot it out so far here, we can intuitively visualize that at low frequencies, the inductance of the series LC would appear as a piece of wire in series with a cap, so the AC source would only see a capacitance at low frequencies. At very high frequencies, the cap would appear shorted

to an AC signal, so the tank would now appear inductive. We conclude that in a practical SRC, ***we would need to operate to the right of the resonant frequency*** for achieving ZVS.

One famous "last-but-not-the-least" type of question remains: if the output falls, do we need to *increase* the frequency or *decrease* it? To figure that out, in Figure 9, we plot out the gain of the series LC (we call gain as "conversion ratio" at various places, but it happens to be just the output divided by the input). We see that in the "ZVS-valid" region to the right of the resonant peak, we need to reduce the frequency as load increases (to get the gain to increase). Conversely, at light loads, we have to significantly increase the frequency to regulate. For the case of R = 100 Ω, we see we need to go from 300 Hz to 170 Hz to regulate the output (keeping the same conversion ratio, since input/line has not changed here). For R = 1000 Ω, we are already in big trouble: theoretically, we have an *almost infinite switching frequency spread* in an SRC, just to regulate to a set level (at ~ zero load). We also know that at very light loads, the voltages and currents can be extremely high in a series LC tank, which not only can damage the switches of an SRC, but result in very poor efficiency at light loads. These are all the major limitations of the series-LC and its practical form, the SRC.

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SERIES LC AT RESONANT FREQUENCY (159.2Hz)

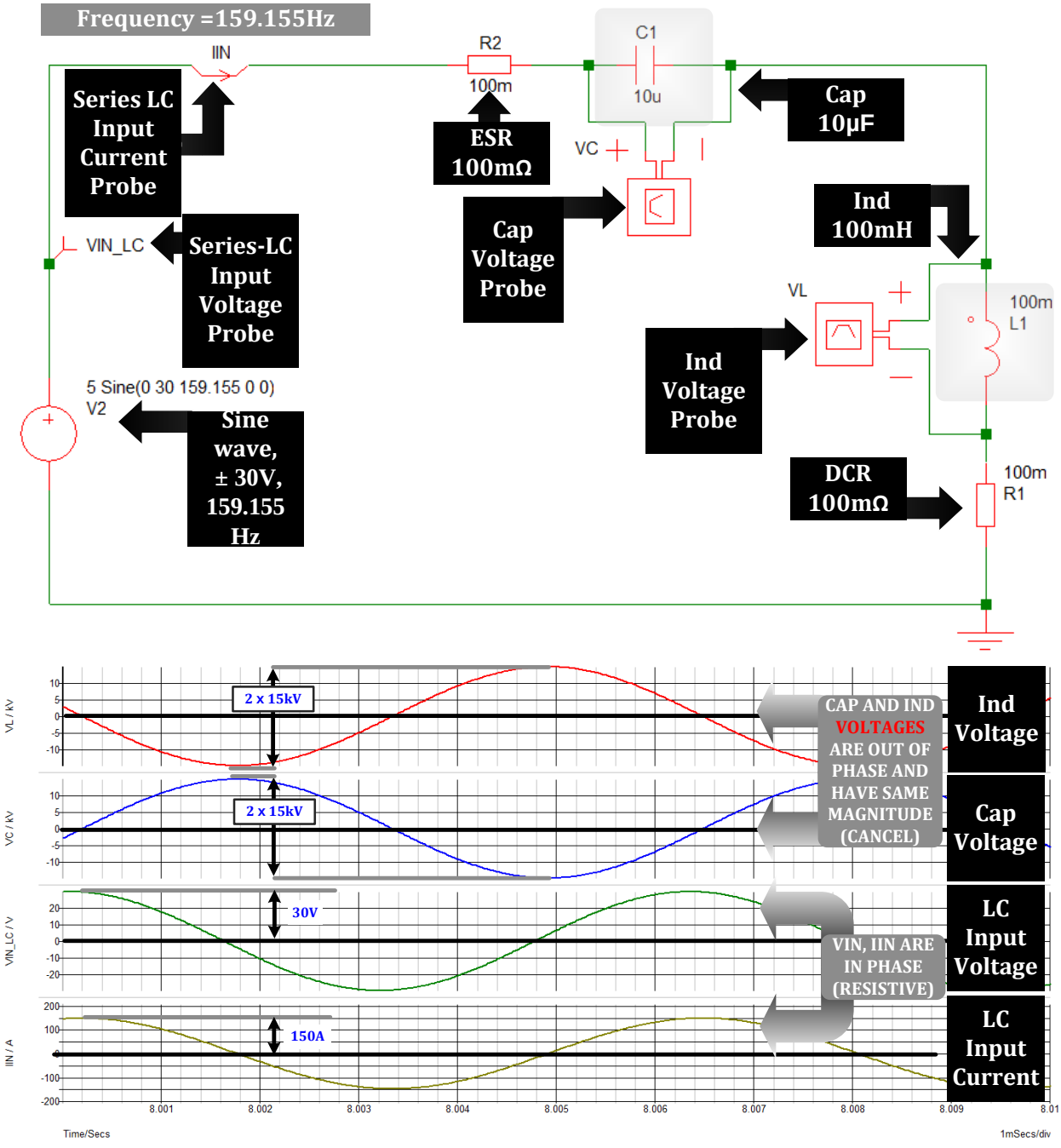

Figure 7: The (almost unloaded) series LC at resonance, showing the high voltages across L and C

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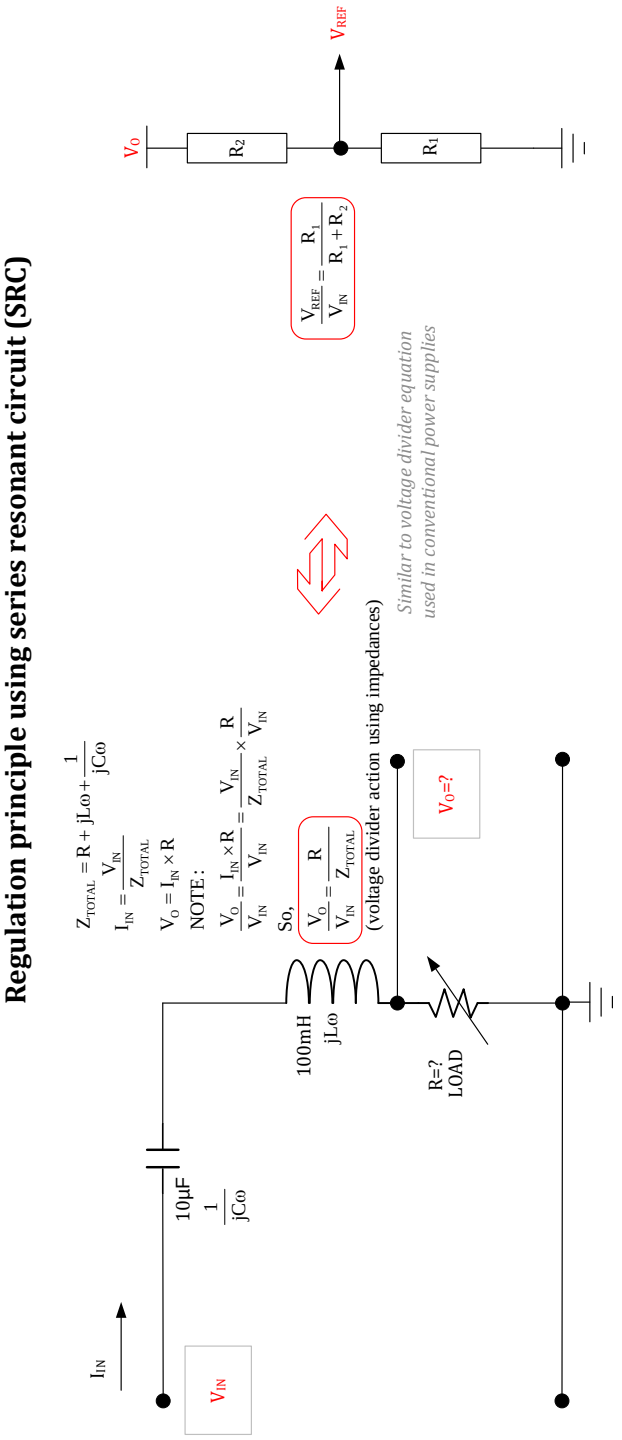

Figure 8: Using the series resonant circuit to create a regulated voltage in principle

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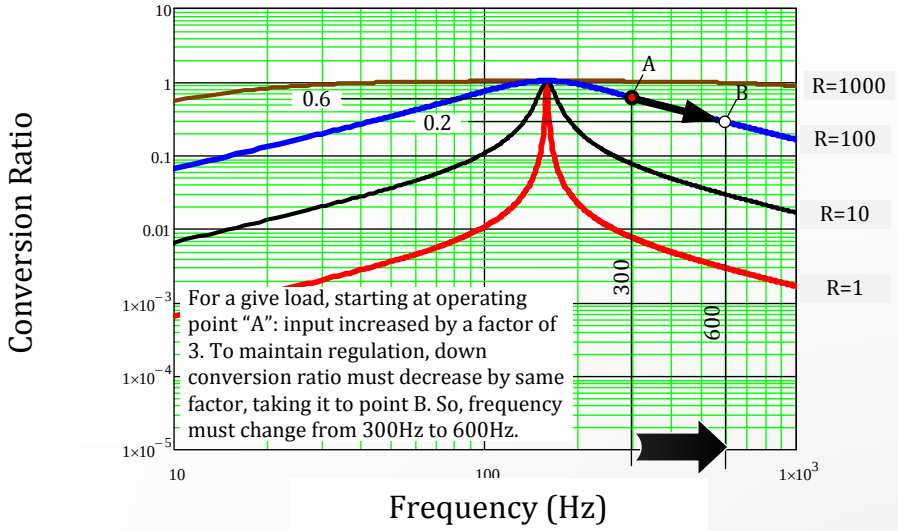
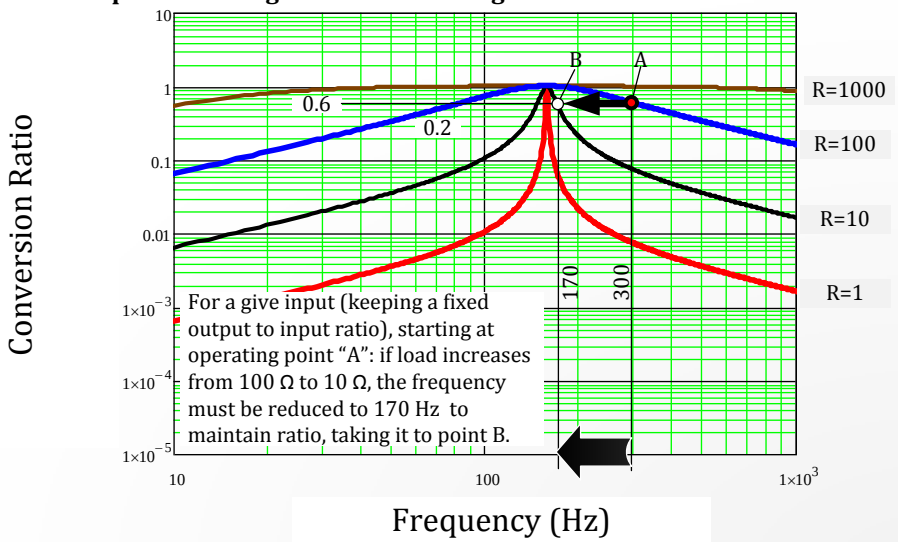
SRC with C=10μF, L=100mH

Example of line regulation locus in regulated series resonant circuit



A) At light loads, line regulation will cause a huge swing in frequency (e.g. R = 1000 Ω curve above).
B) Line regulation can also be achieved to the left of the resonant frequency, but the circuit will appear capacitive (see phase plot), and so, ZVS will be lost.

Example of load regulation locus in regulated series resonant circuit



A) Large down conversion ratios in design will lead to wider frequency shifts for load regulation

If operating to the right side of the resonant peak, in both cases above we see that if output tends to rise, we need to increase frequency, and if output falls, we need to reduce frequency

Figure 9: The series resonant LC tank, showing gain (conversion ratios), and how line and load regulation can possibly be carried out in a practical SRC (series resonant converter)

Introducing the LLC Tank for creating future LLC converters

Here all we do is to take the series LLC tank and add a *relatively large inductor in parallel to the load*, as shown in Figure 10. So, now we have two inductors and one capacitor. We call this "LLC" for L-L-C (two inductors, one capacitor).

Historically, the LLC was not really an unknown topology. But its full significance was not clearly understood till just a few years ago when engineers started looking rather keenly once again at resonant topologies in an effort to reduce switching losses.

Note: It is paradoxical though that the design of LLC converters is still so poorly understood that even though LLC converters are based on a principle that should help achieve very high efficiencies at very high frequencies, (where the last stumbling block was always the "switching loss" term), yet, most commercial LLC converters are still operating only in the range of 80kHz to 200kHz. Technology will certainly improve with a better understanding. There have been 1 MHz LLC prototypes already reported.

We need to understand very clearly how to properly and optimally design an LLC converter --- *based on physical principles and deeper understanding*, rather than just relying on "trial and error" in a real lab, or on simulations in a virtual lab. It is tricky. As even Bob Mammano admitted: it can be "bewildering". We hope to overcome some, if not all, the mystique behind the LLC converter through these pages.
We expect two resonances, because we have one C, which can "resonate" with not one, but two inductors. Note that two L's cannot "resonate" with each other, because we need complementary phase angles to resonate! We have to see how this additional L modifies the series LC circuit, and if it helps overcome some of the previously discussed limitations of the SRC.

In Figure 10, we show how the voltage divider principle can be made to work here too, this time similar to the case of a *three*-resistor voltage divider which i principle, can be used for setting the output in any conventional PWM converter. Then, in Figure 11, we have used Mathcad to plot the equation introduced in Figure 10. But before we get to fully discussing Figure 11 (the gain), let us first analyze the *phase* relationships accruing from the basic equation in Figure 10 , so we can be sure to identify the region of operation *in which the circuit appears "inductive"* and is therefore conducive to establishing ZVS. We have to admit, we cannot analyze all this very intuitively anymore, and need to plot it out mathematically as shown in Figure 12. Note that as for the series LC circuit, we have chosen L_1 to be 100mH, and C is still 10µF. The newly introduced inductance is L_2, and we have used a seemingly arbitrary value of 900mH (a factor of 9 higher as compared to L_1). Actually, that factor is optimally set. If the ratio is larger, the frequency variations are more, and if it is made too small (similar to L_1), the currents cam be much higher and the efficiency much lower.

In the next section, we start by analyzing Figure 12 and then Figure 11 again, going back and forth to draw pointers towards designing a practical LLC switching converter. Note that for now, *we are only discussing how the **LLC tank circuit behaves**, and that too only under a **sine wave** stimulus (AC source). Later we will build a practical switching converter out of it in several steps.*

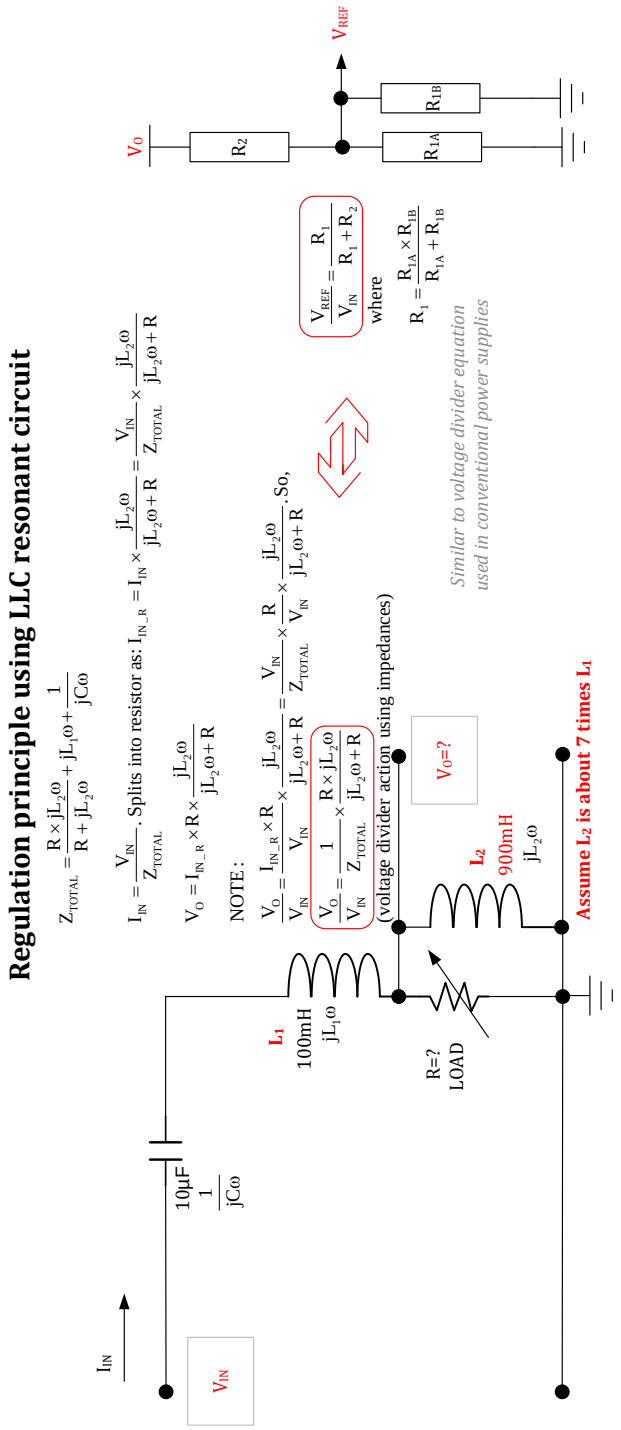


Figure 10: Using the LLC resonant circuit to create a regulated voltage in principle

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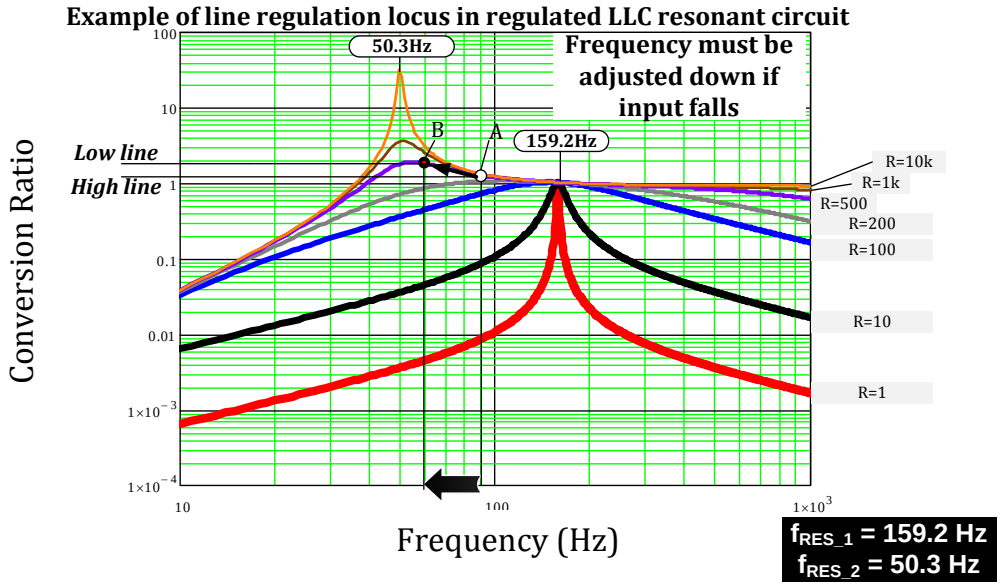
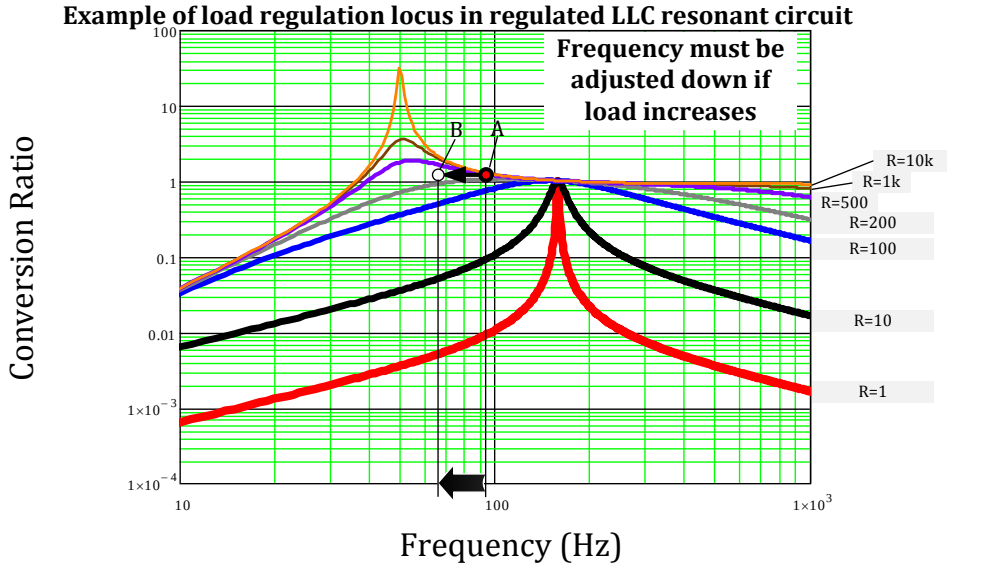
LLC with C=10μF, L_1=100mH, L_2=900mH





Increasing the load or reducing the input, both tend to cause the output to fall, and thus the regulation loop will need to try and correct this by increasing the conversion ratio (Output/Input). A) If the system is operated ***between the two resonant frequencies*** *at all loads, we can set that the logic that the control loop will* ***always simply decrease the switching frequency in response to a falling output****. B) We can also restrict ourselves completely to the right side of the right-hand resonant peak at all loads. But that has all the disadvantages of conventional series resonant circuits (e.g., huge, uncontrolled swing in frequency at light loads). C) We can also decide to restrict ourselves* ***completely to the left side of the left-hand resonant peak,*** *and set the logic such that the control loop will* ***always simply increase the switching frequency in response to a falling output****. That too will work in terms of regulation too, but it will not be ZVS. D) But we can never set an easy control algorithm if we allow operation across either resonant peak, since conversion ratio slope changes on either side.*

Figure 11: The gain (conversion ratio) of the LLC resonant circuit for different loads

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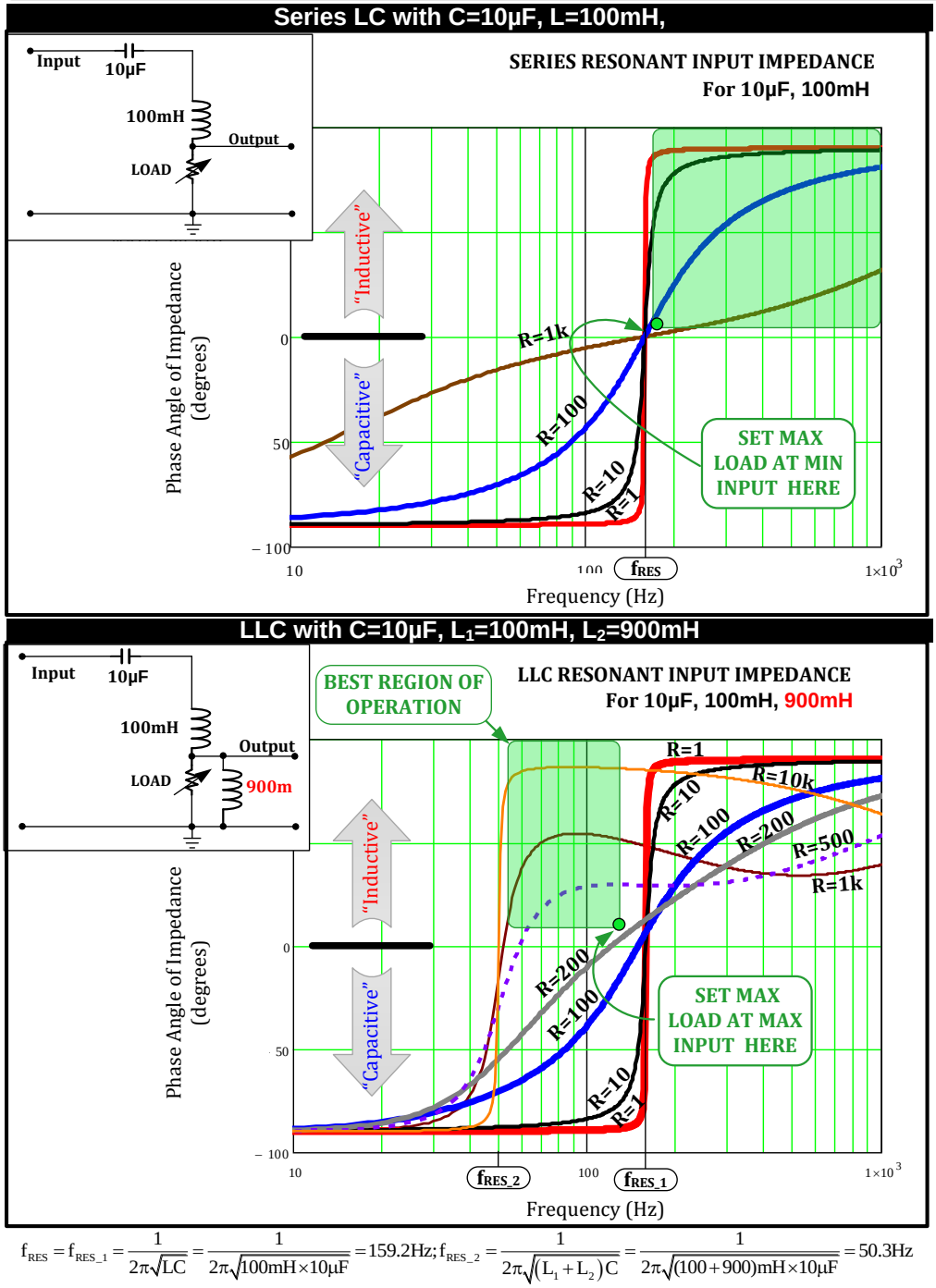


$$f_{RES} = f_{RES\_1} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{100mH \times 10\mu F}} = 159.2Hz; f_{RES\_2} = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}} = \frac{1}{2\pi\sqrt{(100+900)mH \times 10\mu F}} = 50.3Hz$$

Figure 12: The phase of the LLC resonant circuit for different loads, compared to the series LC

Analyzing the Gain- Phase Relationships of the LLC Tank Circuit

Looking at Figure 12, we see that in a series resonant LC, for any load, we always had to be to the right of the resonant peak (~159 Hz), for the phase to be greater than 0° ("inductive", i.e. for current to lag the voltage as desired). That would mean ZVS was possible only for >159Hz (potentially up to very high frequencies). In the LLC tank, we get a "low-frequency phase boost" arising from the lower resonant peak, which in turn is related to L_2, and this makes a wide range of load resistances with ZVS possible *even at lower frequencies*. In fact when we do the full math, we see that we get two resonant peaks, one formed by C and L_1 (as for series resonant tank), and another one formed by C and (L_1+L_2). Hence we have the resonant frequencies designated "f_{RES_1}" and "f_{RES_2}" shown at the bottom of Figure 12. Numerically, for the values chosen, the second peak appears very close to 50Hz. So, we can typically operate to the *right of 50 Hz and up to 159 Hz* for all loads ranging from open-circuit to R = 200 Ω (it seems so far), and achieve ZVS. For loads greater than that (say R < 200 Ω), we have to operate above 159 Hz, otherwise we cannot get ZVS because the phase angle is negative ("capacitive").

You might say: "So what" (if we can operate down to lower frequencies for a range of loads)? That by itself doesn't seem to matter! In fact we usually want to operate at *high* frequencies anyway, and want to try and ensure ZVS at *high* loads primarily. So what is the advantage of the LLC? The real advantage of the second peak in the LLC tank shows up only in Figure 11 (in the *gain* plots). In this figure, we have plotted out the gain, which we often call "conversion ratio" (i.e., output voltage of the LLC stage, divided by input voltage, where output is just the voltage across the inductor in our simple AC case so far), versus frequency (for different loads).

For very high loads (e.g. R = 1), we get a conversion ratio *always less than 1*. That is just like a series resonant LC in which we only get step-down ratios. If we decide to operate in that region with our LLC tank, we can do that. But there is a major stumbling block: For very light loads (such as 1k or 5k, as shown in Figure 11), we cannot even get much less than gain = 1, unless we move to infinite frequencies. We could have a case where we can't even regulate anymore over the full load range. Or worse, maybe we deigned our entire converter to step down, but at light loads the control loop moves in the "wrong direction" --- and ends up on stepping up (perhaps because the shape of the curve, in particular its slope, flipped signs as we moved from one side of the resonant peak, to the other side side. Yes, maybe we can "preload" the converter (at a huge expense to light-load efficiency), so our tank circuit never sees very light loads. In fact, we always need to do that in the SRC just to avoid the huge frequency variation we mentioned previously, but we could end up in the same situation with LLC too, if we are not careful in designing our region of operation, and our control strategy.

Therefore looking at things very practically, we decide we should ***not try and operate an LLC based converter to the right of the higher-frequency resonant peak*** (159 Hz in our case).

Let us keep in mind that designing our system to be "step-up" or "step-down" is actually *our* initial design decision, whatever the relationship of the input and output voltage levels. Because eventually, *we will use a transformer* with an appropriate turns ratio to correct for that. For example, we could design our LLC for a 1:1.1

ratio (an output 10% higher than the input), and then use a transformer with a Primary to Secondary turns ratio, of say 2:1, to bring the output down to about half the input voltage. That is very similar to what we do, or can do, with the conventional Flyback topology too. For example, in a typical universal-input off-line (AC to DC) Flyback power supply, we create an "invisible" *intermediate Primary-side regulated rail* of about 100V. This is for all practical purposes, the output rail as "seen" by the Primary side, and it regulates (and sets duty cycle) to keep this level fixed at 100V. But after that, a 20:1 transformer ratio is inserted via the transformer, to produce 5V from the 100V intermediate rail. Likewise, in *transformer-based resonant topologies* too, we have an additional degree of design freedom coming to us from the turns ratio, and we can voluntarily pick whether we want to operate the Primary side to act as a step-up, or step-down stage. As a corollary, since we will use a transformer anyway (also for creating the magnetic elements of the LLC), isolation is a natural advantage that accrues from an LLC converter (whether we like it/need it, or not).

We have decided not to operate to the right of 159 Hz in Figure 12. What about to the left of the second (lower-frequency) peak: i.e. below 50Hz? Unfortunately, looking at the phase diagrams in Figure 12, we realize that the phase is below 0° in that region, and therefore the network will capacitive to the input source. We know that is not going to lead us to ZVS operation. In other words, finally ***we are left only with the region between 50Hz and 159Hz to operate over the entire line and load variation***. We have no other practical and unambiguous choice really, given the guiding criteria discussed previously and the shape of the gain curves. But one question remains: does this (available) region (fully) meet *all* our needs? Do we need to look more closely?

Let us look again at Figure 11 and see how we intend to implement *line and load regulation*. We can see that, depending on the load, we can get either step-up or step-down (i.e., conversion ratio greater or less than unity). Most of the curves are in fact with a step-up ratio. We can actually close-up in this vital region, as we do in Figure 13, and we realize that the curve of R = 200 Ω, which on the basis of its positive (inductive) phase had been previously deemed "ZVS-capable" and therefore acceptable, won't *work for an entirely different reason*. That is related to one of the two guiding criteria we talked about earlier: do we have a "simple way to implement an unambiguous, almost "knee-jerk" (rapid) response to disturbances, *analogous to what we do in conventional power conversion?"*. For the 200 Ω curve we are failing this requirement for line regulation. We can see from Figure 13 that the 200 Ω curve slopes *downwards* as frequency decreases from f_{RES_1} to f_{RES_2} (159 Hz to 50 Hz). This is *opposite* to all other neighboring curves here. In all the other cases, based on Figure 11 we have obviously designed the converter in such a way that if input falls, we lower the frequency (in knee-jerk fashion), to correct for that. But for the 200 Ω case (as per the closeup in Figure 13), decreasing the frequency will cause the conversion ratio to fall even more, so the output *will collapse*. This is not in the "right direction" for correction, commensurate with neighboring trends and our control strategy.

We therefore conclude that:

Resistive loads less than 200 Ω are definitely considered "overloads" (based on the LLC tank circuit values chosen so far). Output foldback will occur in this case. These values cannot be supported, even though the phase seemed right.

This "dropping off" of gain is coincidentally almost commensurate with the phase just going negative (below zero degrees), as indicated in Figure 13. While plotting these curves, the spreadsheet was set to "test the gain versus the phase condition", and "appear dotted" if the phase was reported to be negative. In general we can safely conclude that whenever the gain starts "heading down", the phase simultaneously is close to dropping below the zero degree line (it becomes negative, and thus capacitive). Therefore, for *two* reasons, not one, the dotted part of the curves in Figure 13 is considered "no man's land" from now on. If the system enters that region, it won't be destroyed, but its efficiency will suddenly worsen (no ZVS), and also, any attempt at output correction, will most likely cause output foldback. On this basis, we rule out 200 Ω --- we can see from Figure 13 that it just doesn't go far enough into the lower frequency region (starting from f_{RES_1}), before it turns "dotted". We also conclude that the max usable load for any LLC converter, based on the LLC tank circuit values we picked in this example, is ***250 Ω*, but also, adding some design margin, *we fix preferably 300 Ω***. Higher loads than that (i.e. smaller load resistance values), are "overloads" by definition.

At very light loads, the frequency will shift close to 159Hz, not more (certainly unlike an SRC which tries to go to infinite frequencies to regulate at light loads).

At very heavy loads, the frequency will shift closer to 50Hz.

We can easily sense, based on the equations for f_{RES_1} and f_{RES_2}, that increasing L_2 significantly will move f_{RES_2} towards much lower frequencies. Though that may help in some way, it is clear that there is a penalty for making L_2 much larger than L_1. For one, the frequency variation spread, going from min load to max load, and from low line to high line, will become much larger.

We have decided we need to ***design for conversion ratios higher than unity*** so we can cover the full load range from 250 Ω (peak load) to higher values (unloaded). In particular, to ensure ZVS, we will set the LLC converter at peak load, at high line, to be at the encircled point at the lower right tip of the shaded area in the LLC phase diagram of Figure 12. At that particular design entry point (shown more clearly and precisely with an ellipse/circle in Figure 13), we will have a frequency closer to the higher resonant peak (~ 125 Hz in our case here), and a corresponding gain (conversion ratio) of about **1.05**. This ***gain target of 1.05 at max load and high line is actually our universal recommended entry point for all LLC converters designs***, because otherwise the gain curve "droops", and the correction loop will take it in the "wrong direction" (foldback) as discussed

previously. If we set it closer to 1, say at 1.02, our design entry point will shift closer to the higher-frequency resonant peak. But that is too marginal.

The full optimum region of operation is also shown (shaded) in the gain curves of Figure 13. This area is the part of the gain curve *for which phase angle is positive (inductive)*. As indicated, we have "AND-ed" the gain and phase curves using Mathcad, so the curves become dotted if unacceptable. As also indicated, this does not mean the system will necessarily stay in this optimum region, or we are somehow constraining it too. That locus of movement is determined solely by the regulation loop, as it relates to the specific line or load variations. So certainly, our selected *design entry point must lie within this shaded region (at the circle/ellipse)*, so that we get ZVS at max load and at high line, but we *may just lose the advantage of ZVS if we leave this shaded area.* For example, if we set the max load as 300 Ω, we will be able to reach a conversion ratio of about 1.18, as per Figure 13, before we leave the ZVS region. That seems to equate to an allowed 18% reduction in input (but we will soon show it is only 12% actually). Either way, we can produce ***derating curves*** to show how we can ***tradeoff max load versus input operating range,*** *weighing it against the price of overall expected efficiency, provided of course the range can be achieved or is acceptable in terms of our guiding criteria*.

The fear of predicting and/or really losing efficiency at low line is perhaps one reason LLC converters are still largely being used only where the input is relatively stable (and comfortably so), such as where the LLC converter is driven off the output HVDC rail of a front-end PFC stage. We can see that if we really want wide-input variation, we have to *overdesign* the converter (300 Ω in our example, will only get us 12% input voltage variation factor as explained later). Holdup time can also be a major issue in AC-DC designs in which the LLC converter stage typically follows a conventional PFC stage.

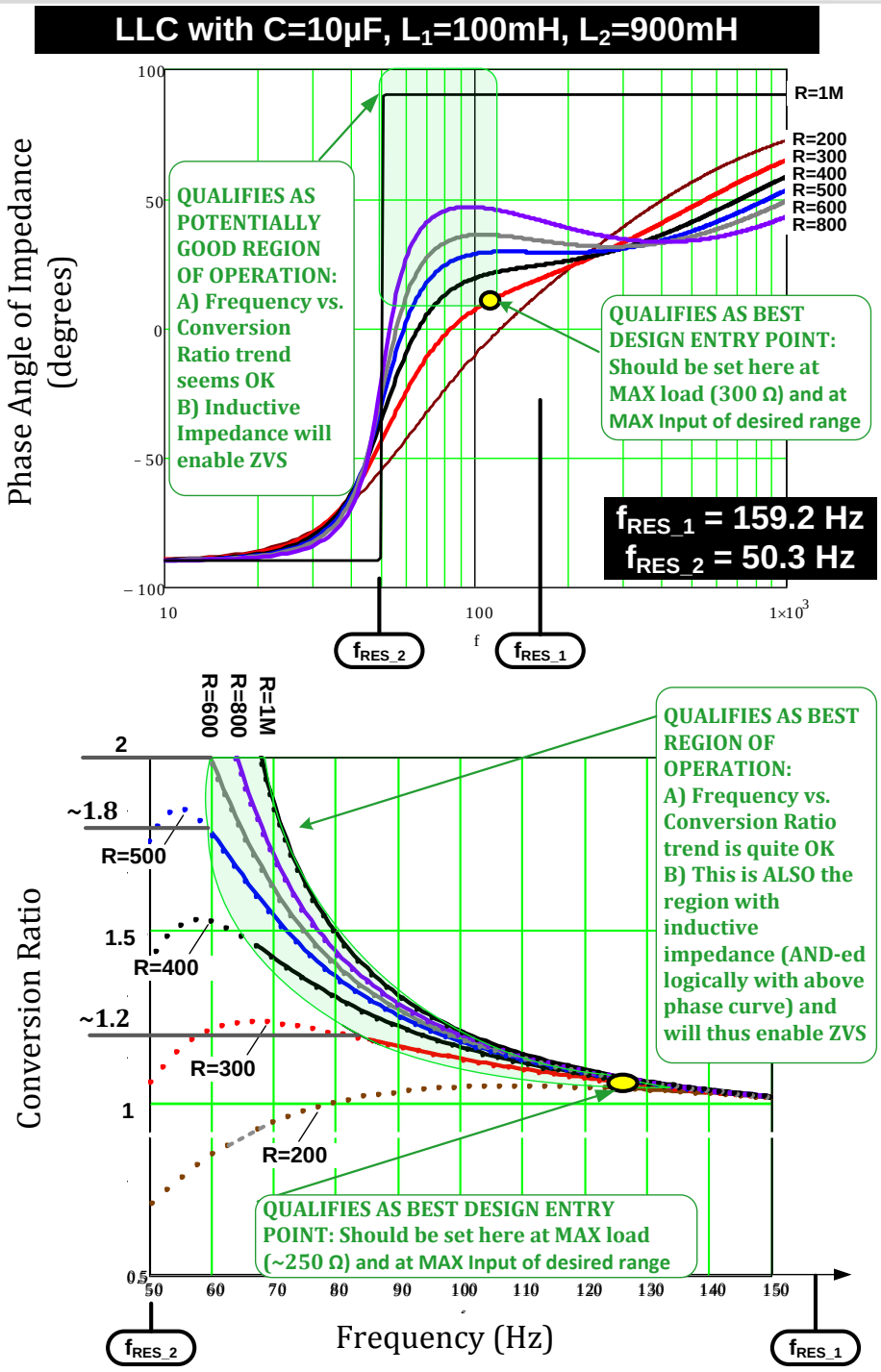


Figure 13: Closeup of phase for different loads, and corresponding conversion ratio (gain) in the usable area of the LLC tank circuit between the two resonant frequencies

Two Resonances in LLC Tank

In related literature, it is often said that the LLC converter has two resonant peaks: one a series resonance between C and L_1, and another "parallel" resonance between C and (L_1 + L_2). So, people call it by many names: f_r, f_s, f_p, f_m, f_o, f_∞ and so on. It can become confusing, which is why we have just preferred to call them f_{RES_1} and f_{RES_2}, based on the simple order they actually appeared in our discussions. Yes, f_{RES_1} does come about from the resonance between C and L_1, whereas the lower frequency peak, f_{RES_2} comes from the resonance between C and (L_1+L_2). But are these series or parallel LC resonances?

We should not get confused by the fact that the conversion ratio (gain) at the first (higher) frequency is less than 1, as is typical of a series LC circuit, whereas the gain at the second (lower) frequency is greater than 1 (which is perceived as true for parallel resonant circuits, in tuned circuits for radio applications etc.). To really find out whether the peaks are series or parallel resonances, we need to plot out the input impedance (as seen by the source). This is presented in Figure 14.

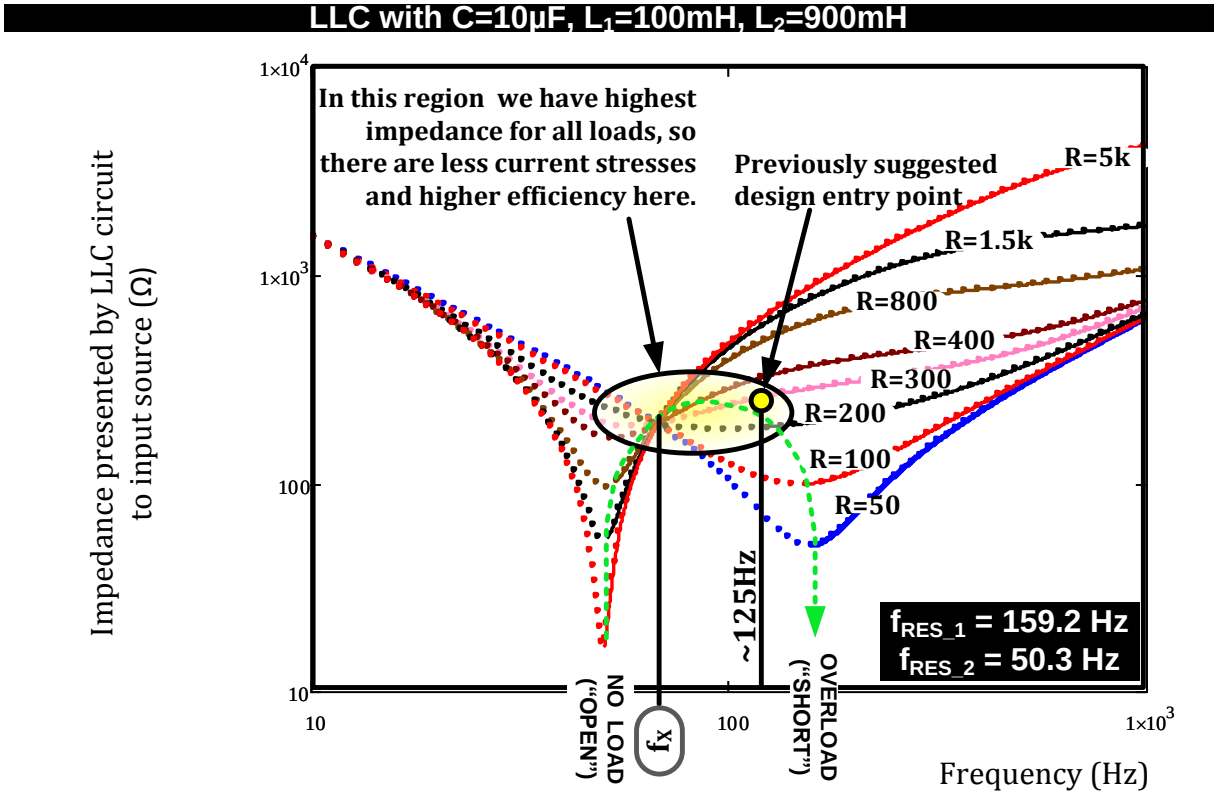
It is interesting that going from a shorted load to no load, the impedance presented to the AC input shifts between what are clearly *two resonant peaks* of series resonant characteristics, because in parallel LC resonance, the impedance becomes very high at resonance, not low as indicated by Figure 14.

One of the contributors to efficiency is switching losses, which we have tried to minimize by invoking ZVS. But that advantage could be easily lost by excessively high conduction losses, as caused by *high circulating currents*. One of the contributors to that circulating current is indeed L_2, which is why typically, L_2 is kept at least 5× larger than L_1 (usually less than 10× though, as explained further below). Especially when we insert a transformer with output diodes, we will see L_2 significantly affects the current distributions in the LLC tank. Therefore, it is recommended to ***keep L_2 between 7 to 11 times L_1 in any practical LLC converter. In our case we have fixed on a factor of 9.***

Note that in a parallel LC, the circulating current sloshes back and forth between the L and C, so the input source may never "see" the high current. But in a series resonant case, the current does pass through the input source and is inversely proportional to the *impedance* the network presents at its input terminals (to the source). If the impedance is high, we will get small circulating currents (and higher efficiency). In Figure 14 we see that there is a *shaded encircled area* of high impedance for almost any load. It is recommended in related literature that we should try to remain here as much as possible. But note that our previously honed choices, R = 250 Ω or R = 300 Ω, fall in a very flat part of the encircled region. In other words, our previous design choice is actually good even from the viewpoint of low conduction losses. We have to do nothing more to optimize.

Just for information, we mention that in related literature, the cusp labeled "f_X" in Figure 14, is mentioned as some sort of LLC converter "design target" because it offers high impedance. Its equation is $f_X = 1/ 2\pi\sqrt{[C\times\{L1+(L2/2)\}]}$. We have however preferred to generalize our approach by describing a certain load resistor

corresponding to max load at high line, one which a) gives an unambiguous direction of correction, and b), makes the network appear just slightly inductive to the source (for ZVS). *The desire for high input impedance is automatically taken care of* as we see from Figure 14.



To the right of the dotted locus line above, for any load, we have inductive phase angle (good for ZVS). To the left we have capacitive. We should thus choose switching frequency so we consciously stay only to the right of this line, at least at max load.

CAUTION: Note that these curves only tell us the input impedance for a given load and frequency, so that we can check whether the network appears inductive (for ZVS) or not. They do *not* provide the frequency variation as we change the load or help pick a good design entry point! That is discussed later.

Figure 14: Plotting input impedance of the LLC tank circuit

PART 3: Microsemi Innovation

One of the perceived disadvantages of the LLC topology is that it handles input line variations poorly. This has restricted it into a niche market, mainly AC-DC, and placed after a Power Factor Correction stage supplying a steady 400V DC to the LLC Half-Bridge. It certainly could be of great advantage to achieve a wide input variation with LLC, say 2:1 or better.

Another perceived disadvantage is that at light loads, LLC engineers are still not able to guarantee operation is restricted at the upper end, especially at light loads. So most LLC controllers only place bounds on the lowermost frequency. However it is advantageous to specify the upper limit too, because for example, the designer may wish to stay decisively below 150kHz, which is the start of the CISPR 22 (EN55022) conducted emissions band. If operation can be guaranteed below 150 kHz for a wide line variation, say 4:1 (e.g. 100VDC to 400VDC, or 110VAC to 240VAC), along with a full load variation (zero to max), it can be of great help in almost eliminating input filtering, especially in AC-DC applications. It could also be of great help in minimizing effects of switching converters on signal integrity where power and data coexist, such as in networking applications.

However the biggest stumbling block to widespread adoption of LLC in industry is simply this: it does not yet fill into a predictable design schedule, so essential in modern development…and that in turn is because engineers still adopt a trial and error approach to fixing the L, L and C values, along with the turns ratio.

In December 2012, Microsemi achieved a breakthrough, and as a result, a predictable design methodology is emerging to account for all the weaknesses above --- wide input variation (4:1 estimated), set upper and lower frequency limits and a commercially acceptable design procedure with minimum bench tweaking.

AND8311/D

Understanding the LLC Structure in Resonant Applications

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ON Semiconductor

ON Semiconductor®

http://onsemi.com

The resonant LLC topology, member of the Series Resonant Converters (SRC) begins to be widely used in consumer applications such as LCD TVs or plasma display panels. In these applications, a high level of safety and reliability is required to avoid catastrophic failures once products are shipped and operated in the consumer field. To face these new challenges, ON Semiconductor has recently released to new controllers, the NCP1395 (low−voltage) and the NCP1396 (high−voltage) dedicated to driving resonant power supplies, usually of LLC type. However, before rushing to design a converter of this type, it is important to understand the resonant structure alone, object of the present application note.

The LLC converter

The LLC converter implies the series association of two inductors (*LL*) and one capacitor (*C*). Figure 1 shows a simplified representation of the resonant circuit where:

L_s is the series inductor
L_m is the magnetizing inductor
C_s represents the series capacitor

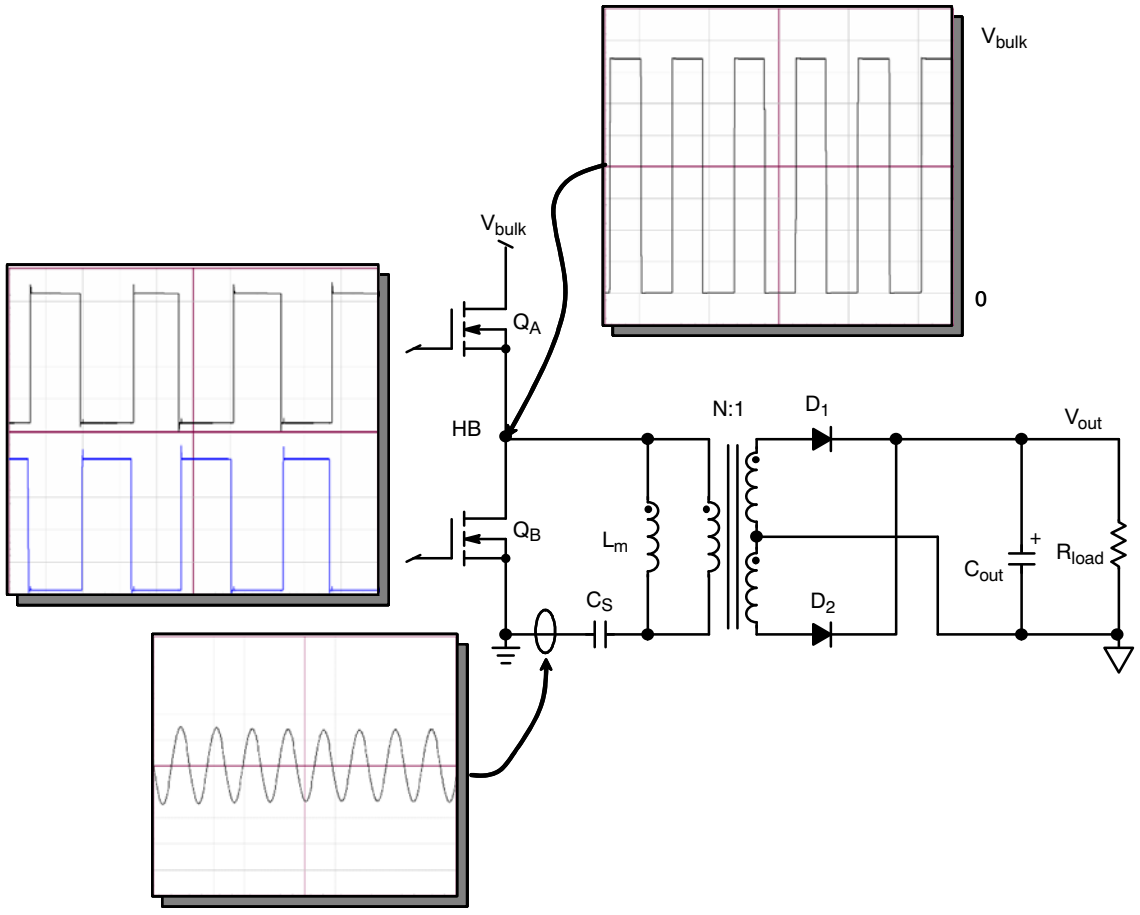


Figure 1. The LLC Topology Uses a Half−Bridge Configuration to Drive the Resonant Circuit

The operating principle is rather simple: a constant 50% duty−cycle switching pattern drives Q_A − Q_B gates and a high−voltage square wave appears on node HB. By adjusting the switching frequency, the controller can control the power flow depending on the output demand. As a transformer is needed for isolation purposes, its magnetizing inductance plays the role of the second inductor L_m. The series inductor, L_s, can either be a separated element or physically lump into the transformer. In this case, a voluntary degradation of both primary and secondary coupling naturally increases the leakage inductance which can act as the series element. There are pros and cons to include the leakage element in the transformer. The cost and the absence of saturation play in favor of the integration but the difficulty to keep a precise value from lots to lots associated with leaky transformers (radiated noise) has to be kept in mind when selecting the final configuration.

When studying the resonant converter, it is convenient to reduce the architecture to a passive element arrangement such as presented on Figure 2. The high−voltage square signal is replaced by its fundamental content thanks to the first harmonic approximation (the so−called FHA in the literature): because we operate a tuned LC filter, all harmonics can be considered as rejected and only the fundamental passes through. Of course, this statement holds as long the controller drives the resonating work in the vicinity of its resonant frequency. Figure 2 offers such a simplified representation of the resonant cell, actually pointing out a series impedance (L_s and C_s) with a parallel impedance (L_m and the reflected load).

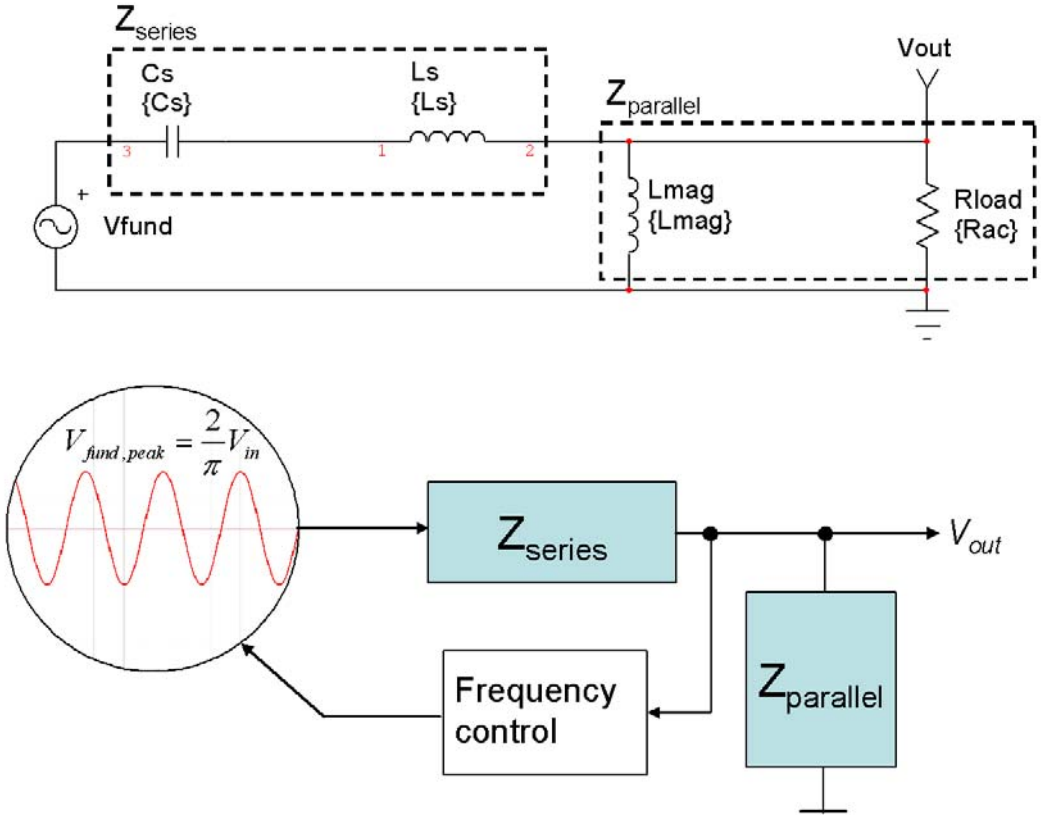


Figure 2. The Impedance Representation Makes the LCC Operation Easier to Understand

Depending on the loading, the network resonant frequency varies between two different values:

- R_L = 0, short−circuit, L_m disappears and Z_{series} becomes a short. The series resonant point for Z_{series} is thus

$$F_{max} = F_S = \frac{1}{2\pi\sqrt{L_S C_S}} \quad \text{(eq. 1)}$$

At $F_{sw} = F_S$, Z_{series} becomes a short and the ac transfer function drops to 1 or 0 dB.

- $R_L = \infty$, light or no load condition, L_m appears in series with L_s and the whole network resonates to

$$F_{min} = \frac{1}{2\pi\sqrt{(L_S + L_m)C_S}} \quad \text{(eq. 2)}$$

- $0 < R_L < \infty$, the resonance which combines L_m and L_s, shifts depending on the total quality coefficient.

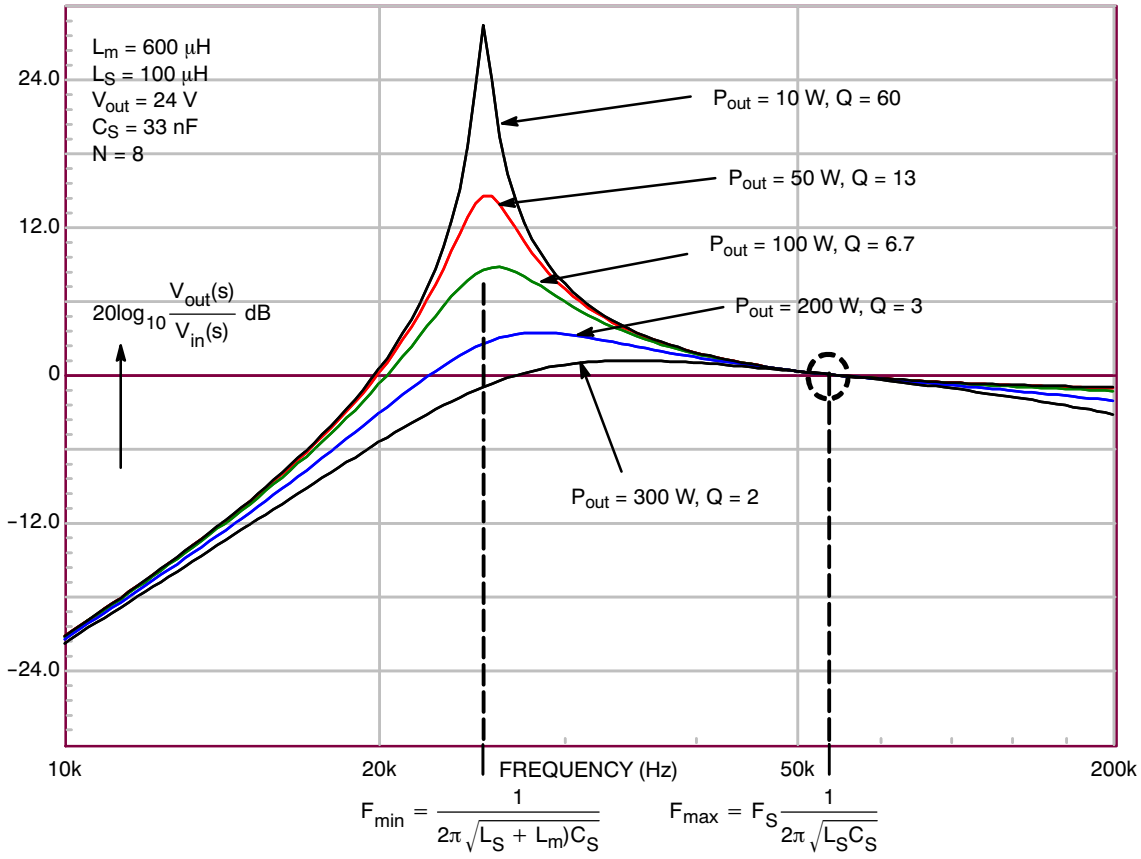


Figure 3. The AC Response of Figure 2 Circuit with Various Load Conditions

This is actually what Figure 3 plots suggest by showing the ac transfer function of Figure 2 as the load changes.

If we now study the impedance seen from the half−bridge node, we have an expression showing a series association of inductors and a capacitor. Sticking to Figure 2 sketch and writing the impedance seen between ground and Node 3, we have:

$$Z_{in} = Z_{L_S} + Z_{C_S} + Z_{L_{in}} \| R_{ac} \quad \text{(eq. 3)}$$

$$Z_{in} = \left[\frac{(\omega L_m)^4 R_{ac}^{\,2}}{\left(R_{ac}^{\,2} + \omega^2 L_m^{\,2}\right)^2} + \left(\omega L_S - \frac{1}{\omega C_S} + \omega L_m \frac{R_{ac}^{\,2}}{R_{ac}^{\,2} + \omega^2 L_m^{\,2}} \right)^2 \right]^2 \quad \text{(eq. 4)}$$

In the low frequency portion, the terms associated with inductors are of less importance and C_s dominates. The impedance is thus capacitive. As the frequency increases, the inductive portion starts to kick−in and the impedance goes up. This is what Figure 4 describes. As one can see, all the curves go through point A whose value is independent from the resistive loading. For the sake of a friendly exercise, we can solve Equation 4 with two different R_{ac} values and find the frequency at which input impedances equal. We obtain:

$$\omega_A = \sqrt{\frac{2}{L_m C_S + 2 L_S C_S}} \quad \text{(eq. 5)}$$

If we substitute this value into Equation 4, the impedance at point A is:

$$Z_A = \frac{\frac{L_m}{2L_S} L_S \omega_S}{\sqrt{\frac{L_m}{2L_S} + 1}} \quad \text{(eq. 6)}$$

If we define the ratio R by L_m/L_s, we can re−arrange equation 6:

$$Z_A = \frac{R}{\sqrt{2(R+2)}} \sqrt{\frac{L_S}{C_S}} = \frac{R}{\sqrt{2(R+2)}} Z_O \quad \text{(eq. 7)}$$

Where Z_0 represents the characteristic impedance of the series resonant network. Using the numerical values noted in the graphs, we obtain a frequency of 43.8 kHz and an impedance of 38.3 dBΩ (82.6 Ω).

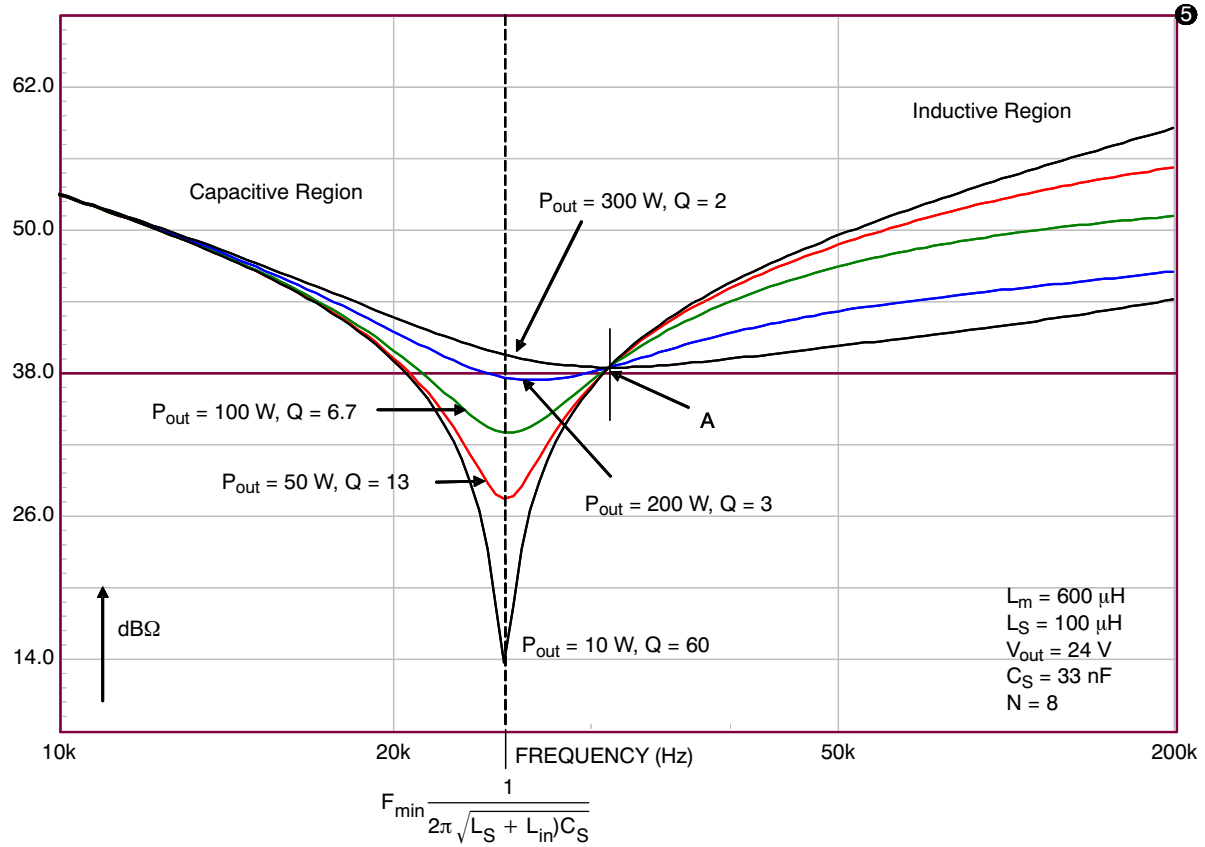


Figure 4. Impedance Plots at Various Power Levels

If we now observe the resonant current waveforms in a LLC converter working below or above the series resonance F_s, we have different types of operation:

- Capacitive mode: in this mode, where the current leads the voltage, the bridge MOSFETs operate in zero current switching (ZCS). ZCS means that power MOSFETs are turned−off at zero current. Back to figure 3, we can see that the output level goes up as the frequency increases.
- Inductive mode: in this mode, the current lags the voltage and the power switches are turned−on at zero volt (ZVS), virtually eliminating all capacitive losses. This operating way implies that a certain delay exists before operating the concerned MOSFET so that its body diode turns on first. Observing figure 3, the output level goes down as the frequency increases.

Most of the LLC converters operate in the inductive region for the second bullet reason. Also, given the feedback polarity, if by mistake the closed−loop LLC enters the left side of the resonance, the control law reverses and a power runaway obviously occurs. It is thus extremely important to clamp down the lower frequency excursion in fault condition or during the startup sequence to avoid falling on the other slope of the characteristics.

The inductive region can be split into two other regions, depending where you operate compared to the resonant series frequency F_s, as defined by Equation 1. Figure 5 represents the classical set of curves often found in the dedicated literature:

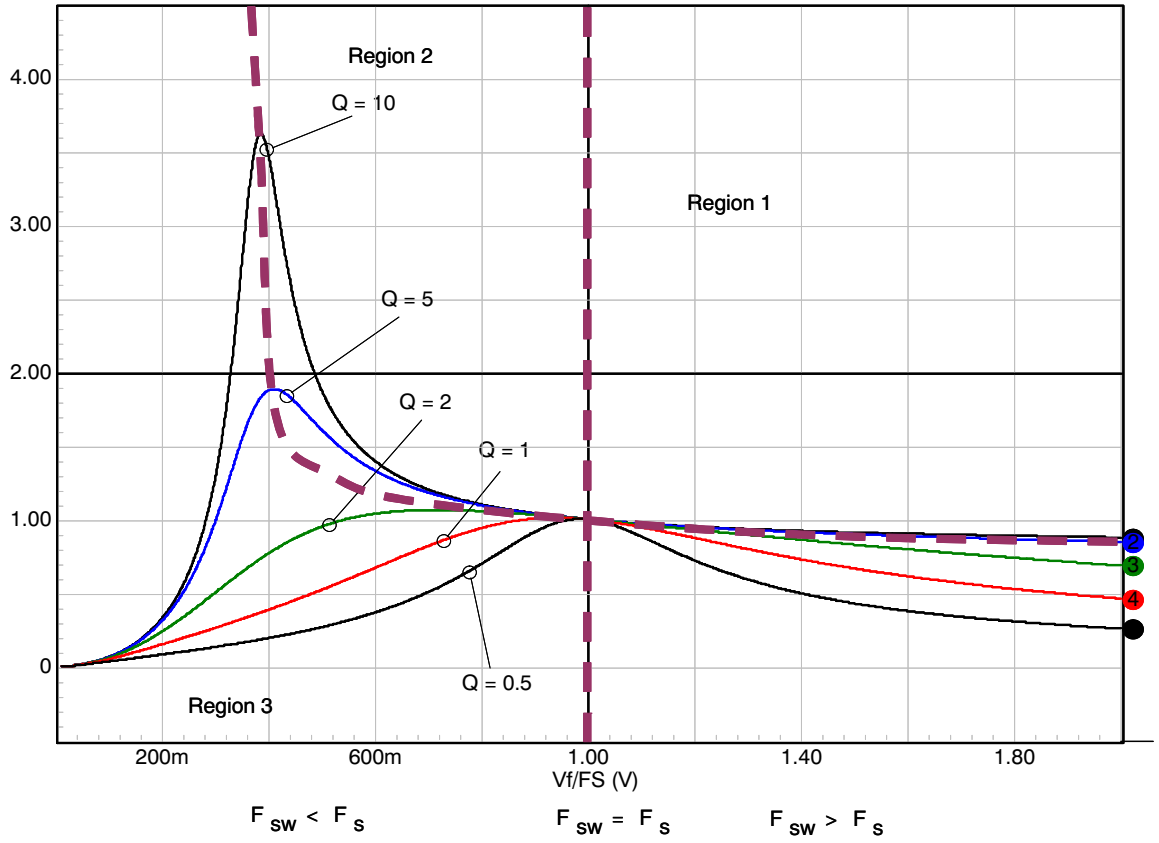


Figure 5. Typical Transmittance Curves with Various Loading Conditions, Highlighting Three Distinct Regions

Region 3 is the capacitive mode where you do not want to operate since ZVS is a wanted feature for the power switches. In regions 1 and 2, you still have ZVS on the power MOSFET's and the output diodes are operated in Zero Current Switching (ZCS), cancelling all associated losses at turn−off. Before discussing the benefits of a particular solution, let us have a look at the various operating phases the LLC converter is made of.

Operating Waveforms Below the Series Resonance, $F_{sw} < F_s$

For this example, we have selected a set of elements which operate the converter below the series resonance defined by Equation 1. The following value have been used:

L_m = 700 µH
L_s = 116 µH
C_s = 28 nF
N = 8

$$F_{max} = F_S = \frac{1}{2\pi\sqrt{L_S C_S}} = \frac{1}{6.28 \times \sqrt{116\mu \times 28n}}$$

$$= 88.3 \text{ kHz}$$

$$F_{min} = \frac{1}{2\pi\sqrt{(L_S + L_m)C_S}}$$

$$= \frac{1}{6.28 \times \sqrt{(116\mu + 700\mu) \times 28n}} = 33 \text{ kHz}$$

F_{sw} = 70 kHz at full load and nominal input voltage.

The converter delivers 24 V@10 A from a 380 Vdc input source and a simulation has been performed using the above values. Figure 6 shows the main waveforms obtained from the simulator. Let us study the switching events step by step to learn about the LLC behavior in this region.

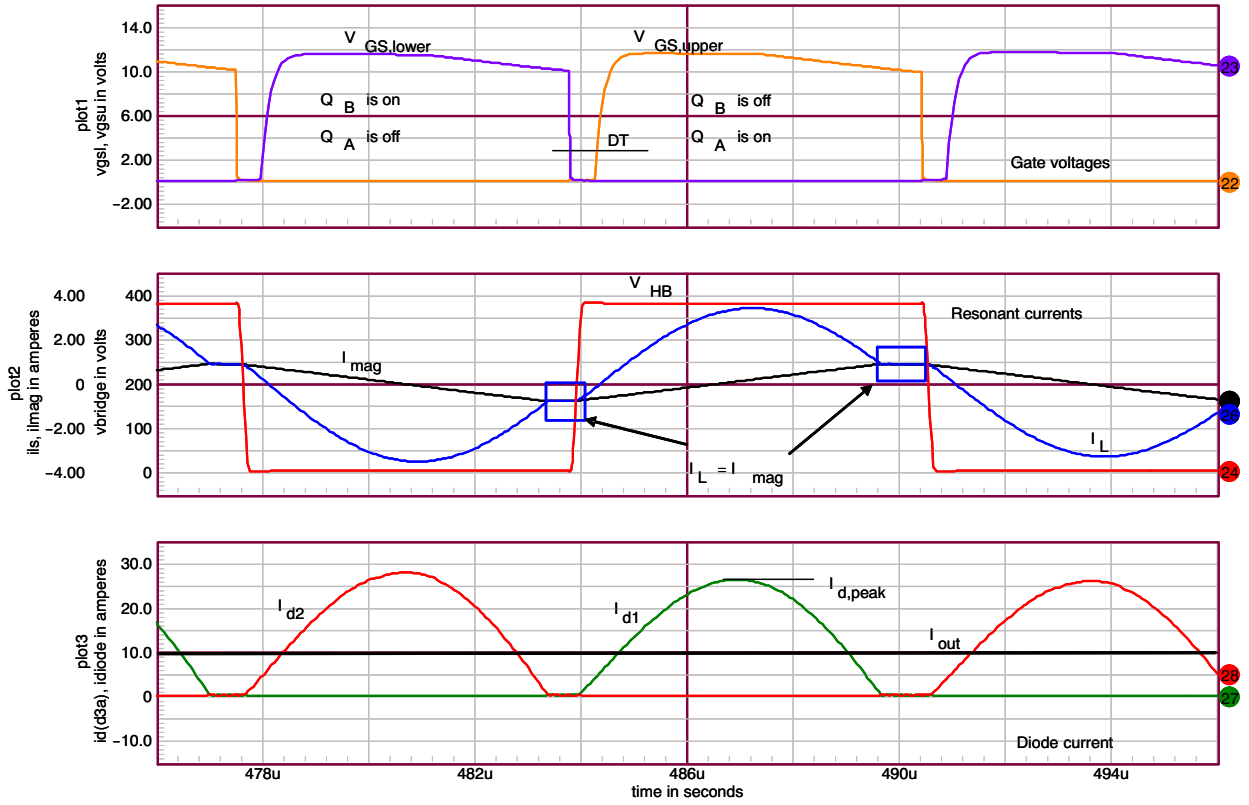


Figure 6. Waveforms Obtained for a Converter Operated Below the Series Resonant Frequency

Q_A is off, Q_B is on, D_2 is conducting :

The low−side MOSFET Q_B imposes a 0 V potential on the half−bridge node and the current circulates from its drain to source (first quadrant). The upper parasitic capacitor C_{ossA} is fully charged to the input voltage V_{bulk} since the HB node is grounded by Q_B. The secondary diode D_2 is conducting and imposes a voltage reflection $-NV_{out}$ over the magnetizing inductor L_m. Its current linearly decreases with a slope of $-NV_{out}/L_{in}$. As this inductor is dynamically shorted by the voltage reflection, it does not participate to the on−going resonance between L_s and C_s which deliver the output energy (the input source is out of the picture). The current flowing into the transformer primary side (given its theoretical representation, L_m associated to a perfect transformer) is the main current I_L minus the magnetizing current I_{mag}. D_1 is blocked and undergoes twice the output voltage given the transformer coupling. The circuit resonates to F_s as L_m is shorted. Figure 7 depicts the situation during this period of time.

Q_A is off, Q_B is on, D_2 turns off:

As the network current I_L resonates in a sinusoidal manner, its amplitude peaks and then starts to dip towards 0. When it reaches a level equal to that of the magnetizing current, no current circulates in the transformer anymore: D_2 blocks and the voltage reflection over L_m disappears. The magnetizing inductor now comes back in series with L_s and C_s and changes the resonant frequency from F_s to F_{min}: the LLC converter is really a multi−resonant structure and the plateau − actually a small arch of a lower sinewave oscillation − in the current as it appears on figure 6 testifies for it. Both diodes are now blocked and this moment lasts until Q_B opens. Figure 8 represents the circuit during this time. As one can see, the output capacitor alone supplies the energy to the load.

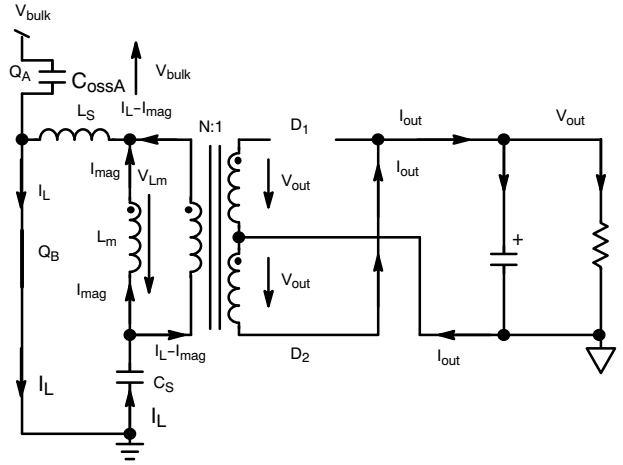


Figure 7. Q_A is Off, Q_B is On and Diode D_2 Conducts Current. L_m is Off the Picture as it is Dynamically Shorted by the Output Voltage Reflection.

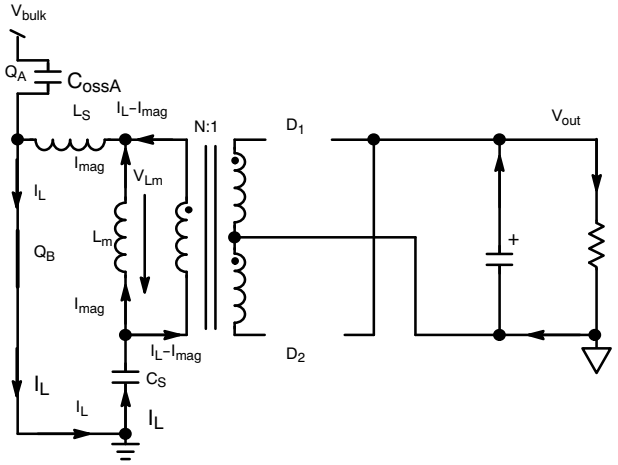


Figure 8. Q_A is Off, Q_B is On and Diode D_2 Blocked. L_m Comes Back Again in the Resonating Network and Changes the Resonant Frequency to F_{min}.

Q_A is off, Q_B is Off, Both Secondary Diodes are Blocked

Both transistors are now open, this is the dead−time period (DT on Figure 6). The dead−time is placed here to avoid cross−conduction between both MOSFETs but also to favor Zero Voltage Switching as we will see in a moment. Because the current was circulating from drain to source in Q_B, the circuit no longer sees an ohmic path when this transistor opens. The current strives to find a way through the parasitic drain−source capacitors C_{oss} of both Q_A and Q_B: C_{ossB} starts to charge (it was previously discharged by Q_B being on) and given the rise of V_{HB} towards the high voltage rail, C_{ossA} sees its terminals voltage going down to zero and then reversing (Figure 9). At this moment, when the HB node reaches V_{bulk} + V_f, the body−diode of Q_A conducts and ensures energy re−cycling through the input source (Figure 10). You understand that this dead−time period must last a time long enough to allow for the complete discharge of C_{ossA} before re−activating Q_A so that its body−diode turns on first. If not, hard switching occurs and efficiency suffers.

As currents are oscillating, a time is reached where I_L and I_{mag} are no longer equal (end of the plateau) and a current circulates again in the primary side. D_1 starts to conduct and NV_{out} appears across L_m :the resonant frequency goes back from F_s to F_{min}. Figure 10 describes this moment.

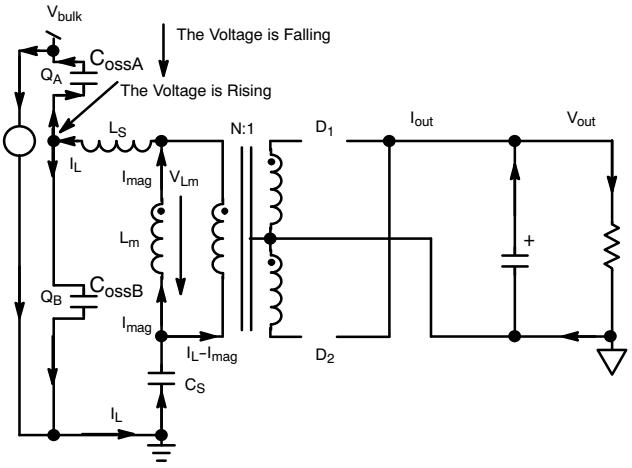


Figure 9. Q_A is Off, Q_B is Off. The Current Finds a Circulating Path Through Both Transistors C_{oss}, Both Secondary−Side Diodes are Off.

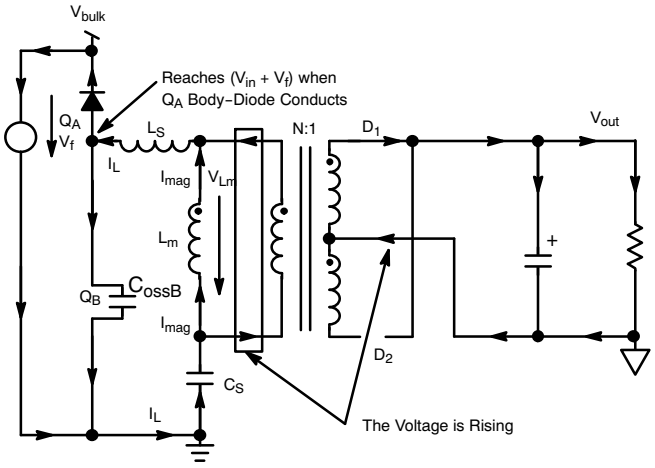


Figure 10. Q_A and Q_B are Still Off. The Current Finds a Circulating Path through the Upper−side Body Diode. D1 Starts Conducting at the End of the Plateau when $I_L \neq I_{mag}$.

Q_A is on, Q_B is off, D_1 is on

Now that Q_A body−diode is conducting, we have a negligible voltage across its drain and source terminals: we can therefore safely turn it on and benefit from Zero Voltage Conditions. As we have a sinusoidal waveform in the network, the resonating current reaches zero and reverses.

L_m is still dynamically shorted as D_1 is conducting. The energy is delivered by the source to the output load. This is illustrated by Figure 11.

Q_A is on, Q_B is off, D_1 turns off

The current I_L is moving down and reaches the magnetizing current level, we are the second plateau on Figure 6. At this point, no current circulates in the transformer and D_1 naturally blocks. As explained before, the magnetizing inductor re−appears in the circuit since the output voltage reflection is gone. The resonant frequency changes from F_{min} to F_s and the energy to the load is delivered by the output capacitor alone. Figure 12 shows the circuit state during this event.

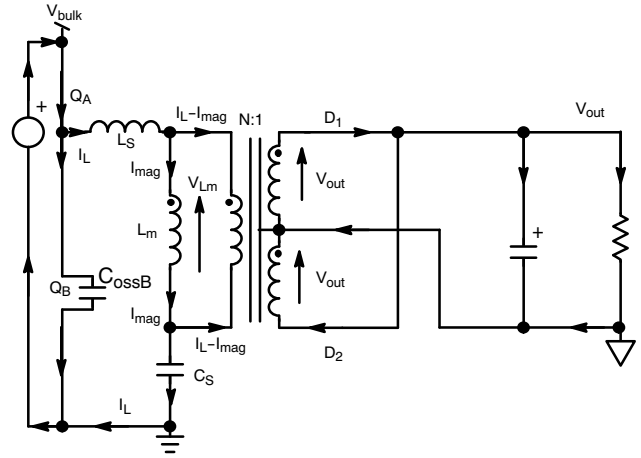


Figure 11. The Current is Now Flowing from the Source to the Output Via the Upper−Side Transistor Q_A.

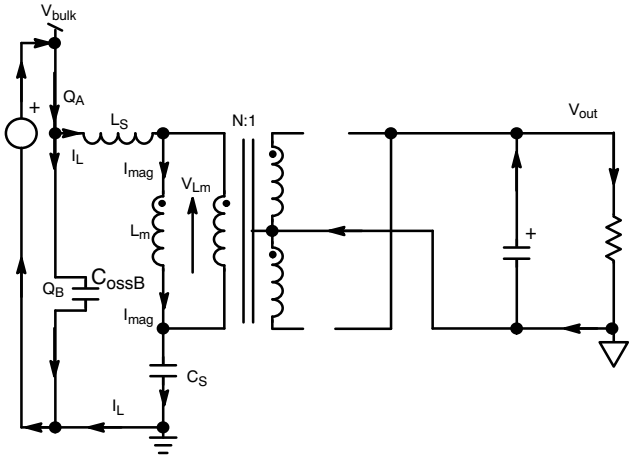


Figure 12. As Both Diodes are Off, the Network Includes the Magnetizing Inductance which Changes the Resonant Frequency.

QA is of, QB is off, both secondary diodes are blocked

At a certain time, both transistors block and only their drain−source capacitors remain in the circuit. The current keeps circulating in the same direction but C_{ossA} starts to charge: the voltage on the HB node drops and C_{ossB} depletes towards ground. The drain falls down in a resonating manner, involving both C_{oss} in parallel and the equivalent inductor made of $L_s + L_m$. Figure 13 represents the circuit during this event.

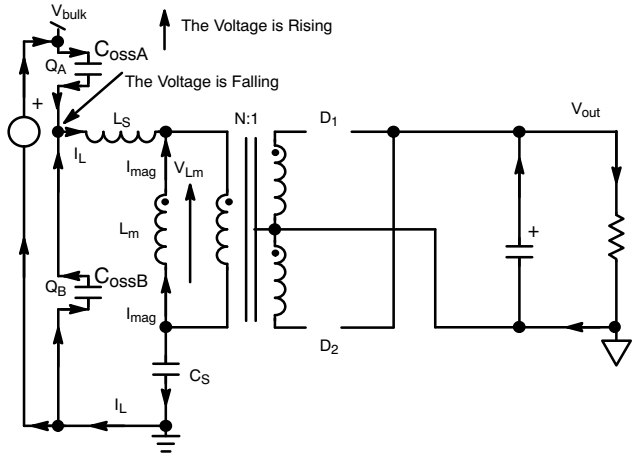


Figure 13. The Current is Still Flowing through the Source and Contributes to Discharge C_{ossB}.

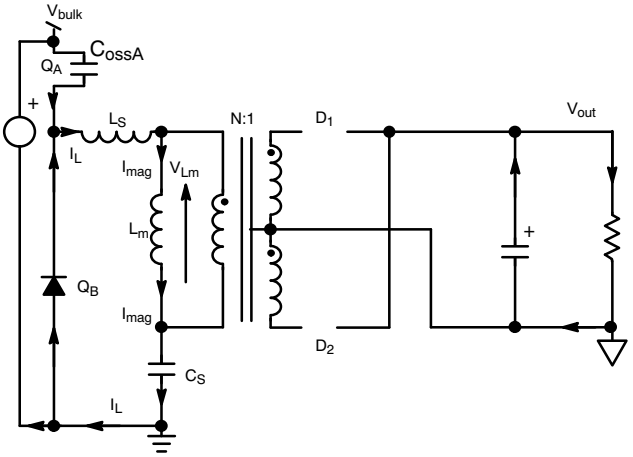


Figure 14. When the Voltage on the Node HB Swings Below Ground, Q_B Body−Diode Conducts.

The bridge voltage further dips and becomes negative until the body−diode of Q_B conducts. This is what Figure 14 suggests. At the end of the plateau, where $I_L = I_{mag}$, D_2 will start conducting, reflecting $-NV_{out}$ over the primary inductance. The energy comes from C_s and L_s, as the source is not playing any role here. The controller now activates Q_B in ZVS and the transistor conducts in its 3rd quadrant for a few moments, until the current reaches zero and swings negative: we are back at the beginning of the first phase.

Zero Voltage Switching

Figure 15 zooms on these ZVS events and show the various signals in play. The MOSFET current starts to be negative before the appearance of its gate−source bias: this is the body−diode conduction period. Then the MOSFET turns−on at a V_f across its drain−source terminals but the current is still negative: we are in the 3rd quadrant conduction. Finally, the current becomes positive and flows from drain to source, back to the 1st quadrant.

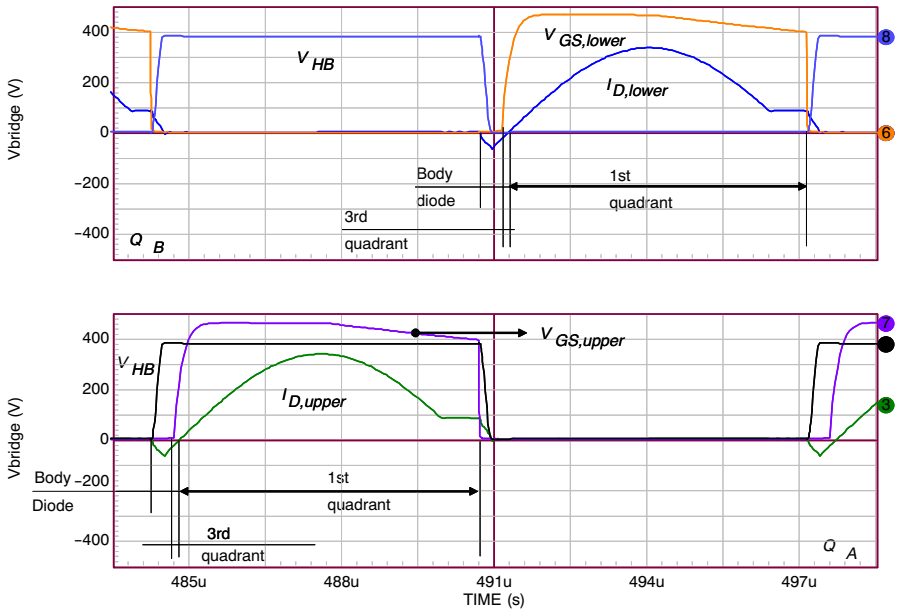


Figure 15. Simulation Results Zooming on the MOSFET Variables

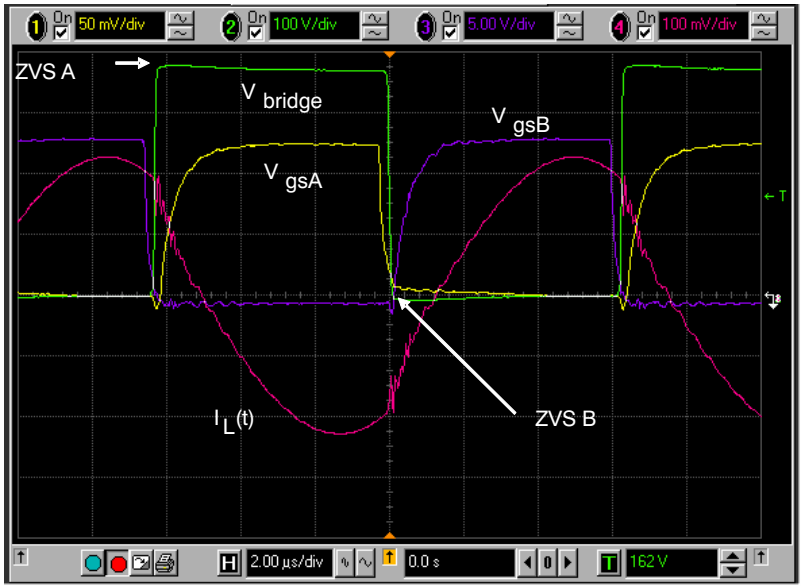


Figure 16. Measured Signals on a Demonstration Board Showing the ZVS Operation on Q_A.

The selection of a controller where the dead−time is adjustable therefore represents an important selection argument to fine tune the behavior and ensure a minimum conduction period of both body−diodes.

Zero Current Switching

By the term ZCS, we assume a natural blocking event when the current in the semiconductor is zero. When operating the LLC converter below F_s, as it is the case in this

example, both secondary−side diodes are operated in ZCS. The current in the concerned diode (D_1 or D_2) naturally reaches 0 when the magnetizing current I_{mag} equals the main resonating current I_L. This is the plateau on figure 6. Observing the diode current in this particular mode gives smooth signals as shown on Figure 17.

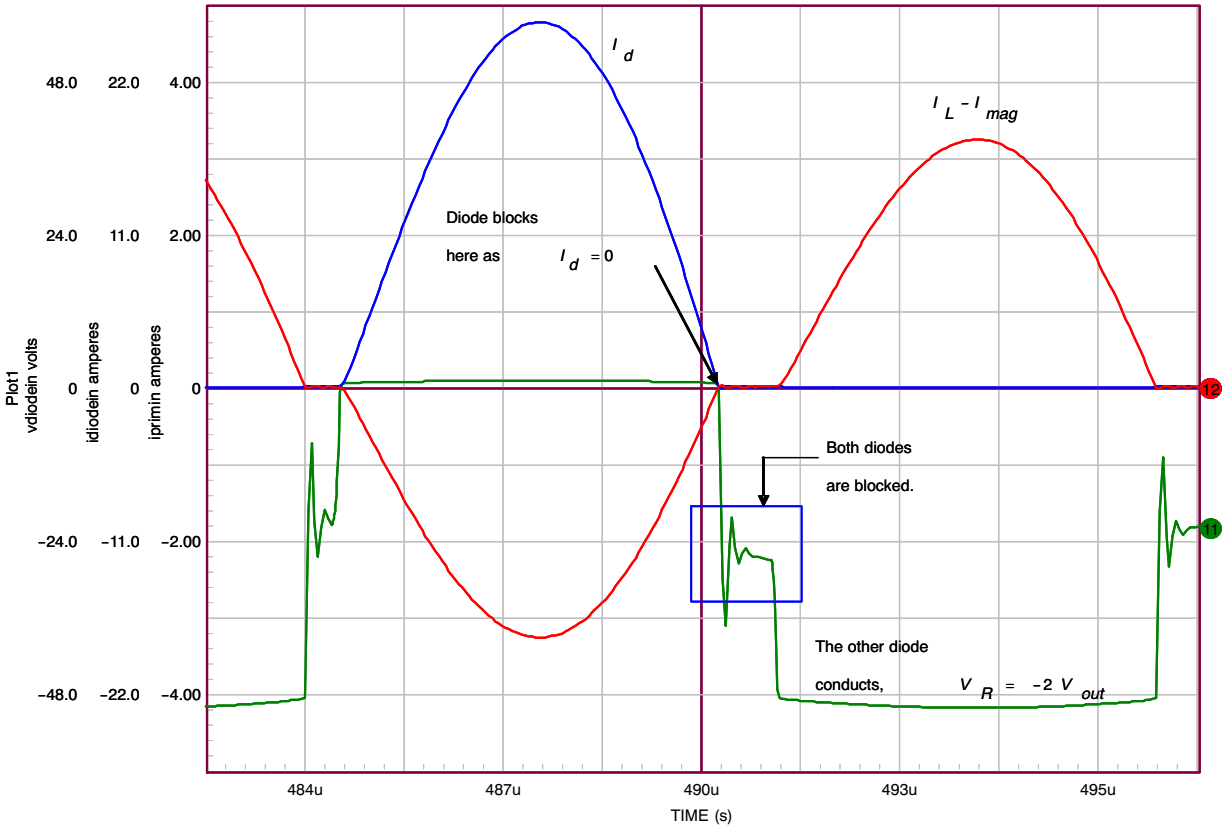


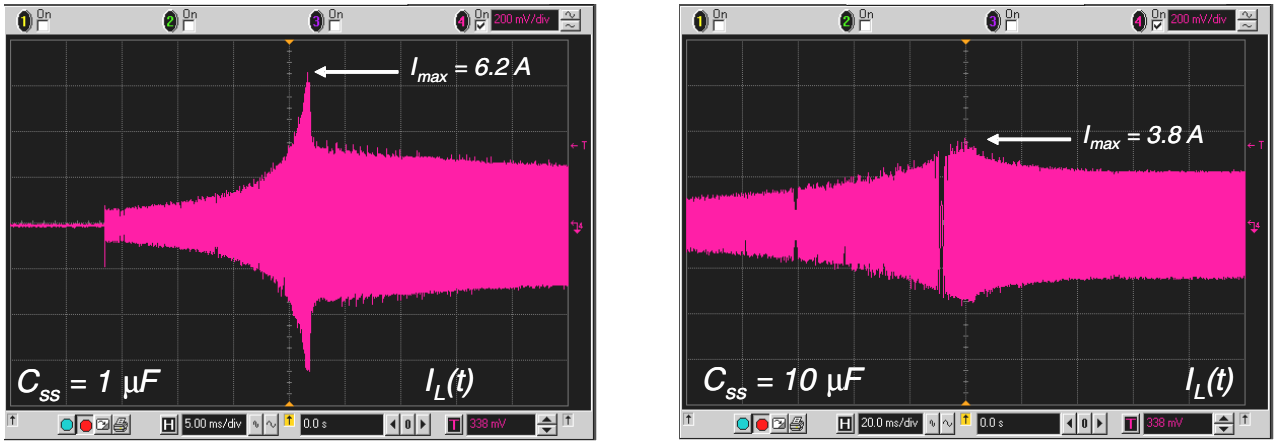
Figure 17. The Secondary−Side Diodes are Naturally Blocked When the Primary Current Vanishes to Zero

Startup sequence and short−circuit

During startup or short−circuit, the magnetizing inductor is shorted and the resonant frequency becomes F_s. Because we designed the LLC converter to operate at a frequency lower than F_s, the operating fault mode (lack of feedback) of the controller naturally lies below F_s. In other words, if the LLC converter quickly starts−up, without soft−start at all, the controller will quickly sweep from a high frequency value down to the minimum authorized in case of fault. The current in the network can therefore peak to a high value (at resonance, the LC impedance is only limited by ohmic losses) and destroy the power MOSFETs instantaneously. Figure 18a shows an oscilloscope shot captured on a LLC circuit started with a short soft−start period (≈20 ms): the current peaks to 6 A. Increasing the soft−start period to a few hundred of milliseconds clearly helps to smooth the peak and keep it below 4 A.

Short−circuit protection is more difficult to achieve given the resonating nature of the circuit. Some solutions exist like differentiating the voltage across the capacitor C_s and routing the resulting voltage to a fast latch input. Figure 19 shows this solution where the component values must be adjusted to avoid false triggering in normal operating transients.

Reference [1] has experimented a solution where the resonating capacitor is split in two values − C_s/2 − and two high voltage diodes clamp the voltage excursion between ground and the bulk rail. As the voltage across the capacitor is limited, the resonant current is also clamped. The solution appears in Figure 20. There are several drawbacks associated to the usage of this diode arrangement such as a variable clamping level in relationship to the high−voltage rail. However, experience shows that this simple circuit brings an efficient protection to the converter experiencing a short−circuit. The diodes must be of fast types, MUR260 can be selected for this purpose.



a b

Figure 18. The LLC converter peaks to a high current if started too quickly. Increasing the soft−start sequence naturally calms down the current excursion.

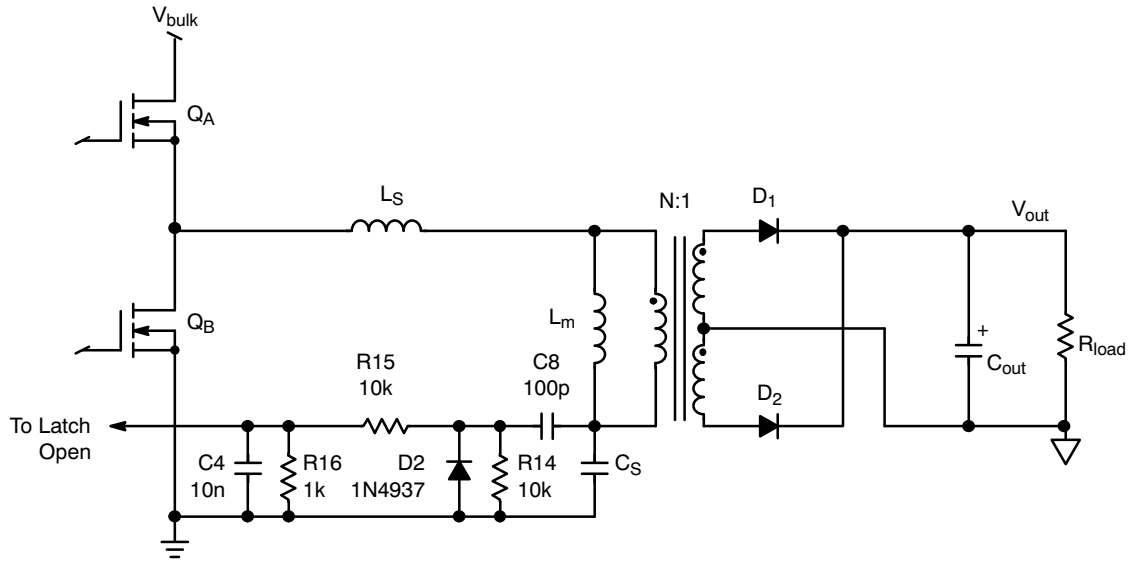


Figure 19. Differentiating the Voltage Across the Resonant Capacitor Gives an Indication of the Current Flowing Through it

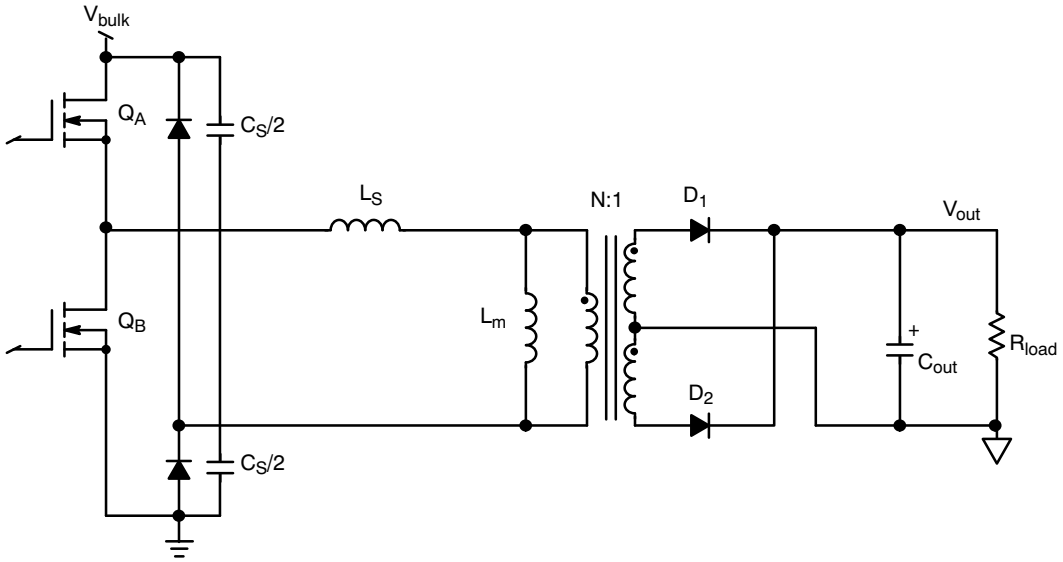


Figure 20. To Keep the Voltage Excursion on the Resonant Capacitor within Safe Limits, a Diode Network Forbids any Lethal Runaways

Operating Waveforms Above the Series Resonance, $F_{sw} > F_s$

For this example, we have selected a set of elements which operate the converter above the series resonance defined by equation 1. The following values have been used:

L_m = 1.2 mH
L_s = 200 μH
C_s = 44 nF
N = 6

$$F_{max} = F_S = \frac{1}{2\pi\sqrt{L_S C_S}} = \frac{1}{6.28 \times \sqrt{200\mu \times 44n}}$$

$$= 53.7\ \text{kHz}$$

$$F_{min} = \frac{1}{2\pi\sqrt{(L_S + L_m)C_S}}$$

$$= \frac{1}{6.28 \times \sqrt{(200\mu + 1.2m) \times 44n}} = 20\ \text{kHz}$$

F_{sw} = 70 kHz at full load and nominal input voltage.

The converter still delivers 24 V@10 A from a 380 Vdc input source and a simulation has been conducted using the above values. Figure 21 shows the main waveforms obtained from the simulator. There are several differences between this operating mode and the previous one:

1. In the previous mode, the magnetizing inductance was released at a point where both secondary−side diodes were blocked ($I_L = I_{mag}$). The resonant frequency was therefore moved from F_s to F_{min} during a certain time (the plateau on Figure 6). When operated above the series frequency F_s, the magnetizing inductance is always shorted by the reflected voltage NV_{out} or $-NV_{out}$ as one of the secondary diode is always conducting. In other words, a single resonance occurs in this mode at full power, implying L_s and C_s only. L_m is out of the picture as long as the converter operates in continuous conduction mode (full load operation).
2. Observing Figure 21, we can see that the main resonant current I_L changes from a sinusoidal waveshape to a straight line, implying a change in the operating mode. This change occurs when a voltage discontinuity appears across L_s terminals. This discontinuity comes from the delay between the bridge signal V_{HB} and the reflected voltage polarity across the magnetizing inductor L_m. Figure 22 zooms on this particular moment where we can see that the bridge voltage goes down to zero via the body−diode activation of Q_B, but because there is still current flowing in the transformer primary side (I_L is different than I_{mag}), one of the secondary diode is still conducting, imposing a constant reflected output voltage across L_m. The voltage across L_s is up by one step which starts to reset it towards zero. This is the beginning of the linear segment, if we consider the voltage across L_s almost constant. When I_L reaches the magnetizing current I_{mag}, the conducting diode blocks and the primary current transitions to the second diode which now conducts. The voltage polarity across L_m reverses and the resonant current goes back to its sinusoidal shape. The next segment occurs when Q_B opens and the bridge voltage jumps to V_{in} via Q_A body−diode. This segment lasts until I_L reaches I_{mag} again.

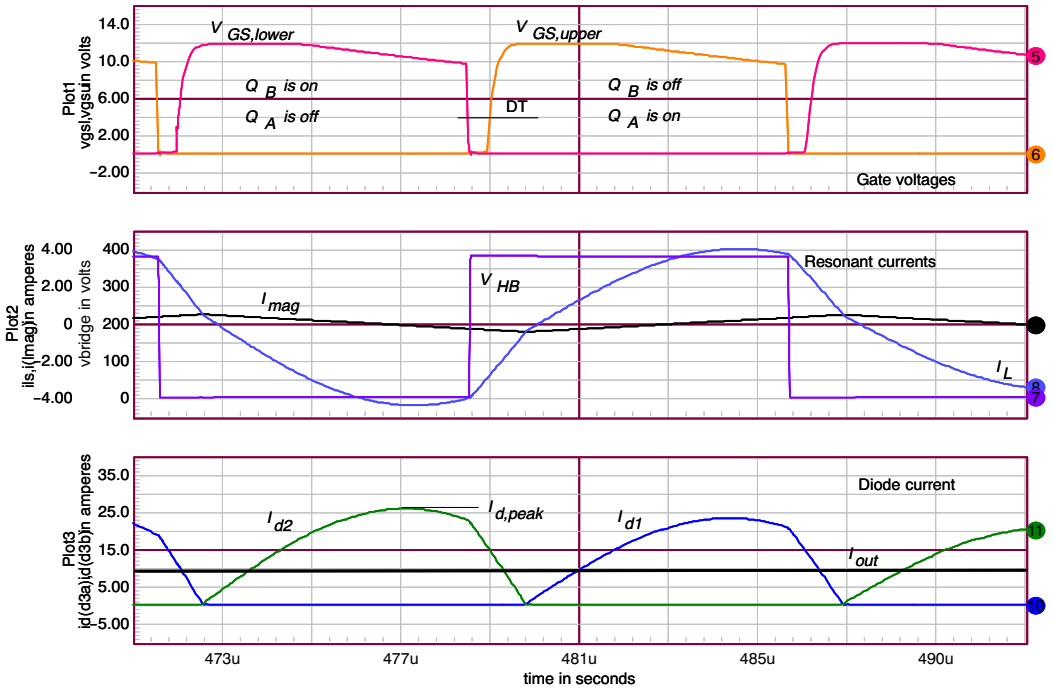


Figure 21. Figure 6 Waveforms Updated with a Converter now Operating Above the Series−Resonant Frequency F_s

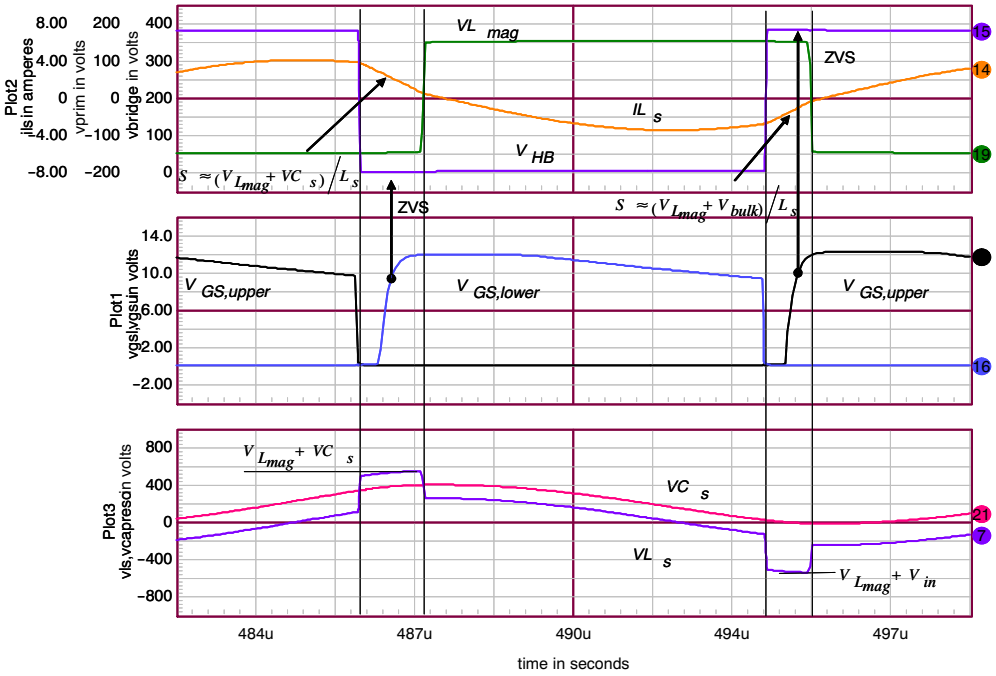


Figure 22. The Voltage Discontinuity Across Ls Induces a Linear Segment in the Resonant Waveform

1. The diode are still operated in ZCS despite a switching frequency above F_s. This is thanks to the linear reset taking place on the resonant current (the segment on $I_L(t)$) which smoothly leads the concerned diode to a blocking state. Figure 23 illustrates this fact.

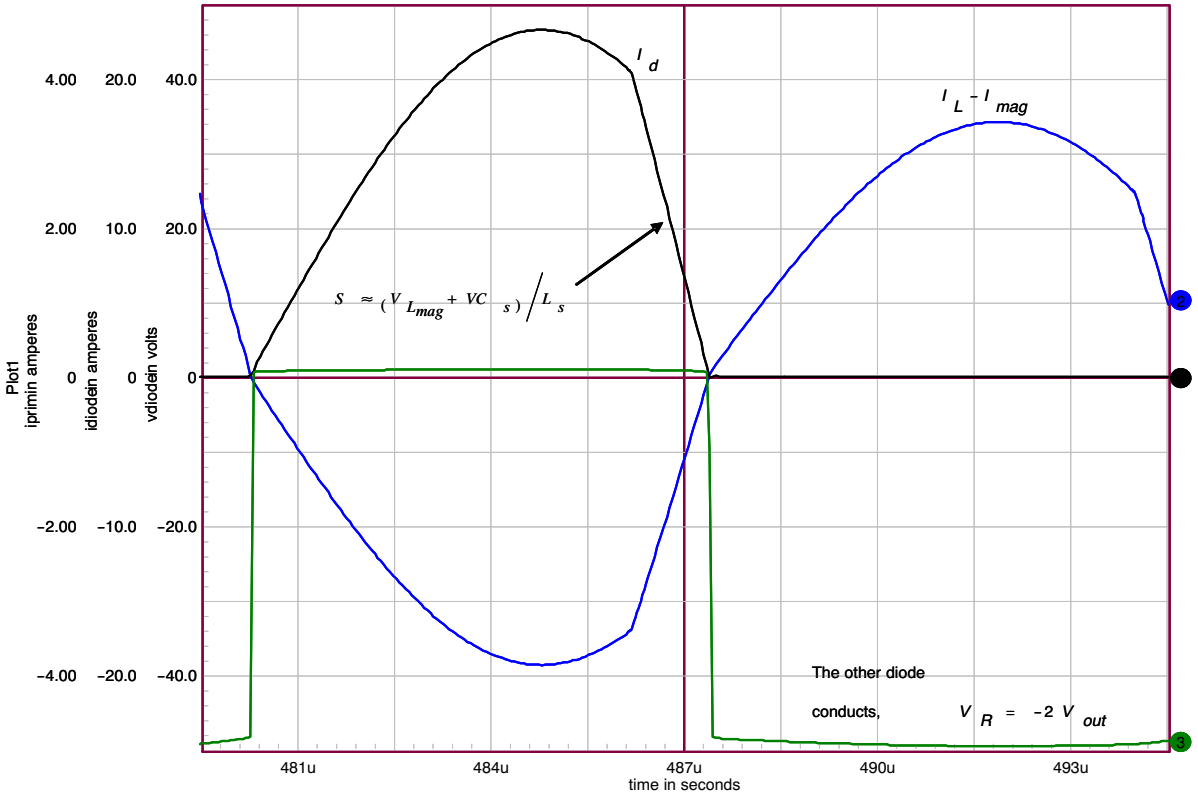


Figure 23. A Zoom on the Switching Diodes Reveal a ZCS Operation for F_{sw} greater than F_s

Operating Waveforms at the Series Resonance, $F_{sw} = F_s$

For this final example, we have selected a set of elements which operate the converter at the series resonance defined by Equation 1. The following values have been used:

L_m = 1.6 mH
L_s = 277 μH
C_s = 17 nF
N = 8

$$F_{max} = F_S = \frac{1}{2\pi\sqrt{L_S C_S}} = \frac{1}{6.28 \times \sqrt{277\mu \times 17n}}$$

$$= 73.4\ \text{kHz}$$

$$F_{min} = \frac{1}{2\pi\sqrt{(L_S + L_m)C_S}}$$

$$= \frac{1}{6.28 \times \sqrt{(277\mu + 1.6m) \times 44n}} = 28.2\ \text{kHz}$$

F_{sw} = 73 kHz at full load and nominal input voltage.

When operated at the tank resonant frequency, the main current $I_L(t)$ is sinusoidal as confirmed by Figure 24.

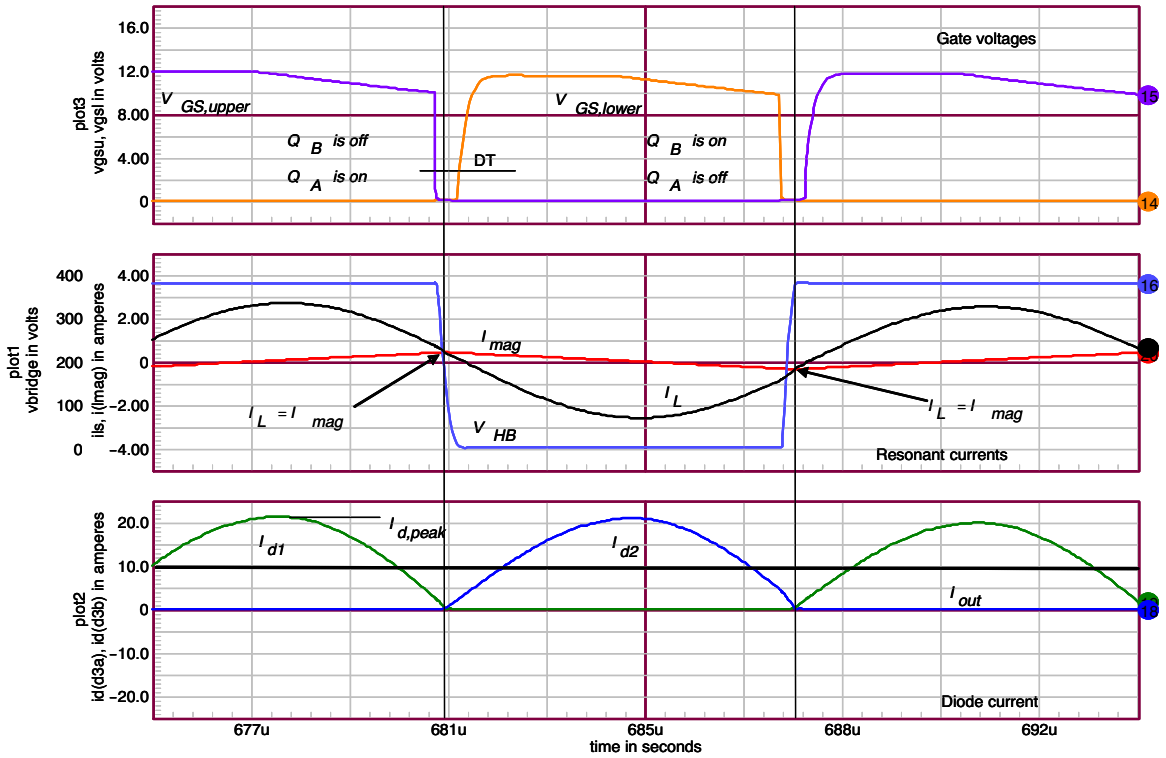


Figure 24. At the Resonant Frequency, the Main Current is Sinusoidal. Also, There is no Deadtime Between the Secondary−Side Diode Conduction Periods.

In this mode, the EMI signature is excellent as the distortion is least compared to the other modes. The secondary−side currents are at the boundary between the segment−like shape and the dead−time period, as respectively observed for $F_{sw} > F_s$ and $F_{sw} < F_s$. As we observed before, the diode block when the resonant current equal the magnetizing current I_{mag}.

Operating the LLC at the series resonant frequency offers another advantage. Back to Figure 3, we can see a point where all curves cross. This point, for which $V_{out}/V_{in} = 1$, is reached at the series resonance. When operated at this particular position, the LLC resonant network transfer function becomes insensitive to load variations. This characteristics is sometimes exploited when a LLC converter is designed to operate at a fixed switching frequency locked to F_s and the feedback loop drives the output voltage of a pre−converter.

The RMS current in the output capacitor is also at its lowest value as no discontinuity, or deadtime, exists as shown on figure 6 for $F_{sw} < F_s$. We can quickly derive its value in presence of sinusoidal signals:

$$I_{d.RMS} = \frac{I_{d.peak}}{\sqrt{2}} \qquad \text{(eq. 8)}$$

The total dc current contributed by both diodes in the output current delivered by the converter. This dc current can be linked to the equivalent full−wave rectification and equals:

$$I_{dc} = \frac{2I_{d.peak}}{\pi} \qquad \text{(eq. 9)}$$

We can then evaluate the ac current flowing into the output capacitor applying the following equation:

$$I_{Cou.RMS} = \sqrt{I_{RMS}^2 - I_{dc}^2} = \sqrt{\frac{I_{peak}^2}{2} - \frac{4I_{d.peak}^2}{\pi^2}} \approx 0.3\, I_{d.peak} \qquad \text{(eq. 10)}$$

In the simulated example, if we have a diode peak current of 15.7 A at steady−state, the RMS current flowing in the capacitor is therefore 4.7 A. If we simulate a similar converter in a 100 kHz 2−switch forward configuration, the RMS current in the output capacitor reduces down to 0.5 Arms. That is one of the major disadvantage of the resonant operation. The switching losses are almost removed, allowing high−frequency operation, but conduction losses increase significantly.

Conclusion

This quick study of the LLC converter explores the various operating modes of the power supply, mainly dictated by the switching frequency value in relationship to the series resonant frequency F_s. Most of LLC designs are operated at the series resonance in full load and nominal input voltage conditions. The controller allows operation below F_s during an input voltage drop and lets the frequency exceed F_s in light load conditions. Despite sinusoidal

currents, care must be taken in the selection of the output capacitor given the high ac ripple. Compared to buck−derived applications, this is the penalty to pay with LLC converters, however, largely compensated by the reduction in switching losses on both the primary transistors (ZVS) and the secondary−side diodes (ZCS).

References:

1. Bo Yang, Fred C. Lee, Matthew Concannon, Over Current Protection Methods for LLC Resonant Converter, IEEE Conference 2003
2. Bo Yang, “Topology Investigation for Front−End dc−dc Power Conversion for Distributed Power System”, Virginia Tech Dissertation, 2003” http://scholar.lib.vt.edu/theses/available/etd−09152003−180228/unrestricted/

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MODELLING AND CONTROL OF THE LLC RESONANT CONVERTER

by

Brian Cheak Shing Cheng

B.Sc., Queen's University, 2010

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THE REQUIREMENT FOR THE DEGREE OF

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(Electrical & Computer Engineering)

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(Vancouver)

December 2012

Abstract

To achieve certain objectives and specifications such as output voltage regulation, any power electronics converter must be coupled with a feedback control system. Therefore, a topic of considerable interest is the design and implementation of control systems for the LLC resonant converter. Additionally, with the current trend of smaller, more cost effective and reliable digital signal processors, the implementation of digital feedback control systems has garnered plenty of interest from academia as well as industry.

Therefore, the scope of this thesis is to develop a digital control algorithm for the LLC resonant converter. For output voltage regulation, the LLC resonant converter varies its switching frequency to manipulate the voltage gain observed at the output. Thus, the plant of the control system is represented by the small signal control-to-output transfer function, and is given by $P(s) = \frac{V_o}{f}$.

The difficulty in designing compensators for the LLC resonant converter is the lack of known transfer functions which describe the dynamics of the control-to-output transfer function. Thus, the main contribution of this thesis is a novel derivation of the small signal control-to-output transfer function. The derivation model proposes that the inclusion of the third and fifth harmonic frequencies, in addition to the fundamental frequency, is required to fully capture the dynamics of the LLC resonant converter. Additionally, the effect of higher order sideband frequencies is also considered, and included in the model.

In this thesis, a detailed analysis of the control-to-output transfer function is presented, and based on the results, a digital compensator was implemented in MATLAB®. The compensator's functionality was then verified in simulation.

A comparison of the derivation model and the prototype model (based on bench measurements) showed that the derivation model is a good approximation of the true system dynamics. It was therefore concluded that both the bench measurement model and the derivation model could be used to design a z-domain digital compensator for a digital negative feedback control system. By using the derivation model, the main advantages are reduced computational power and the requirement for a physical prototype model is diminished.

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List of Symbols

a_n	n^{th} coefficient of 2P2Z transfer function denominator
b_n	n^{th} coefficient of 2P2Z transfer function numerator
C_o	output capacitor
C_p	parallel resonant capacitor
C_r	series resonant capacitor
E	energy of carrier and sideband frequency signals
$e[k-n]$	n^{th} previous error term
f_s	switching frequency
f_{sample}	sampling frequency
f_{max}	maximum bandwidth frequency
$J_n(\beta)$	Bessel function of the first kind
K_{VCO}	VCO gain constant
L_M	magnetizing inductor
L_r	series resonant inductor
N	transformer turns ratio
$N_{primary}$	number of turns on primary side of transformer
$N_{secondary}$	number of turns on secondary side of transformer
p_i	i^{th} pole
P_{sw}	power loss of semiconductor switch device
Q	ratio between the characteristic impedance and the output load
r	reference input
R_{ac}	equivalent AC resistance
R_c	output capacitor equivalent series resistance
R_o	output resistance
R_r	series resistance
T	sampling time
T_{off}	semiconductor switch device turn off time
T_{on}	semiconductor switch device turn on time
$u[k-n]$	n^{th} previous term of compensator output
V_{ctrl}	control voltage
V_{ds}	drain-source voltage
V_g	input voltage
V_o	output voltage
V_p	peak voltage

$V_{s,1}$	fundamental component voltage expression
$V_{s,3}$	third harmonic voltage expression
$V_{s,5}$	fifth harmonic voltage expression
z_i	i^{th} zero
β	modulation index
ϵ	amplitude of small signal perturbation
$\Gamma(x)$	gamma function
ω_c	angular carrier frequency
ω_m	angular modulation frequency
ω_r	angular resonant frequency
$\hat{\omega}$	voltage controlled oscillator free-running angular frequency
$=$	equals
$\neq$	not equal to
$\approx$	approximately equal to
$\pm$	plus and minus

List of Abbreviations

2P2Z	2-pole-2-zero
AC	alternating current
ADC	analog-to-digital converter
AM	amplitude modulation
DAC	digital-to-analog converter
CLA	Control Law Accelerator™
CPU	central processing unit
DC	direct current
DSP	digital signal processor
EMI	electromagnetic interference
FM	frequency modulation
GUI	graphical user interface
LCC	inductor-capacitor-capacitor
LLC	inductor-inductor-capacitor
LPF	low pass filter
MOSFET	metal oxide semiconductor field effect transistor
P	proportional control
PI	proportional, integral control
PID	proportional, integral, derivative control
PWM	pulse-width modulation
RHPZ	right hand plane zero
SISO	single input single output
SMPS	switched-mode power supply
SR	synchronous rectifier
UPS	uninterruptible power supply
VCO	voltage-controlled oscillator
ZVS	zero-voltage switching
ZCS	zero-current switching
ZOH	zero-order hold

List of SI Units and Prefixes

A	amperes
dB	decibel
Hz	hertz
s	seconds
V	volts
$^\circ$	degrees

p	pico(10^{-12})
n	nano (10^{-9})
μ	micro (10^{-6})
m	milli (10^{-3})
k	kilo (10^{3})
M	Mega (10^{6})
G	Giga (10^{9})
T	Tera (10^{12})

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I would first like to express my sincere and utmost gratitude to my research supervisor, Dr. William Dunford, for his patience and guidance throughout my studies at UBC. His support and mentorship in both my academic and professional endeavors has been invaluable, and I am indebted to him for his help over the past two years.

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Finally, I would like to acknowledge and thank my grandfather, whose memory remains strong with us to this very day.

Dedicated to my parents

1 Introduction

1.1 Background

Switched-mode power supplies (SMPS) are now found in many different industrial applications and their function can vary from high power electric vehicles to low power biomedical devices and equipment. There is particular interest in applying SMPS to medium and high power applications for uninterruptible power supplies (UPS) designed for telecommunications-grade applications.

The next generation of SMPS aim to achieve high efficiency, high reliability, high power density, as well as low cost. As an example, in renewable energy applications, due to constraints in cost and the physical limitations of energy storage, the benefits of a well designed SMPS are immediate.

The application of DC-DC converters has recently become an important area of SMPS design as the emergence of distributed generation and battery-based systems continues to grow. Additionally, as the number of DC loads increases [1], using local DC power sources becomes more of a sensible solution, and further encourages the development of DC-DC conversion technology.

For some applications, DC-DC converters are particularly useful, as it provides a direct interface between energy storage elements, which are typically DC voltage sources, and DC loads. By reducing the number of intermediate energy conversion processes, the overall efficiency of the system can be increased, while also potentially minimizing the cost of the system. To meet safety and protection requirements, DC-DC converters can also be implemented with galvanic isolation between the input source and output load.

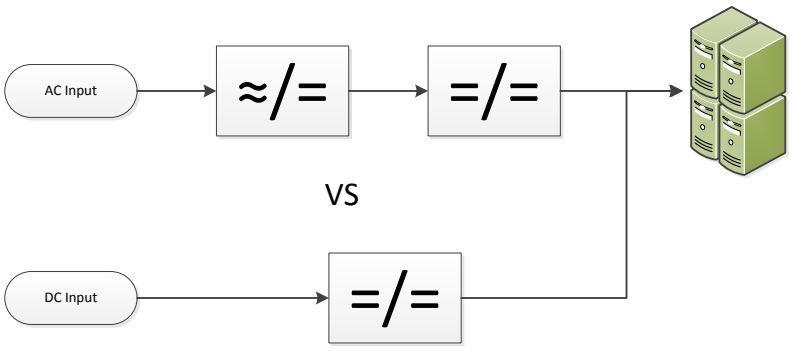


Figure 1: A direct link between DC source(s) and load(s)

A particular form of DC-DC converter is the resonant converter. In literature, resonant converters have been thoroughly studied and it has been shown that they can offer many benefits in performance, size, and cost [2]. For example, resonant converters are able to achieve low switching losses through the use of soft-switching techniques, and are able to be operated at greater switching

frequencies than other comparable converters.

The ability to operate at higher switching frequencies has the superior advantage of increasing efficiency, as well as decreasing the size of the discrete components, notably inductors and capacitors, within the hardware. This is in comparison to pulse-width modulation (PWM) converters, where the turn-on and turn-off losses of the switching devices at high switching frequencies can be high enough to prohibit operation of the converter, even when soft-switching techniques are used [3].

Moreover, PWM converters utilizing high switching frequency operation can cause disturbances such as electromagnetic interference (EMI) and suffer from the effects of parasitic impedances. However, under proper design, it is possible for resonant converters to utilize the leakage inductances of the circuit as part of the resonant tank circuit. It was also found that certain resonant converters are able to operate with low EMI [4]. Because of these advantages, resonant converters with switching frequencies in the range of MHz are conceivable [2][5].

Some typical resonant topologies include the series resonant, parallel resonant, and the series-parallel resonant converters.

1.2 Motivation

Because of the demand for resonant conversion, methods on how to design effective feedback control systems for resonant converters becomes a topic of considerable interest. To make a converter valuable for practical system applications, and to achieve specifications such as output voltage regulation, it is necessary to adopt some form of feedback control. Furthermore, with the advancements in digital signal processors, digital control techniques have become a feasible option. The application of digital controllers has allowed for more flexible designs when compared to analog controllers, and allows for much greater reliability and system integration.

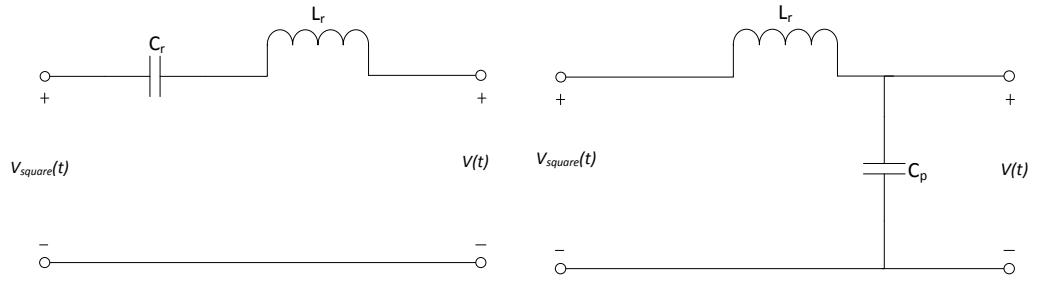
Consequently, this thesis will be centered around designing and implementing a digital control system for a resonant power electronics converter topology to be used in a medium power application. Chapter 2 will discuss in detail a resonant converter topology, followed by discussion on implementing a digitally controlled negative feedback control loop for output voltage regulation in Chapters 3 and 4. Lastly, a novel mathematical model of the small signal control-to-output transfer function is presented in Chapter 5.

2 LLC Resonant Converter

Resonant power converters contain L-C networks, or resonant tanks, whose voltage and current waveforms vary sinusoidally during one or more subintervals of each switching period [6]. Three well-known resonant topologies include the series resonant, parallel resonant, and series-parallel resonant. Although there are peculiar differences in each of these topologies, the essential operation is the same: a square pulse of voltage or current is generated, and applied to the resonant tank circuit. Energy circulating within the resonant tank will then either be fully supplied to the output load, or be dissipated within the tank circuit [2].

As documented in [7], the series and parallel resonant topologies shown in Figure 2 have several limiting factors which make them the non-ideal choice for practical applications. For the series resonant converter topology, light load operation requires a very wide range of switching frequencies in order to retain output voltage regulation. It was also observed that for high input voltage conditions, the series resonant converter suffers from high conduction losses, and the switching network transistors experience high turn-off current.

Compared to the series resonant converter, the parallel resonant converter topology does not require a wide range of switching frequencies to maintain output voltage regulation. However, at high input voltage conditions, the parallel resonant converter shows worse conduction losses, and higher turn-off currents.



(a) Series resonant converter (b) Parallel resonant converter

Figure 2: Resonant tank circuits of resonant converter topologies

One possible solution to overcome the deficiencies found in the above two converters is the series-parallel or LCC (inductor-capacitor-capacitor) converter shown in Figure 3. Since it is known that the operation around the resonant frequency has the greatest efficiency, it is desired to operate the converter around this operating point [7].

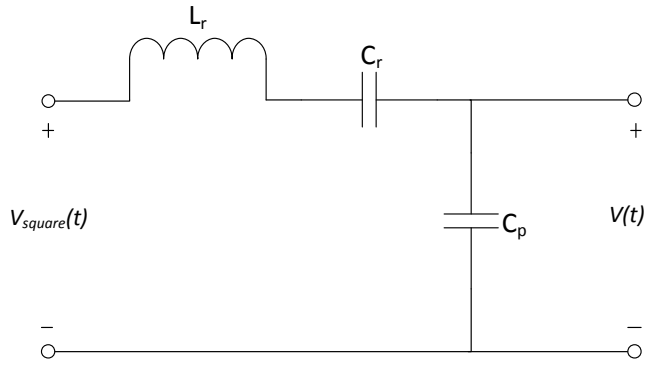


Figure 3: LCC resonant tank circuit schematic

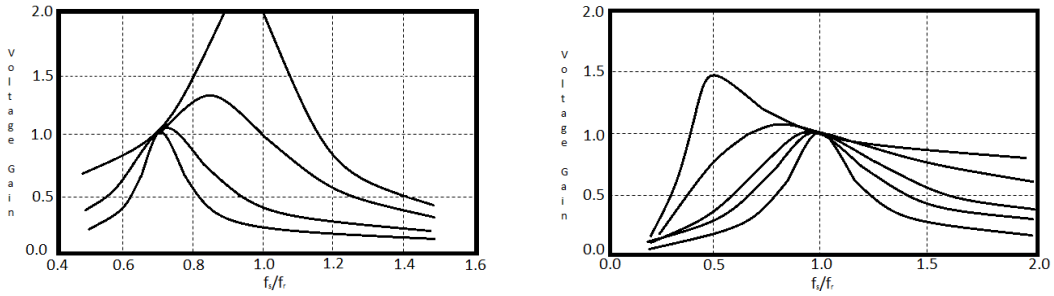
Figure 4a plots the DC gain characteristic of the LCC resonant converter with different values of the variable Q, and it can be seen in Figure 4a that more than one resonant frequency exists, depending on value of Q. Q is defined as the ratio between the characteristic impedance and the output load and can be given by Equation 1 [8].

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R} \tag{1}$$

where R is defined as the value of the output load resistance.

Furthermore, from the DC gain characteristic of Figure 4, it is understood that the segments of the DC gain characteristic with a positive gradient are regions intended for zero-current switching (ZCS) operation [7]. Given that the designed converter is to use metal-oxide field effect transistors (MOSFET) as the semiconductor switching device, the desired region of operation should therefore be on the negative gradient, a region intended for zero-voltage switching (ZVS) operation [7]. This is because the preferred soft-switching mechanism of MOSFET devices is ZVS. As outlined in [6], ZVS mitigates the switching loss otherwise caused by diode recovery charge and semiconductor capacitance often found in MOSFET switching devices.

Since it is known that operation on the negative gradient of the DC gain characteristic is desired, the characteristics of this operating region should be observed. As an example, it can be seen in Figure 4a that to achieve a gain value of 1.0 for increasing values of Q, the range of the ratio of the switching frequency to the resonant frequency $\frac{f_s}{f_r}$ varies from 0.7 to 1.2. Therefore, it can be noted that a fairly large range of switching frequencies is required to maintain a gain value of 1.0 when the output load is changing.



(a) LCC (b) LLC

Figure 4: Comparison of LCC and LLC DC gain characteristic with varying Q-factors

With this understanding of the LCC converter characteristics, the LLC (inductor-inductor-capacitor) resonant converter shown in Figure 5 becomes a potential solution. Essentially the dual of the LCC converter, the DC gain characteristics of Figure 4a are reversed in the LLC resonant converter and are shown in Figure 4b.

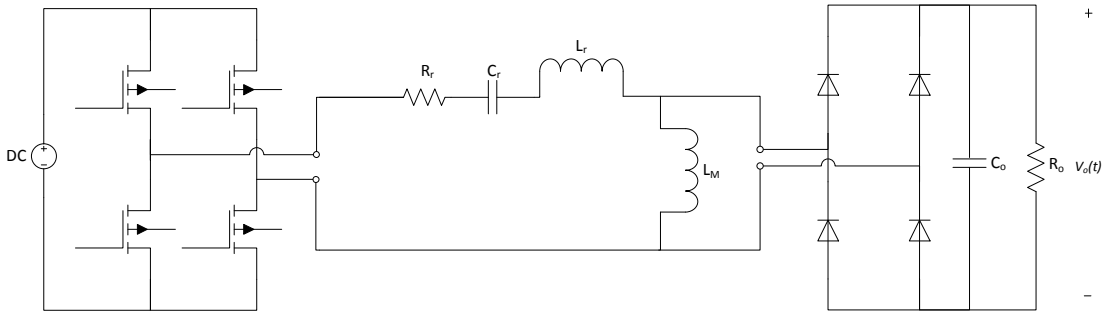


Figure 5: LLC resonant converter circuit schematic

From Figure 4b, it can be seen that the operation at around the resonant frequency, the operation is in a region such that the DC gain characteristic has a negative gradient and therefore, ZVS capabilities can be achieved in this region. Furthermore, by observing the DC characteristic of Figure 4b, and what was noted about the switching frequency range of the LCC, it can be seen that in the LLC resonant converter, the gain value of 1.0 can be achieved for all loading conditions within a very narrow range of switching frequencies.

An additional benefit of the LLC DC gain characteristic is that the resonant frequency of Figure 4b has now shifted to a higher switching frequency in comparison to the equivalent ZVS region resonant frequency of Figure 4a, and thus the potential for improvements in efficiency and

power density are greatly improved.

Some other advantages of the LLC resonant converter over other resonant topologies is its ability to maintain ZVS characteristics under light load conditions, and low electromagnetic interference (EMI) [4].

Since it has now been determined that the LLC resonant converter has many favorable features for DC-DC conversion applications, Sections 2.1 - 2.4 will discuss each stage of the LLC resonant converter, as well as the theory of operation.

2.1 H-bridge Inverter

The first stage of the LLC resonant circuit is the H-bridge inverter. It is composed of four triode-mode MOSFET transistors which are used to invert the input DC voltage to an AC sinusoidal waveform. The use of MOSFET switches are preferred since they have high input impedance and can operate at very fast switching speeds [9]. And as previously discussed, for efficiency purposes, the LLC resonant converter utilizes ZVS to eliminate the switching losses of the MOSFETs. Finally, the frequency at which the switches are turned on and off will determine the frequency to be applied to the resonant tank.

To be more precise, the H-bridge generates a square wave with frequency f_s equal to the frequency of the MOSFET switching. This quasi-square wave is established by switching on diagonally placed switches at the same time to generate the high and low values of the square-wave waveform.

It can also be noted that to prevent a shoot through condition, a small dead band time can be included between the turn-on and turn-off times of the diagonal switches.

Finally, the quasi-square wave output can be mathematically characterized by Equation 2 and the basic circuit configuration of the H-bridge inverter can be given by Figure 6.

$$v_{square}(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_g}{n\pi} \sin(n2\pi f_c t) \tag{2}$$

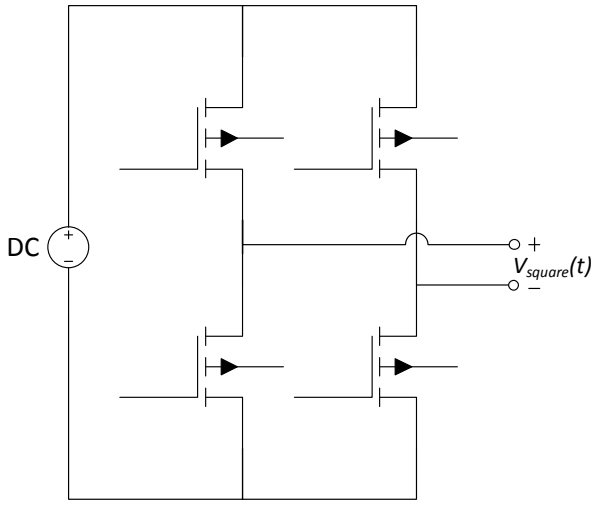


Figure 6: H-bridge inverter circuit schematic

2.1.1 Zero Voltage Switching

Zero voltage switching (ZVS) is the preferred soft-switching mechanism for MOSFET devices, as it mitigates the switching loss caused by diode recovery charge and semiconductor output capacitance [6]. In [10], switching loss is defined as the simultaneous overlap of voltage and current in power MOSFET switches.

It is shown in [10] that by allowing the drain-to-source voltage V_{ds} to reach zero before the switch turns on, the switching power loss is made to be zero. However, when there is overlap between V_{ds} and the current i_{ds}, a non-zero loss can be observed. To allow V_{ds} to reach zero, the internal capacitance of the MOSFET must be discharged by reversing the direction of the current flow through the MOSFET.

In general, ZVS occurs when the switching network is presented with an inductive load, and hence, the switch voltage zero crossings lead the zero crossings of the switch current [6]. In the case of the LLC resonant converter, ZVS operation of the H-bridge inverter switching devices is achieved and maintained by the presence of the magnetizing inductance [3][11].

An additional benefit of ZVS is the reduction of electromagnetic interference (EMI) typically associated with switching device capacitances [6].

2.2 Resonant Tank

The resonant tank circuit is the chief constituent of the LLC resonant converter, and is comprised of series resonant inductor L_r, series resonant capacitor C_r, and a parallel resonant inductor L_M. There are numerous possible configurations in which the tank components can be arranged, but the most frequently used arrangement found in literature is the connection of L_r and C_r in series and inductor L_M in parallel to the load. This arrangement is identical to the series resonant topology with the addition of inductor L_M. For a more complete model of the resonant tank, a series resistor can also be included.

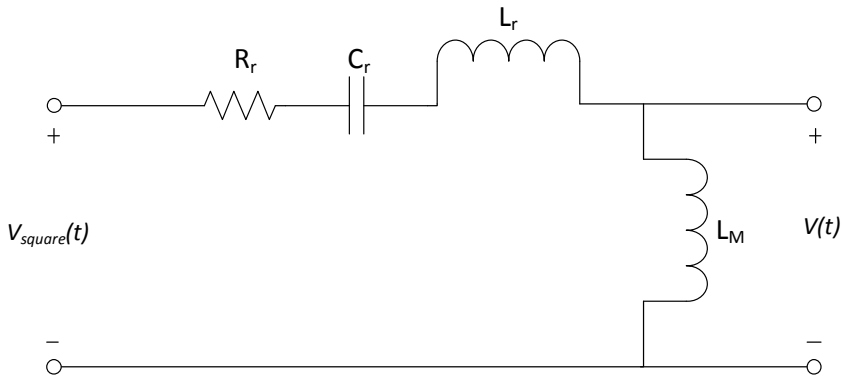


Figure 7: Resonant tank circuit schematic

The no-load transfer function of the LLC resonant tank circuit shown Figure 7 is given by Equation 3

$$H(s) = \frac{s^2(L_M C_r)}{s^2 C_r(L_M + L_r) + sC_r R_r + 1} \tag{3}$$

Well-known relationships between impedance and frequency are given by Equation 4.

$$\begin{aligned} Z_L &= j\omega L \\ Z_C &= \frac{1}{j\omega C} \end{aligned} \tag{4}$$

From these fundamental equations, it is shown that the impedance of the resonant tank can be tuned according to the frequency applied to the tank circuit. It can then be said that by varying the impedance of the resonant tank, that the voltage gain seen at the output will differ, depending

on the frequency applied to the resonant tank. It is then concluded that this voltage gain will determine the attainable output voltage value, and thus is the method in which output voltage regulation can be achieved with the LLC resonant converter.

2.2.1 Resonant Frequencies ω_{r1},ω_{r2}

From the values of L_r, C_r, and L_M, two important operating conditions can be identified: ω_{r1} and ω_{r2}. These operating points are defined as the resonant frequencies, and are defined by the applied loading condition. From Figure 7, it can be seen that at the no-load condition, the inductance L_M is seen by the tank circuit as a passive load and thus, the resonant frequency can be given by Equation 5.

$$\omega_{r2} = \frac{1}{\sqrt{(L_r + L_M)C_r}} \tag{5}$$

In the case where a nominal load is applied, the load seen by the resonant tank is effectively the large output capacitance C_o in parallel with inductance L_M. Thus, the inductor L_M is bypassed by the effective AC short circuit and the resonant frequency can be given by Equation 6.

$$\omega_{r1} = \frac{1}{\sqrt{L_r C_r}} \tag{6}$$

In this thesis, operation is focused around the resonant frequency given by Equation 6, as this operating point allows for greater efficiency, and allows for regulation using only a narrow range of switching frequencies.

2.2.2 High Frequency Isolation Transformer

Following the resonant tank circuit is a high frequency isolation transformer that can be used to either buck or boost the sinusoidal voltage to the secondary side of the converter. The transformer also serves the dual purpose of providing galvanic isolation, such that no direct current flows between the input and output.

A rather remarkable feature of the transformer is that the magnetizing and leakage inductances can be used as part of the tank circuit. For instance, the magnetizing inductance of the transformer can be used as or part of the parallel resonant inductance L_M, therefore potentially reducing the number of additional discrete components required. Similarly, the leakage inductance can be made a part of the series inductor L_r, depending on the design of the transformer parameters. This so-called integrated magnetic can therefore be designed to serve the purpose of potentially increasing the converter's power density.

The transformer ratio between the primary and secondary sides is given by the transformer turns ratio and shown by Equation 7.

$$N = \frac{N_{secondary}}{N_{primary}} \tag{7}$$

2.3 Rectifier

The last stage of the LLC resonant converter is the full bridge rectifier with capacitor output filter, which transforms the AC waveform to DC output. Similar to what was found in [6] and [12], the full bridge rectifier with capacitor filter is modelled as resistor R_{ac}. The relationship between R_{ac} and the output load is given by

$$R_{ac} = \frac{V_I}{I_{ac}} = \frac{8V_o}{\pi^2 I_o} = \frac{8}{\pi^2} R_o \tag{8}$$

R_{ac} can then be reflected onto the primary side by multiplying Equation 8 by the transformer turns ratio given by Equation 7.

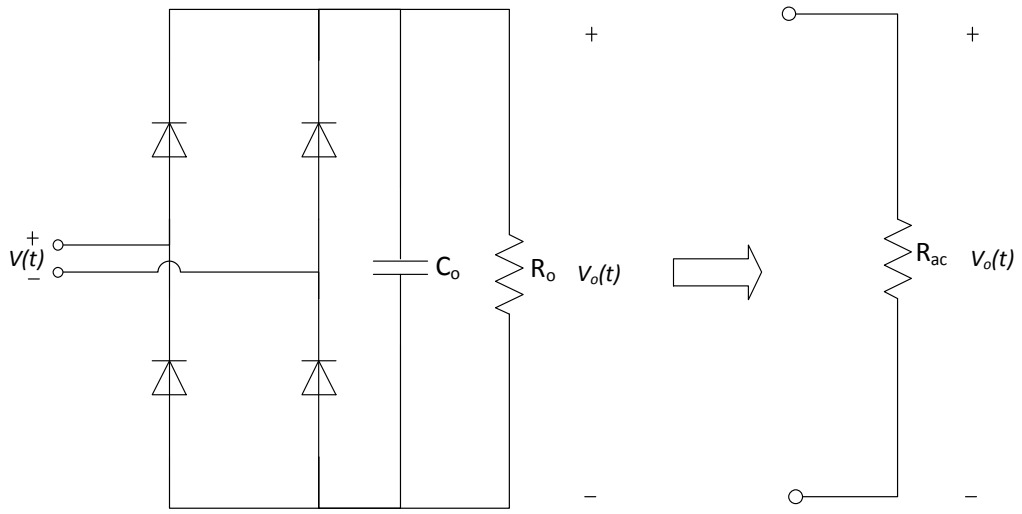


Figure 8: Rectifier circuit modelled as R_{ac}

From [6], the final DC value of the output voltage and the output voltage ripple can also be determined by the following relationships.

$$V_{o,dc} = V_p(1 - \frac{1}{2f_s C_o R_o}) \tag{9}$$

For the case of an ideal full bridge rectifier that has negligible ripple, the switching frequency f_s and output capacitance C_o are large such that the DC output voltage can be approximated by

Equation 10.

$$V_{o,dc} \approx V_p \tag{10}$$

where V_p is the peak value of the AC input voltage, $V(t)$.

2.3.1 Synchronous Rectification

To further increase the efficiency of the LLC resonant converter, a synchronous rectification (SR) network can be implemented in lieu of the full bridge diode rectifier. In a synchronous rectifier, the diodes are replaced with MOSFET devices, and when current flow is detected on the secondary side, the MOSFETs are turned on to allow current flow to the load.

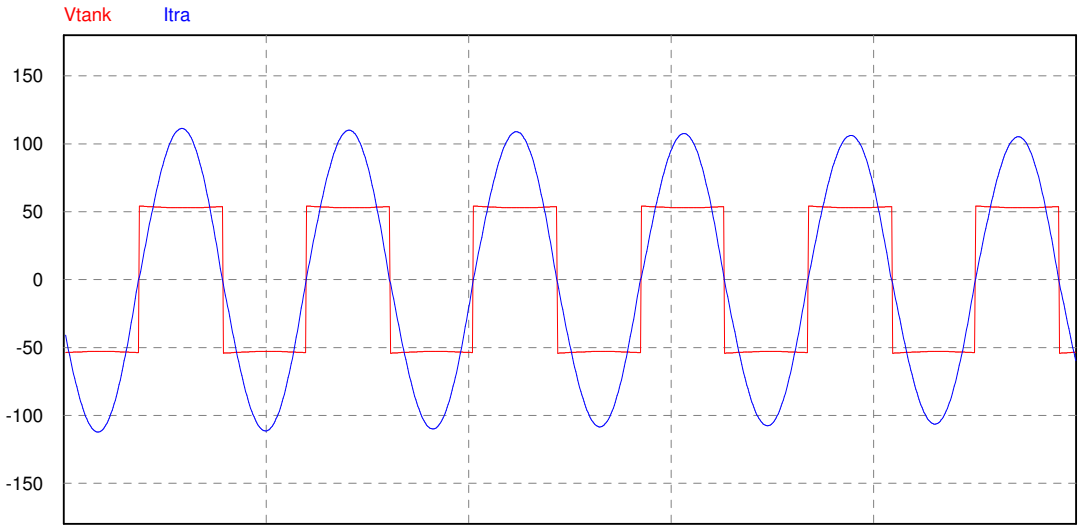
This is a much more efficient strategy in comparison to the diode rectifier, as the voltage drop across the diode is eliminated. Additionally, unlike diodes, which are only able to provide unidirectional flow of power, a SR network makes bidirectional power flow between the input and output feasible.

The disadvantage of implementing SR with the LLC resonant converter is the increased complexity. Computer simulations of Figure B-1 found in Appendix B show the presence of a phase delay between the voltage and current when the switching frequency is away from the resonant frequency. The results of the simulation are shown in Figure 9.

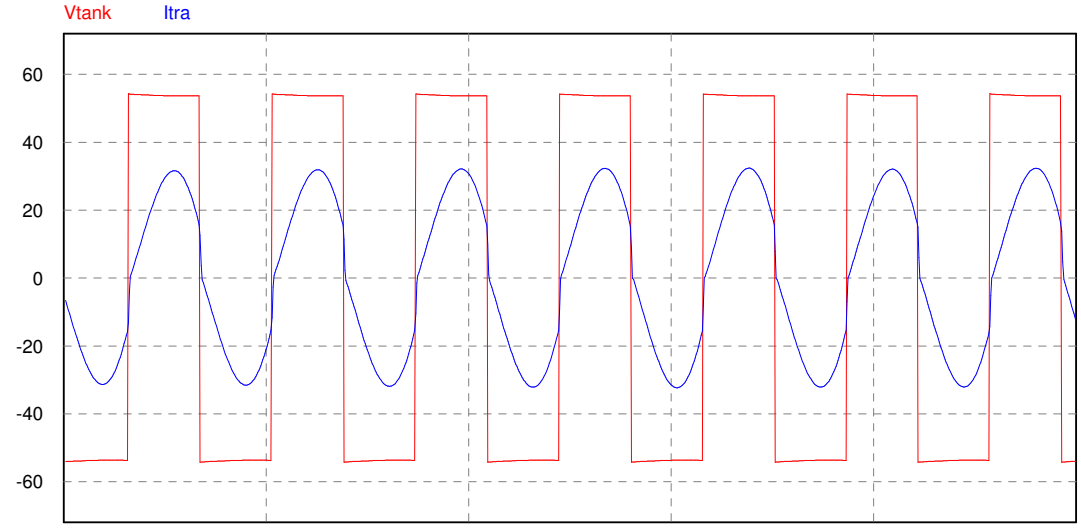
Because of this, it is difficult to determine the timing of the SR turn-on and turn-off. Usually, additional detection circuitry is required on the secondary side to determine when there is current flow through the rectifier, and to determine the control signal to the gates of the SR MOSFETs. Furthermore, since MOSFETs do not have the ability for automatic reverse current blocking, the timing of the turn-off is also important, such that shoot through conditions are avoided.

Some literature has been produced on the control of the SR gate drive signals in [13][14][15]. It is known that the critical event for triggering the SR gate drive signal is the detection of current in the secondary side. It was outlined in [15], that there are two main methods in which this can be accomplished. The first is to directly sense the current using a current transformer. Although this may be the simplest method of detection, the use of a current transformer introduces limitations of the power density as well as the maximum achievable switching frequency. Additionally, the increased series inductance is detrimental to current commutation in the synchronous rectification switch network [15].

Another possible method is to detect the drain-source voltage, V_{ds} of the synchronous rectifier switches. The sensed value of V_{ds} is then processed by control circuits to determine the turn-on and turn-off time of the SRs. This approach can be relatively easily verified in simulation, but the difficulty of this method is determining a method in which V_{ds} can be accurately measured. Because there exists a package inductance from the MOSFETs in the SR, the measured value of



(a) Voltage and current waveforms in phase when $f_s = f_{r1}$



(b) Voltage and current waveforms out of phase when $f_s \neq f_{r1}$

Figure 9: SR phase delay

V_{ds} becomes highly deviated if the package inductance is not properly considered. If the physically sensed value is far deviated from the true value of V_{ds}, a false trigger of the SR circuits may occur, and the potential for shoot through condition increases.

Some literature proposed by [13][14], have shown a number of methods to improve the accuracy of sensing V_{ds}. This is at the expense of circuit complexity, as several additional compensating components are required.

A computer simulation using a current-sensing method has been proposed and is shown in Figure 10.

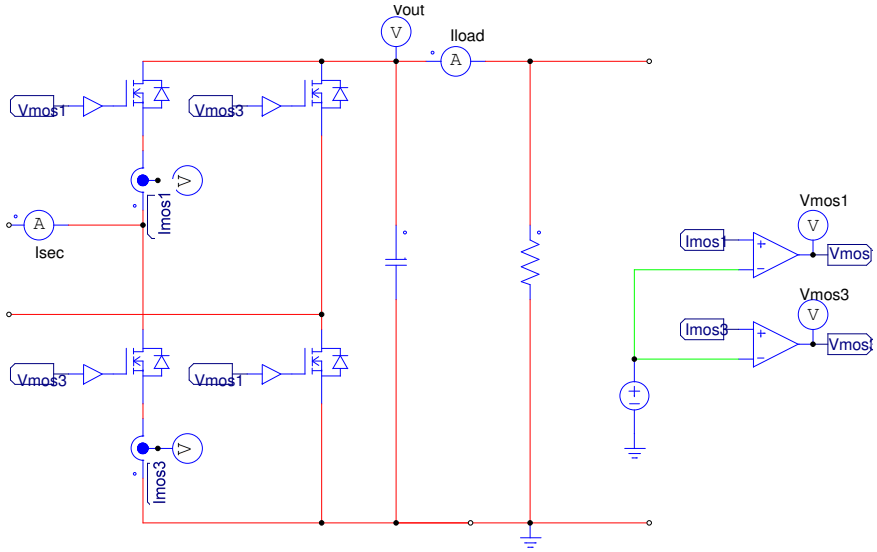


Figure 10: Synchronous rectification PSIM® model

2.4 Theory of Operation

The fundamental operation of the LLC resonant converter is based on applying a voltage with frequency f_s to the resonant tank to vary the impedance of the tank circuit, thus controlling the achievable gain seen at the output. From Figure 11, it can be seen that as the switching frequency is increased, the output gain is decreasing. This implies that as the switching frequency is increased, the impedance of the resonant tank is increased, and therefore, a larger voltage drop is observed across the resonant tank circuit components, and less voltage is transferred to the load. The reverse is true as well, such that as the switching frequency decreases, the DC gain increases, implying that the voltage drop across the tank circuit has decreased, and the output voltage gain can be increased.

In the following sections, the operation of the LLC resonant converter is more closely considered, and a single switching interval is analyzed.

There are three main regions of operation, commonly described as Region 1, 2, and 3. Operation in Region 1, 2, and 3 is determined by the location of the operating point on the DC gain curve shown in Figure 11. Region 1 and 2 are located on the negative gradient of the DC gain curve, and Region 3 is located on the positive gradient. Region 1 is the set of switching frequencies greater than the resonant frequency, while Region 2 is the set of switching frequencies below the resonant frequency.

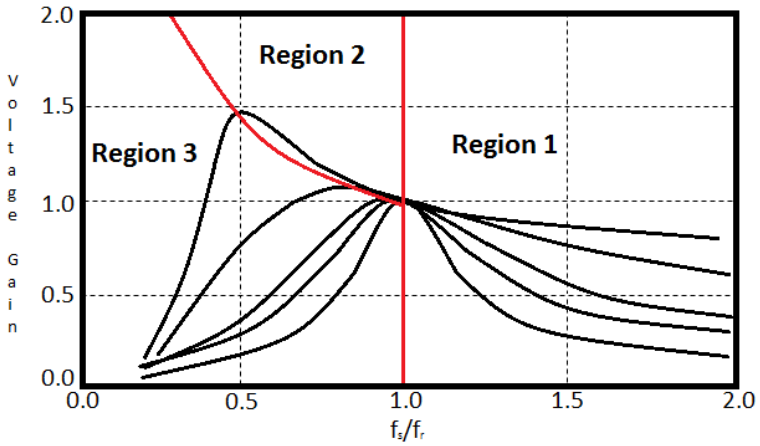


Figure 11: Regions 1, 2, and 3

Depending on the design specifications and requirements that are desired, operation in any of these regions is possible. As it is preferred to switch the MOSFET devices under ZVS conditions, the focus will be on operation in Regions 1 and 2, which is graphically shown in Figure 11 as the negative gradients of the DC gain curves.

2.4.1 Region 1

In Region 1, the magnetizing inductance L_M from the transformer does not resonate with the other tank circuit components, and is viewed as a passive load by the resonating series inductor and series capacitor. Because there is always this passive load, it is possible for the LLC resonant converter to operate at no load without having to force the switching frequency to very high levels. The passive load also ensures ZVS is achieved for all loading conditions [7]. Region 1 operates at the resonant frequency given by Equation 6.

2.4.2 Region 2

In Region 2, there are two distinct operating modes. In the first time sub-interval, the series inductor and series capacitor resonate together while the magnetizing inductance is clamped to the output voltage, and has operation similar to that of Region 1. Therefore, the resonance only occurs between L_r and C_r. The current in the resonant tank I_r then begins to increase and continues to increase until the magnetizing current I_M and I_r are the same. When the two currents are equal, L_M starts to resonate with L_r and C_r, and the second sub-interval begins. Since L_M is now also resonating with the L_r and C_r, the resonant frequency is given by Equation 5.

In Region 2, since multiple resonant frequencies are observed over one switching period, the LLC resonant converter is considered to be a multi-resonant converter. Figure 13 shows the plots of the LLC resonant converter operating in Region 2. Operation in the second sub-interval begins during the time interval in which the output current is equal to zero.

Figures 12 and 13 show the plots of the gate-source drive signal V_{gs}, the resonant current I_r, the magnetizing current I_{LM}, the capacitor voltage V_{Cr} and the output current I_o. Figure B-2 in Appendix B shows the labelled circuit schematic used to obtain the plots of Figures 12 and 13.

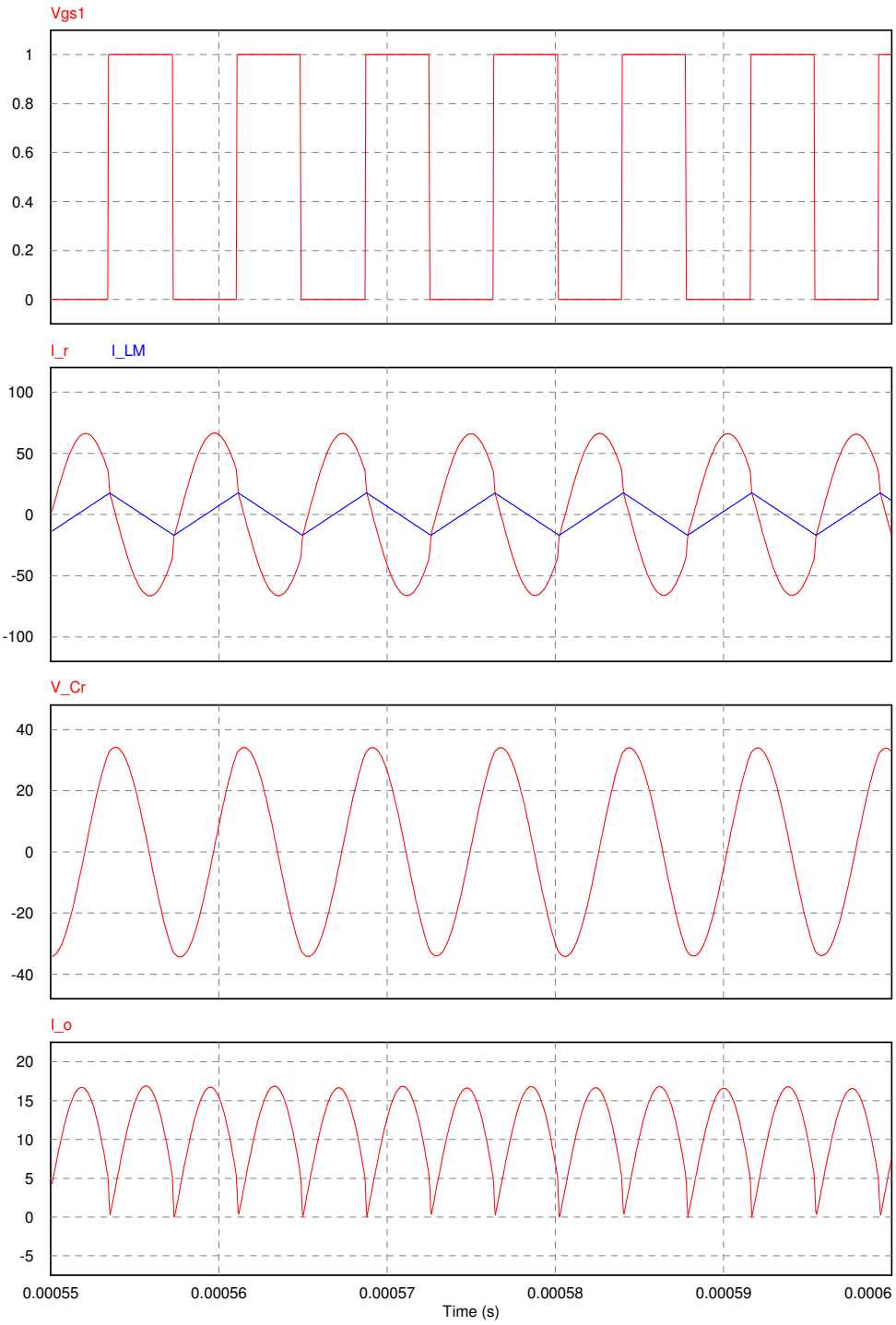


Figure 12: Operation of LLC resonant converter in region 1

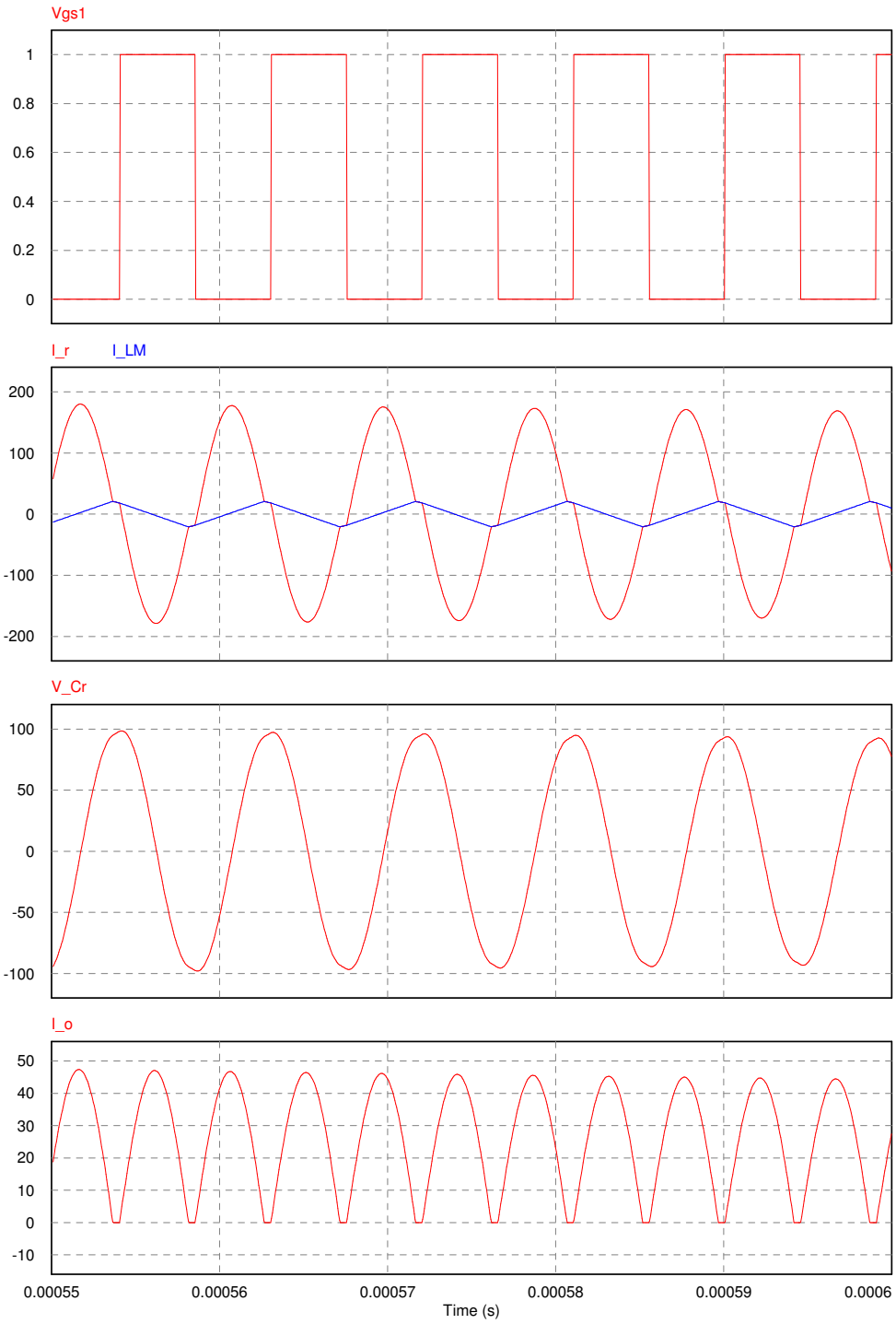


Figure 13: Operation of LLC resonant converter in region 2

3 Control of LLC Resonant Converter

When correctly applied, the application of control theory and feedback can eliminate steady state errors, moderate system sensitivity to parameter changes and disturbances, modify the gain or phase of the system over a desired frequency range, and make unstable systems stable.

For this thesis, the objective is to design a voltage control loop to regulate the output voltage, according to a predefined reference voltage. In other words, regardless of disturbances to the system, and more specifically, the load; the output voltage is to remain at a constant value. Consequently, a negative feedback loop was designed to achieve these specifications.

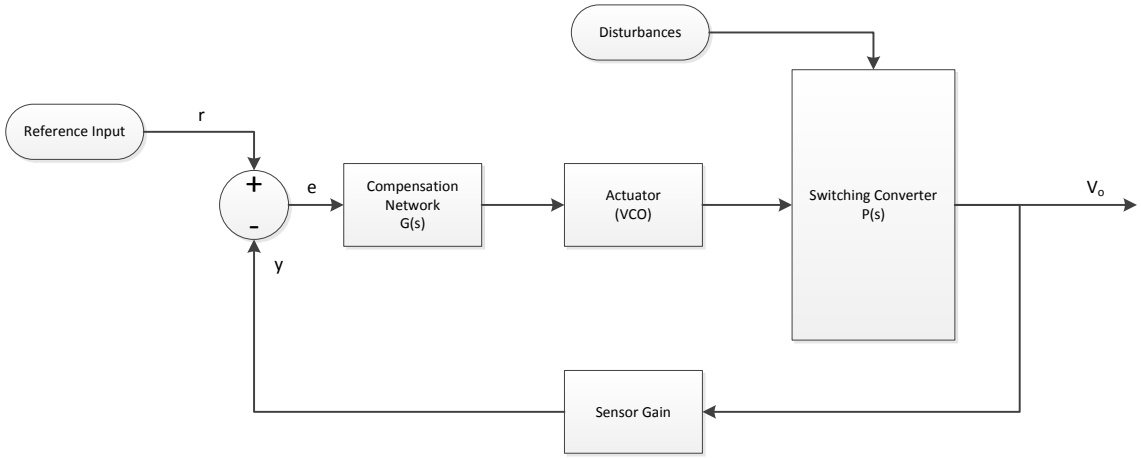


Figure 14: Block diagram of negative feedback loop

From Figure 14, it can be seen that the function of the negative feedback control loop is to determine an input to the plant, such that the desired output behavior can be obtained. Specifically, for the LLC resonant converter, the objective is to generate a set of gate driving signals of frequency f_s for the primary side switch network.

Figure 14 shows that by sensing the output y and comparing it to reference input r, the compensator network $G(s)$ can generate the gate drive signals based on the given error signal e. The error signal is the difference between the y and r, and in a functional control loop, tends to zero after some time period.

3.0.3 Variable Frequency Control

Under normal operating conditions, the LLC resonant converter uses variable frequency control to regulate the output voltage. This type of control requires a gate drive signal that has constant duty cycle, but varying frequency.

To implement variable frequency control, an actuator that can produce a variable frequency signal is required and can be realized by a voltage controlled oscillator (VCO). The VCO is an electronic circuit designed to produce an oscillation frequency based on the control voltage V_{ctrl} and can be implemented as an analog circuit or with a digital signal processor. The relationship between the input signal V_{ctrl} and the output frequency signal ω_o is shown in Equation 11.

$$\omega_o = \hat{\omega} - K_{VCO} V_{ctrl} \tag{11}$$

In Equation 11, $\hat{\omega}$ is the free-running frequency of the VCO, and K_{VCO} is the gain of the voltage controlled oscillator.

3.0.4 Pulse Width Modulation

Pulse-width modulation (PWM) is a fixed frequency control method, and modifies the duty cycle of the pulses to regulate the output voltage. It has been suggested in the literature [16][17] that for light and no load conditions that it may be more effective to control the LLC resonant converter by using PWM rather than variable frequency control. However, in this work, it will be assumed that the converter always operates under nominal loading conditions, and therefore only requires the use of the variable frequency control method.

3.1 Digital Control

Digital controllers have many advantages over analog designs. Digital controllers can be designed to be more robust, and can be easily manipulated for optimal control performance. Additionally, the recent decreases in the cost and size of programmable micro-controllers and digital signal processors (DSP) has made digital control a viable option for power electronics applications.

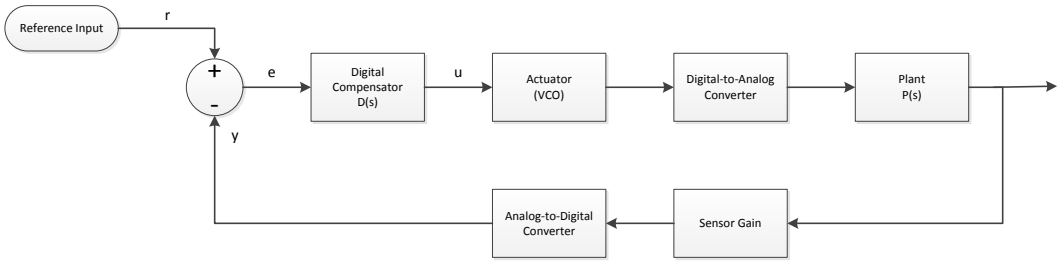


Figure 15: Block diagram of digital negative feedback loop

3.1.1 Effects of Sampling Frequency

An essential consideration that is relevant to digital systems is the principle of sampling, a non-zero timed event to capture the continuous-time data. Sampling is required to convert continuous-time data to discrete-time for processing in the digital signal processor and is physically realized with an analog-to-digital (A/D) converter. The aim of the A/D converter is to accept measured signals from the output of the power electronic converter and then convert these signals into an electrical voltage level that can be read by the DSP. Conversely, once the processing has been completed in the DSP, a digital-to-analog (D/A) converter is used to produce a physical signal to be read by the power electronic converter.

A crucial factor in digital design is the sampling rate at which the continuous-time signal is sampled. Ideally, the sampling rate is infinite such that the discrete-time system is equivalent to the continuous-time model. Unfortunately, since this is not a realistic solution, the alternative solution is to apply the Nyquist rate shown in Equation 12.

$$f_{sample} \geq 2f_{max} \tag{12}$$

The Nyquist rate states that the sampling frequency must be at least twice the maximum bandwidth in the system. By satisfying this criterion, aliasing and signal distortion in the reconstructed signal can be avoided. It can be added that, in fact, it is recommended in [6] to make the sampling frequency ten times the maximum bandwidth.

3.1.2 Design of Digital Control Systems

Digital controllers can be implemented using two primary methods: emulation and direct digital design.

Digital controllers designed through emulation method use the continuous-time plant model, and obtain the compensator model in continuous-time. The continuous-time s-domain model is then converted to a discrete-time z-domain compensator by applying mathematical transformations.

Numerous methods to transform continuous-time transfer functions to discrete-time transfer functions exists. Some typical methods include the Tustin method, zero-order hold, first-order hold, etc. From [18], it was found that for the most accurate models, the first-order hold is the most accurate discretization method, but at the expense of computational complexity. A more general method that is typically used is the zero-order hold discretization as it provides a balance of accuracy and computational efficiency.

The advantage of the emulation method is that well-developed and familiar continuous-time design methods can be applied. This method produces reasonably accurate results given that the sampling rate is very fast. The main disadvantage of the emulation method is that after mapping

the compensator from continuous to discrete-time, it is possible that the control system can no longer achieve the same performance characteristics as in the continuous-time domain model [18].

The other method which can be used to design a digital compensator is by using the direct digital design methodology. Compensators implemented using the direct digital design technique usually have significantly better performance when implemented on digital signal processors. This method of design immediately begins with a plant model already in discrete-time, and then the compensator is designed based off the digitized plant model in the z-domain [19]. Thus, the probability of obtaining unexpected controller response and dynamics are mitigated when the controller is implemented using a DSP.

3.1.3 2-Pole-2-Zero Compensator

Irrespective of which compensator design method is used, the end goal is to design a compensator $G(s)$ to supply the correct signals to maintain output voltage regulation. Loop compensation is achieved by the placement of additional poles and zeros to the feedback system, in conjunction with the system's natural poles and zeros. The system loop gain can then be shaped to the desired performance and stability characteristics by the new poles and zeros introduced to the system. An example of compensator in the digital domain is the 2-pole-2-zero compensator (2P2Z).

The 2-pole-2-zero compensator was selected as the compensator of choice as it can be simply implemented in the z-domain as a difference equation. Its transfer function is given by Equation 13.

$$H_{2p2z}(z) = \frac{b_o + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \tag{13}$$

Determining the roots of the quadratic numerator and denominator of Equation 13 gives the location of the zeros and poles of the compensator respectively.

Compared to P, PI, or PID controllers, the 2P2Z compensator allows for five degrees of freedom, and allows for the use of complex poles and zeros [20]. In fact, the P, PI, and PID controllers are simply particular cases of the 2P2Z. For example, the PID controller uses the assumption that the coefficients $a_1 = -1$ and $a_2 = 0$.

$$H_{PID}(z) = \frac{b_o + b_1 z^{-1} + b_2 z^{-2}}{1 - z^{-1}} \tag{14}$$

Furthermore, for implementation in the digital signal processor, the 2P2Z compensator transfer function can be easily re-written in the form of a difference equation.

$$u(k) = b_o e(k) + b_1 e(k-1) + b_2 e(k-2) - a_1 u(k-1) - a_2 u(k-2) \tag{15}$$

A functional block diagram of the 2P2Z is shown in Figure 16.

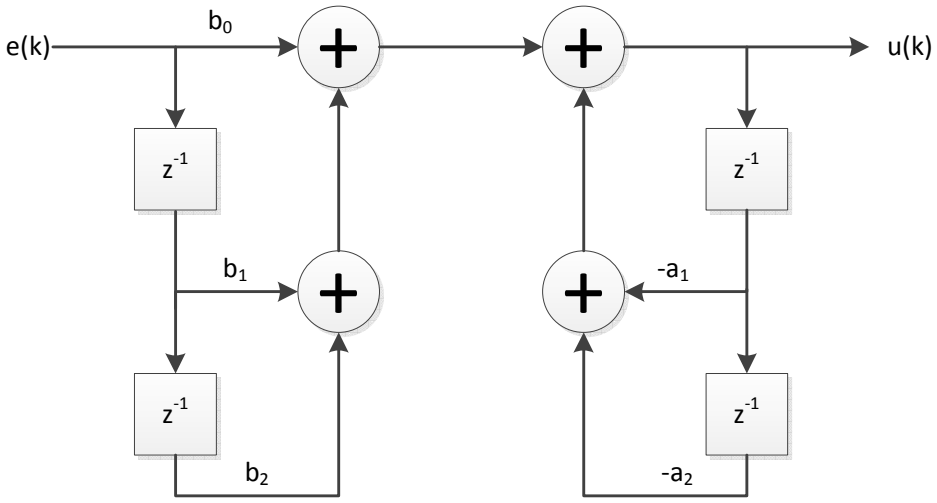


Figure 16: 2 pole 2 zero DSP implementation

3.2 Compensator Design

Two popular methods in which a compensator can be designed for a feedback system are the Bode diagram and root locus.

3.2.1 Root Locus

The root locus method is a plot of all system poles of the closed loop transfer function as some parameter of the system is varied. This design method relocates the closed-loop poles to meet performance specifications such as overshoot, rise and settling times. This method is ensures that acceptable transient response characteristics are reached, as well as robust compensator design [21]. A disadvantage of the root locus method is that the system under test must be able to be approximated as a second order system.

3.2.2 Bode Diagram

The Bode diagram displays the magnitude and phase response of a feedback system as two separate plots with respect to the logarithmic frequency [22]. The Bode diagram is useful since the multiplication of transfer functions simply become problems of summation. The phase plot is generally given in degrees (°) and the magnitude plot is given in decibels (dB) scale.

The conversion of magnitude to magnitude in decibels is given by Equation 16.

$$X_{dB} = 20log_{10}|X| \tag{16}$$

The performance of compensators designed using the Bode diagram method are based on the bandwidth, gain margin and phase margin [21].

In the Bode diagram, a pole is represented by a 20 dB per decade decay, and a zero is a 20 dB per decade increase.

3.3 Stability

To verify that the designed compensator and plant form a stable system, the stability of the closed loop feedback system can be studied in either the continuous-time domain or the discrete-time domain. The differences in characteristic between the continuous-time and discrete-time domains are discussed in Appendix A.

In this thesis, the stability of the control system will be observed using the Bode and Nyquist diagrams.

3.3.1 Bode Diagram

The stability of the feedback system can be determined from the Bode diagram by observing the gain and phase margins. The phase margin is defined as the phase difference from -180° at the crossover frequency f_c. The crossover frequency is defined as the instance at which the magnitude plot is at unity. The phase margin can be calculated using Equation 17.

$$P.M. = 180 + \angle P(j\omega_{crossover}) \tag{17}$$

The gain margin is the point on the magnitude plot that corresponds to the point on the phase plot at which the phase crosses the -180° axis.

Typically, the target phase margin is between $45° - 60°$, and can be negotiated depending on the requirements for the transient settling time and the stability. For the gain margin, it is generally accepted that good gain margin is greater than 9 dB [23].

3.3.2 Nyquist Plot

Alternatively, the stability of the system can be observed using the Nyquist plot. The Nyquist plot displays the frequency response as a single plot in the complex plane, and is a graphical representation of the loop transfer function as $j\omega$ traverses the contour map [24].

Stability in the Nyquist plot can be observed by applying the Nyquist stability criterion. This criterion is determined by examination of the enclosure around the critical point $(-1, 0)$. For closed loop stability, the Nyquist plot must encircle the critical point once for each right hand pole, in a direction that is opposite to the contour map [24].

It would be appropriate and useful to relate the Nyquist stability criterion to the Bode diagram magnitude and phase plots [25]. There are two main relationships that can be made:

- The unit circle of the Nyquist plot is equivalent to the 0 dB line of the magnitude plot.
- The negative real axis of the Nyquist plot is equivalent to the -180° phase line of the phase plot.

4 Implementation and Verification

In this thesis, the plant process is given by the ratio of the output voltage to the switching frequency, and is expressed in Equation 18. Since it was determined that the direct digital design method gives superior results, it is the selected method for the design of the compensator.

$$P(s) = \frac{V_o}{f_s} \tag{18}$$

Consequently, the first step is to obtain a description of the plant process model, in either continuous or discrete time, which can be discretized so that the compensator may be directly designed in the discrete-time z-domain.

However, since the mathematical relationship described by Equation 18 is not well-defined in the literature, one proposed solution is to measure the frequency response of the LLC resonant converter using a network analyzer. The frequency response can be obtained by probing the output voltage, and the switching frequency while the switching frequency is undergoing small signal perturbations around a designated operating point.

This methodology has the main advantage of capturing the true behavior and dynamics of the LLC resonant converter, as well as any additional behaviors that appear due to parasitic components. This measurement method provides the most realistic representation of the plant process model, however it assumes a prototype model has already been designed and is functional.

4.1 Design Methodology

4.1.1 Overview

The approach taken to design the digital controller was to first use a laboratory bench prototype model and network analyzer to obtain the frequency response data of the plant process model. Different loading conditions were then applied to the prototype model to observe the changes in the frequency response. Additionally, bench data of the DC gain characteristics under different loading conditions were obtained to compare with the theoretical models presented in Chapter 2.

The obtained frequency response data of the physical plant model was then imported into the MATLAB® environment, and based on the obtained data, a compensator was designed in MATLAB®. To verify that the compensator design is satisfactory, the designed compensator coefficients can be extracted from MATLAB®, and then exported to a software more suitable for power electronics simulation.

Finally, an example implementation using a Texas Instruments®-based digital signal processor (DSP) is given.

4.1.2 Bench Test Results

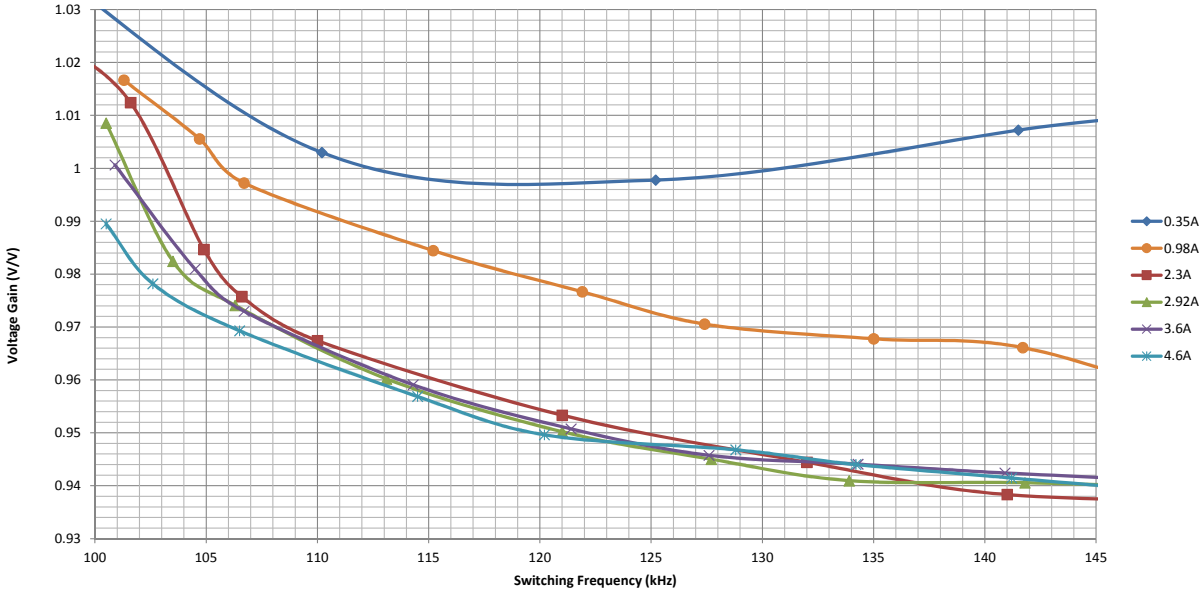


Figure 17: Bench test result of DC gain characteristic for Region 1

Figure 17 shows the DC voltage gain characteristic of the prototype model when operated above the resonant frequency. From these results, it is evident that for light loading conditions, the LLC resonant converter begins to display non-linear characteristics, which suggests a separate control loop may be necessary for light load operation. For loading conditions approaching the nominal load, it appears that the prototype model follows the theoretical DC gain characteristics as given by Figure 4b. Figure 17 also shows that the boundary condition between nominal and light loading conditions for this particular converter lies around 2.3 A.

Given that the resonant frequency is the quiescent operating point, Figure 18 shows the frequency response of the prototype model with different loading conditions. Figure 18 plots the magnitude of the ratio between the output voltage and control voltage in decibels (dB) with respect to the relative frequency in Hertz (Hz). From these results, it was determined that the frequency response of the plant model also has a large dependency on the loading conditions.

Since there may be frequent changes to the load, the compensator design should be based on the plant process model that represents the worst-case scenario. For this thesis, it will be assumed that the converter is operated under nominal operating conditions, and thus, the worst-case is defined as the loading condition such that the phase margin is minimum, as this is the condition that is

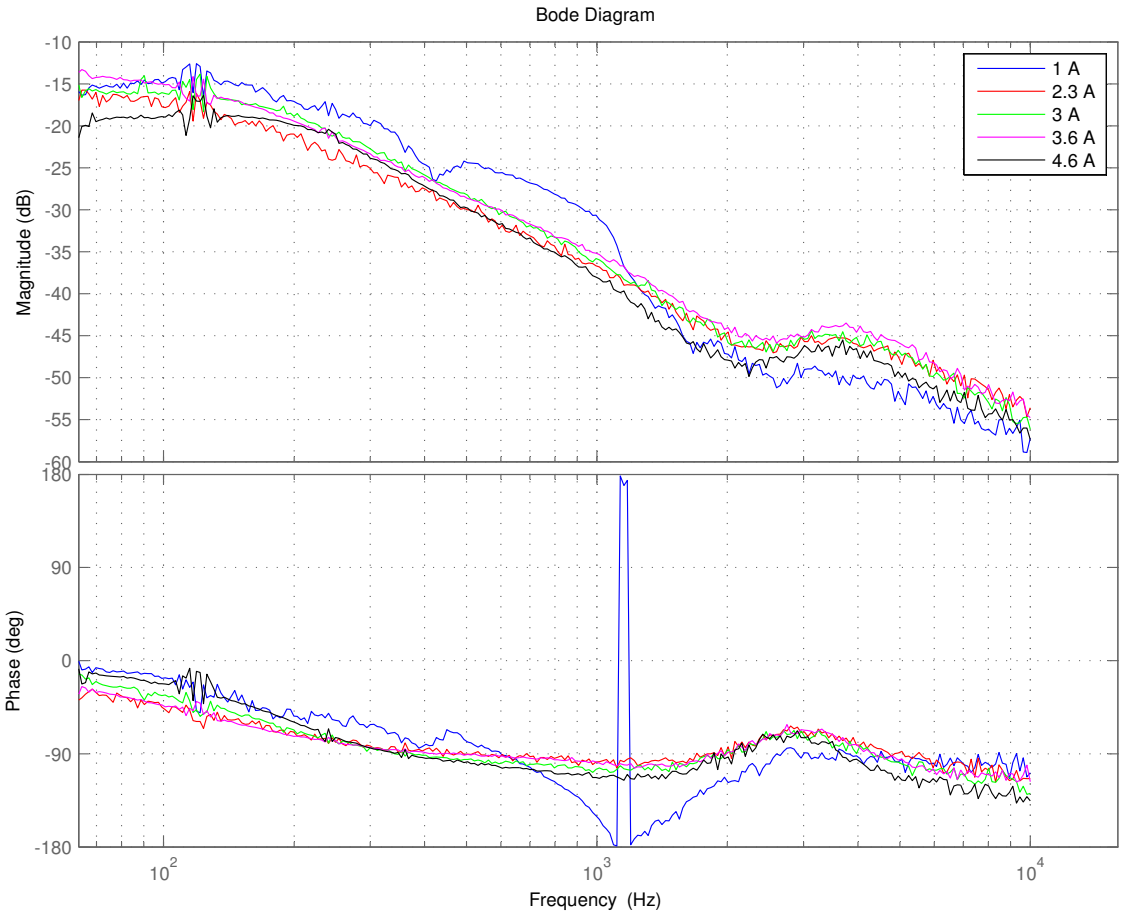


Figure 18: Plot of relative frequency response of prototype model under different loading conditions

most likely to be overcome by problems of instability. In Figure 18, this scenario is represented by the curve '4.6 A.'

It can be noted that the frequency response generally follows the form of a low-pass filter (LPF), with the addition of a high frequency pole-zero combination. Because this system appears to be greater than second order, design of the compensator using the Bode diagram technique is preferred over other design methods.

4.1.3 Compensator Design Results

MATLAB® has several useful tools for digital controller development. Firstly, built-in functions such as '*c2d*' make it straightforward to convert continuous-time s-domain models to discrete-time z-domain models. Secondly, the Control System Toolbox features the SISO Design Tool which

allows for simple, visual design of control systems.

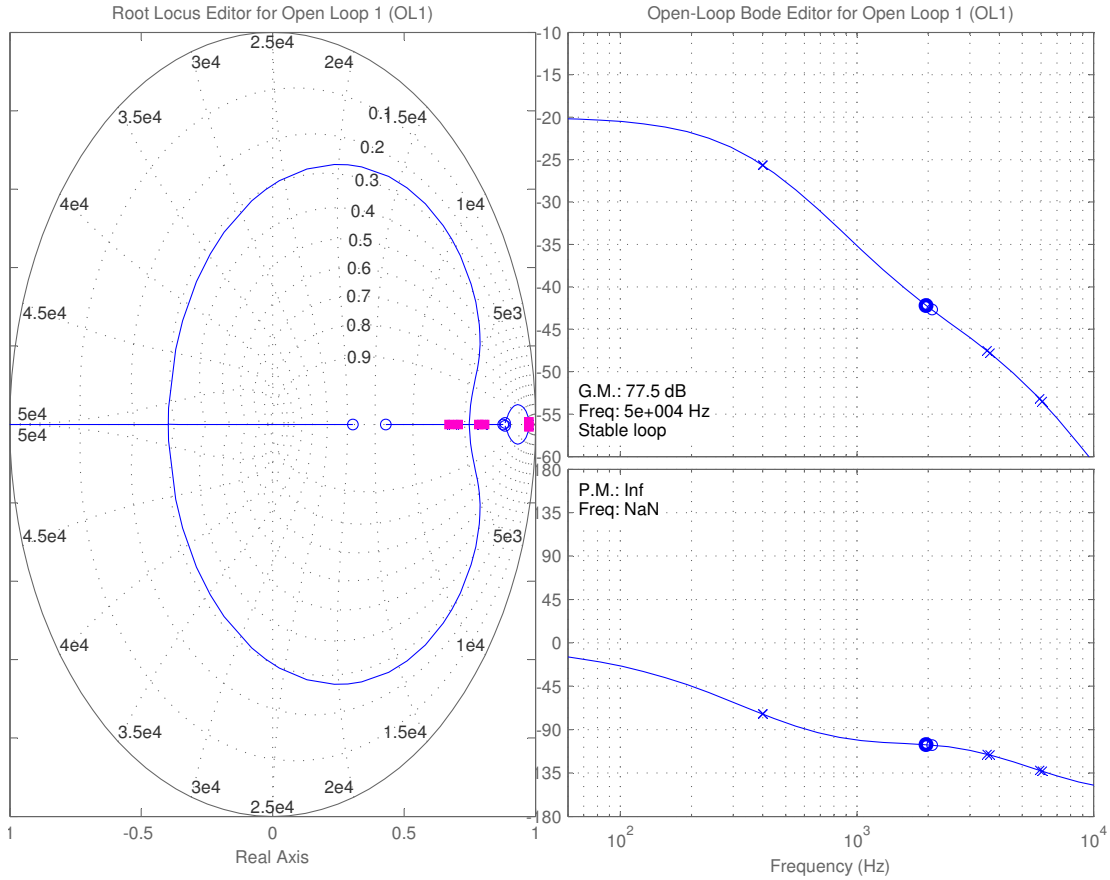


Figure 19: Prototype model frequency response data in MATLAB® SISOTOOL GUI environment

In this case, the frequency response data of the plot '4.6 A,' a continuous-time domain function, is transformed into a discrete-time z-domain frequency response plot with the '*c2d*' command and an appropriate sampling time.

With the z-domain frequency response in hand, the '*sisotool*' command opens the SISO Design GUI for interactive compensator design, and allows for controller design using root locus, Bode diagram, and Nichols techniques.

Using the Bode diagram design editor, the '*sisotool*' GUI environment allows the user to manually add and position the poles and zeros of the compensator according to the specifications required for the control system [26]. The bandwidth, gain and phase margins, as well as the closed-loop step response can then be easily obtained from the GUI environment to verify the stability and performance of the designed compensator model.

Figure 20 shows the response of the open-loop system with the designed digital compensator. The open loop response appears to be stable and has a gain and phase margin of 53.8 dB and 60° respectively.

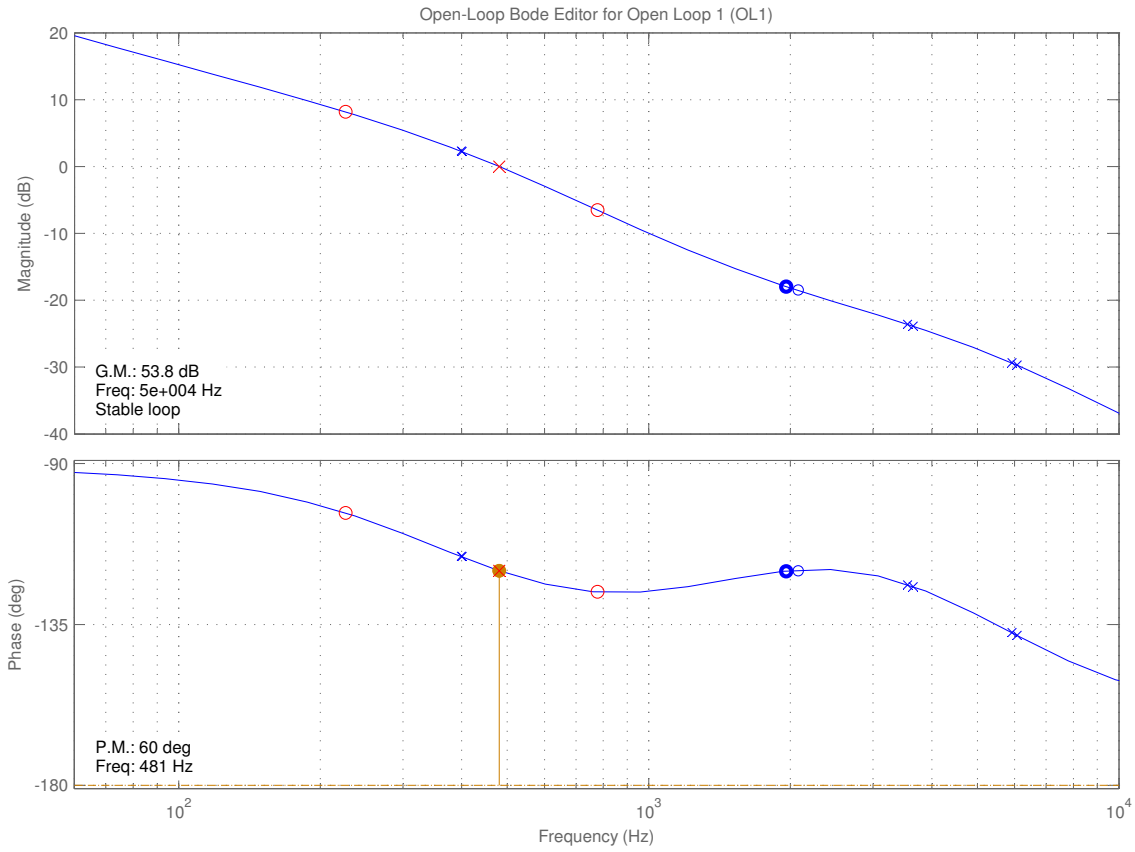


Figure 20: Open-loop Bode plot of prototype frequency response data

Given that a step change to the control voltage input is applied to the system, the closed-loop step response of the system is given by Figure 21, and shows a rise time of approximately 1 ms, and after 2.5 ms, the steady state error is reduced to zero. The overshoot of the step response is approximately 10%.

From the results of Figure 20 and Figure 21, it appears that a stable compensator with appropriate gain and phase margin has been designed. Since these results appear to be reasonable, the designed compensator coefficients can be exported to the PSIM® simulation model for verification.

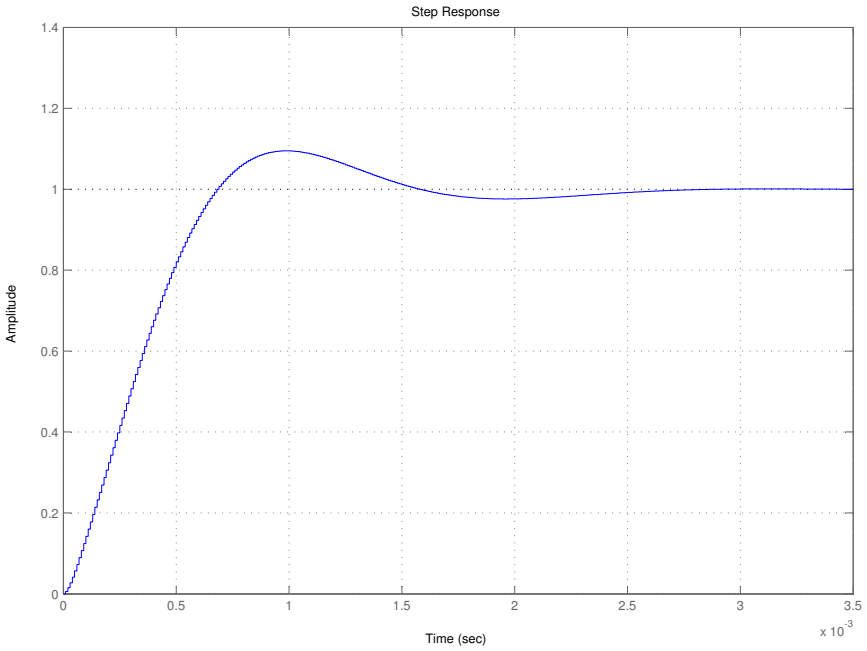


Figure 21: MATLAB® step response of closed-loop system using prototype model

4.1.4 Verification in PSIM®

The negative feedback control loop of Figure 15 was implemented and simulated using Powersim's PSIM® simulation software, a software specifically designed for power electronics simulation [27]. The simulation file includes a model of the LLC resonant converter in a negative feedback loop configuration. Additionally, to more closely model the effects of the DSP circuit, the sample-and-hold, and quantization effects of the analog-to-digital converter are also included in the model. As seen in [28], the A/D converter can be approximately modelled as an ideal switch switching at frequency f_{sample} and a zero-order hold (ZOH) block. It will be assumed that the sampling rate is high enough such that the sampling can be considered ideal. Additionally, a quantization block been included to simulate the quantization error during typical A/D conversion [27].

The complete circuit schematic of the PSIM® simulation model is shown in Figure 22, and the controller components are shown in Figure 23. The model of the 2P2Z compensator is implemented in the difference equation format according to Figure 16, and the VCO actuator is designed according to Equation 11.

In the simulation, the reference set point value of the voltage control loop was set to be 190 V. Figure 24 shows that the steady-state value of the error voltage approaches zero, and confirms that the controller meets the output regulation requirement.

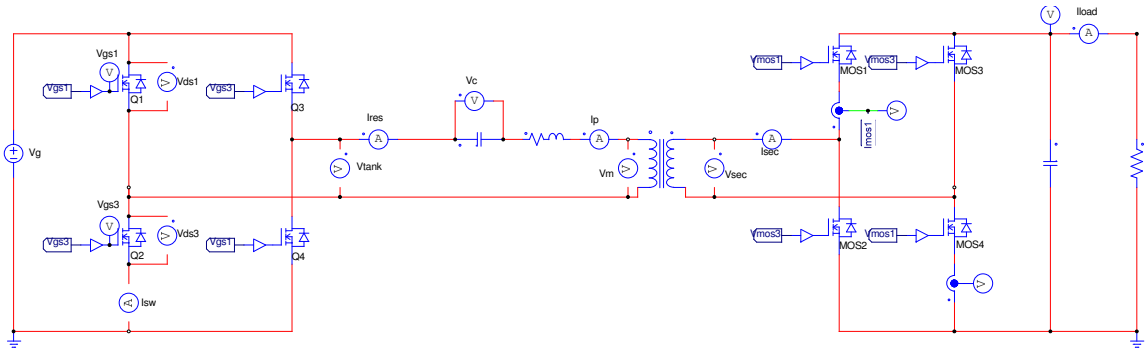


Figure 22: PSIM® circuit schematic of LLC resonant converter

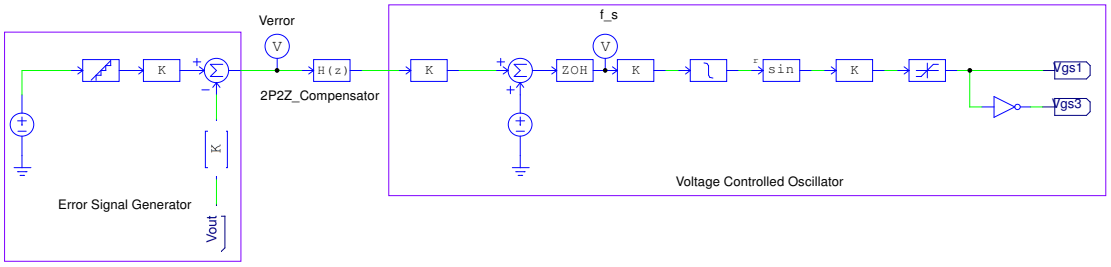


Figure 23: PSIM® controller schematic of LLC resonant converter

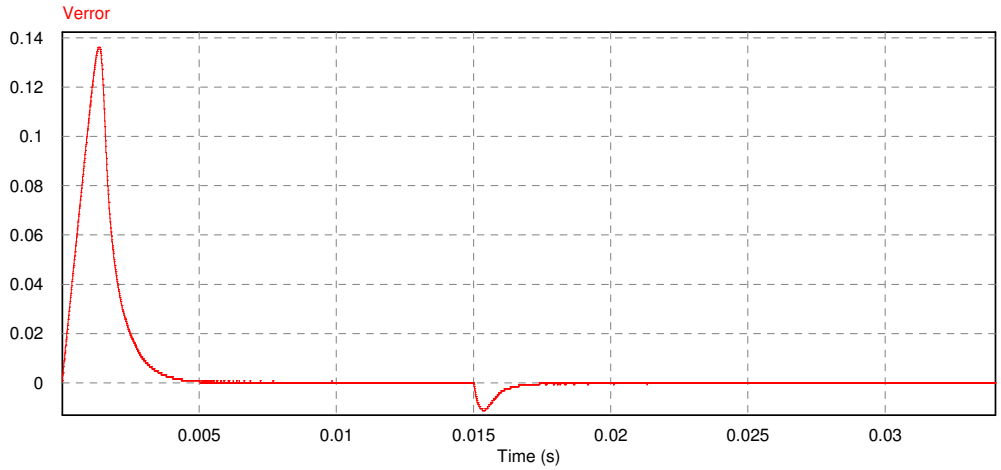


Figure 24: Error voltage of prototype model

A study of the effects of a steady-state load step change are shown in Figure 26. A step load change in the simulation is applied at t = 15ms, and from the results of Figure 26, it has been verified that the designed control system that has been implemented is functional and is able to maintain output voltage regulation even when undergoing changing loading conditions. As expected, the switching frequency f_s increases when the load was decreased. Figure 26 also shows the response of the current through the resonant tank, and the switching frequency.

For interest, the ripple voltage of the output voltage was also observed and was found to be approximately 1.4 mV and is shown in Figure 25.

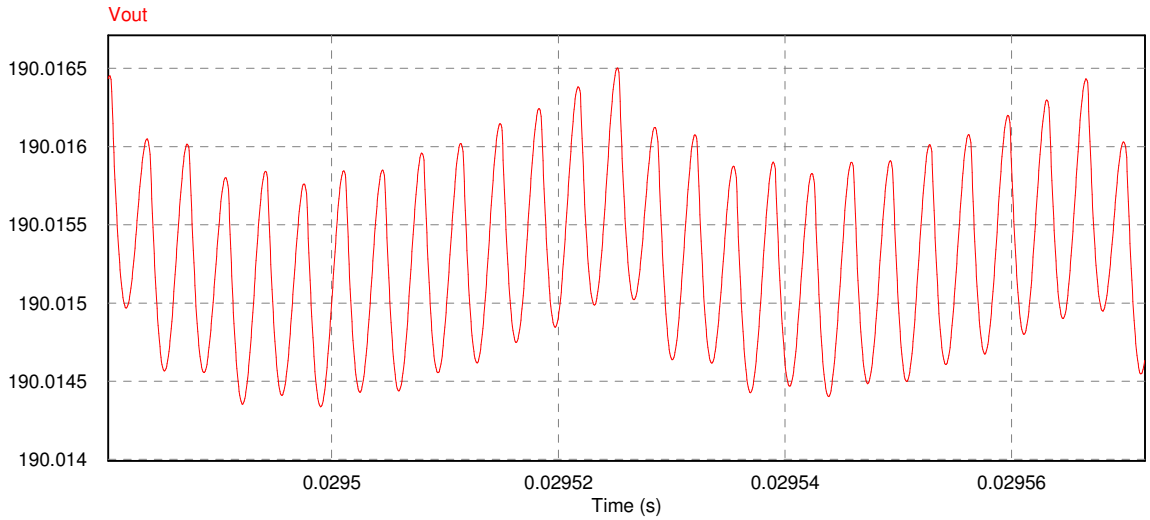


Figure 25: Output voltage ripple of prototype model

The results of the simulation are summarized in Table 1. Based on the final results, it can be concluded that a sufficient digital controller has been designed to achieve output regulation.

Output voltage value:	190 V
Steady-state error:	0 V
Output voltage ripple	1.4 mV
% overshoot:	10%
Rise-time:	1 ms
Settling-time:	2.5 ms

Table 1: Results of prototype model

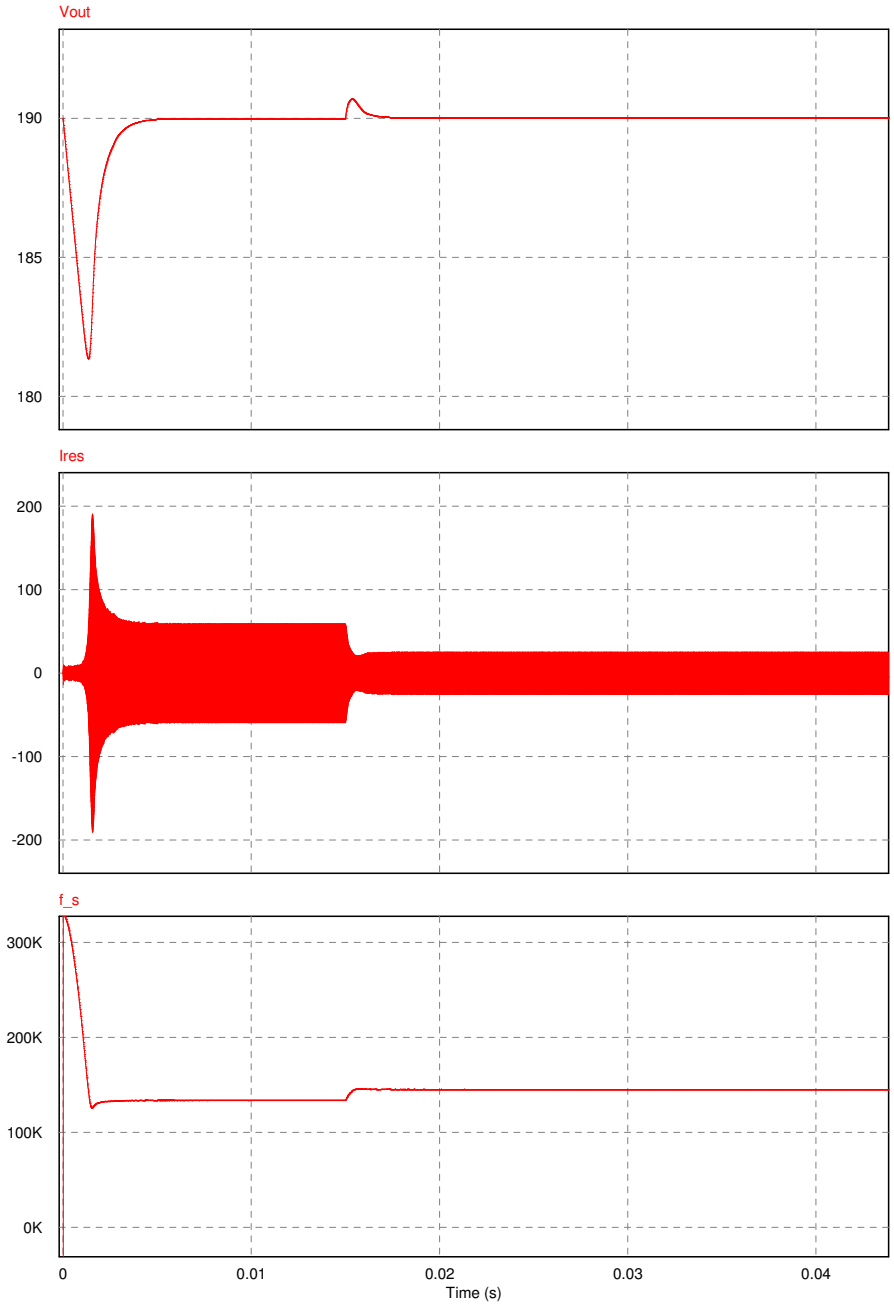


Figure 26: PSIM® closed-loop response to step load change using prototype model

4.2 Texas Instruments® DSP

To implement the voltage control loop digitally, a DSP is required. Texas Instruments® (TI) has a large portfolio of micro-controllers and digital signal processors available for use.

In this thesis, the TMS320F28035 Piccolo was selected as the ideal digital signal processor as it has the capability to use both the on-board central processing unit (CPU) as well as the additional Control Law Accelerator™ (CLA) platform. The CLA has the advantage of minimizing the processing latency of regular DSPs since it can execute time-critical control algorithms in parallel with the main CPU [29].

The voltage control loop can be implemented onto the CLA partition of the TMS320F28035 DSP using assembly language programming. To assist with the programming related to the CLA, the controlSUITE™package offered by TI provides many example code snippets for use.

Figure 27 shows an algorithm that can be used to implement the voltage control loop with the CLA.

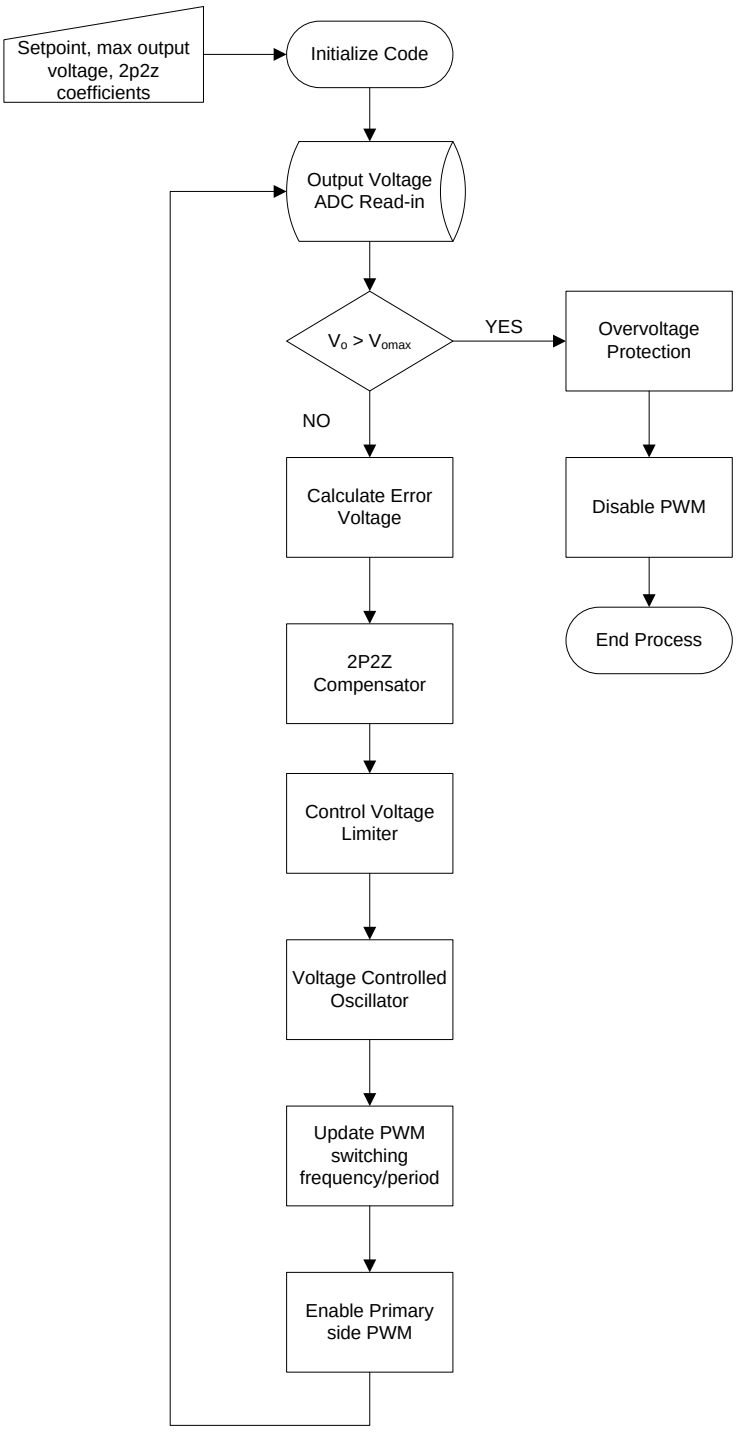


Figure 27: Voltage loop flow diagram for DSP implementation

5 Derivation of Control-to-Output Transfer Function

5.1 Overview

The control-to-output transfer function of the LLC resonant converter represents the ratio of the output voltage V_o to small signal variations in the switching frequency f_s. The difficulty in designing compensators for the LLC resonant converter lies in the fact that there are few known examples in literature of the control-to-output transfer function, which in this case represents the plant process model of the control loop.

Modelling the small signal characteristics of the LLC resonant converter is particularly difficult because many averaging techniques, such as state space models cannot be used. In [7] and [30], it is noted that unlike PWM converters, the control-to-output transfer of the converter cannot be obtained by the state space averaging methods, due to the way energy is processed in the LLC resonant converter.

Currently, most known applications ([30][31]) rely on bench measurements and frequency response data to help determine the plant process model for the design of the compensation network. In practice, the transfer function can be obtained by using a network analyzer to measure the frequency response of the plant process model, and then using the data to design the compensator. This methodology has the inherent disadvantage of requiring a pre-built functioning prototype model.

A proposed control-to-output transfer function that does not use frequency response data was presented in [32]. It was proposed that the control-to-output transfer function could be approximated as a third order polynomial. However, for the transfer function to be computed, variables such as the damping factor and the beat frequency of the converter need to be known. Additionally, a third order polynomial equation would not be able to predict the high frequency pole-zero shown in Figure 32.

Finally, similar to the method proposed in [7], computer simulation can also be used. The difficulty in creating a simulation model that can accurately model the true component and parasitic models may be difficult. With digital controllers, computer simulation is further complicated since the modelling of the effects of the DSP hardware can only be approximated. Additionally, as noted in [7], the computer simulation method requires extensive computing power.

5.2 Transfer Function Derivation

In the proceeding sections, a novel model of the small signal characteristics of the control-to-output transfer for the LLC resonant converter will be presented. A MATLAB® -based software program has been developed to determine the frequency response of the derivation results, and will be compared to the frequency response data obtained in Chapter 4.

As per Chapter 2, resonant converters that utilize variable frequency control regulate the output voltage by supplying sinusoids of different frequencies to the input of the resonant tank. The effect of this is to alter the tank impedance, and thus control the voltage drop across the resonant tank. Generating the appropriate sinusoid is accomplished by varying the switching frequency of the primary side switch network.

In order to develop a method to calculate the small signal control-to-output transfer function of the LLC resonant converter, techniques borrowed from communications theory can be used. More specifically, the operation and analysis of the converter can be described by using analogies similar to that of frequency modulation (FM), as well as amplitude modulation (AM).

The generalized block diagram shown in Figure 28 shows the steps of the analysis that will be taken for the development of the derivation model.

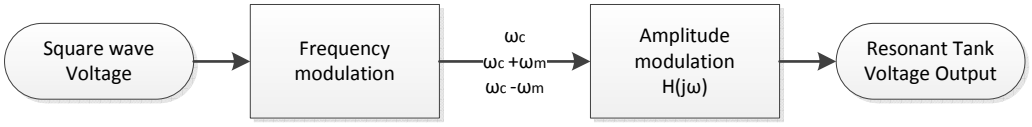


Figure 28: Analysis road map

5.2.1 Frequency Modulation

Recall that the general equation for a sinusoid is given by

$$v(t) = A\cos\left(\phi(t)\right) \tag{19}$$

Frequency modulation is defined as a deviation in frequency from the carrier signal frequency. Mathematically, this deviation in frequency can be expressed as the addition of an additional cosine term to the carrier frequency [33]. The radial frequency of a signal undergoing frequency modulation can be expressed as

$$\omega_s(t) = n\omega_c t + \Delta\omega\cos(\omega_m t) \tag{20}$$

In the above equation, $\Delta\omega$ is defined as the amplitude of the deviation from the carrier frequency, and ω_m, the modulating frequency, is defined as the rate of carrier deviation.

To arrive at an equation that can be substituted into Equation 19, the following relationship between the angular velocity $\omega_s(t)$ and the angle $\phi(t)$ is used.

$$\phi(t) = \int \omega_s(t)dt$$
$$\phi(t) = n\omega_c t + \frac{\Delta\omega \sin(\omega_m t)}{\omega_m} \tag{21}$$

In the scope of this thesis, it is known that the deviation is actuated by a voltage controlled oscillator and $\Delta\omega$ can be substituted by

$$\Delta\omega = 2\pi K_{VCO}\epsilon \tag{22}$$

where K_{VCO} is the gain of the voltage controlled oscillator, and the amplitude of the applied small signal perturbation is given by the constant ϵ.

Therefore, Equation 21 can be expressed as

$$\phi(t) = 2\pi \left(n f_c t + \frac{K_{VCO}\epsilon \sin(\omega_m t)}{\omega_m} \right) \tag{23}$$

To simplify Equation 23, the modulation index β can be substituted and is defined as

$$\beta = \frac{2\pi K_{VCO}\epsilon}{\omega_m} \tag{24}$$

5.2.2 Square Wave Approximation

The aforementioned mathematical relationships give a description of the effects of frequency modulation on the carrier frequency. However, prior to applying the above equations for use in analysis, the form of the original unmodulated signal must be determined.

The aperiodic square wave waveform is supplied from a DC voltage source and is produced as a result of switching complementary pairs of field effect transistor (FET) switches in the primary side FET bridge. Mathematically, a generic square wave signal undergoing frequency modulation is given as

$$V_s(t) = \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_g}{n\pi} \sin(n2\pi f_c t + \beta \sin(\omega_m t)) \tag{25}$$

In [7], it is acknowledged that analysis including harmonics up to the fifth harmonic may be useful in modelling the control-to-output transfer function of the LLC resonant converter. Computer simulations recorded in [7] show that by including the harmonic content, the accuracy of the models are improved.

The model proposed in this thesis includes the third and fifth harmonics, in addition to the fundamental frequency of the square wave waveform. By including the third and fifth harmonics in the model, a more accurate understanding of the true dynamics of the converter can be observed. Additionally, the effects of including supplementary sideband frequencies (for the case where $|\beta|$ does not meet the condition $|\beta| << 1$) are studied and included in the new model.

Equation 25 is therefore defined as

$$\begin{aligned} V_s(t) = &\frac{4V_g}{\pi}\sin\left(\omega_c t + \beta\sin(\omega_m t)\right) \\ &+\frac{4V_g}{3\pi}\sin\left(3\omega_c t + \beta\sin(\omega_m t)\right) \\ &+\frac{4V_g}{5\pi}\sin\left(5\omega_c t + \beta\sin(\omega_m t)\right) \end{aligned} \tag{26}$$

For simplicity, each individual harmonic component is redefined as $V_{s1}(t), V_{s3}(t)$, and $V_{s5}(t)$.

5.2.3 Bessel Functions of the First Kind

To gain better insight to the effects of frequency modulation, Bessel functions are used to determine the amplitudes of the carrier and resulting sideband frequencies.

Expanding Equation 26 by using Bessel functions has the advantage of determining the locations of the modulated frequencies in the frequency spectrum, as well as giving the amplitude of each frequency component. As an example, $V_{s1}(t)$ can be expanded using Bessel functions and is given by

$$\begin{aligned} V_{s1}(t) = J_o(\beta)\frac{4V_g}{\pi}\sin(\omega_c t) \pm J_1(\beta)\frac{4V_g}{\pi}\sin\left((\omega_c \pm \omega_m)t\right) \\ \pm J_2(\beta)\frac{4V_g}{\pi}\sin\left((\omega_c \pm 2\omega_m)t\right) \pm ... \pm J_n(\beta)\frac{4V_g}{\pi}\sin\left((\omega_c \pm n\omega_m)t\right) \end{aligned} \tag{27}$$

$J_n(\beta)$ is denoted as a Bessel function of the first kind and can be calculated by

$$J_n(\beta) = \sum_{m=0}^{\infty}\frac{(-1)^m}{m!\Gamma(m+n+1)}\left(\frac{\beta}{2}\right)^{2m+n} \tag{28}$$

In Equation 28, the variable n is the n^{th} sideband frequency, and β is the modulation index. In lieu of Equation 28, there are existing tables developed in [34], which can be used to determine corresponding values of $J_n(\beta)$ given the value of β.

In [35], there is an assumption that the value of $|\beta|$ is much less than one. This is normally a useful assumption as the following simplifications of the Bessel functions become valid.

$$J_0(\beta) \approx 1$$
$$J_n(\beta) \approx \frac{\beta^n}{n!2^n} \tag{29}$$

As can be seen in Equation 29, for values of β much less than one, higher order sideband frequencies will be approximately equal to zero.

However, since the assumption that β is much less than one is not always valid, the use of Equation 29 is quite restrictive. Therefore, in this thesis, the assumption of $|\beta|$ being much less than one is not used. Instead, the values of $|\beta|$ are determined and calculated in MATLAB® with the function '*besselj*'. This function is based on the tables found in [34].

Since the $|\beta|$ value is no longer assumed to be small, the higher order values of $J_n(\beta)$ become significant. Therefore, the n^{th} highest sideband to be considered remains to be determined.

It is known that the number of sidebands for the fundamental and harmonic components are determined by the value of the modulation index β. Theoretically, under frequency modulation, there are an infinite number of sideband frequencies, and therefore, a finite number of sideband frequencies must be selected in a way such that the majority of the signal's energy is captured.

According to Equation 24, β is inversely proportional to ω_m. From this, the conclusion can be drawn that as ω_m increases, the modulation index becomes small, and the total number of sideband frequencies is reduced.

Therefore, it can be said that the "worst-case" is the scenario when ω_m is at its smallest value, such that the value of $|\beta|$ becomes large. For the purpose of this thesis, the value of ω_m is taken to be located at 1000π rad/s. By setting ω_m to 1000π rad/s, a corresponding value of β is determined, and the number of sidebands required can also be determined.

To verify that there are a sufficient number of sideband frequencies, the sideband frequencies that account for 99% of the signal energy (in the pre-determined worst case) are considered.

The energy of a carrier and sideband signals is determined by

$$E = J_o(\beta)^2 + \sum_{n=1}^{x} 2(J_n(\beta))^2 \tag{30}$$

To determine how many sidebands are needed to have 99% of the signal energy, an increasing number of sidebands x is added to the carrier frequency amplitude until the value of E is equal to 0.99.

It was determined that by including three pairs of symmetrical sideband frequencies to the fun-

damental, third and fifth harmonic components, that 99% of the signal energy would be accounted for the case where ω_m is greater than 1000π rad/s. Thus, Equation 27 can be written as

$$V_{s1}(t) = J_o(\beta)\frac{4V_g}{\pi}\sin(\omega_c t) \pm J_1(\beta)\frac{4V_g}{\pi}\sin\left((\omega_c \pm \omega_m)t\right) \\ \pm J_2(\beta)\frac{4V_g}{\pi}\sin\left((\omega_c \pm 2\omega_m)t\right) \pm J_3(\beta)\frac{4V_g}{\pi}\sin\left((\omega_c \pm 3\omega_m)t\right) \tag{31}$$

5.2.4 Amplitude Modulation

Each individual frequency component is then passed through and filtered by the resonant tank circuit at their respective frequencies. This is equivalent to amplitude modulation (AM) and is mathematically equivalent to multiplying each frequency component with the resonant tank transfer function at the corresponding frequency. The resulting signal represents a voltage, that will be eventually applied to the secondary side of the converter.

As an example, the carrier, upper and lower sideband frequencies of the third harmonic undergoing amplitude modulation are given by Equations 32 - 38. Similar equations can be determined for the fundamental and fifth harmonic components.

$$V_{s3,carrier} = J_0(\beta) \times \frac{4V_g}{3\pi}\sin(3\omega_c t) \times H(3j(\omega_c)) \tag{32}$$

$$V_{s3,upper1} = J_1(\beta) \times \frac{4V_g}{3\pi}\sin\left((3\omega_c + \omega_m)t\right) \times H(j(3\omega_c + \omega_m)) \tag{33}$$

$$V_{s3,lower1} = -J_1(\beta) \times \frac{4V_g}{3\pi}\sin\left((3\omega_c - \omega_m)t\right) \times H(j(3\omega_c - \omega_m)) \tag{34}$$

$$V_{s3,upper2} = J_2(\beta) \times \frac{4V_g}{3\pi}\sin\left((3\omega_c + 2\omega_m)t\right) \times H(j(3\omega_c + 2\omega_m)) \tag{35}$$

$$V_{s3,lower2} = -J_2(\beta) \times \frac{4V_g}{3\pi}\sin\left((3\omega_c - 2\omega_m)t\right) \times H(j(3\omega_c - 2\omega_m)) \tag{36}$$

$$V_{s3,upper3} = J_3(\beta) \times \frac{4V_g}{3\pi}\sin\left((3\omega_c + 3\omega_m)t\right) \times H(j(3\omega_c + 3\omega_m)) \tag{37}$$

$$V_{s3,lower3} = -J_3(\beta) \times \frac{4V_g}{3\pi}\sin\left((3\omega_c - 3\omega_m)t\right) \times H(j(3\omega_c - 3\omega_m)) \tag{38}$$

The Euler formula is useful in this case, and is given by

$$\sin(\theta) = \frac{e^{j\theta} - e^{-j\theta}}{j2} \tag{39}$$

Applying Equation 39 to the trigonometric term of the resonant tank outputs, the above equations can be rewritten. As an example, the equations of the carrier and sideband frequencies for the third harmonic are shown in Equations 40 - 46. The equations for the fundamental and fifth harmonic components can be determined similarly.

$$V_{s3,carrier} = \frac{B_o e^{j3\omega_c t} - B_o^* e^{-j3\omega_c t}}{j2} \tag{40}$$

$$V_{s3,upper} = \frac{(B_u e^{j3\omega_m t})e^{j\omega_c t} - (B_u e^{j\omega_m t})^* e^{-j3\omega_c t}}{j2} \tag{41}$$

$$V_{s3,lower} = \frac{(B_l e^{-j\omega_m t})e^{j3\omega_c t} - (B_l e^{-j\omega_m t})^* e^{-j3\omega_c t}}{j2} \tag{42}$$

$$V_{s3,upper2} = \frac{(B_{u,2} e^{j2\omega_m t})e^{j3\omega_c t} - (B_{u,2} e^{j2\omega_m t})^* e^{-j3\omega_c t}}{j2} \tag{43}$$

$$V_{s3,lower2} = \frac{(B_{l,2} e^{-j2\omega_m t})e^{j3\omega_c t} - (B_{l,2} e^{-j2\omega_m t})^* e^{-j3\omega_c t}}{j2} \tag{44}$$

$$V_{s3,upper3} = \frac{(B_{u,3} e^{j3\omega_m t})e^{j3\omega_c t} - (B_{u,3} e^{j3\omega_m t})^* e^{-j3\omega_c t}}{j2} \tag{45}$$

$$V_{s3,lower3} = \frac{(B_{l,3} e^{-j3\omega_m t})e^{j3\omega_c t} - (B_{l,3} e^{-j3\omega_m t})^* e^{-j3\omega_c t}}{j2} \tag{46}$$

Where $B_o, B_u, B_l, B_{u,2}, B_{l,2}, B_{u,3}, B_{l,3}$ are defined by Equations 47 - 53

$$B_o = J_0(\beta) \times \frac{4V_g}{\pi} H(j3\omega_c) \tag{47}$$

$$B_u = J_1(\beta) \times \frac{4V_g}{3\pi} H(j(3\omega_c + \omega_m)) \tag{48}$$

$$B_l = -J_1(\beta) \times \frac{4V_g}{3\pi} H(j(3\omega_c - \omega_m)) \tag{49}$$

$$B_{u,2} = J_2(\beta) \times \frac{4V_g}{3\pi} H(j(3\omega_c + 2\omega_m)) \tag{50}$$

$$B_{l,2} = -J_2(\beta) \times \frac{4V_g}{3\pi} H(j(3\omega_c - 2\omega_m)) \tag{51}$$

$$B_{u,3} = J_3(\beta) \times \frac{4V_g}{3\pi} H(j(3\omega_c + 3\omega_m)) \tag{52}$$

$$B_{l,3} = -J_3(\beta) \times \frac{4V_g}{3\pi} H(j(3\omega_c - 3\omega_m)) \tag{53}$$

The resonant tank circuit $H(s)$ is given by Figure 29 and the s-domain transfer function is given by Equation 54.

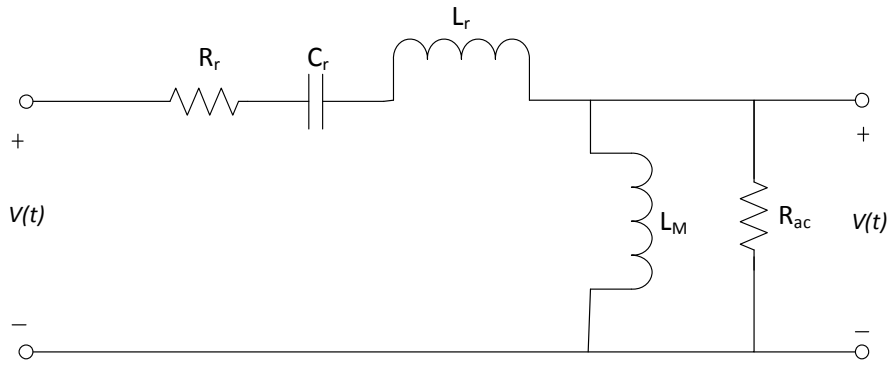


Figure 29: Tank filter circuit schematic with equivalent resistance R_{ac}

$$H(s) = \frac{s^2 C_r R_{ac} L_M}{s^3 L_r C_r L_M + s^2(C_r R_{ac} L_M + L_M C_r R_r + L_r C_r R_{ac}) + s(L_M + R_r C_r R_{ac}) + R_{ac}} \tag{54}$$

In the above equations, the frequency domain variable s is taken such that $s = j\omega_m$, and $j\omega_c$ is the quiescent operating point. This is done in order to work in terms of the relative frequency, rather than the absolute frequency.

The individual mathematical representations of the fundamental, third and fifth harmonic voltage outputs from the resonant tank have now been determined. The total output voltage of the resonant tank is then the sum of the harmonic output equations. The complete output voltage equation can therefore be written as

$$v(t) = ||A|| \sin(\omega_c t + \angle A) + ||B|| \sin(3\omega_c t + \angle B) + ||C|| \sin(5\omega_c t + \angle C) \tag{55}$$

Continuing with the previous given example, the vector B is therefore defined as

$$B = B_o + B_u e^{j\omega_m t} + B_l e^{-j\omega_m t} + B_{u,2} e^{j2\omega_m t} + B_{l,2} e^{-j2\omega_m t} + B_{u,3} e^{j3\omega_m t} + B_{l,3} e^{-j3\omega_m t} \tag{56}$$

Equation 55 represents the output voltage as a sinusoid having time-varying amplitude and also time-varying phase.

Since the goal of this analysis is to determine the change in output voltage due to the effect of small variations to the switching frequency, the magnitude of Equation 55 must be evaluated. As was discussed, the effect of passing frequency signals through the resonant tank is the same as applying amplitude modulation (AM). Therefore, similar to AM analysis techniques, the envelope of the waveform should be extracted to study the change in the output voltage [33].

From AM analysis, it is known that the magnitude of the coefficients $||A||$, $||B||$, and $||C||$ contain the envelope of the signal. The square of the magnitude can firstly be determined by multiplying the vector with its complex conjugate. E.g. for B, the magnitude can be determined by

$$||B||^2 = BB^* \tag{57}$$

To make use of some mathematical simplifications, it is assumed that only the dominant DC components are relevant. If this is true, then the following approximation can be made.

$$\sqrt{1+\xi} \approx 1 + \frac{1}{2}\xi \tag{58}$$

Thus, the magnitudes of A, B, and C are determined to be

$$\begin{aligned}
||A|| = {} & ||A_o|| + ||A_l|| \\
& + \frac{||A_o A_l^* + A_u A_o^* + A_l A_{l,2}^* + A_{u,2} A_u^*||}{||A_o||} \sin(\omega_m t + \angle(A_o A_l^* + A_u A_o^* + A_l A_{l,2}^* + A_{u,2} A_u^*)) \\
& + \frac{||A_o A_{l,2}^* + A_u A_l^* + A_l A_{l,3}^* + A_{u,2} A_o^* + A_{u,3} A_u^*||}{||A_o||} \sin(3\omega_m t + \angle(A_o A_{l,2}^* + A_u A_l^* + A_l A_{l,3}^* + A_{u,2} A_o^* + A_{u,3} A_u^*)) \\
& + \frac{||A_o A_{l,3}^* + A_u A_{l,2}^* + A_{u,2} A_l^* + A_{u,3} A_o^*||}{||A_o||} \sin(5\omega_m t + \angle(A_o A_{l,3}^* + A_u A_{l,2}^* + A_{u,2} A_l^* + A_{u,3} A_o^*))
\end{aligned} \tag{59}$$

$$
\begin{aligned}
||B|| &= ||B_o|| + ||B_l|| \\
&\quad + \frac{||B_o B_l^* + B_u B_o^* + B_l B_{l,2}^* + B_{u,2} B_u^*||}{||B_o||} \sin(\omega_m t + \angle(B_o B_l^* + B_u B_o^* + B_l B_{l,2}^* + B_{u,2} B_u^*)) \\
&+ \frac{||B_o B_{l,2}^* + B_u B_l^* + B_l B_{l,3}^* + B_{u,2} B_o^* + B_{u,3} B_u^*||}{||B_o||} \sin(3\omega_m t + \angle(B_o B_{l,2}^* + B_u B_l^* + B_l B_{l,3}^* + B_{u,2} B_o^* + B_{u,3} B_u^*)) \\
&\quad + \frac{||B_o B_{l,3}^* + B_u B_{l,2}^* + B_{u,2} B_l^* + B_{u,3} B_o^*||}{||B_o||} \sin(5\omega_m t + \angle(B_o B_{l,3}^* + B_u B_{l,2}^* + B_{u,2} B_l^* + B_{u,3} B_o^*)) \quad (60)
\end{aligned}
$$

$$
\begin{aligned}
||C|| &= ||C_o|| + ||C_l|| \\
&\quad + \frac{||C_o C_l^* + C_u C_o^* + C_l C_{l,2}^* + C_{u,2} C_u^*||}{||C_o||} \sin(\omega_m t + \angle(C_o C_l^* + C_u C_o^* + C_l C_{l,2}^* + C_{u,2} C_u^*)) \\
&+ \frac{||C_o C_{l,2}^* + C_u C_l^* + C_l C_{l,3}^* + C_{u,2} C_o^* + C_{u,3} C_u^*||}{||C_o||} \sin(3\omega_m t + \angle(C_o C_{l,2}^* + C_u C_l^* + C_l C_{l,3}^* + C_{u,2} C_o^* + C_{u,3} C_u^*)) \\
&\quad + \frac{||C_o C_{l,3}^* + C_u C_{l,2}^* + C_{u,2} C_l^* + C_{u,3} C_o^*||}{||C_o||} \sin(5\omega_m t + \angle(C_o C_{l,3}^* + C_u A_{l,2}^* + C_{u,2} C_l^* + C_{u,3} C_o^*)) \quad (61)
\end{aligned}
$$

In Equations 59, 60, and 61, it is shown that each harmonic component has a DC and a small signal cosine term. It is known that the envelope function is represented by the amplitude of the small signal term, and this is the value of output voltage that is to be observed in the control-to-output transfer function.

Therefore, to get the transfer function $P(s) = \frac{V_o}{f}$, the magnitude of the envelope voltage expression is divided by the small signal variation in frequency represented by $\frac{\Delta\omega}{2\pi}$, as defined by Equation 22.

5.2.5 Results of Frequency and Amplitude Modulation

Figure 30 shows the frequency response of each harmonic component and shows the contribution of each harmonic after being filtered by the resonant tank circuit. The results of Figure 30 confirm the third and fifth harmonic components have significant contribution to the transfer function, and therefore it has been shown that they may not be neglected in analysis.

The result of the summation of the fundamental, third and fifth harmonic components is also shown in Figure 30.

For comparison, Figure 31 is a plot of the fundamental harmonic component and shows the effect of including and not including the sideband frequencies in the derivation model. From the results of Figure 31, it can be seen that the sideband frequencies have a significant effect on the resulting magnitude plot.

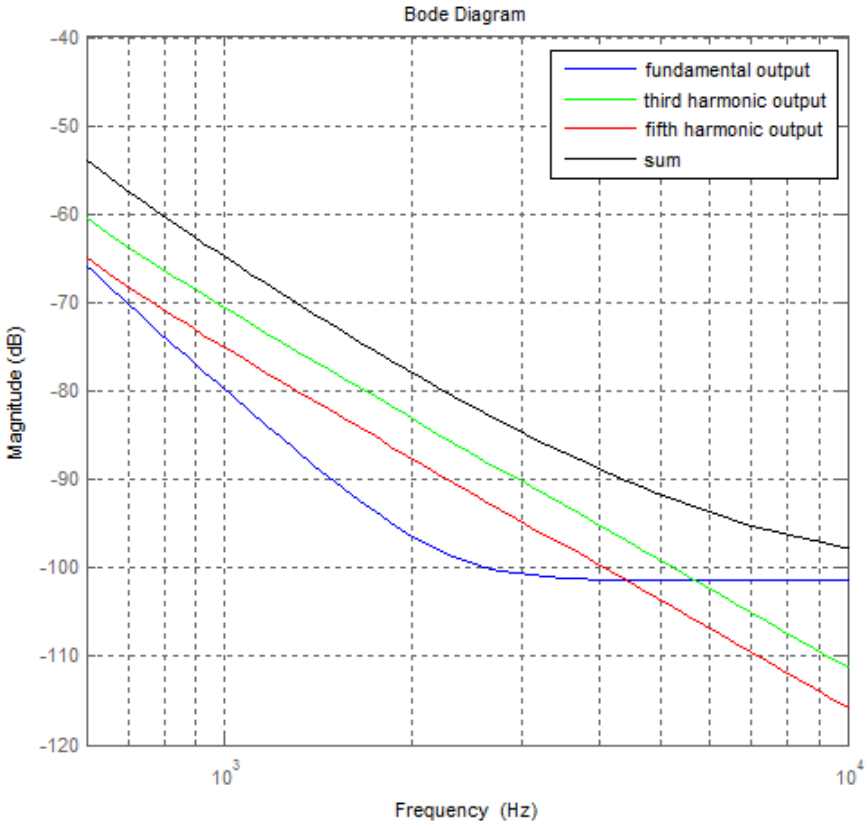


Figure 30: Comparison of the significance between fundamental, third and fifth harmonics

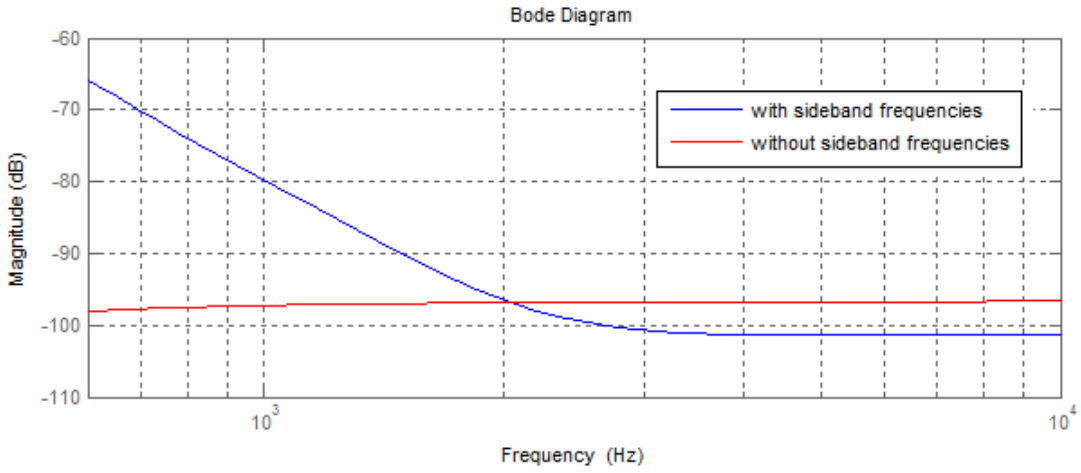


Figure 31: Comparison of the fundamental component, with and without sideband frequencies

5.2.6 Isolation Transformer and Rectification Stage

The next stage of the LLC resonant topology is the high frequency isolation transformer, located after the resonant stage. To model the effect of the transformer on the control-to-output transfer function, the transformer turns ratio can be multiplied to the magnitude of Equation 55 in order to get an equation of the voltage seen on the secondary side of the converter.

$$v_{secondary}(t) = \frac{N_1}{N_2} \times v(t) \tag{62}$$

The frequency response data of Figure 18 shows that a pole-zero combination appears at high frequencies. It was determined that the cause of the zero is a result of the output capacitor equivalent series resistance, as well as the presence of a right hand plane zeros (RHPZ). In [36], it is stated that the RHPZ is a result of the inductor current not being able to instantaneously change, and is a function of the inductance and load [37].

The ESR zero is located at a fixed frequency, and is given by Equation 63.

$$\omega_{esr} = \frac{1}{C_o R_c} \tag{63}$$

The ESR and RHPZ zeros are compensated by high frequency poles which were determined to be contributed by system delays [38]. A system delay in the s-domain can be given by

$$H_{delay}(s) = e^{-sT} \tag{64}$$

To evaluate Equation 64, the third order Padé approximation is used and the transfer function of the high frequency pole is given by Equation 65 [39].

$$e^{-sT} \approx \frac{60 - 24sT + 3(sT)^2}{60 + 36sT + 9(sT)^2 + (sT)^3} \tag{65}$$

By combining all of the above effects presented with the results of Figure 30, the analysis finally gives the magnitude plot of the derivation model of the control-to-output transfer function. The results of the analysis can be compared to the frequency response data of Chapter 4 and are shown in Figure 32.

5.2.7 Results of Analysis of the Derivation Model

Figure 32 compares the results of the derivation model and the frequency response data of the prototype model. From the results, it can be seen that the derivation model is a good approximation of the frequency response data, and therefore confirms the proposed model is adequate for modelling the small signal control-to-output transfer function. Therefore, it has been shown that by including

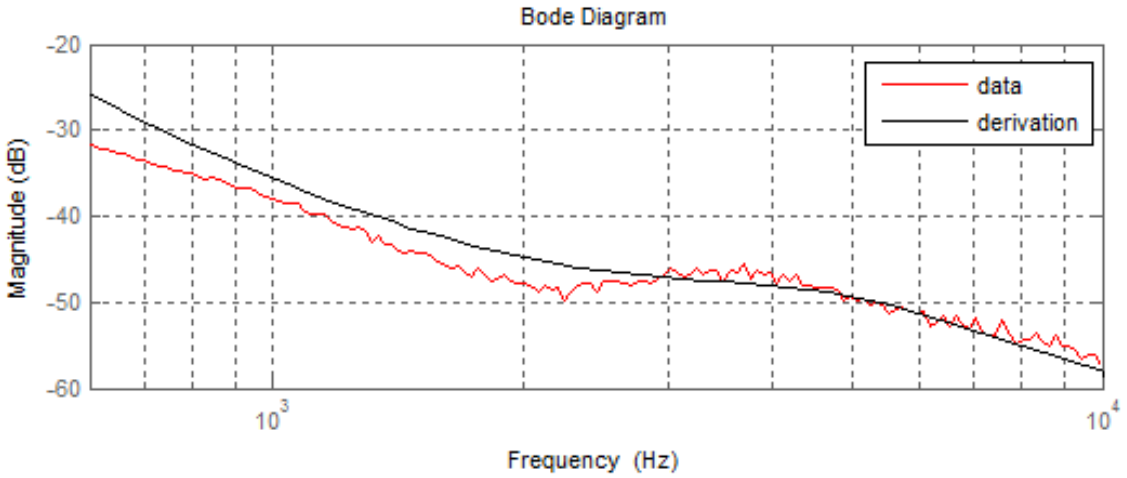


Figure 32: Comparison of prototype frequency response data and derivation model (magnitude)

harmonics up to the fifth harmonic, as well as sideband frequencies in the derivation model, a reasonably accurate model of the small signal control-to-output transfer function can be achieved.

From Figure 32, it is observed that at the lower frequencies, the error is largest, and there is approximately a maximum of 5 dB difference between the frequency response data and the derivation model. This non-conformity can be attributed to have not included enough of the sideband frequencies in the model.

As was discussed in Section 5.2.3, the derivation model only considers the sideband frequencies that appear under the condition $\omega_m = 1000\pi$ rad/s. The equivalent value of this ω_m in frequency is at 500 Hz, and from Figure 32, it can be seen that this is approximately the point at which the discrepancies appear. Therefore, if the chosen value of ω_m was smaller, more sideband frequencies would have been added to the model, and the accuracy of the derivation model would improve for the low frequency region.

The importance of the sideband frequencies is further shown in Figure 32, such that for frequencies greater than 2 kHz, the derivation model gives a very close approximation of the magnitude response of the bench prototype model.

5.2.8 Phase Response of Control-to-Output Transfer Function

To gain an understanding of the phase response of the control-to-output transfer function, the asymptotic Bode tracing technique of [40] can be applied to the magnitude response. This method approximates the s-domain transfer function of frequency response plots by using knowledge of the behaviors of simple poles and zeros.

$$|H(s)| = k\frac{\prod_{i=1}^{m}|(s-z_i)|}{\prod_{i=1}^{n}|(s-p_i)|} \tag{66}$$

$$\angle H(s) = \sum_{i=1}^{m}\angle(s-z_i) - \sum_{i=1}^{n}\angle(s-p_i) \tag{67}$$

By extracting an approximate s-domain transfer function equation of the magnitude response, the corresponding phase response can be obtained. The accuracy of the plot can be increased simply by increasing the number of poles and zeros used to model the magnitude response.

The curve fit result is shown in Figure 33 and is compared to the frequency response phase data.

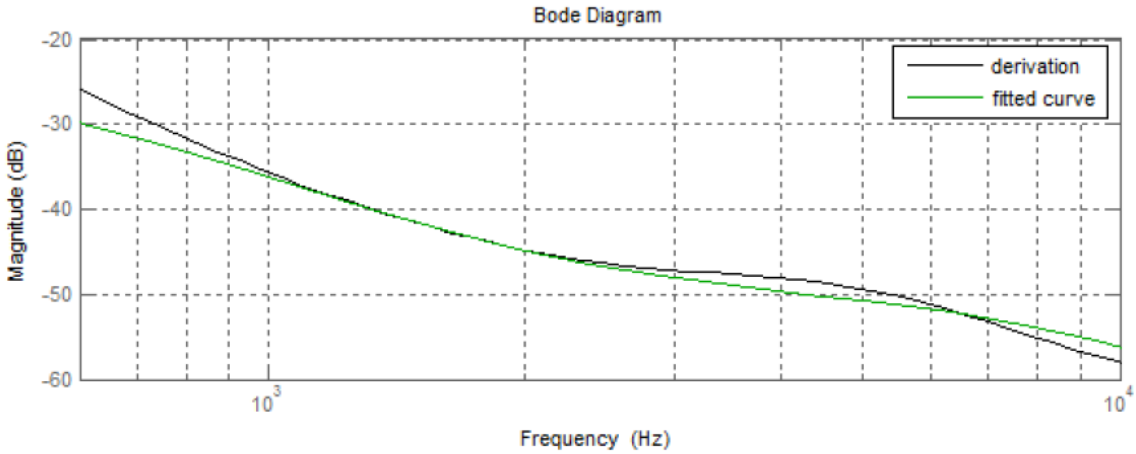


Figure 33: Comparison of derivation model and curve fit model (magnitude)

Figure 33 shows a reasonable curve fitting of the derivation model frequency response. As previously stated, the accuracy of the curve fit can be adjusted by increasing the number of poles and zeros used during the curve fitting process.

There are several alternative methods in which a curve fit of the frequency response can be obtained. However, compared to asymptotic Bode tracing, many of the analytical methods presented in literature such as [41] [42], are cumbersome and unmanageable for normal use, and methods that use software tools are costly to acquire and offer little to no flexibility in terms of pole/zero placement [30].

Figure 34 compares the results of the phase plot from the derivation model and is compared with the frequency response data of Chapter 4. The results appear to be a good quality approximation of the obtained data. However, it can be noted that the curve fit model presents a more pessimistic view of the phase response, and was unable to capture phase lead characteristic between 2 and 4 kHz.

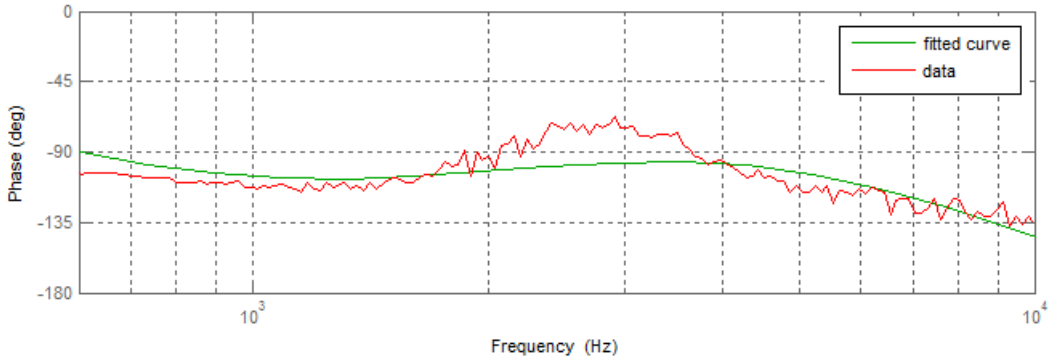


Figure 34: Comparison of prototype frequency response data and curve fit model (phase)

5.3 Verification of Derivation Model in PSIM®

To verify that the derivation model can be used as an approximation of the control-to-output transfer function, a compensator based on the derivation model results was designed in MATLAB®. The results are shown in Figures 35 - 38, and are summarized in Table 2.

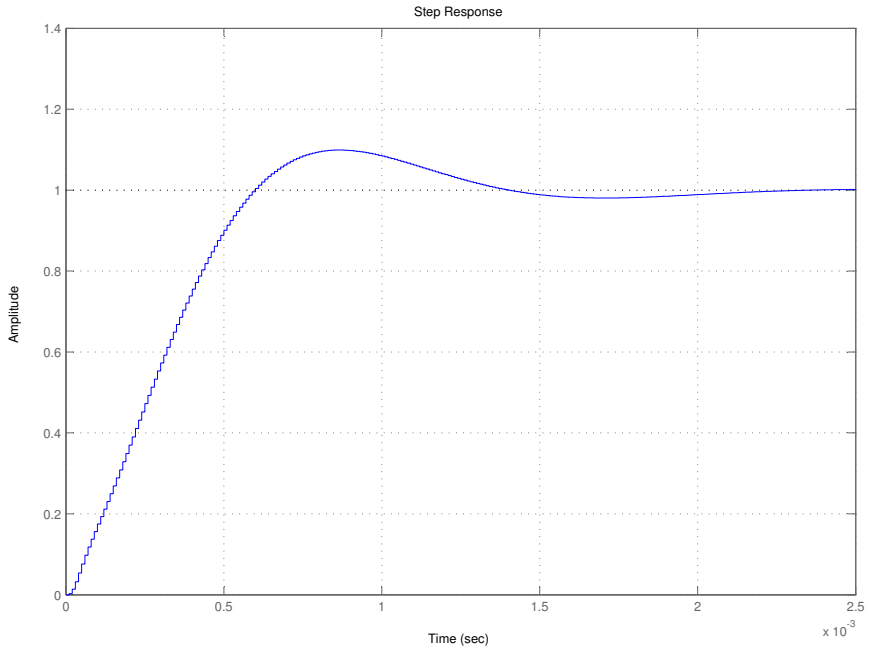


Figure 35: MATLAB® step response of closed-loop system using derivation model

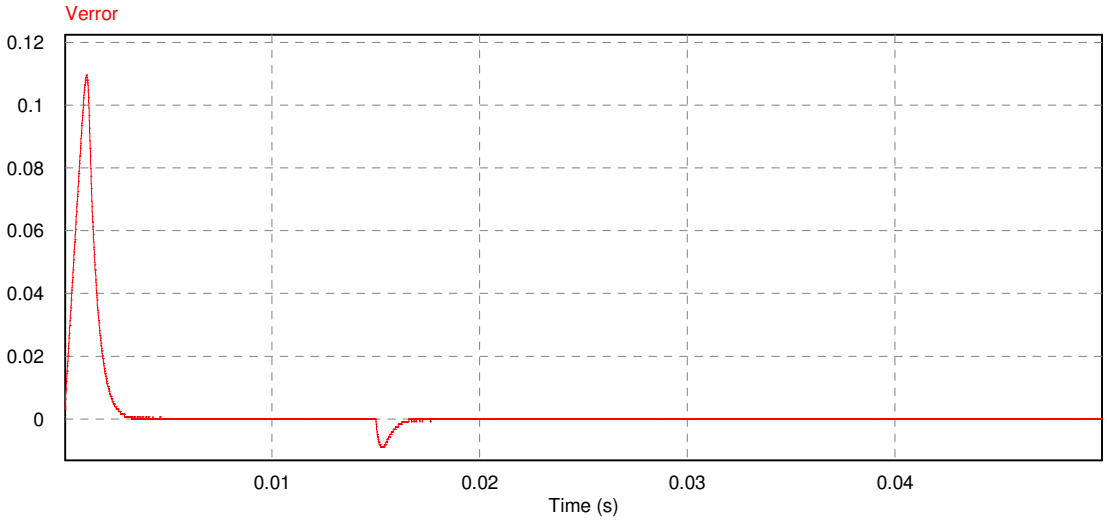


Figure 36: Error voltage of derivation model

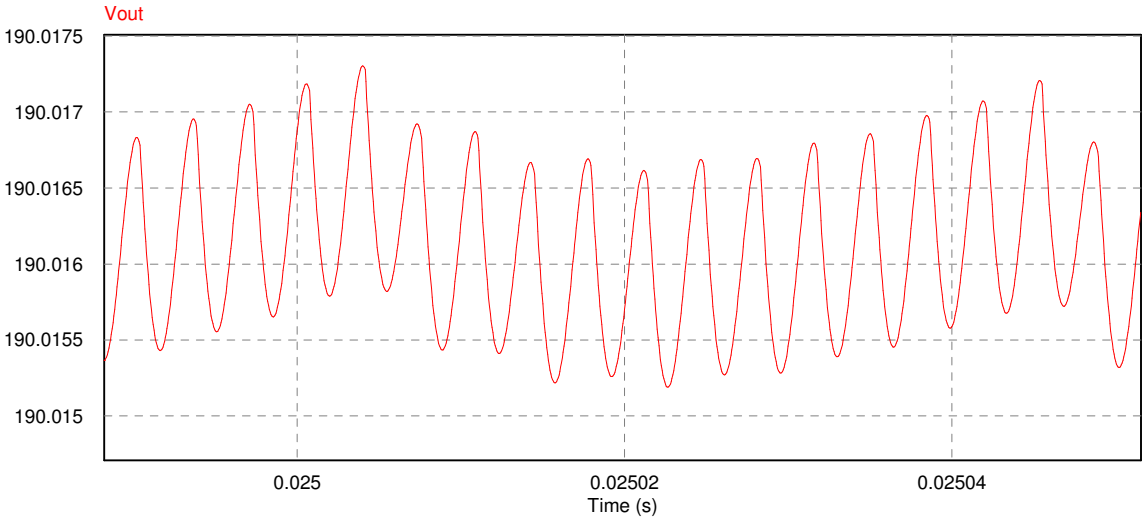


Figure 37: Output voltage ripple of derivation model

The results of the digital negative feedback control system designed by using the derivation model are summarized in Table 2. It was found that the results of Table 2 are comparable to those of Table 1 found in Chapter 4. Therefore, it can be concluded that the derivation model can be used for digital compensator design, and is able to produce similar results to a compensator designed based on physical prototype data.

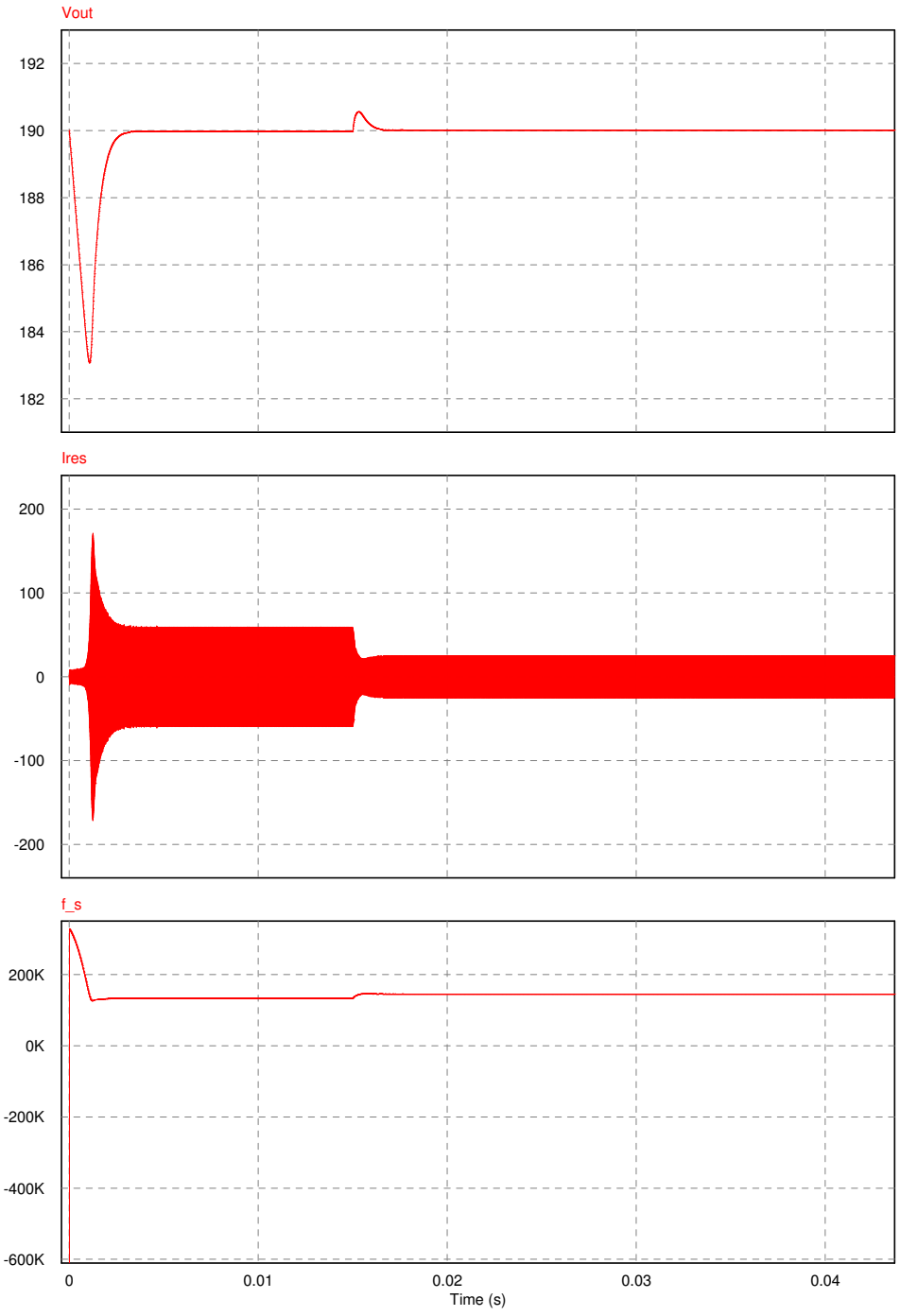


Figure 38: PSIM® closed-loop response to step load change using prototype model

Output voltage value:	190 V
Steady-state error:	0 V
Output voltage ripple	1.5 mV
% overshoot:	10%
Rise-time:	0.9 ms
Settling-time:	2 ms

Table 2: Results of derivation model

The merit of these results is the confirmation that the small signal control-to-output transfer function obtained by the derivation model can also be used to determine a digital compensator in lieu of using prototype frequency response data. The first advantage of the derivation model method is that only the circuit parameters of the proposed LLC resonant converter are required, and no physical prototype model is needed to obtain the frequency response data. Secondly, compared to computer simulation software which can also be used to obtain the plant transfer function, the derivation model requires significantly less computational power, and is considerably faster in terms of simulation run-time.

6 Conclusions and Future Work

6.1 Summary

In this thesis, the LLC resonant converter topology and the variable frequency control method for output voltage regulation was discussed in detail.

In Chapter 2, it was determined that the LLC resonant converter is an excellent choice for a power electronic converter topology to be used in isolated DC-DC conversion applications. The LLC resonant converter was found to feature high efficiency, high power density, and the ability to operate over a wide range of loading conditions. The LLC resonant converter also has many other advantageous features including low electromagnetic interference, and soft-switching capabilities.

Chapter 3 discusses the application of a controller to the LLC resonant converter. It was determined that the preferred control method under nominal loading conditions is variable frequency control, a method which varies the switching frequency of the converter to regulate the output voltage. The 2-pole-2-zero compensator was introduced as a possible suitor for a digital control system, as it can be easily implemented within digital signal processors by using difference equations. The stability of continuous and discrete-time control systems was also discussed and the application of Bode diagrams and Nyquist plots for control system design was explored.

It was then shown in Chapter 4 that by using a combination of laboratory bench measurements, and computer simulation, that a digital compensator could be designed to very tightly regulate the output voltage. An algorithm was then presented to implement the voltage control loop in a digital signal processor.

In Chapter 5, a novel derivation of the small signal control-to-output transfer function was completed. The model includes the use of the fundamental, third and fifth harmonics, and showed that the higher order harmonics have a significant contribution to the overall transfer function, and it should be necessary to include them to capture the true dynamics of the control-to-output transfer function. The new model also includes higher order sideband frequencies and it was confirmed that the higher order sideband frequencies are required for modelling the converter for the case(s) where the magnitude of the modulation index β does not meet the condition $|\beta| << 1$.

It was then verified that the small signal control-to-output transfer function developed in the derivation model could used to design a digital compensator for a digital negative feedback control system. The simulation results show that an acceptable closed-loop step response and output voltage regulation was achieved, and had comparable results to the results of Chapter 4.

Finally, it was concluded that the results of Chapter 5 were comparable to the results of Chapter 4 and that the small signal control-to-output transfer function could be obtained using the derivation model. The advantages of using the derivation model are reduced computational complexity and the diminished requirement for a physical prototype model.

6.2 Future Work

There are several areas which can be explored further to improve the modelling of the LLC resonant converter control-to-output transfer function.

Firstly, development of the model for the low frequency range can be investigated, and can be achieved by decreasing the value of ω_m, and therefore, introducing the case where modulation index β is large. To calculate large values of β, a different method to calculate and obtain the Bessel function coefficient $J_n(\beta)$ may be required.

Secondly, a more in depth method to describe the rectifier model is also needed. As there are certain loading conditions which cause the LLC resonant converter to go into discontinuous conduction mode, the linearizion of the rectifier circuit may not be valid for all scenarios.

Thirdly, another topic of interest would be to determine a practical method in which synchronous rectification can be achieved. In addition to an increase in the efficiency of the converter, there is also potential of having bidirectional power flow between the input and output. In the case where a battery is used to provide DC power at the input, this means the battery could also be charged by the load without any additional conversion processes.

Fourthly, it was also observed that there was a significant effect on the control-to-output transfer function from the output capacitance and its equivalent series resistance. Therefore, a self-tuning controller has potential to be of great value for the design of controllers for the LLC resonant converter. It may be able to offset errors in the modelling process that are caused by the tolerances, the effects of aging capacitance, or the variation in capacitance from operation in environments with non-ideal temperatures.

Lastly, there have also been several improvements in switching device technology since the beginning of this work. Silicon carbide-based transistors and diodes have been shown many significant advantages including lower conduction losses, higher frequency operation, as well as higher operable temperatures.

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Appendices

Appendix A: Observation of Stability in Continuous and Discrete-time domains

A1: Continuous-time domain

To determine the stability and the dynamic characteristics of the closed loop feedback system of Figure 14, the transfer function of Figure 14 can be described by Equation A-1. Assuming that the actuator has a gain equal to 1,

$$T(s) = \frac{G(s)P(s)}{1 + G(s)P(s)} \tag{A-1}$$

In the continuous-time domain, the stability of the feedback system is observed on the s-domain plane. The stability can be determined by evaluating the denominator of Equation A-1, also known as the characteristic equation. Solving for the roots of the characteristic equation gives the poles of the system, which are indicators of the system's stability.

A system that contains only poles on the left hand side of the $j\omega$ axis of the s-domain plane are considered to be stable, while systems with poles on the right hand side of the $j\omega$ axis are unstable. Marginally stable systems have poles on the $j\omega$ axis.

A2: Discrete-time domain

In the discrete-time domain, the stability of the feedback system is observed with respect to the z-domain unit circle. Stable systems have all poles located inside of the unit circle, while unstable systems have poles located outside of the unit circle. Finally, marginally stable systems have poles located on the unit circle.

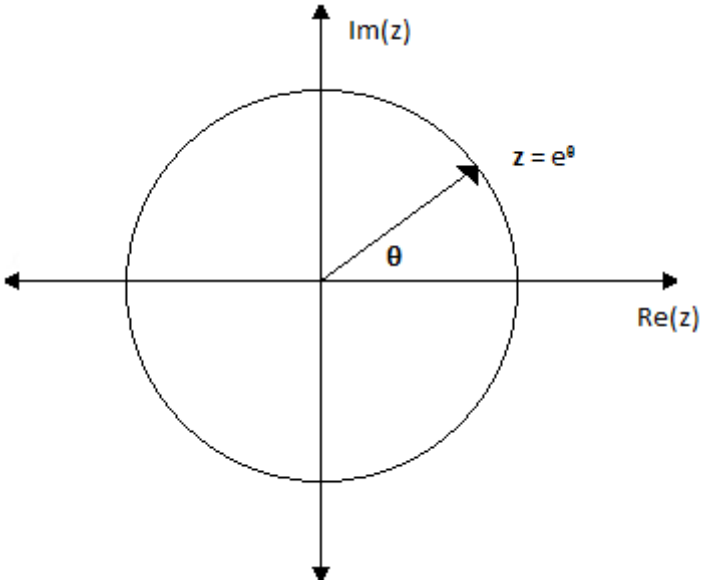

Figure A-1: Unit circle in the z-domain

Appendix B: PSIM®simulation schematics

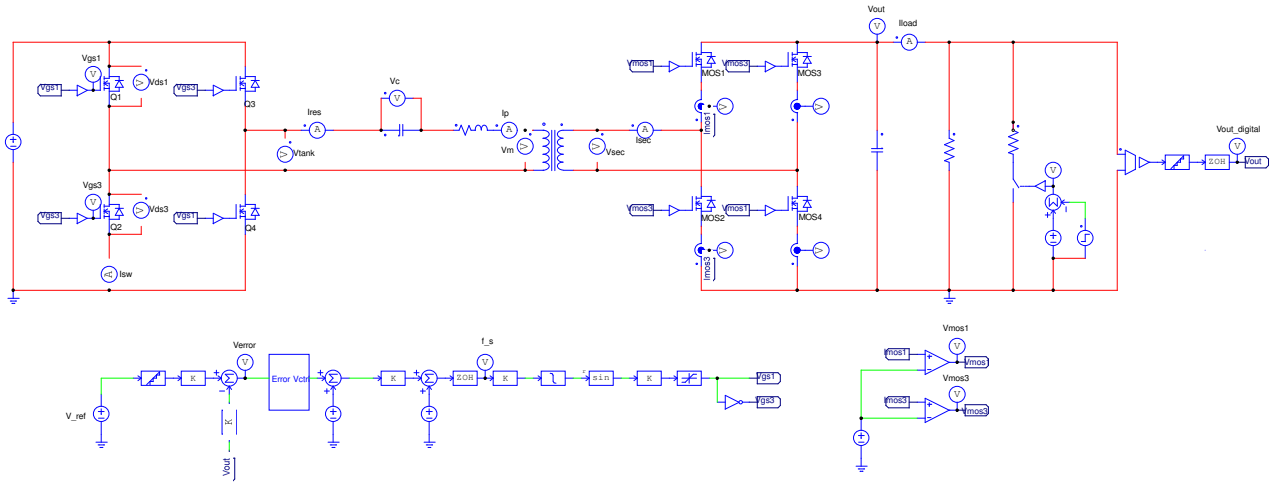

Figure B-1: PSIM® closed loop circuit schematic of LLC resonant converter

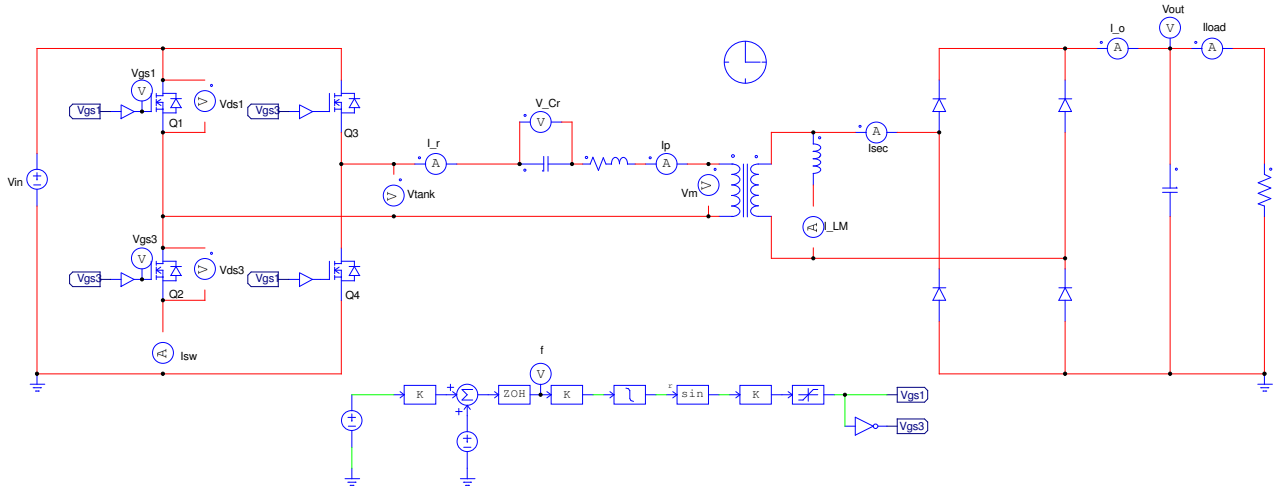

Figure B-2: PSIM® open loop circuit schematic of LLC resonant converter

Appendix C: MATLAB®derivation model code

```
clear all
close all
clc

Vg = 48;
Kvco = 32779;
Tratio = 15/4;

delta_w = 2*pi*(Kvco)*0.02;

Lm = (80e-6)*((4/15)^2);
Lr = (10e-6)/((15/4)^2);
Cr = 9*270e-9;
R = 1;
Rr = R;
Ro = 170/4.6;
Rac = ((8*Tratio^2)/pi^2)*Ro;

res_freq = 1/(sqrt(Lr*Cr)*2*pi)
w_so = 2*pi*res_freq;

V_s1 = (4/pi)*Vg;
V_s3 = (4/(3*pi))*Vg;
V_s5 = (4/(5*pi))*Vg;

Rc = 0.159;
C = 470e-6;
ESRzero = tf([(C*Rc) 1],[1]);
[mag_ESRzero phase_ESRzero] = bode(ESRzero,logspace(1,6,200));
mag_ESRzero = squeeze(mag_ESRzero);
phase_ESRzero = squeeze(phase_ESRzero);

fz = 3100;
RHPzero = tf([-1/(2*pi*fz) 1],[1]);
[mag_RHPzero phase_RHPzero] = bode(RHPzero,logspace(1,6,200));
mag_RHPzero = squeeze(mag_RHPzero);
phase_RHPzero = squeeze(phase_RHPzero);

T = 1/8000;
ZOHpole = tf([3*T^2 -24*T 60],[T^3 9*T^2 36*T 60]);
[mag_ZOHpole phase_ZOHpole] = bode(ZOHpole,logspace(1,6,200));
mag_ZOHpole = squeeze(mag_ZOHpole);
phase_ZOHpole = squeeze(phase_ZOHpole);

%%%%%%%%fundamental frequency
```

```
a = Cr*Rac*Lm;
b = Lr*Cr*Lm;
c = (Cr*Rac*Lm)+(Lm*Cr*Rr)+(Lr*Cr*Rac);
d = Lm+(Rr*Cr*Rac);
e = Rac;

%with Rload
H_jwso = tf([a*(i*w_so)^2],[b*(i*w_so)^3+c*(i*w_so)^2+d*(i*w_so)+e]);
H_jwsoConj = tf([a*(-i*w_so)^2],[b*(-i*w_so)^3+c*(-i*w_so)^2+d*(-i*w_so)+e]);

%with Rload
H_jwsoPluswm = tf([a a*2*i*w_so -a*w_so^2],[b (b*3*i*w_so+c) (-b*3*w_so^2+c*2*i*w_so
    +d) (e-c*w_so^2-b*i*w_so^3+d*i*w_so)]);
H_jwsoPluswmConj = tf([a a*2*i*w_so -a*w_so^2],[-b (-b*3*i*w_so+c) (b*3*w_so^2+c*2*i
    *w_so-d) (b*i*w_so^3-c*w_so^2-d*i*w_so+e)]);

%with Rload
H_jwsoMinuswm = tf([a -2*i*w_so*a -a*w_so^2],[-b (b*3*i*w_so+c) (b*3*w_so^2-c*2*i*
    w_so-d) (e-b*j*w_so^3-c*w_so^2+d*i*w_so)]);
H_jwsoMinuswmConj = tf([a -2*i*w_so*a -a*w_so^2],[b (-b*3*i*w_so+c) (-b*3*w_so^2-c
    *2*i*w_so+d) (e-c*w_so^2+b*i*w_so^3-d*i*w_so)]);

%with Rload
H_jwsoPlus2wm = tf([4*a 4*a*i*w_so -a*w_so^2],[8*b (12*b*i*w_so+4*c) (-b*6*w_so^2+4*
    i*c*w_so+2*d) (e+d*i*w_so-b*i*w_so^3-c*w_so^2)]);
H_jwsoPlus2wmConj = tf([4*a 4*a*i*w_so -a*w_so^2],[-8*b (-12*b*i*w_so+4*c) (b*6*w_so
    ^2+4*i*w_so*c-2*d) (b*i*w_so^3-c*w_so^2-d*i*w_so+e)]);

%with Rload
H_jwsoMinus2wm = tf([4*a -4*a*i*w_so -a*w_so^2],[-8*b (12*b*i*w_so+4*c) (6*b*w_so
    ^2-4*c*i*w_so-2*d) (e+d*i*w_so-b*j*w_so^3-c*w_so^2)]);
H_jwsoMinus2wmConj = tf([4*a -4*a*i*w_so -a*w_so^2],[8*b (-12*b*i*w_so+4*c) (-6*b*
    w_so^2-4*c*i*w_so+2*d) (e-i*d*w_so-c*w_so^2+b*i*w_so^3)]);

%wth Rload
H_jwsoPlus3wm = tf([9*a 6*a*i*w_so -a*w_so^2],[27*b (27*b*i*w_so+9*c) (-9*b*w_so
    ^2+6*c*i*w_so+3*d) (e+d*i*w_so-c*w_so^2-b*i*w_so^3)]);
H_jwsoPlus3wmConj = tf([9*a 6*a*i*w_so -a*w_so^2],[-27*b (-27*b*i*w_so+9*c) (9*b*
    w_so^2+6*c*i*w_so-3*d) (e-i*d*w_so-c*w_so^2+b*i*w_so^3)]);

%with Rload
H_jwsoMinus3wm = tf([9*a -6*a*i*w_so -a*w_so^2],[-27*b (27*b*i*w_so+9*c) (9*b*w_so
    ^2-6*c*i*w_so-3*d) (e+d*i*w_so-c*w_so^2-b*i*w_so^3)]);
H_jwsoMinus3wmConj = tf([9*a -6*a*i*w_so -a*w_so^2],[27*b (-27*b*i*w_so+9*c) (-9*b*
    w_so^2-6*c*i*w_so+3*d) (e-d*i*w_so-c*w_so^2+b*i*w_so^3)]);

beta = tf([delta_w],[-1*i 0]);
```

```
[mag_beta phase_beta wout] = bode(beta, logspace(1,6,200));
mag_beta = squeeze(mag_beta);
phase_beta = squeeze(phase_beta);

%fundamental, sideband 0
alpha = 0;
J0_1  =besselj(alpha,mag_beta);

[mag_H_jwso phase_H_jwso] = bode(H_jwso, logspace(1,6,200));
mag_H_jwso = squeeze(mag_H_jwso);
phase_H_jwso = squeeze(phase_H_jwso);

[mag_H_jwsoConj phase_H_jwsoConj] = bode(H_jwsoConj, logspace(1,6,200));
mag_H_jwsoConj = squeeze(mag_H_jwsoConj);
phase_H_jwsoConj = squeeze(phase_H_jwsoConj);

Ao_mag = V_s1*J0_1.*mag_H_jwso;
AoConj_mag = V_s1*J0_1.*mag_H_jwsoConj;

%fundamental sideband 1
alpha1_1 = 1;
J1_1  =besselj(alpha1_1,mag_beta);

%plus
[mag_H_jwsoPluswm phase_H_jwsoPluswm] = bode(H_jwsoPluswm, logspace(1,6,200));
mag_H_jwsoPluswm = squeeze(mag_H_jwsoPluswm);
phase_H_jwsoPluswm = squeeze(phase_H_jwsoPluswm);

[mag_H_jwsoPluswmConj phase_H_jwsoPluswmConj] = bode(H_jwsoPluswmConj, logspace
    (1,6,200));
mag_H_jwsoPluswmConj = squeeze(mag_H_jwsoPluswmConj);
phase_H_jwsoPluswmConj = squeeze(phase_H_jwsoPluswmConj);

Au_mag = V_s1*J1_1.*mag_H_jwsoPluswm;
AuConj_mag = V_s1*J1_1.*mag_H_jwsoPluswmConj;

%minus
[mag_H_jwsoMinuswm phase_H_jwsoMinuswm] = bode(H_jwsoMinuswm, logspace(1,6,200));
mag_H_jwsoMinuswm = squeeze(mag_H_jwsoMinuswm);
phase_H_jwsoMinuswm = squeeze(phase_H_jwsoMinuswm);

[mag_H_jwsoMinuswmConj phase_H_jwsoMinuswmConj] = bode(H_jwsoMinuswmConj, logspace
    (1,6,200));
mag_H_jwsoMinuswmConj = squeeze(mag_H_jwsoMinuswmConj);
phase_H_jwsoMinuswmConj = squeeze(phase_H_jwsoMinuswmConj);

Al_mag = -V_s1*J1_1.*mag_H_jwsoMinuswm;
```

```
126 AlConj_mag = -V_s1*J1_1.*mag_H_jwsoMinuswmConj;
127
128 %fundamental, sideband 2
129 alpha2 = 2;
130 J2_1  =besselj(alpha2,mag_beta);
131
132 %plus2wm
133 [mag_H_jwsoPlus2wm phase_H_jwsoPlus2wm] = bode(H_jwsoPlus2wm, logspace(1,6,200));
134 mag_H_jwsoPlus2wm = squeeze(mag_H_jwsoPlus2wm);
135 phase_H_jwsoPlus2wm = squeeze(phase_H_jwsoPlus2wm);
136
137 [mag_H_jwsoPlus2wmConj phase_H_jwsoPlus2wmConj] = bode(H_jwsoPlus2wmConj, logspace
      (1,6,200));
138 mag_H_jwsoPlus2wmConj = squeeze(mag_H_jwsoPlus2wmConj);
139 phase_H_jwsoPlus2wmConj = squeeze(phase_H_jwsoPlus2wmConj);
140
141 Au2_mag = V_s1*J2_1.*mag_H_jwsoPlus2wm;
142 Au2Conj_mag = V_s1*J2_1.*mag_H_jwsoPlus2wmConj;
143
144 %minus2wm
145 [mag_H_jwsoMinus2wm phase_H_jwsoMinus2wm] = bode(H_jwsoMinus2wm, logspace(1,6,200));
146 mag_H_jwsoMinus2wm = squeeze(mag_H_jwsoMinus2wm);
147 phase_H_jwsoMinus2wm = squeeze(phase_H_jwsoMinus2wm);
148
149 [mag_H_jwsoMinus2wmConj phase_H_jwsoMinus2wmConj] = bode(H_jwsoMinus2wmConj,
      logspace(1,6,200));
150 mag_H_jwsoMinus2wmConj = squeeze(mag_H_jwsoMinus2wmConj);
151 phase_H_jwsoMinus2wmConj = squeeze(phase_H_jwsoMinus2wmConj);
152
153 Al2_mag = V_s1*J2_1.*mag_H_jwsoMinus2wm;
154 Al2Conj_mag = V_s1*J2_1.*mag_H_jwsoMinus2wmConj;
155
156 %fundamental,sideband3
157 alpha3 = 3;
158 J3_1  =besselj(alpha3,mag_beta);
159
160 %plus3wm
161 [mag_H_jwsoPlus3wm phase_H_jwsoPlus3wm] = bode(H_jwsoPlus3wm, logspace(1,6,200));
162 mag_H_jwsoPlus3wm = squeeze(mag_H_jwsoPlus3wm);
163 phase_H_jwsoPlus3wm = squeeze(phase_H_jwsoPlus3wm);
164
165 [mag_H_jwsoPlus3wmConj phase_H_jwsoPlus3wmConj] = bode(H_jwsoPlus3wmConj, logspace
      (1,6,200));
166 mag_H_jwsoPlus3wmConj = squeeze(mag_H_jwsoPlus3wmConj);
167 phase_H_jwsoPlus3wmConj = squeeze(phase_H_jwsoPlus3wmConj);
168
169 Au3_mag = V_s1*J3_1.*mag_H_jwsoPlus3wm;
```

```
Au3Conj_mag = V_s1*J3_1.*mag_H_jwsoPlus3wmConj;

%minus3wm
[mag_H_jwsoMinus3wm phase_H_jwsoMinus3wm] = bode(H_jwsoMinus3wm, logspace(1,6,200));
mag_H_jwsoMinus3wm = squeeze(mag_H_jwsoMinus3wm);
phase_H_jwsoMinus3wm = squeeze(phase_H_jwsoMinus3wm);

[mag_H_jwsoMinus3wmConj phase_H_jwsoMinus3wmConj] = bode(H_jwsoMinus3wmConj,
    logspace(1,6,200));
mag_H_jwsoMinus3wmConj = squeeze(mag_H_jwsoMinus3wmConj);
phase_H_jwsoMinus3wmConj = squeeze(phase_H_jwsoMinus3wmConj);

Al3_mag = V_s1*J3_1.*mag_H_jwsoMinus3wm;
Al3Conj_mag = V_s1*J3_1.*mag_H_jwsoMinus3wmConj;

a1 = (Ao_mag.*AlConj_mag)+(Au_mag.*AoConj_mag)+(Al_mag.*Al2Conj_mag)+(Au2_mag.*
    AuConj_mag);
a2 = (Ao_mag.*Al2Conj_mag)+(Au_mag.*AlConj_mag)+(Al_mag.*Al3Conj_mag)+(Au2_mag.*
    AoConj_mag)+(Au3_mag.*AuConj_mag);
a3 = (Ao_mag.*Al3Conj_mag)+(Au_mag.*Al2Conj_mag)+(Au2_mag.*AlConj_mag)+(Au3_mag.*
    AoConj_mag);

fundamentalOutput = (sqrt((1/3)*(a1.^2+a2.^2+a3.^2))./(Ao_mag);
fundamentalOutput = ((1/delta_w)*fundamentalOutput);

%%%%%%%third harmonic

%with Rload
H_3jwso = tf([a*(3*i*w_so)^2],[b*(3*i*w_so)^3+c*(3*i*w_so)^2+d*(3*i*w_so)+e]);
H_3jwsoConj = tf([a*(-3*i*w_so)^2],[b*(-3*i*w_so)^3+c*(-3*i*w_so)^2+d*(-3*i*w_so)+e
    ]);

%with Rload
H_3jwsoPluswm = tf([a a*6*i*w_so -a*9*w_so^2],[b (b*9*i*w_so+c) (-b*27*w_so^2+c*6*i*
    w_so+d) (e-9*c*w_so^2-27*b*i*w_so^3+3*d*i*w_so)]);
H_3jwsoPluswmConj = tf([a a*6*i*w_so -a*9*w_so^2],[-b (-b*9*i*w_so+c) (b*27*w_so^2+c
    *6*i*w_so-d) (27*b*i*w_so^3-c*9*w_so^2-3*d*i*w_so+e)]);

%with Rload
H_3jwsoMinuswm = tf([a -6*i*w_so*a -9*a*w_so^2],[-b (b*9*i*w_so+c) (b*27*w_so^2-c*6*
    i*w_so-d) (e-27*b*j*w_so^3-9*c*w_so^2+3*d*i*w_so)]);
H_3jwsoMinuswmConj = tf([a -6*i*w_so*a -9*a*w_so^2],[b (-b*9*i*w_so+c) (-b*27*w_so
    ^2-c*6*i*w_so+d) (e-c*9*w_so^2+27*b*i*w_so^3-3*d*i*w_so)]);

%with Rload
 H_3jwsoPlus2wm = tf([4*a 12*a*i*w_so -9*a*w_so^2],[8*b (36*b*i*w_so+4*c) (-b*54*
     w_so^2+12*i*c*w_so+2*d) (e+3*d*i*w_so-27*b*i*w_so^3-9*c*w_so^2)]);
```

```
H_3jwsoPlus2wmConj = tf([4*a 12*a*i*w_so -9*a*w_so^2],[-8*b (-36*b*i*w_so+4*c) (b*54*w_so^2+12*i*w_so*c-2*d) (27*b*i*w_so^3-9*c*w_so^2-3*d*i*w_so+e)]);

%with Rload
H_3jwsoMinus2wm = tf([4*a -12*a*i*w_so -9*a*w_so^2],[-8*b (36*b*i*w_so+4*c) (54*b*w_so^2-12*c*i*w_so-2*d) (e+3*d*i*w_so-27*b*j*w_so^3-9*c*w_so^2)]);
H_3jwsoMinus2wmConj = tf([4*a -12*a*i*w_so -9*a*w_so^2],[8*b (-36*b*i*w_so+4*c) (-54*b*w_so^2-12*c*i*w_so+2*d) (e-3*i*d*w_so-9*c*w_so^2+27*b*i*w_so^3)]);

%wth Rload
 H_3jwsoPlus3wm = tf([9*a 18*a*i*w_so -9*a*w_so^2],[27*b (81*b*i*w_so+9*c) (-81*b*w_so^2+18*c*i*w_so+3*d) (e+3*d*i*w_so-9*c*w_so^2-27*b*i*w_so^3)]);
H_3jwsoPlus3wmConj = tf([9*a 18*a*i*w_so -9*a*w_so^2],[-27*b (-81*b*i*w_so+9*c) (81*b*w_so^2+18*c*i*w_so-3*d) (e-3*i*d*w_so-9*c*w_so^2+27*b*i*w_so^3)]);

%with Rload
H_3jwsoMinus3wm = tf([9*a -18*a*i*w_so -9*a*w_so^2],[-27*b (81*b*i*w_so+9*c) (81*b*w_so^2-18*c*i*w_so-3*d) (e+3*d*i*w_so-9*c*w_so^2-27*b*i*w_so^3)]);
 H_3jwsoMinus3wmConj = tf([9*a -18*a*i*w_so -9*a*w_so^2],[27*b (-81*b*i*w_so+9*c) (-81*b*w_so^2-18*c*i*w_so+3*d) (e-3*d*i*w_so-9*c*w_so^2+27*b*i*w_so^3)]);

%third Harmonic, sideband 0
alpha0_3 = 0;
J0_3 = besselj(alpha0_3,mag_beta);

[mag_H_3jwso phase_H_3jwso] = bode(H_3jwso, logspace(1,6,200));
mag_H_3jwso = squeeze(mag_H_3jwso);
phase_H_3jwso = squeeze(phase_H_3jwso);

[mag_H_3jwsoConj phase_H_3jwsoConj] = bode(H_3jwsoConj, logspace(1,6,200));
mag_H_3jwsoConj = squeeze(mag_H_3jwsoConj);
phase_H_3jwsoConj = squeeze(phase_H_3jwsoConj);

Bo_mag = V_s3*J0_3.*mag_H_3jwso;
BoConj_mag = V_s3*J0_3.*mag_H_3jwsoConj;

%thirdHarmonic, sideband1
alpha1_3 = 1;
J1_3  =besselj(alpha1_3,mag_beta);

%3plus
[mag_H_3jwsoPluswm phase_H_3jwsoPluswm] = bode(H_3jwsoPluswm, logspace(1,6,200));
mag_H_3jwsoPluswm = squeeze(mag_H_3jwsoPluswm);
phase_H_3jwsoPluswm = squeeze(phase_H_3jwsoPluswm);

[mag_H_3jwsoPluswmConj phase_H_3jwsoPluswmConj] = bode(H_3jwsoPluswmConj, logspace(1,6,200));
```

```
246 mag_H_3jwsoPluswmConj = squeeze(mag_H_3jwsoPluswmConj);
247 phase_H_3jwsoPluswmConj = squeeze(phase_H_3jwsoPluswmConj);
248
249 Bu_mag = V_s3*J1_3.*mag_H_3jwsoPluswm;
250 BuConj_mag = V_s3*J1_3.*mag_H_3jwsoPluswmConj;
251
252 %3minus
253 [mag_H_3jwsoMinuswm phase_H_3jwsoMinuswm] = bode(H_3jwsoMinuswm, logspace(1,6,200));
254 mag_H_3jwsoMinuswm = squeeze(mag_H_3jwsoMinuswm);
255 phase_H_3jwsoMinuswm = squeeze(phase_H_3jwsoMinuswm);
256
257 [mag_H_3jwsoMinuswmConj phase_H_3jwsoMinuswmConj] = bode(H_3jwsoMinuswmConj,
        logspace(1,6,200));
258 mag_H_3jwsoMinuswmConj = squeeze(mag_H_3jwsoMinuswmConj);
259 phase_H_3jwsoMinuswmConj = squeeze(phase_H_3jwsoMinuswmConj);
260
261 Bl_mag = -V_s3*J1_3.*mag_H_3jwsoMinuswm;
262 BlConj_mag = -V_s3*J1_3.*mag_H_3jwsoMinuswmConj;
263
264 %thirdHarmonic, sideband2
265 alpha2_3 = 2;
266 J2_3  =besselj(alpha2_3,mag_beta);
267
268 %3plus2
269 [mag_H_3jwsoPlus2wm phase_H_3jwsoPlus2wm] = bode(H_3jwsoPlus2wm, logspace(1,6,200));
270 mag_H_3jwsoPlus2wm = squeeze(mag_H_3jwsoPlus2wm);
271 phase_H_3jwsoPlus2wm = squeeze(phase_H_3jwsoPlus2wm);
272
273 [mag_H_3jwsoPlus2wmConj phase_H_3jwsoPlus2wmConj] = bode(H_3jwsoPlus2wmConj,
        logspace(1,6,200));
274 mag_H_3jwsoPlus2wmConj = squeeze(mag_H_3jwsoPlus2wmConj);
275 phase_H_3jwsoPlus2wmConj = squeeze(phase_H_3jwsoPlus2wmConj);
276
277 Bu2_mag = V_s3*J2_3.*mag_H_3jwsoPlus2wm;
278 Bu2Conj_mag = V_s3*J2_3.*mag_H_3jwsoPlus2wmConj;
279
280 %3minus2
281 [mag_H_3jwsoMinus2wm phase_H_3jwsoMinus2wm] = bode(H_3jwsoMinus2wm, logspace
        (1,6,200));
282 mag_H_3jwsoMinus2wm = squeeze(mag_H_3jwsoMinus2wm);
283 phase_H_3jwsoMinus2wm = squeeze(phase_H_3jwsoMinus2wm);
284
285 [mag_H_3jwsoMinus2wmConj phase_H_3jwsoMinus2wmConj] = bode(H_3jwsoMinus2wmConj,
        logspace(1,6,200));
286 mag_H_3jwsoMinus2wmConj = squeeze(mag_H_3jwsoMinus2wmConj);
287 phase_H_3jwsoMinus2wmConj = squeeze(phase_H_3jwsoMinus2wmConj);
288
```

```
289 Bl2_mag = -V_s3*J2_3.*mag_H_3jwsoMinus2wm;
290 Bl2Conj_mag = -V_s3*J2_3.*mag_H_3jwsoMinus2wmConj;
291
292 %thridHarmonic, sideband3
293 alpha3_3 = 3;
294 J3_3  =besselj(alpha3_3,mag_beta);
295
296 %3plus3
297 [mag_H_3jwsoPlus3wm phase_H_3jwsoPlus3wm] = bode(H_3jwsoPlus3wm, logspace(1,6,200));
298 mag_H_3jwsoPlus3wm = squeeze(mag_H_3jwsoPlus3wm);
299 phase_H_3jwsoPlus3wm = squeeze(phase_H_3jwsoPlus3wm);
300
301 [mag_H_3jwsoPlus3wmConj phase_H_3jwsoPlus3wmConj] = bode(H_3jwsoPlus3wmConj,
        logspace(1,6,200));
302 mag_H_3jwsoPlus3wmConj = squeeze(mag_H_3jwsoPlus3wmConj);
303 phase_H_3jwsoPlus3wmConj = squeeze(phase_H_3jwsoPlus3wmConj);
304
305 Bu3_mag = V_s3*J3_3.*mag_H_3jwsoPlus3wm;
306 Bu3Conj_mag = V_s3*J3_3.*mag_H_3jwsoPlus3wmConj;
307
308 %3minus3
309 [mag_H_3jwsoMinus3wm phase_H_3jwsoMinus3wm] = bode(H_3jwsoMinus3wm, logspace
        (1,6,200));
310 mag_H_3jwsoMinus3wm = squeeze(mag_H_3jwsoMinus3wm);
311 phase_H_3jwsoMinus3wm = squeeze(phase_H_3jwsoMinus3wm);
312
313 [mag_H_3jwsoMinus3wmConj phase_H_3jwsoMinus3wmConj] = bode(H_3jwsoMinus3wmConj,
        logspace(1,6,200));
314 mag_H_3jwsoMinus3wmConj = squeeze(mag_H_3jwsoMinus3wmConj);
315 phase_H_3jwsoMinus3wmConj = squeeze(phase_H_3jwsoMinus3wmConj);
316
317 Bl3_mag = -V_s3*J3_3.*mag_H_3jwsoMinus3wm;
318 Bl3Conj_mag = -V_s3*J3_3.*mag_H_3jwsoMinus3wmConj;
319
320 b1 = (Bo_mag.*BlConj_mag)+(Bu_mag.*BoConj_mag)+(Bl_mag.*Bl2Conj_mag)+(Bu2_mag.*
        BuConj_mag);
321 b2 = (Bo_mag.*Bl2Conj_mag)+(Bu_mag.*BlConj_mag)+(Bl_mag.*Bl3Conj_mag)+(Bu2_mag.*
        BoConj_mag)+(Bu3_mag.*BuConj_mag);
322 b3 = (Bo_mag.*Bl3Conj_mag)+(Bu_mag.*Bl2Conj_mag)+(Bu2_mag.*BlConj_mag)+(Bu3_mag.*
        BoConj_mag);
323
324 thirdHarmonicOutput = (sqrt((1/3)*(b1.^2+b2.^2+b3.^2))./(Bo_mag);
325 thirdHarmonicOutput = ((1/delta_w)*thirdHarmonicOutput);
326
327 %%%%%%%%fifth harmonic
328
329 %with Rload
```

```
330 H_5jwso = tf([a*(5*i*w_so)^2],[b*(5*i*w_so)^3+c*(5*i*w_so)^2+d*(5*i*w_so)+e]);
331 H_5jwsoConj = tf([a*(-5*i*w_so)^2],[b*(-5*i*w_so)^3+c*(-5*i*w_so)^2+d*(-5*i*w_so)+e
    ]);
332
333 %with Rload
334 H_5jwsoPluswm = tf([a a*10*1i*w_so -a*25*w_so^2],[b (b*15*i*w_so+c) (-b*75*w_so^2+c
    *10*i*w_so+d) (e-25*c*w_so^2-125*b*i*w_so^3+5*d*i*w_so)]);
335 H_5jwsoPluswmConj = tf([a a*10*i*w_so -a*25*w_so^2],[-b (-b*15*i*w_so+c) (b*75*w_so
    ^2+c*10*i*w_so-d) (125*b*i*w_so^3-c*25*w_so^2-5*d*i*w_so+e)]);
336
337 %with Rload
338 H_5jwsoMinuswm = tf([a -10*i*w_so*a -25*a*w_so^2],[-b (b*15*i*w_so+c) (b*75*w_so^2-c
    *10*i*w_so-d) (e-125*b*j*w_so^3-25*c*w_so^2+5*d*i*w_so)]);
339 H_5jwsoMinuswmConj = tf([a -10*i*w_so*a -25*a*w_so^2],[b (-b*15*i*w_so+c) (-b*75*
    w_so^2-c*10*i*w_so+d) (e-c*25*w_so^2+125*b*i*w_so^3-5*d*i*w_so)]);
340
341 %with Rload
342 H_5jwsoPlus2wm = tf([4*a 20*a*i*w_so -25*a*w_so^2],[8*b (60*b*i*w_so+4*c) (-b*150*
    w_so^2+20*i*c*w_so+2*d) (e+5*d*i*w_so-125*b*i*w_so^3-25*c*w_so^2)]);
343 H_5jwsoPlus2wmConj = tf([4*a 20*a*i*w_so -25*a*w_so^2],[-8*b (-60*b*i*w_so+4*c) (b
    *150*w_so^2+20*i*w_so*c-2*d) (125*b*i*w_so^3-25*c*w_so^2-5*d*i*w_so+e)]);
344
345 %with Rload
346 H_5jwsoMinus2wm = tf([4*a -20*a*i*w_so -25*a*w_so^2],[-8*b (60*b*i*w_so+4*c) (150*b*
    w_so^2-20*c*i*w_so-2*d) (e+5*d*i*w_so-125*b*j*w_so^3-25*c*w_so^2)]);
347 H_5jwsoMinus2wmConj = tf([4*a -20*a*i*w_so -25*a*w_so^2],[8*b (-60*b*i*w_so+4*c)
    (-150*b*w_so^2-20*c*i*w_so+2*d) (e-5*i*d*w_so-25*c*w_so^2+125*b*i*w_so^3)]);
348
349 %wth Rload
350 H_5jwsoPlus3wm = tf([9*a 30*a*i*w_so -25*a*w_so^2],[27*b (135*b*i*w_so+9*c) (-225*b*
    w_so^2+30*c*i*w_so+3*d) (e+5*d*i*w_so-25*c*w_so^2-125*b*i*w_so^3)]);
351 H_5jwsoPlus3wmConj = tf([9*a 30*a*i*w_so -25*a*w_so^2],[-27*b (-135*b*i*w_so+9*c)
    (225*b*w_so^2+30*c*i*w_so-3*d) (e-5*i*d*w_so-25*c*w_so^2+125*b*i*w_so^3)]);
352
353 %with Rload
354 H_5jwsoMinus3wm = tf([9*a -30*a*i*w_so -25*a*w_so^2],[-27*b (135*b*i*w_so+9*c) (225*
    b*w_so^2-30*c*i*w_so-3*d) (e+5*d*i*w_so-25*c*w_so^2-125*b*i*w_so^3)]);
355 H_5jwsoMinus3wmConj = tf([9*a -30*a*i*w_so -25*a*w_so^2],[27*b (-135*b*i*w_so+9*c)
    (-225*b*w_so^2-30*c*i*w_so+3*d) (e-5*d*i*w_so-25*c*w_so^2+125*b*i*w_so^3)]);
356
357 %fifthHarmonic, sideband0
358 alpha0_5 = 0;
359 J0_5 = besselj(alpha0_5,mag_beta);
360
361 [mag_H_5jwso phase_H_5jwso] = bode(H_5jwso, logspace(1,6,200));
362 mag_H_5jwso = squeeze(mag_H_5jwso);
363 phase_H_5jwso = squeeze(phase_H_5jwso);
```

```
364
365 [mag_H_5jwsoConj phase_H_5jwsoConj] = bode(H_5jwsoConj, logspace(1,6,200));
366 mag_H_5jwsoConj = squeeze(mag_H_5jwsoConj);
367 phase_H_5jwsoConj = squeeze(phase_H_5jwsoConj);
368
369 Co_mag = V_s5*J0_5.*mag_H_5jwso;
370 CoConj_mag = V_s5*J0_5.*mag_H_5jwsoConj;
371
372 %fifthHarmonic, sideband1
373 alpha1_5 = 1;
374 J1_5  =besselj(alpha1_5,mag_beta);
375
376 %5plus
377 [mag_H_5jwsoPluswm phase_H_5jwsoPluswm] = bode(H_5jwsoPluswm, logspace(1,6,200));
378 mag_H_5jwsoPluswm = squeeze(mag_H_5jwsoPluswm);
379 phase_H_5jwsoPluswm = squeeze(phase_H_5jwsoPluswm);
380
381 [mag_H_5jwsoPluswmConj phase_H_5jwsoPluswmConj] = bode(H_5jwsoPluswmConj, logspace
      (1,6,200));
382 mag_H_5jwsoPluswmConj = squeeze(mag_H_5jwsoPluswmConj);
383 phase_H_5jwsoPluswmConj = squeeze(phase_H_5jwsoPluswmConj);
384
385 Cu_mag = V_s5*J1_5.*mag_H_5jwsoPluswm;
386 CuConj_mag = V_s5*J1_5.*mag_H_5jwsoPluswmConj;
387
388 %5minus
389 [mag_H_5jwsoMinuswm phase_H_5jwsoMinuswm] = bode(H_5jwsoMinuswm, logspace(1,6,200));
390 mag_H_5jwsoMinuswm = squeeze(mag_H_5jwsoMinuswm);
391 phase_H_5jwsoMinuswm = squeeze(phase_H_5jwsoMinuswm);
392
393 [mag_H_5jwsoMinuswmConj phase_H_5jwsoMinuswmConj] = bode(H_5jwsoMinuswmConj,
      logspace(1,6,200));
394 mag_H_5jwsoMinuswmConj = squeeze(mag_H_5jwsoMinuswmConj);
395 phase_H_5jwsoMinuswmConj = squeeze(phase_H_5jwsoMinuswmConj);
396
397 Cl_mag = -V_s5*J1_5.*mag_H_5jwsoMinuswm;
398 ClConj_mag = -V_s5*J1_5.*mag_H_5jwsoMinuswmConj;
399
400 %fifthHarmonic, sideband2
401 alpha2_5 = 2;
402 J2_5  =besselj(alpha2_5,mag_beta);
403
404 %5plus2
405 [mag_H_5jwsoPlus2wm phase_H_5jwsoPlus2wm] = bode(H_5jwsoPlus2wm, logspace(1,6,200));
406 mag_H_5jwsoPlus2wm = squeeze(mag_H_5jwsoPlus2wm);
407 phase_H_5jwsoPlus2wm = squeeze(phase_H_5jwsoPlus2wm);
408
```

```
409 [mag_H_5jwsoPlus2wmConj phase_H_5jwsoPlus2wmConj] = bode(H_5jwsoPlus2wmConj,
        logspace(1,6,200));
410 mag_H_5jwsoPlus2wmConj = squeeze(mag_H_5jwsoPlus2wmConj);
411 phase_H_5jwsoPlus2wmConj = squeeze(phase_H_5jwsoPlus2wmConj);
412
413 Cu2_mag = V_s5*J2_5.*mag_H_5jwsoPlus2wm;
414 Cu2Conj_mag = V_s5*J2_5.*mag_H_5jwsoPlus2wmConj;
415
416 %5minus2
417 [mag_H_5jwsoMinus2wm phase_H_5jwsoMinus2wm] = bode(H_5jwsoMinus2wm, logspace
        (1,6,200));
418 mag_H_5jwsoMinus2wm = squeeze(mag_H_5jwsoMinus2wm);
419 phase_H_5jwsoMinus2wm = squeeze(phase_H_5jwsoMinus2wm);
420
421 [mag_H_5jwsoMinus2wmConj phase_H_5jwsoMinus2wmConj] = bode(H_5jwsoMinus2wmConj,
        logspace(1,6,200));
422 mag_H_5jwsoMinus2wmConj = squeeze(mag_H_5jwsoMinus2wmConj);
423 phase_H_5jwsoMinus2wmConj = squeeze(phase_H_5jwsoMinus2wmConj);
424
425 Cl2_mag = -V_s5*J2_5.*mag_H_5jwsoMinus2wm;
426 Cl2Conj_mag = -V_s5*J2_5.*mag_H_5jwsoMinus2wmConj;
427
428 %fifthHarmonic, sideband3
429 alpha3_5 = 3;
430 J3_5  =besselj(alpha3_5,mag_beta);
431
432 %5plus3
433 [mag_H_5jwsoPlus3wm phase_H_5jwsoPlus3wm] = bode(H_5jwsoPlus3wm, logspace(1,6,200));
434 mag_H_5jwsoPlus3wm = squeeze(mag_H_5jwsoPlus3wm);
435 phase_H_5jwsoPlus3wm = squeeze(phase_H_5jwsoPlus3wm);
436
437 [mag_H_5jwsoPlus3wmConj phase_H_5jwsoPlus3wmConj] = bode(H_5jwsoPlus3wmConj,
        logspace(1,6,200));
438 mag_H_5jwsoPlus3wmConj = squeeze(mag_H_5jwsoPlus3wmConj);
439 phase_H_5jwsoPlus3wmConj = squeeze(phase_H_5jwsoPlus3wmConj);
440
441 Cu3_mag = V_s5*J3_5.*mag_H_5jwsoPlus3wm;
442 Cu3Conj_mag = V_s5*J3_5.*mag_H_5jwsoPlus3wmConj;
443
444 %5minus3
445 [mag_H_5jwsoMinus3wm phase_H_5jwsoMinus3wm] = bode(H_5jwsoMinus3wm, logspace
        (1,6,200));
446 mag_H_5jwsoMinus3wm = squeeze(mag_H_5jwsoMinus3wm);
447 phase_H_5jwsoMinus3wm = squeeze(phase_H_5jwsoMinus3wm);
448
449 [mag_H_5jwsoMinus3wmConj phase_H_5jwsoMinus3wmConj] = bode(H_5jwsoMinus3wmConj,
        logspace(1,6,200));
```

```
mag_H_5jwsoMinus3wmConj = squeeze(mag_H_5jwsoMinus3wmConj);
phase_H_5jwsoMinus3wmConj = squeeze(phase_H_5jwsoMinus3wmConj);

Cl3_mag = -V_s5*J3_5.*mag_H_5jwsoMinus3wm;
Cl3Conj_mag = -V_s5*J3_5.*mag_H_5jwsoMinus3wmConj;

c1 = (Co_mag.*ClConj_mag)+(Cu_mag.*CoConj_mag)+(Cl_mag.*Cl2Conj_mag)+(Cu2_mag.*
    CuConj_mag);
c2 = (Co_mag.*Cl2Conj_mag)+(Cu_mag.*ClConj_mag)+(Cl_mag.*Cl3Conj_mag)+(Cu2_mag.*
    CoConj_mag)+(Cu3_mag.*CuConj_mag);
c3 = (Co_mag.*Cl3Conj_mag)+(Cu_mag.*Cl2Conj_mag)+(Cu2_mag.*ClConj_mag)+(Cu3_mag.*
    CoConj_mag);

fifthHarmonicOutput = (sqrt((1/3)*(c1.^2+c2.^2+c3.^2))./(Co_mag);
fifthHarmonicOutput = ((1/delta_w)*fifthHarmonicOutput);


 finalOutput = (fundamentalOutput+thirdHarmonicOutput+fifthHarmonicOutput)*2*pi*
     Tratio.*(mag_ESRzero).^1.*(mag_RHPzero).^2.*(mag_ZOHpole).^3;

% plots
 plota =  semilogx(wout/(2*pi),20*log10(fundamentalOutput),'b');hold on,
 plotb =  semilogx(wout/(2*pi),20*log10(thirdHarmonicOutput),'g');hold on,
 plotc = semilogx(wout/(2*pi),20*log10(fifthHarmonicOutput),'r');hold on,
 hold on,   plotd= semilogx(wout/(2*pi),20*log10(finalOutput),'k')
 hold on, bode([0],[1],[2*pi*600,2*pi*1e4])
 hold on
legend([plota,plotb,plotc,plotd])
```

A design methodology for LLC resonant converters based on inspection of resonant tank currents.

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***Abstract* -- This paper presents a simple and accurate design methodology for LLC resonant converters, based on a semi-empirical approach to model steady-state operation in the "below-resonance" region. This model is framed in a design strategy that aims to design a converter capable of operating with soft-switching in the specified input voltage range with a load ranging from zero up to the maximum specified level.**

***Index Terms* – Large-signal model, LLC resonant converter, soft-switching, zero-current switching, zero-voltage switching.**

I. INTRODUCTION

Although resonant conversion has been with us for many years, the use of this technique in offline powered equipment has for a long time been confined to niche applications. Quite recently, emerging applications, such as flat panel TVs, and the introduction of new regulations concerning an efficient use of energy, are pushing power designers to find increasingly efficient ac-dc conversion systems. This has revamped the interest in resonant conversion, especially in the so-called LLC resonant converter that seems to be one of the topologies with the most favorable benefit/drawback ratio.

Many design methodologies are available today for this converter. Those based on exact models [1-5] are accurate, but not simple to handle without sophisticated calculation tools. Additionally, it is not easy to frame design constraints and objectives into the models.

The methodologies based on first harmonic approximation (FHA) analysis [6-12] are much simpler to handle but lack accuracy, especially in the so-called below-resonance region, as shown in [13]. This is a problem because the closed-loop operating frequency and the tank peak current in that region need to be quite accurately predicted to design the current limitation circuitry properly.

In [10], it has been shown how to incorporate the design constraints related to achieving soft-switching under all operating conditions, as well as zero-load operation ability, in an organic design procedure based on the FHA approach.

In this paper, a design procedure based on the same strategy used in [10] is proposed, but using different mathematical tools. The core of this procedure is a model of the converter operating in the below-resonance region, derived from inspection of the tank current waveforms under a particular operating mode that is the design target.

The paper starts with a brief review of the LLC resonant converter and its main features, recalls its most significant operating modes, and provides the general guidelines of the design strategy. The conditions for zero-voltage-switching (ZVS) to occur and no-load operation to be ensured are reviewed.

Then the current waveforms for the below-resonance operating region are considered, suitable approximations based on simple geometrical considerations are made, and the analysis is carried out, leading to relationships that can be used to calculate all the main electrical quantities.

Finally, the design procedure is detailed and a design example given. The experimental results are compared to the theoretical predictions to validate the approach.

II. LLC RESONANT CONVERTER MAIN FEATURES

The circuit schematic of an LLC resonant converter in its half-bridge implementation is shown in Figure 1. In this paper we refer to this case in particular but, with obvious adaptations, the results that are provided are entirely applicable to the full-bridge implementation too.

The half-bridge driver switches the two MOSFETs Q1 and Q2 on and off 180º out-of-phase at the frequency *fs*. The on-time of each MOSFET is exactly the same and is slightly shorter than 50% of the switching period $Ts = 1/fs$. In fact, a small dead-time *Td* is inserted between the turn-off of either MOSFET and the turn-on of the other one. This is essential for the operation of the converter: it ensures that Q1 and Q2 do not cross-conduct and allows soft-switching for both of them, that is, zero-voltage switching at turn-on (ZVS). This concept is clarified in section V.

The resonant tank includes three reactive elements (*Cr*, *Ls* and *Lp*) and thus features two resonance frequencies.

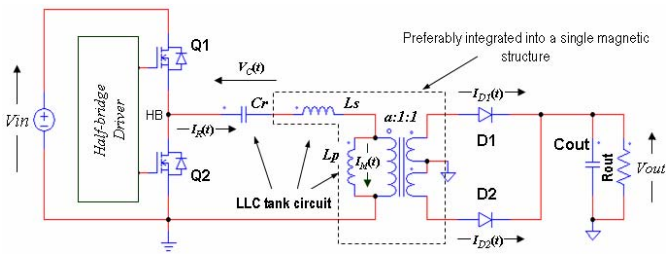

Figure 1. LLC resonant half-bridge converter

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One is related to secondary winding conduction: only *Ls* is active, while *Lp* disappears because there is a constant voltage across it reflected back from the secondary side; its value is:

$$f_{R1} = \frac{1}{2\pi\sqrt{Ls\,Cr}} \quad . \tag{1}$$

The other resonant frequency corresponds to the condition of the secondary winding(s) being open. The tank circuit turns from LLC to LC because *Ls* and *Lp* are effectively in series:

$$f_{R2} = \frac{1}{2\pi\sqrt{(Ls+Lp)Cr}} . \tag{2}$$

The following, of course, is true: $f_{R1} > f_{R2}$. The separation between f_{R1} and f_{R2} depends on the *Lp* to *Ls* ratio: the larger it is, the further the two frequencies are and vice versa.

Power flow is controlled by the operating frequency *fs*; normally, a reduced power demand from the load produces a frequency rise, while an increased power demand causes a frequency decrease.

When working at a frequency $fs = f_{R1}$, the converter is said to operate at resonance; naturally, therefore, operation at frequencies $fs > f_{R1}$ is termed above-resonance and in the frequency region $fs < f_{R1}$ below-resonance.

This last region is practically limited to a relatively narrow range $f_{min} < fs < f_{R1}$, with $f_{min} > f_{R2}$, to prevent the converter from losing soft-switching of the half-bridge leg. In fact, this is what would happen if *fs* got too close to f_{R2}. Losing ZVS would cause such adverse effects that the converter's safety would be seriously compromised.

Neglecting power losses, whether the converter operates at, above or below resonance depends only on the input voltage (*Vin*), the output voltage (*Vout*) and the transformer turn ratio *a*. For the half-bridge, we have specifically:

$$\begin{aligned} Vin &< 2\,a\,(Vout + V_F) \quad \rightarrow \text{Below resonance} \\ Vin &= 2\,a\,(Vout + V_F) \quad \rightarrow \text{At resonance} \\ Vin &> 2\,a\,(Vout + V_F) \quad \rightarrow \text{Above resonance} \end{aligned} \tag{3}$$

where V_F is the estimated voltage drop across each of the secondary rectifiers.

From the design point of view, since *Vin* and *Vout* are specified, it is the selection of the turn ratio *a* that determines whether the converter operates at, below or above resonance.

In these three fundamental operating regions, essentially related to the input voltage, different operating modes can be seen [3], depending on the load. In this context, we focus on the operating modes occurring at full load in the below-resonance operating region, that is, at the lower end of *Vin*.

The waveforms of a typical below-resonance mode are shown in Figure 2. This mode, which is unique to the below-resonance region, is a discontinuous conduction mode (DCM), because in the time interval (*Tz*, *Ts*/2), no current flows on the secondary side.

Here the multi-resonant nature of the LLC converter appears: whereas in the interval (0, *Tz*), where *Cr* resonates with *Ls* only, the tank current is a sinusoid with a frequency f_{R1}, in the interval (*Tz*, *Ts*/2), both secondary rectifiers are open

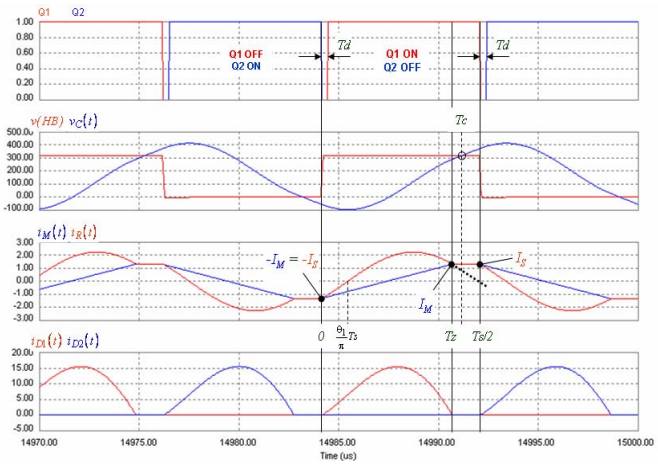

Figure 2. Typical waveforms of the LLC resonant half-bridge operated below resonance.

and *Cr* rings with (*Ls* + *Lp*), so that the second resonance frequency f_{R2} appears.

This is one of the fundamental advantages of the LLC resonant converter. In fact, it extends the ZVS range for both MOSFETs: at $t = Tz$, the tank circuit current $i_R(t)$ is decaying and would approach zero and reverse before $t = Ts/2$ if it followed the same sinusoid at frequency $f = f_{R1}$ (see the extrapolated black dotted line). This lower frequency sinusoid prevents the tank current from decreasing and then the switched current $i_R(Ts/2)$ from reversing before $t = Ts/2$, which is a necessary condition to achieve ZVS.

III. General Design Guidelines

Assuming the LLC resonant half-bridge is powered by a PFC pre-regulator providing a regulated *Vin*, changes in *Vin* are due to either the dynamic response of the PFC stage or to abnormal line conditions, such as missing line cycles.

In [10] it is pointed out that a good design strategy is:

1. make the converter work at resonance under nominal input voltage Vin_{nom} (e.g. ≈400 V) to take advantage of operation at the load-independent point (see [6]);

2. use the above-resonance region to handle the PFC's output overvoltage conditions, e.g. resulting from an abrupt load decrease;

3. use the below-resonance region to both handle the PFC's output undervoltage conditions (e.g. due to an abrupt increase of the load) and provide the converter with the specified hold-up capability while the line voltage is abnormally low and the resonant converter is delivering the maximum power energized only by the PFC's output bulk capacitor.

Point 1) of the strategy allows an easy determination of the transformer's turn-ratio *a*; from (3) we have:

$$a = \frac{Vin_{nom}}{2\,(Vout + V_F)}, \tag{4}$$

As to point 2) of the strategy, the worst-case scenario occurs when the load of the LLC resonant converter drops to zero and the output overvoltage protection (OVP) of the PFC is tripped. The converter must then be able to regulate with no load at the

maximum input voltage (Vin_{max} = PFC's OVP level) at a reasonably specified operating frequency fs_{max} (that is, not too high). This is expanded in the next section.

Concerning point 3), when the input voltage is at the minimum specified value (Vin_{min}) the input current reaches the maximum peak and rms values and the switching frequency its minimum value (fs_{min}); the overcurrent protection circuits have to be designed so that the converter is still able to regulate the output voltage under these conditions, but should trip in case of further input current increase. For this, the tank peak current must be known with a certain degree of accuracy; if the switching frequency is bottom-limited as an additional overcurrent countermeasure, also fs_{min} should be quite accurately predicted. Unfortunately these operating conditions are also those where the FHA-based models are less accurate. Hence the need for a different model, as simple as the FHA-based ones, but more accurate.

IV. No-load operation capability

Typically, the converter is required to regulate the output voltage even under no-load conditions.

For any input and output voltage, a frequency region exists where the LLC resonant converter delivers zero power to the output. This is called cutoff region and its lowest frequency is called cutoff frequency. In [3] it is shown that the cutoff frequency is:

$$f_{co} = \frac{\pi}{2}\sqrt{\frac{1}{1+\lambda}}\frac{1}{\cos^{-1}\left[\frac{\lambda}{2aM(1+\lambda)}\right]} f_{R1}, \qquad (5)$$

with the following parameter definitions:

$\lambda = \frac{Lp}{Ls}$: parallel-to-series inductance ratio;

$M = \frac{Vout + V_F}{Vin}$: dc voltage conversion ratio;

and where a is the transformer turn ratio.

Mathematically, a necessary condition for the cutoff region to exist is that the argument of the inverse cosine function be less than unity, that is:

$$M \geq \frac{1}{2a}\frac{\lambda}{1+\lambda}, \qquad (6)$$

which is the same result found in [6], [10].

Physically, cutoff occurs when the voltage developed across Lp and reflected to the secondary side is not large enough to forward bias the secondary rectifiers over an entire switching cycle. This is essentially what (6) states.

It is intuitive that in a closed-loop regulated converter, the switching frequency under no-load conditions is equal to the cutoff frequency. Making sure that the converter is able to regulate the output voltage at no-load and maximum input voltage can therefore be translated into solving (5) for λ with an assigned value for $f_{co} = f_{max}$ and with:

$$M = M_{min} = \frac{Vout + V_F}{Vin_{max}}. \qquad (7)$$

Equation (5) can be re-written as:

$$\frac{\lambda}{2aM_{min}(1+\lambda)} = \cos\left(\frac{\pi}{2}\sqrt{\frac{1}{1+\lambda}}\frac{f_{R1}}{f_{co}}\right); \qquad (8)$$

Expanding the cosine function in MacLaurin series to the second order, the resulting equation can be solved for λ:

$$\lambda = \frac{1}{4}\frac{aM_{min}}{1-2aM_{min}}\left[8-\left(\pi\frac{f_{R1}}{f_{max}}\right)^2\right]. \qquad (9)$$

Figure 3 shows the most important waveforms during no-load operation. The currents $i_R(t)$ and $i_M(t)$ are coincident and composed of pieces of sinusoids of frequency f_{R2}. However, since it is normally $f_{co} >> f_{R2}$, they look triangular.

It is of practical interest to find their common peak value I_{Mco} at $t = Ts/2$. Again from the results provided in [3], and after adapting the formula to the notation used in this text, it is possible to find:

$$I_{Mco} = \frac{Vin_{max}}{4\pi f_{R1} Lp}\sqrt{4(1+\lambda)a^2M_{min}^2 - \frac{\lambda^2}{1+\lambda}}. \qquad (10)$$

V. ZVS operation capability

For the MOSFETs Q1 and Q2 to operate with ZVS, it is necessary and sufficient that:

1. The switched current I_S, that is, the tank current $i_R(t)$ when either MOSFET is switched off, and the fundamental component of the square wave voltage applied to the tank circuit have the same sign. In other words, the tank current has to lag behind the input voltage; this is often referred to as inductive-mode operation. Obviously, if the tank current leads the applied voltage, we have capacitive-mode operation, which prevents ZVS.

2. The tank current lags behind the applied voltage by an angle large enough so as not to change sign during the dead-times Td: in this way, after the rail-to-rail swing, the voltage of the half-bridge leg midpoint (the node HB in Figure 1) has no oscillations before the other MOSFET is switched on.

3. The (absolute) value of I_S is larger than a minimum value I_{Smin} such that the node HB swings rail-to-rail within Td.

Note once again that operating in inductive-mode is only one necessary condition. This is due to the existence of a parasitic capacitance associated to the node HB, which needs energy to be completely charged or depleted during Td.

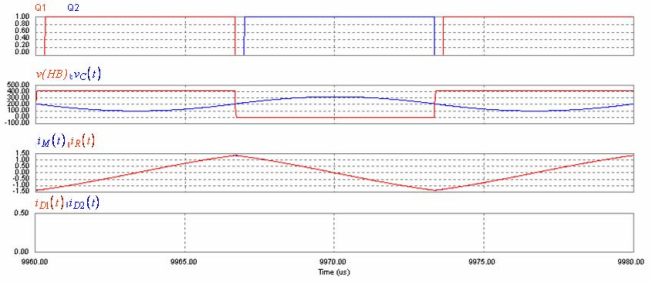

Figure 3. Typical waveforms of the LLC resonant half-bridge operated with no load.

To accomplish this task, the energy is obviously taken from that of the resonant tank, which therefore must have an adequate level. This is the physical meaning of points 2 and 3.

It is useful to consider the circuit in Figure 4, where the drain-to-source capacitances $Coss_1$, $Coss_2$ of Q1 and Q2, as well as other contributors (the capacitance formed between the case of the MOSFETs and the heat sink, the transformer's intrawinding capacitance, etc.) combined together into C_{Stray}, are shown. Note that $Coss_1$ is effectively connected in parallel to $Coss_2$ and C_{Stray}; they can thus all be conveniently combined into a single capacitor C_{HB} connected from HB to ground. Since the same MOSFET is typically used for Q1 and Q2, $Coss_1 = Coss_2 = Coss$; thereby:

$$C_{HB} = 2\,Coss + C_{Stray}\,. \tag{11}$$

Note also that $Coss_1$ and $Coss_2$ are non-linear capacitors, that is, their value is a function of the drain-to-source voltage; their time-related equivalent value should be considered [14].

If the necessary and sufficient conditions for ZVS to occur are met, normally the tank current $i_R(t)$ does not change much during Td, and changes even less during the time $T_T \le Td$ while the node HB swings.

With good approximation, it is possible to assume:

$$i_R(t) \approx i_R(\,jTs/2) = I_S\;,\; t \in (jTs/2\,,\,jTs/2+Td),\,\forall j\,, \tag{12}$$

and then, neglecting the MOSFET switching time at turn-off, it is possible to state that C_{HB} is charged/depleted by a constant current source equal to I_S.

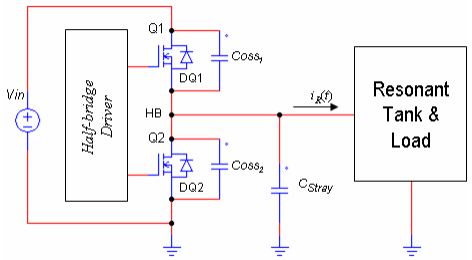

Figure 4. Reference circuit for analysis of resonant transitions in the LLC resonant half-bridge to determine ZVS conditions.

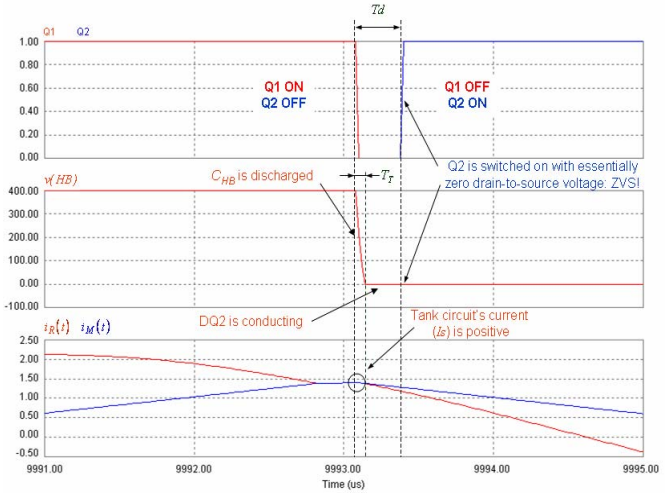

Figure 5. Detail of resonant transition with ZVS in DCM operation.

This approximation is better when the LLC resonant converter operates in DCM (see the timing diagram of Figure 5), which is actually the condition we are more interested in: the converter works in this mode both at full-load with minimum input voltage and at no-load with maximum input voltage. It is possible to show that in CCM operation (that is, when $|i_R(jTs/2)| > |i_M(jTs/2)|$), this approximation may be not as good; however, this condition is of no concern for ZVS because it is less critical than DCM [14].

The minimum value I_{Smin} that provides a rail-to-rail swing of the node HB in a time $T_T \le Td$ is given by:

$$I_{S\,min} = \frac{C_{HB}}{T_d} Vin\,. \tag{13}$$

and the actual value of I_S must be greater than I_{Smin} under all operating conditions.

VI. Modeling Operation Below Resonance

Let us refer again to Figure 2, where the main waveforms of an LLC resonant converter in the below-resonance region are shown. In the time interval (0, Tz), the tank current and the magnetizing current are respectively expressed by:

$$i_{R1}(t) = \frac{I_S}{sin\,\theta_1} sin(2\pi\, f_{R1}\, t - \theta_1) \tag{14}$$

$$i_{M1}(t) = -I_S + \frac{I_M + I_S}{Tz} t \tag{15}$$

The secondary current, flowing through the rectifier D1, is:

$$i_{D1}(t) = a\,[\,i_{R1}(t) - i_{M1}(t)]. \tag{16}$$

In the interval (Tz, $Ts/2$), $i_R(t) = i_M(t)$ (DCM operation) and they both are described by the equation:

$$i_{R2}(t) = i_{M2}(t) = I_A\, sin(2\pi\, f_{R2}\, t - \theta_2)\,, \tag{17}$$

while the secondary current $i_{D1}(t)$ is identically zero. The tank current $i_{R2}(t)$ looks flat and we now make the fundamental assumption:

$$i_{R1}(Tz) = i_{M1}(Tz) = I_M = i_{R2}\left(\frac{Ts}{2}\right) = i_{M2}\left(\frac{Ts}{2}\right) = I_S\,, \tag{18}$$

that is, the tank current I_M at $t = Tz$ equals the switched current I_S.

This equality holds true if the peak of the sinusoid (17) occurs exactly at the midpoint Tx of the interval (Tz, $Ts/2$):

$$Tx = \frac{1}{2}\left(Tz + \frac{Ts}{2}\right). \tag{19}$$

In turn, for this to occur, the voltage across the transformer's primary winding ($Ls + Lp$) must be zero at this point, so the voltage V_C across the resonant capacitor Cr, $V_C(Tx)$, must equal the input voltage to the converter Vin. We use this condition later to finalize the model.

Because of the symmetry of the tank current, it is always:

$$-i_{R1}(0) = i_{R2}\left(\frac{Ts}{2}\right) = I_S \tag{20}$$

regardless of the operating conditions for the converter; the assumption (19) implies $-i_{R1}(0) = i_{R1}(Tz)$ and, consequently:

$$Tz = \frac{1}{2}T_{R1} \quad (T_{R1} = 1/f_{R1}). \tag{21}$$

Figure 2 shows that even if the instant *Tc* when $V_C = Vin$ is not exactly coincident with *Tx,* the $I_M = I_S$ approximation is still excellent.

Considering (21), (15) and (19) can be rewritten as follows:

$$i_{M1}(t) = I_S\left(\frac{4}{T_{R1}}t - 1\right) \tag{22}$$

$$Tx = \frac{1}{4}(T_{R1} + Ts). \tag{23}$$

Concerning (17), another consequence of (18) is:

$$I_S = I_A\, sin(\pi f_{R2}T_{R1} - \theta_2) = I_A\, sin(\pi f_{R2}Ts - \theta_2), \tag{24}$$

from which it is possible to derive the value of θ_2, remembering that supplementary angles have the same sine:

$$\theta_2 = \frac{\pi}{2}\left(\frac{Ts + T_{R1}}{T_{R2}} - 1\right), \tag{25}$$

and that of I_A:

$$I_A = \frac{I_S}{cos\left(\frac{\pi}{2}\frac{Ts - T_{R1}}{T_{R2}}\right)}, \tag{26}$$

where $T_{R2} = 1/f_{R2}$.

As to the converter's dc output current *Iout*, considering that each secondary rectifier carries half the total value, it is possible to write:

$$Iout = \frac{2}{Ts}\int_0^{T_{R1}/2} i_{D1}(t)dt\,. \tag{27}$$

Substituting (16) in (27), taking (14) and (22) into consideration and developing the integral, we find:

$$Iout = \frac{2a\,I_S}{\pi tan(\theta_1)}\frac{T_{R1}}{Ts}\,. \tag{28}$$

The dc input current *Iin* can be found by integrating the tank current along a switching half-cycle:

$$Iin = \frac{1}{Ts}\left[\int_0^{T_{R1}/2} i_{R1}(t)dt + \int_{T_{R1}/2}^{Ts/2} i_{R2}(t)dt\right]. \tag{29}$$

Developing the two integrals separately and taking (25) and (26) into account, after some calculations we find:

$$Iin = \frac{I_S}{Ts}\left[\frac{T_{R1}}{\pi tan(\theta_1)} + \frac{T_{R2}}{\pi}tan\left(\frac{\pi}{2}\frac{Ts - T_{R1}}{T_{R2}}\right)\right]. \tag{30}$$

To find the unknown quantities *Ts* (*fs*) and θ_1, this equation should be solved simultaneously with (28), but unfortunately they form a transcendent system that does not have a closed-form solution. However, in the interval (T_{R1}/2, *Ts*/2) the tank current $i_{R2}(t)$ is maximally flat. It can be approximated by a horizontal line ($i_{R2}(t) \approx I_S$) and the area below the curve by that of a rectangle. Then, the result of the second integral in (30) can be replaced by:

$$I_S\left(\frac{Ts}{2} - \frac{T_{R1}}{2}\right) = \frac{1}{2}I_S(Ts - T_{R1}) \tag{31}$$

Note that if we consider the first-order series expansion of the tangent function in (30), we get the same result. In the end, (30) can be rewritten as:

$$Iin = \frac{I_S}{2}\left[\left(\frac{2}{\pi tan(\theta_1)} - 1\right)\frac{T_{R1}}{Ts} + 1\right] \tag{32}$$

The simultaneous solution of (28) and (32) provides:

$$\begin{cases} fs = \left(1 - \dfrac{2a\,Iin - Iout}{a\,I_S}\right)f_{R1} \\ tan(\theta_1) = \dfrac{2}{\pi}\left(1 - a\dfrac{2\,Iin - I_S}{Iout}\right) \end{cases} \tag{33}$$

Table 1 shows the most important electrical quantities useful for the design of the converter that can be derived from (28), (32) and (33).

The voltage V_C across the resonant capacitor *Cr* can be expressed as:

$$V_C(t) = \begin{cases} V_C(0) + \dfrac{1}{Cr}\displaystyle\int_0^t i_{R1}(t)dt & 0 \le t \le \frac{T_{R1}}{2} \\ V_C\left(\dfrac{T_{R1}}{2}\right) + \dfrac{1}{Cr}\displaystyle\int_{T_{R1}/2}^t i_{R2}(t)dt & \dfrac{T_{R1}}{2} \le t \le \dfrac{Ts}{2} \end{cases} \tag{34}$$

As to the value of $V_C(Ts/2)$, on the one hand it is given by:

$$V_C\left(\frac{Ts}{2}\right) = V_C(0) + \frac{1}{Cr}\left[\int_0^{T_{R1}/2} i_{R1}(t)dt + \int_{T_{R1}/2}^{Ts/2} i_{R2}(t)dt\right], \tag{35}$$

which, by comparison with (29), can be written as:

$$V_C\left(\frac{Ts}{2}\right) = V_C(0) + \frac{Iin}{Cr}Ts\,. \tag{36}$$

On the other hand, remembering that V_C has a dc value equal to *Vin*/2, for symmetry the following identity holds true:

$$V_C\left(\frac{Ts}{2}\right) - \frac{Vin}{2} = \frac{Vin}{2} - V_C(0) \rightarrow V_C\left(\frac{Ts}{2}\right) = -V_C(0) + Vin \tag{37}$$

Combining (36) and (37) it is possible to find:

$$V_C(0) = \frac{1}{2}\left(Vin - \frac{Iin}{Cr}Ts\right) \tag{38}$$

With this information, (35) is totally defined and can be used to calculate the peak voltage on *Cr* listed in Table 1, as well as $V_C(Tx)$; after some algebra we find:

TABLE 1
MAIN ELECTRICAL QUANTITIES

Parameter	Value
Primary peak current	$\frac{Is}{sin\,\theta_1}$
Primary rms current	$\frac{\sqrt{2}}{2}I_S\sqrt{2+\frac{fs}{f_{R1}}\left(\frac{1}{sin^2\theta_1}-2\right)}$
Q1 and Q2 rms current	$\frac{1}{2}I_S\sqrt{2+\frac{fs}{f_{R1}}\left(\frac{1}{sin^2\theta_1}-2\right)}$
Secondary peak current	$aI_S\left[1+\sqrt{\frac{1}{sin^2\theta_1}-\frac{4}{\pi^2}}-\frac{2}{\pi}\left(\theta_1+cos^{-1}\left(\frac{2}{\pi}sin\theta_1\right)\right)\right]$
Secondary rms current (x diode)	$\frac{aI_S}{2\pi\,sin\,\theta_1}\sqrt{\frac{fs}{f_{R1}}\left(\pi^2-\frac{48-2\pi^2}{3}sin^2\theta_1\right)}$
Secondary total rms current	$\frac{\sqrt{2}\,aI_S}{2\pi\,sin\,\theta_1}\sqrt{\frac{fs}{f_{R1}}\left(\pi^2-\frac{48-2\pi^2}{3}sin^2\theta_1\right)}$
Resonant cap peak voltage	$\frac{Vin}{2}+\frac{I_S}{4\pi f_{R1}Cr}\left[\pi\left(\frac{f_{R1}}{fs}-1\right)+\frac{2}{sin\,\theta_1}\right]$

$$Vc(Tx) = \frac{1}{2}\left(Vin + \frac{1}{\pi tan(\theta_1)} \frac{I_S}{Cr} T_{R1} \right) \quad (39)$$

As previously said, for model consistency, the voltage $V_C(Tx)$ must equal the input voltage *Vin*; this condition needs to be fulfilled at the minimum input voltage Vin_{min}. Then:

$$\frac{1}{\pi tan(\theta_1)} \frac{I_S}{Cr} T_{R1} = Vin_{min} . \quad (40)$$

Note that the switched current I_S, by virtue of (18), can be expressed as a function of the parallel inductance *Lp*:

$$I_S = \frac{a}{4} \frac{Vout + V_F}{Lp\, f_{R1}} . \quad (41)$$

If now we substitute the expression (33) of $tan(\theta_1)$ and express *Cr* in terms of T_{R1} (f_{R1}) in (40), then solve for I_S and compare the result with (41), a constraint may be found on the parallel inductor *Lp*. Introducing the series-to-parallel inductance ratio λ and the dc conversion ratio *M* defined in section IV, the required *Lp* value may be found:

$$Lp = \frac{a^2}{2 f_{R1}} \frac{\lambda (Vout + V_F)}{4a\lambda\, Iin + \left(\pi^2 a\, M_{max} - 2\lambda\right) Iout} . \quad (42)$$

VII. Discussion of the Model

The waveforms of Figure 2 and the model derived by their inspection in the previous section actually refer to a particular operating condition, the DCMB2 mode described in [3]. This can be considered a good design choice for the converter when it works at the lower end of its input voltage range and with its maximum or peak load.

There are at least two reasons for this. One is that it is a reasonable trade-off between a good utilization of the below-resonance region, and a reasonably safe distance - the entire DCMB1 operating region [3] – from the undesired capacitive operating mode, which takes parameter spread of both the tank circuit and the control circuit into consideration.

Another reason is that in the time interval (*Tz*, *Ts*/2) where the total primary inductance resonates with the tank capacitor, the tank and the magnetizing currents are nearly constant, and the induction level inside the magnetic core does not increase significantly either. In terms of Δ*B*, then, the transformer can be designed as if it was operated at the resonance frequency f_{R1} instead of the actual (lower) operating frequency *fs*.

The accuracy of the model is expected to be excellent: the approximation concerns just a minor portion of the waveform. The biggest source of error is probably in the value of *Iin*, which depends on a correct estimate of the converter's efficiency η. Experience and comparison with similar designs will help make an estimate as close to reality as possible.

C_{HB} is another crucial parameter. However, just the maximum expected value needs to be estimated and, again, experience and comparison with similar designs will be a guide.

Equation (42) provides the value of the parallel inductor *Lp* that makes the converter operate in the desired DCMB2 mode and provides no-load operation capability. This *Lp* value, however, must be such that ZVS is ensured as well.

ZVS under no-load conditions is ensured if the switched current I_{Mco} given by (10) is larger than I_{Smin} given by (13) at maximum input voltage. Solving for *Lp* yields:

$$Lp \le \frac{Td}{4\pi f_{R1} C_{HB}} \sqrt{4(1+\lambda) a^2 M_{min}^2 - \frac{\lambda^2}{1+\lambda}} \quad (43)$$

Actually, the switched current given by (41) should also be checked for being greater than I_{Smin}. However, remember that always $|I_S| = |i_R(jTs/2)| \ge |i_M(jTs/2)|$ as long as the converter works in the inductive region; note also that with the present design, $i_M(jTs/2)$ is nearly constant in the below-resonance region and is inversely proportional to frequency in the above-resonance region; thus it takes its minimum value at $f = f_{max}$, where it equals I_{Mco} given by (10), by design.

Therefore, if the value resulting from (42) fulfills (43), the I_S given by (41) is also larger than I_{Smin} and ZVS is ensured throughout the operating range. If (43) is not fulfilled, one or more of the following actions can solve the issue:

a) reduce fs_{max}; b) increase f_{R1}; c) reduce *a*; d) reduce C_{HB}.

An *Lp* value much smaller than the limit given by (43) is not good either: this would imply $I_S >> I_{Smin}$, which would lead to higher switching losses at turn-off. Ideally, the optimum condition is when the value of *Lp* given by (42) equals the limit (43). However, since component tolerance must be taken into account, some margin (10-15 %) is recommended.

VIII. Design Procedure

The proposed design procedure, based on the previous analysis, can be outlined in nine steps, starting from the design specification detailed in Table 2.

Step 1 – Calculate the min. and max. dc conversion ratios M_{min}, M_{max}, and the dc input current *Iin* at $Vin = Vin_{min}$:

$$Iin = \frac{Vout\, Iout}{\eta Vin_{min}} .$$

Step 2 – Calculate the transformer turn ratio *a* using (4). Set $V_F = 0.6$ V for Schottky rectifiers, $V_F = 0.2$ V if synchronous rectification is going to be used.

Step 3 – Calculate the parallel-to-series inductance ratio λ using (9).

Step 4 – Calculate the parallel inductance *Lp* required for maximum model validity using (42).

Step 5 – Check that the value of *Lp* fulfills the ZVS condition (43). If not, try either reducing fs_{max} or increasing f_{R1} or else reducing *a* or C_{HB} and go back to Step 4. Adjust one or more of the above parameters also if *Lp* is much lower than the minimum needed for ZVS.

Step 6 – Calculate the value of *Ls* and *Cr*:

$$Ls = \frac{Lp}{\lambda}; \quad Cr = \frac{1}{Ls(2\pi f_{R1})^2} .$$

Step 7 – Calculate the switched current I_S at full load and minimum input voltage from (41).

Step 8 – Calculate the operating frequency at full load and minimum input voltage $fs_{min} = fs$ and the tank current displacement angle θ_1 from (33).

Step 9 – Calculate all the tank circuit's electrical quantities using the relationships in Table 1.

TABLE 2
DESIGN SPECIFICATION OF THE EXEMPLARY LLC CONVERTER

Parameter	Symbol	Value	Unit
Input voltage range	Vin_{min} - Vin_{max}	320 - 430	V
Nominal input voltage	Vin_{nom}	390	V
Regulated output voltage	*Vout*	36	V
Maximum (peak) output current	*Iout*	8.5	A
Resonance frequency	f_{R1}	120	kHz
Maximum operating frequency	fs_{max}	200	kHz
Expected efficiency (@ Vin_{min})	η	95	%
Parasitic capacitance of node HB (max.)	C_{HB}	200	pF
Dead time of driver circuit (min.)	*Td*	200	ns

IX. EXPERIMENTAL VERIFICATION

An LLC resonant half-bridge based on the electrical specification given in Table 2 has been designed using the procedure previously outlined, and a prototype has been built and evaluated on the bench.

The resonant-tank parameters, as well as the converter's operating conditions @ *Vin* = 320 V dc, *Iout* = 8.5 A resulting from the design procedure are listed in Table 3, where actual values and bench measurements are shown too. Notice that the measured values match the calculated ones very well.

The oscilloscope picture in Figure 6 shows some significant waveforms of the converter's operation under the same *Vin* and *Iout* conditions.

TABLE 3
RESONANT TANK PARAMETERS AND OPERATING CONDITIONS OF THE CONVERTER SPECIFIED IN TABLE 2

Parameter (Symbol)	Calculated	Measured	Unit
Parallel resonant inductance (*Lp*)	305	296	µH
Series resonant inductance (*Ls*)	56.3	54	µH
Primary-to-secondary turns ratio (*a*)	5.783	23/4=5.75	---
Resonant capacitance (*Cr*)	31.3	33	nF
Resonance frequency (f_{R1})	120	119.2	kHz
Min. switching frequency (*fs*)	80.7	80.6	kHz
Max. switching frequency (*fs*)	200	202.4	kHz
Peak primary current (Ip_{pk})	3.96	3.92	A
Switched current (I_S)	1.37	1.33	A
Tank current phase angle (θ_1)	20.3	19.1	Deg
Resonant capacitor peak voltage (V_{Cpk})	362.3	360	V

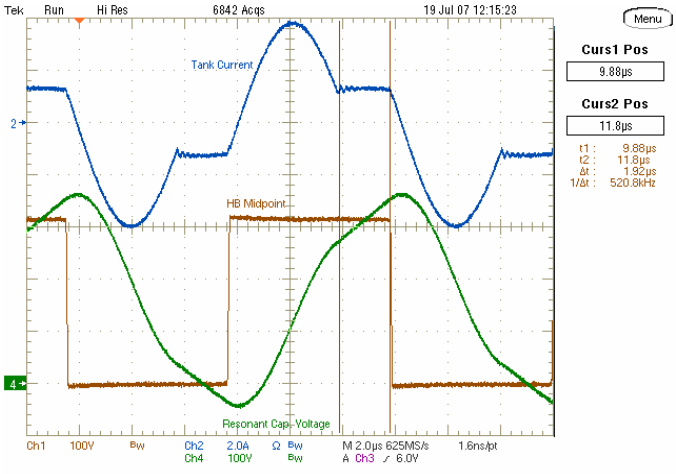

Figure 6. Main waveforms taken on a prototype of the LLC converter specified in Table 2 @ *Vin* = 320 V dc, *Iout* = 8.5 A.

X. CONCLUSIONS

The LLC resonant converter has been analyzed in a well-defined below-resonance operating condition with a semi-empirical approach based on inspection of the tank current waveforms. This has lead to a simple yet accurate design-oriented model and to a simple step-by-step design procedure that ensures stable operation at no load, ZVS under all operating conditions, and optimum operation under nominal conditions. The validity of the approach and the points that need more attention in the design procedure have been discussed.

To validate the model, a converter has been designed following the proposed step-by-step procedure and a prototype built and evaluated on the bench. This has shown that the theoretical predictions match the experimental results very well, thus proving the accuracy of the model.

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Analysis and Design of LLC Resonant Converter with Integrated Transformer

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***Abstract*- LLC resonant converter has a lot of advantages over the conventional series resonant converter and parallel resonant converter; narrow frequency variation over wide load and input variation, Zero Voltage Switching (ZVS) for entire load range and integration of magnetic components. This paper presents analysis and design consideration for half-bridge LLC resonant converter with integrated transformer. Using the fundamental approximation, the gain equation is obtained, where the leakage inductance in the transformer secondary side is also considered. Based on the gain equation, the practical design procedure is investigated to optimize the resonant network for a given input/output specifications. The analysis and design procedure are verified through an experimental prototype converter.**

I. INTRODUCTION

The Conventional PWM technique processes power by controlling the duty cycle and interrupting the power flow. All the switching devices are hard-switched with abrupt change of currents and voltages, which results in severe switching losses and noises. Meanwhile, the resonant switching technique process power in a sinusoidal form and the switching devices are softly commutated. Therefore, the switching losses and noises can be dramatically reduced. This also allows the reduction of the passive component size by increasing the switching frequency. For this reason, resonant converters have drawn a lot of attentions in various applications [1-3]. Among many resonant converters, half-bridge LLC-type series-resonant converter has been the most popular topology for many applications since this topology has many advantages over other topologies; it can regulate the output over wide line and load variations with a relatively small variation of switching frequency, it can achieve zero voltage switching (ZVS) over the entire operating range, the magnetic components can be integrated into a transformer and all essential parasitic elements, including junction capacitances of all semi-conductor devices, are utilized to achieve ZVS.

While a lot of researches have been done on the LLC resonant converter topology ever since this topology was first introduced in 1990's [4], most of the researches have focused on the steady state analysis rather than practical design consideration. In [5], the low noise features were mainly investigated and no design procedure was studied. Reference [6] discussed the above resonance operation in buck mode only, where LLC topology was introduced as "LCL type series resonant converter." In [7], detailed analysis was done on the buck mode operation as well as on the boost mode operation, but no design consideration was given. References [8-12] investigated LLC topology in detail using fundamental approximation, but simplified the AC equivalent circuit by ignoring the leakage inductance in the secondary side. In general, the magnetic components of the LLC resonant converter are implemented with one core by utilizing the leakage inductance as the resonant inductor and consequently the leakage inductance exists not only in the primary side but also in the secondary side. Since the leakage inductance in the secondary side affects the gain equation, ignoring the leakage inductance in the secondary side results in incorrect design.

This paper presents design consideration for half bridge LLC resonant converter. Using the fundamental approximation, the gain equation is obtained, where the leakage inductance in the transformer secondary side is also considered. Based on the gain equation, the practical design procedure is investigated to optimize the resonant network for a given input/output specifications. The design procedure is verified through an experimental prototype converter of 120W half-bridge LLC resonant converter.

II. OPERATION PRINCIPLES AND FUNDAMENTAL APPROXIMATION

Fig. 1 shows the simplified schematic of half-bridge LLC resonant converter. The magnetic components are integrated into a transformer; L_m is the magnetizing inductance and L_{lkp} and L_{lks} are the leakage inductances in the primary and secondary, respectively. Fig. 2 shows the typical waveforms of LLC resonant converter. Operation of the LLC resonant converter is similar as that of the conventional LC series resonant converter. The only difference is that the value of the magnetizing inductance is relatively small and therefore the resonance between L_m+L_{lkp} and C_r affects the converter operation. Since the magnetizing inductor is relatively small, there exists considerable amount of magnetizing current (I_m).

In general, the LLC resonant topology consists of three stages as shown in Fig. 1; square wave generator, resonant network and rectifier network.

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- The square wave generator produces a square wave voltage, V_d by driving switches, Q1 and Q2 with alternating 50% duty cycle for each switch. The square wave generator stage can be built as a full-bridge or half bridge type.
- The resonant network consists of capacitor and leakage inductances and magnetizing inductance of the transformer. The resonant network has an effect of filtering the higher harmonic currents. Thus, essentially only sinusoidal current is allowed to flow through the resonant network even though square wave voltage is applied to the resonant network. The current is lagging the voltage applied to the resonant network (that is, the fundamental component of the square wave applied by the half-bridge totem pole), which allows the MOSFETs to be turned on with zero voltage. As can be seen in Fig. 2, the MOSFET turns on while the current is flowing through the anti-parallel diode and the voltage across the MOSFET is zero.
- The rectifier network produces DC voltage by rectifying the AC current with a capacitor. The rectifier network can be implemented as a full-wave bridge or center-tapped configuration with capacitive output filter.

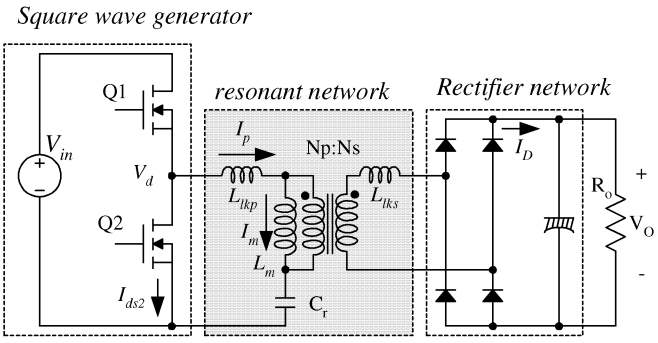

Figure 1. A schematic of half-bridge LLC resonant converter

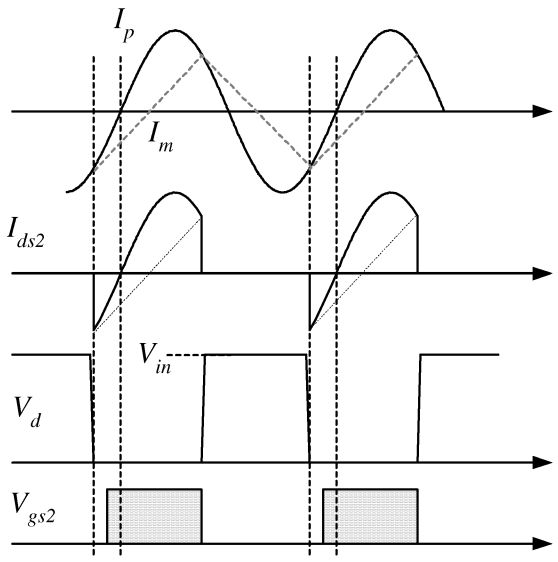

Figure 2. Typical waveforms of half-bridge LLC resonant converter

The filtering action of the resonant network allows the classical fundamental approximation to obtain the voltage gain of the resonant converter, which assumes that only the fundamental component of the square-wave voltage input to the resonant network contributes to the power transfer to the output. Because the rectifier circuit in the secondary side acts as an impedance transformer, the equivalent load resistance is different from actual load resistance. Fig. 3 shows how this equivalent load resistance is derived. The primary side circuit is replaced by a sinusoidal current source, I_{ac} and a square wave of voltage, V_{RO} appears at the input to the rectifier. Since harmonic components of V_{RO} are not involved in the power transfer, AC equivalent load resistance can be calculated by dividing the fundamental component of V_{RO} by I_{ac} as

$$R_{ac} = \frac{V_{RO}^{\ F}}{I_{ac}} = \frac{8}{\pi^2}\frac{V_o}{I_o} = \frac{8}{\pi^2}R_o \qquad (2)$$

By using the equivalent load resistance, the AC equivalent circuit is obtained as illustrated in Fig. 4.

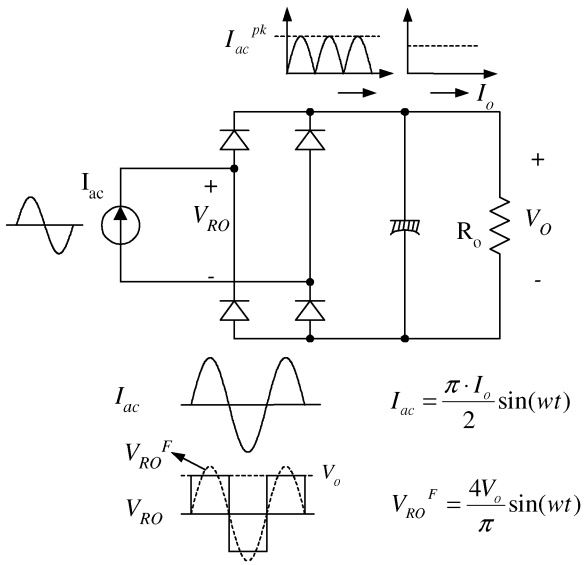

Figure 3. Derivation of equivalent Load resistance R_{ac}

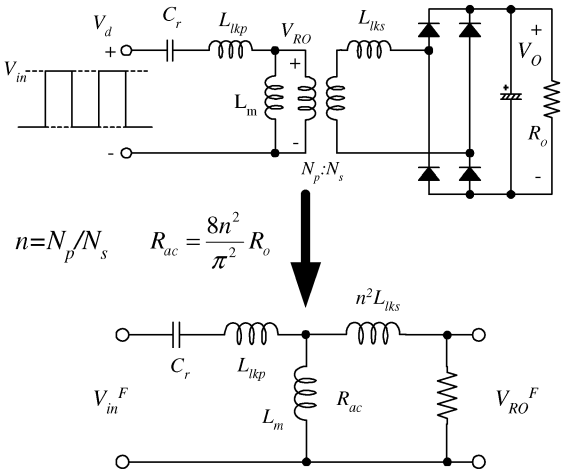

Figure 4. AC equivalent circuit for LLC resonant converter

With the equivalent load resistance obtained in (2), the characteristics of the LLC resonant converter can be derived. Using the AC equivalent circuit of Fig. 4, the voltage gain is obtained as

$$M = \frac{2n \cdot V_O}{V_{in}} = \left| \frac{\omega^2 L_m R_{ac} C_r}{j\omega \cdot (1 - \frac{\omega^2}{\omega_o^2}) \cdot (L_m + n^2 L_{lks}) + R_{ac}(1 - \frac{\omega^2}{\omega_p^2})} \right| \quad (3)$$

where

$$R_{ac} = \frac{8n^2}{\pi^2} R_o$$

$$L_p = L_m + L_{lkp} \ , \ L_r = L_{lkp} + L_m // (n^2 L_{lks})$$

$$\omega_o = \frac{1}{\sqrt{L_r C_r}} \ , \quad \omega_p = \frac{1}{\sqrt{L_p C_r}}$$

As can be seen in (3), there are two resonant frequencies. One is determined by L_r and C_r while the other is determined by L_p and C_r. In actual transformer, L_p and L_r can be measured in the primary side with the secondary side winding open circuited and short circuited, respectively.

Important feature that should be observed in (3) is that the gain is fixed at resonant frequency (w_o) regardless of the load variation, which is given as

$$M_{@\omega=\omega_o} = \frac{L_m}{L_p - L_r} = \frac{L_m + n^2 L_{lks}}{L_m} \quad (4)$$

Without considering the leakage inductance in the transformer secondary side, the gain in (4) becomes unity. In the previous research, the leakage inductance in the transformer secondary side was ignored to simplify the gain equation [7-12]. However, as observed, there exists considerable error when ignoring the leakage inductance in the transformer secondary side, which generally results in non optimized design.

By assuming that $L_{lkp}=n^2 L_{lks}$, the gain in (2) can be simplified as

$$M = \frac{2n \cdot V_O}{V_{in}} = \left| \frac{(\frac{\omega^2}{\omega_p^2}) \frac{k}{k+1}}{j(\frac{\omega}{\omega_o}) \cdot (1 - \frac{\omega^2}{\omega_o^2}) \cdot Q \frac{(k+1)^2}{2k+1} + (1 - \frac{\omega^2}{\omega_p^2})} \right| \quad (5)$$

where

$$k = \frac{L_m}{L_{lkp}} \quad (6)$$

$$Q = \frac{\sqrt{L_r / C_r}}{R_{ac}} \quad (7)$$

The equation (4) is plotted in Fig. 5 for different Q values with k=5 and f_o=100kHz. The gain at the resonant frequency (w_o) is also simplified in terms of k as

$$M_{@\omega=\omega_o} = \frac{L_m + n^2 L_{lks}}{L_m} \cong \frac{L_m + L_{lkp}}{L_m} = \frac{k+1}{k} \quad (8)$$

As observed in Fig. 5, the LLC resonant converter shows nearly load independent characteristics when the switching frequency is around the resonant frequency. This is a distinctive advantage of LLC-type resonant converter over conventional series-resonant converter. Therefore, it is natural to operate the converter around the resonant frequency to minimize the switching frequency variation at light load condition.

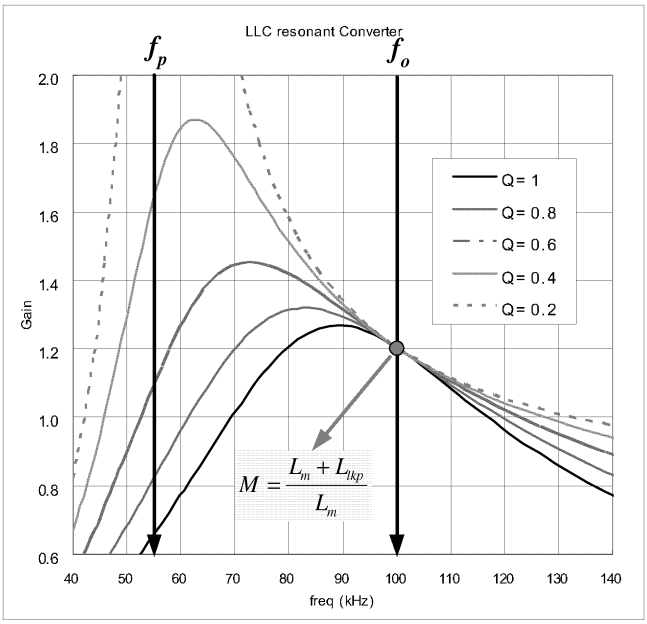

Figure 5. Typical gain curves of LLC resonant converter

The operation range of LLC resonant converter is determined by the available peak voltage gain. As shown in Fig. 5, higher peak gain is obtained as Q decreases (as load decreases). Another important factor that determines the peak gain is the ratio between L_m and L_{lkp} which is defined as k in (5). Even though the peak gain at a given condition can be obtained by using the gain in (4), it is difficult to express the peak gain in explicit form. Moreover, the gain obtained from (4) has some error at frequencies below the resonant frequency (f_o) due to the fundamental approximation. In order to simplify the analysis and design, the peak gains are obtained using simulation tool and depicted in Fig. 6, which shows how the gain varies with Q for different k values. It appears that higher peak gain can be obtained by reducing k or Q values. With a given resonant frequency (f_o), decreasing k or Q means reducing the magnetizing inductance, which results in increased circulating current. Accordingly, there is a trade-off between the available gain range and conduction loss.

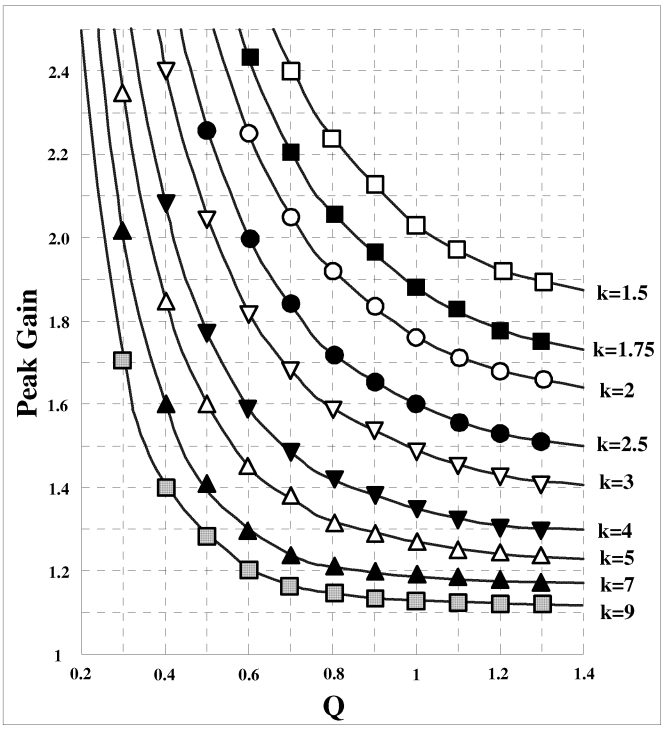

Figure 6. Peak gain versus Q for different k values

III. Design Consideration

Based on the previous analysis, the practical design procedure is presented in this section. It discusses optimizing the resonant network for a given input/output specifications.

(1) Operation mode: While the conventional LC series resonant converter always operates at a frequency above the resonant frequency, LLC resonant converter can operate at frequency below or above the resonance frequency. Fig 8 shows the waveforms of the currents in the transformer primary side and secondary side. As can be observed, operation below the resonant frequency (case I) allows the soft commutation of the rectifier diodes in the secondary side while the circulating current is relatively large. Meanwhile, operation above the resonant frequency (case II) allows the circulating current to be minimized, but the rectifier diodes are not softly commutated. Thus, below resonance operation is preferred for high output voltage application where reverse recovery loss in the rectifier diode is severe. On the other hand, above resonance operation can show better efficiency for application where the output voltage is low and schottky diodes are available for the secondary side rectifiers since the conduction loss is minimized.

(2) Maximum Gain: The operation range of LLC resonant converter is determined by the available peak voltage gain. Since the peak gain takes place when the converter operates at the boundary of zero voltage switching (ZVS) and zero current switching (ZCS) mode, ZVS condition is lost at the maximum gain condition [12]. Therefore, some margin is required when determining the maximum gain. Based on the maximum gain, the proper Q and k values can be obtained from Fig. 6. Even though higher gain is obtained with small k, too small k value results in poor coupling of the transformer. It is typical to set k to be 5~10, which results in a gain of 1.1~1.2 at the resonant frequency.

The value of k affects the losses of the converter. The major portion of the conduction loss is caused by the magnetizing current whose peak value is given by

$$I_m^{pk} = \frac{nV_o}{L_m}\frac{T_s}{4} \tag{8}$$

The value of k also affects the switching loss. Since the turn-on switching loss is removed by zero voltage switching, the turn-off switching loss is dominant. The turn off switching loss is proportional to the turn-off current, which is same as the peak magnetizing current of (8). Therefore, magnetizing current should be minimized for high efficiency.

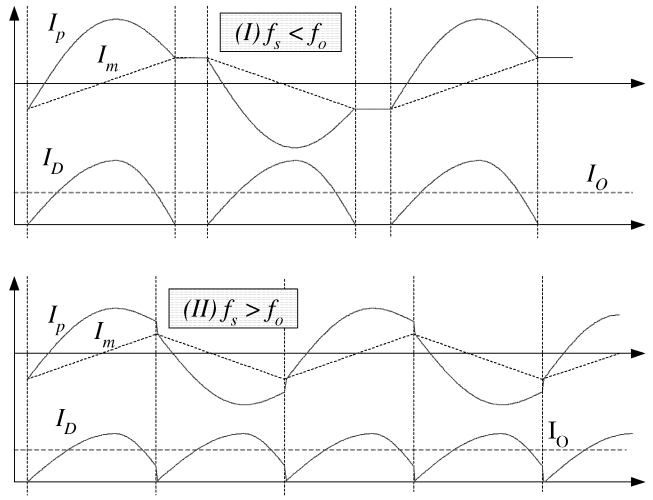

Figure 7. Waveforms of current in the transformer primary side and secondary sides for difference operation modes

IV. Experimental Results

In order to show validity of the previous analysis and design consideration, an experimental prototype converter of 120W half-bridge LLC resonant converter has been built and tested. The schematic of the converter and circuit components are shown in Fig. 8. The input voltage is 220Vac~270Vac and the output is 24V/5A. In terms of DC voltage, the input voltage is 260~380V considering holdup time.

The ratio (k) between L_m and L_{lkp} is determined as 6.5, which results in the gain at the resonant frequency as

$$M_{@\,\omega=\omega_o} = \frac{k+1}{k} = 1.15 \tag{9}$$

As observed in the previous analysis, there is a trade-off between the available gain range and conduction loss. Since the input voltage varies over wide range, if the converter is designed to operate only at below resonance frequencies, the excessive circulating current can deteriorate the efficiency.

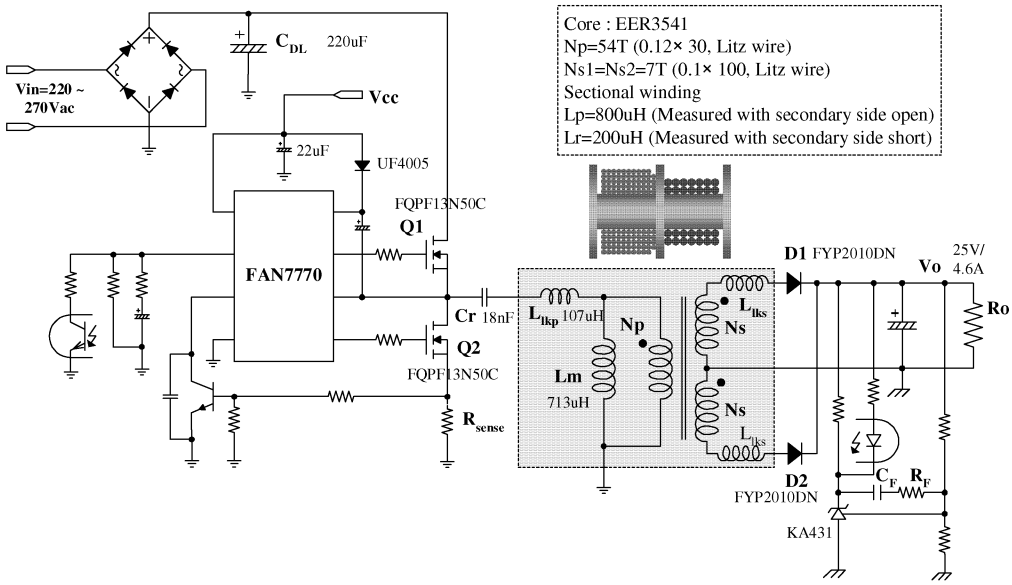

Figure.8 Schematic of half-bridge LLC resonant converter

Thus, the converter is designed to operate above resonance at high input voltage condition and below resonance at low input voltage to minimize the conduction loss caused by circulating current. The minimum gain at full load is determined as 1.0. With the minimum gain, the transformer turn ratio is obtained as

$$n = \frac{N_p}{N_s} = \frac{M_{\min} \cdot V_{in}^{\max} / 2}{(V_o + V_F)} = \frac{1 \cdot 380/2}{(24+0.8)} = 7.66 \qquad (10)$$

where V_F is the diode forward voltage drop.

The maximum gain to cover the input voltage variation is 380/260=1.46. With 10% margin, maximum gain of 1.6 is required. From the gain curves in Fig 9, Q is obtained as 0.4.

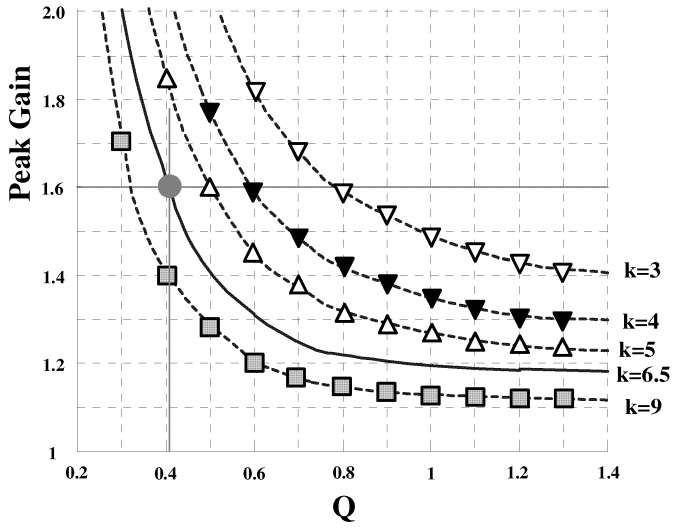

Figure 9. Design gain curves

By selecting the resonant frequency as 85kHz, the resonant network is determined as L_m=713uH, L_{lkp}=107uH (L_p=800uH, L_r=200uH) and C_r=18nF. The transformer is implemented with a sectional stacking method to increase the leakage inductance as depicted in Fig. 8.

Fig. 10 and 11 show the operation waveforms for full load condition with input voltage of 220Vac and 270Vac, respectively. Fig. 12 and 13 show the operation waveforms for no load condition with input voltage of 220Vac and 270Vac, respectively. As can be seen, ZVS is achieved for entire input/output range.

Fig. 14 shows the measured efficiency. As expected, efficiency decreases for low input voltage condition due to the increased circulating current.

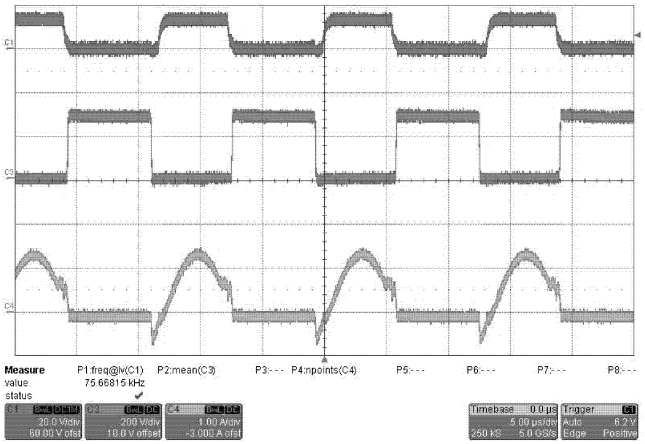

Figure 10. Operation waveforms : 220Vac input and full load
C1: gate drive signal (20V/div), C3: Drain voltage (200V/div)
C4: Drain current (1A/div)

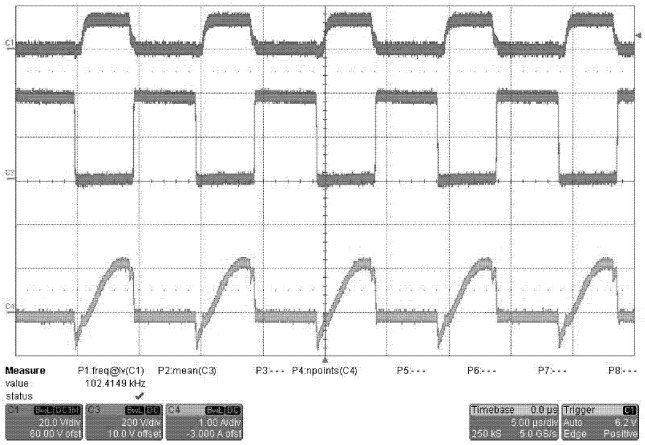

Figure 11. Operation waveforms : 270Vac input and full load
C1: gate drive signal (20V/div), C3: Drain voltage (200V/div)
C4: Drain current (1A/div)

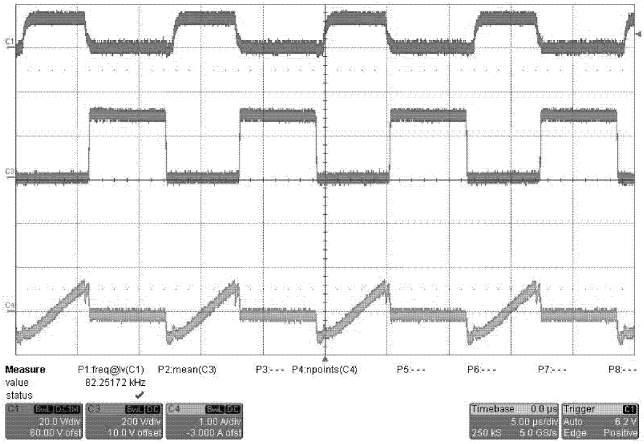

Figure 12. Operation waveforms : 220Vac input and no load
C1: gate drive signal (20V/div), C3: Drain voltage (200V/div)
C4: Drain current (1A/div)

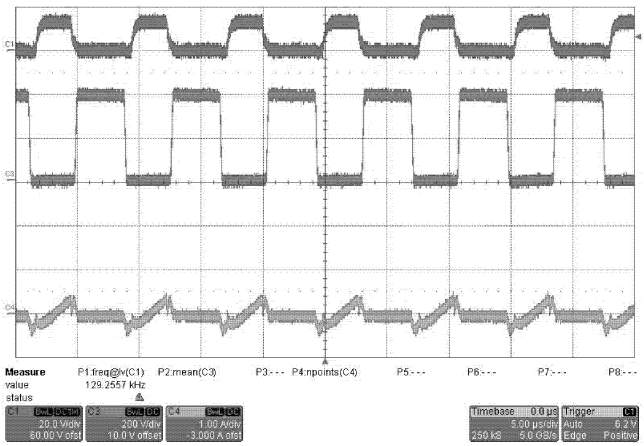

Figure 13. Operation waveforms : 270Vac input and no load
C1: gate drive signal (20V/div), C3: Drain voltage (200V/div)
C4: Drain current (1A/div)

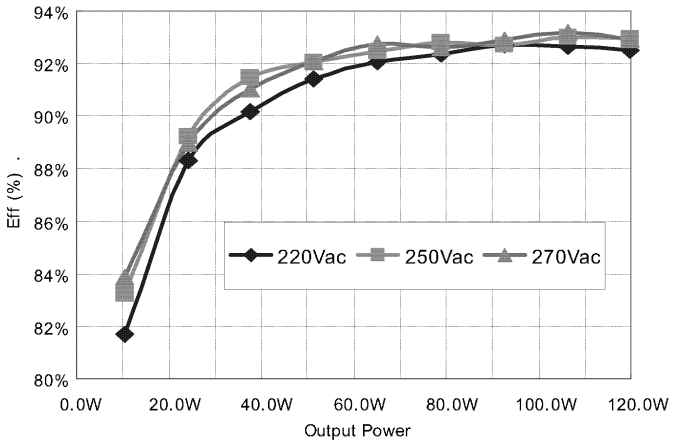

Figure 14. Measured efficiency

V. CONCLUSION

This paper has presented design consideration for LLC resonant converter with integrated transformer, which utilizes the leakage inductances and magnetizing inductance of transformer as resonant components. The leakage inductance in the transformer secondary side was also considered in the gain equation. The design procedure was verified through experimental results.

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