Underside Federal de Juiz de Fora
Programa de Pós-Graduação em
Engenharia Elétrica

Guilherme Márcio Soares

CAPACITANCE REDUCTION IN OFF-LINE LED DRIVERS BY USING ACTIVE RIPPLE COMPENSATION TECHNIQUES

Tese de Doutorado

Juiz de Fora
2017

Guilherme Márcio Soares

Capacitance Reduction in Off-line LED Drivers by Using Active Ripple Compensation Techniques

Tese submetida ao corpo docente da coordenação do Programa de Pós Graduação em Engenharia Elétrica, área de concentração: Sistemas Eletrônicos, da Faculdade de Engenharia da Universidade Federal de Juiz de Fora como parte dos requisitos do curso de doutorado em engenharia elétrica.

Orientador: Prof. Henrique Antônio Carvalho Braga, Dr. Eng.
Coorientador: Prof. José Marcos Alonso Alvarez, Dr. Eng.

Juiz de Fora
2017

Ficha catalográfica elaborada através do programa de geração
automática da Biblioteca Universitária da UFJF,
com os dados fornecidos pelo(a) autor(a)

Soares, Guilherme Márcio.
Capacitance Reduction in Off-line LED Drivers by Using Active Ripple Compensation Techniques / Guilherme Márcio Soares. -- 2017.
287 p.

Orientador: Henrique Antônio Carvalho Braga
Coorientador: José Marcos Alonso Alvarez
Tese (doutorado) - Universidade Federal de Juiz de Fora, Faculdade de Engenharia. Programa de Pós-Graduação em Engenharia Elétrica, 2017.

1. Conversores para o acionamento de LEDs. 2. Compensação de ondulação de corrente. 3. Redução de capacitâncias. 4. Otimização de conversores estáticos. 5. Correção do fator de potência. I. Carvalho Braga, Henrique Antônio, orient. II. Alonso Alvarez, José Marcos, coorient. III. Título.

Guilherme Márcio Soares

Capacitance Reduction in Off-line LED Drivers Using Active Ripple Compensation Techniques

Tese submetida ao corpo docente da coordenação do Programa de Pós Graduação em Engenharia Elétrica, área de concentração: Sistemas Eletrônicos, da Faculdade de Engenharia da Universidade Federal de Juiz de Fora como parte dos requisitos do exame de qualificação do curso de doutorado em engenharia elétrica.

Aprovada em 18 de novembro de 2017.

BANCA EXAMINADORA:

Prof. Henrique Antônio Carvalho Braga, Dr. Eng.

Universidade Federal de Juiz de Fora, UFJF

Prof. José Marcos Alonso Álvarez, Dr. Ing.

Universidade de Oviedo, UNIOVI

Prof. Marco Antônio Dalla Costa, Dr.

Universidade Federal de Santa Maria, UFSM

Prof. Edilson Mineiro Sá Júnior, Dr. Eng.

Instituto Federal de Educação, Ciência e Tecnologia do Ceará, IFCE

Prof. Pedro Gomes Barbosa, Dsc.

Universidade Federal de Juiz de Fora, UFJF

Prof. Leonardo Willer de Oliveira, Dsc.

Universidade Federal de Juiz de Fora, UFJF

To my family.

ACKNOWLEDGMENT

This work is the result of the contribution of several people, and without them, it would not be developed in the way it was. Because of this, I need to make a brief acknowledgment.

First of all I thank God and his son, Jesus Christ, who were my first great teachers.

To my parents, because they supported me in the most difficult moments. I also thank my sister for her companionship during all these years.

To my girlfriend Camila, for the affection and understanding during this journey.

To all the professors of the electrical engineering course of the Federal University of Juiz de Fora, who shared their knowledge and helped in my professional growth. I am especially grateful to professor Henrique Braga, my supervisor, for the opportunity to research and make science. Furthermore, I thank professor José Marcos Alonso, my co-supervisor, which had a major contribution in this thesis and was very kind to me at the time I was in Gijón-ES.

To my colleagues of the Lighting Research Group (NIMO-UFJF), because this work also has a contribution of each one of them.

Finally, to my friends, for being with me in difficult times.

"*Persistence is the shortest path to success.*"

Charles Chaplin

RESUMO

Este documento apresenta uma nova técnica para a minimização da ondulação de baixa frequência, típica de conversores para o acionamento de LEDs alimentados a partir da rede elétrica. Esta estratégia baseia-se na modulação em baixa frequência da razão cíclica do conversor de modo que a ondulação de corrente possa ser reduzida e, consequentemente, as capacitâncias de filtragem do conversor possam ser minimizadas. Esta técnica foi desenvolvida para a aplicação em conversores de malha única, como é o caso de conversores de estágio único ou mesmo dois estágios integrados. A modulação da razão cíclica é projetada de maneira que o comportamento de baixa frequência das principais variáveis do conversor seja alterado, permitindo uma redução da ondulação da corrente de saída ao custo de um incremento cotrolado no conteúdo harmônico da corrente de entrada. Duas possíveis metodologias para a implementação da técnica proposta são discutidas ao longo do trabalho. A primeira envolve a injeção de harmônicas específicas no sinal da razão cíclica do conversor através de ramos adicionais na estrutura de controle. Esta abordagem foi aplicada para projetar um controlador de LEDs baseado em um conversor flyback e também em uma topologia integrada baseada na conexão cascata de dois conversores buck-boost. Este estudo inicial foi expandido para outros conversores e uma análise generalizada acerca da influência da modulação da razão cíclica no comportamento de controladores de LED alimentados a partir da rede elétrica é apresentada. A segunda metodologia para a implementação da compensação ativa da ondulação de baixa frequência do conversor é baseada na otimização de um controlador proporcional-integral a fim de que tal elemento influencie não só no comportamento dinâmico do circuito, mas também na caracteística de baixa frequência do conversor. Por fim são discutidas as principais contribuições da tese e algumas propostas para trabalhos futuros são apresentadas.

Palavras-chave: conversores para o acionamento de LEDs, fontes de alimentação, conversores alimentados a partir da rede elétrica, compensação ativa da ondulação de baixa frequência, redução de capacitâncias, correção do fator de potência, conversores sem capacitores eletrolíticos, fontes de alta confiabilidade, otimização de conversores estáticos.

ABSTRACT

This document presents a novel approach for low-frequency output current ripple minimization in off-line light-emitting diode (LED) drivers. This strategy is based on the large-signal modulation of the duty-cycle so that the output ripple can be reduced and, consequently, the required filtering capacitances of the converter can be somehow decreased. This technique is devised to be used on converters in which a single control loop is employed, such as off-line single-stage or integrated converters. The duty-cycle modulation is used to change the shape of the main waveforms of the converter, especially the input and output currents. This allows for a reduction of the output current peak-to-peak ripple while the harmonic content of the input current is increased but kept within the limits imposed by the IEC standard. Two methodologies for implementing the proposed technique are discussed along the text. The first one is related to the injection of harmonic components to the duty cycle signal by means of additional branches inserted in the conventional control structure. This approach was applied to design an off-line flyback-based LED driver and also a circuit based on the Integrated Double Buck-boost converter. This first study was expanded to other topologies and a generalized analysis regarding the impact of the duty cycle modulation on off-line converters is then presented. The second methodology for implementing the ripple compensation is based on the optimization of a proportional-integral controller so that this element is designed to influence not only in the dynamic behavior of the circuit, but also in its low-frequency characteristic. Finally, the main contributions of this work are discussed and the proposals for future works are presented.

Keywords: LED drivers, power supplies, off-line operation, active ripple compensation, capacitance reduction, power factor correction, electrolytic capacitor avoidance, high reliability, power converter optimization.

LIST OF ILLUSTRATIONS

LIST OF TABLES

LIST OF ABBREVIATIONS

ABNT Association of Technical Standards (Associação Brasileira de Normas Técnicas)

ac alternating current

Al-Caps Aluminum Electrolytic Capacitors

AP-Caps Aluminum Polymer Capacitors

ARC Active Ripple Compensation

ARCT Active Ripple-Compensation Technique

BCM Boundary Conduction Modes

CCM Continuous Conduction Mode

CCT correlated color temperature

CMC current-mode control

CRI color rendering index

dc direct current

DCM Discontinuous Conduction Mode

EMI electromagnetic interference

ES Exhaustive Search

ESR Equivalent Series Resistence

FIT Failures in Time

FoM figure of merit

HPF High Power Factor

HPS High-pressure Sodium

IBuFly Integrated Buck Flyback Converter

IDBB Integrated Double Buck-Boost

IHS Information Handling Services

INMETRO Instituto Nacional de Metrologia, Qualidade e Tecnologia

ISBB Integrated SEPIC buck-boost

LED Light-emitting Diode

LFR Low-frequency Ripple

MLC-Caps Multilayer Ceramic Capacitors

MPPF-Caps Metallized Polypropylene Film Capacitors

MTBF Mean-Time Between Failures

PC Power Control

PC-LED Phosphor-converted LED

POHC Partial Odd Harmonic Current

PF power factor

PFC Power Factor Correction

RGB Red-Green-Blue

SMPS switched-mode power supplies

SRC Series Resonant Converter

SSL Solid-State Lighting

THD Total Harmonic Distortion

VMC voltage-mode control

ZCS zero current switching

ZCD zero cross detector

CONTENTS

1 INTRODUCTION

1.1 EVOLUTION OF LIGHTING TECHNOLOGIES

The evolution of lighting technologies is closely linked with the change of habits of the society. The revolution of modern lighting systems occurred with the advent of the first lamp which used electricity for light emission. Owing to the development and production on an industrial scale by Thomas Edison, incandescent bulbs led to the beginning of night activities in greater profusion, making this invention one of the icons of 19^{th} century development.

Over the years, the need for creating more efficient techniques to produce light became evident, since the lighting systems represent a considerable portion in the global electricity consumption. According to Dreyfus and Gallinat (2015), electric lighting sources consume 15% of the total global electricity production.

From the emergence of discharge lamps, best light efficacy indexes were achieved, leading to the replacement of obsolete technologies. In this context, the use of fluorescent lamps and high-intensity discharge lamps (*e.g.*, high-pressure sodium lamps) became very popular in indoor and outdoor lighting systems, respectively.

The emergence of InGaN-based LEDs allowed for the generation of white light using solid state technology. With this discovery, studies regarding the use of this technology in artificial lighting began. Like most semiconductors, LEDs have a very sharp evolution, showing that the solid-state lighting systems will become increasingly popular.

Figure 1 shows the evolution of the efficacy of the main lighting sources according to Craford (2007). As can be seen, the evolution of the luminous efficacy of the light-emitting diodes is the sharpest among the evaluated light sources. Nowadays there commercial products that can reach more than 200 lm/W, such as the LED LM301B from Samsung Electronics (Samsung Electronics, 2017).

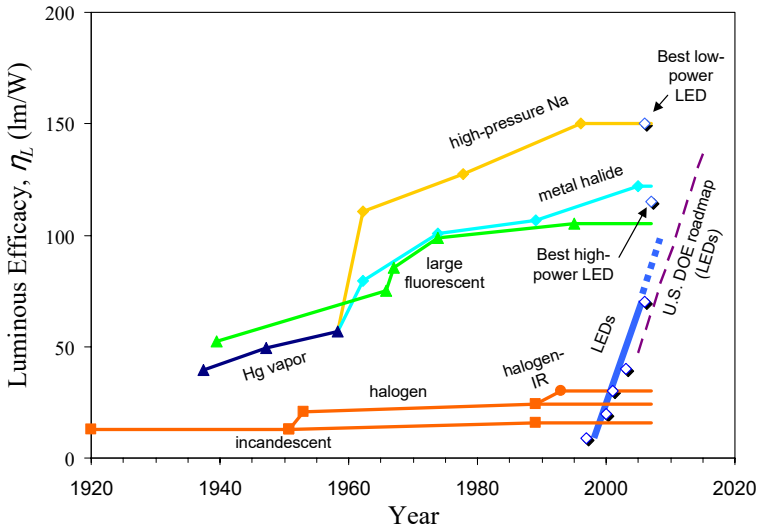


Figure 1: Evolution of the luminous efficacy of several lighting sources. (CRAFORD, 2007).

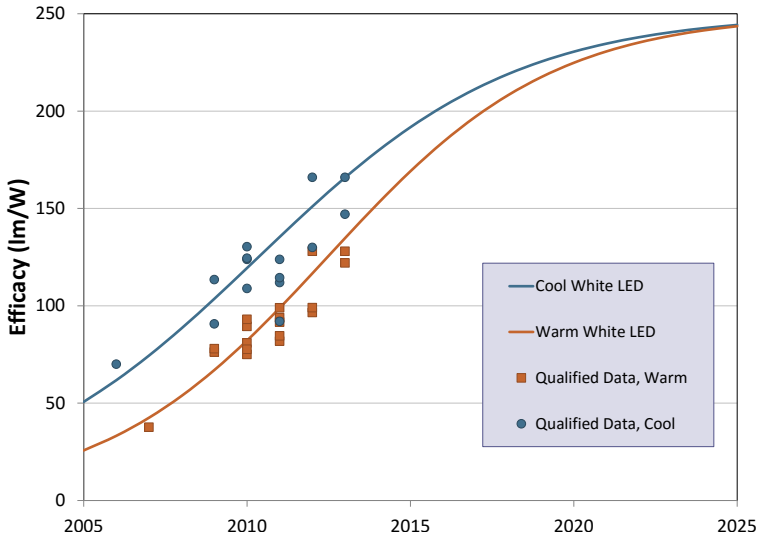


Figure 2: White-light phosphor-converted LED projections for commercial products. (BARDSLEY et al., 2014b).

Despite the evolution of the LEDs, the success of the Solid-State Lighting (SSL) systems also depends on the evolution of other components, such as the driver and the optical structure. Figure 3 shows the main parts of a typical street lighting LED luminaire. Next sections explore some characteristics of each element, starting from the main component: the LEDs.

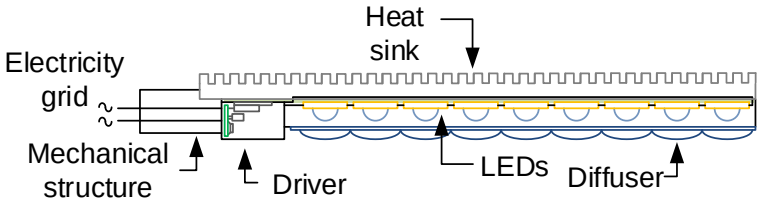


Figure 3: Main components of an LED luminaire.

1.2 LIGHT-EMITTING DIODES AS A LIGHT SOURCE

1.2.1 Working principle and characteristics

The light-emitting diodes are semiconductor devices composed by two layers, a P-type and a N-type. Its working principle is illustrated in Figure 4.

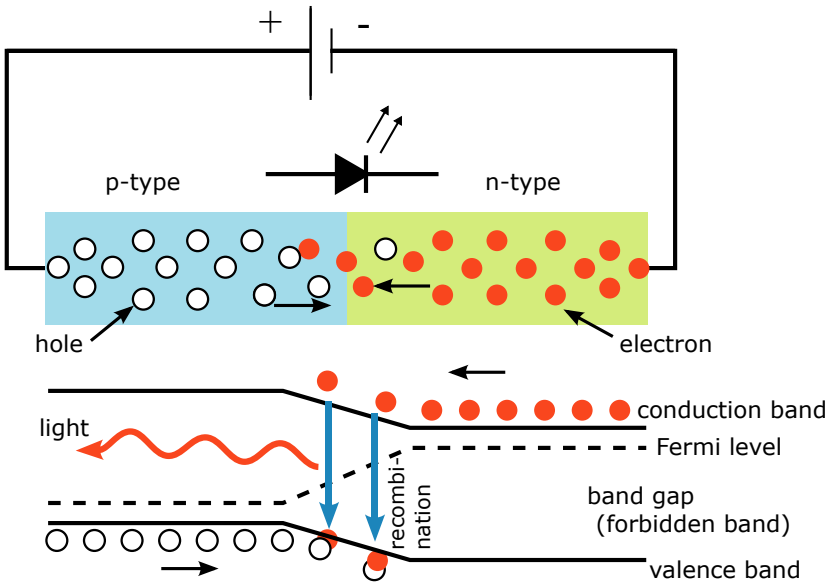


Figure 4: Diagram of a light emitting diode. (S-KEI, 2011).

When the P-N junction is polarized directly, there is a flow of electrons and holes. When the electron has enough energy to get through the PN junction, it goes from the conduction band to the valence band, recombining with a hole. Since there is an energy difference between the conduction band and the valence band, this process releases energy in the form of radiation and heat. The wavelength of the resultant radiation depends on the materials that are used in the semiconductor doping, since they influence in the energy difference between conduction and valence bands (SCHUBERT; GESSMANN & KIM, 2005).

The described operating principle reveals a very close relationship between the light emitted from an LED and current that circulates through it. Thus, it is possible to

state that the luminous flux produced by an LED is directly related to the electrical current of the device.

Although the electroluminescence[1] phenomenon has been reported since the experiment of Henry J. Round in 1907 (ROUND, 1907), the usage of LEDs in lighting applications only became viable with the advent of devices that emitted white light, as already commented. The most common ways to get white light through this semiconductor are by using a phosphor layer on the casing of the LED, which is the strategy used in the majority of lighting applications, or using Red-Green-Blue (RGB) devices, which are more common in architectonic applications and are not discussed in this work.

The phosphor-converted LEDs comprises semiconductors that emit a radiation with wavelengths around 470 nm (blue light) and a package covered with phosphorus. When photons pass through the above-mentioned coverage, there is a wavelength shift in part of the original radiation. Therefore, the combination of the original radiation (blue) and the shifted one (yellowish) gives rise to a device that emits white light. The described operation principle is illustrated in Figure 5a and the resulting emission spectrum of a phosphor-based white LED is presented in Figure 5b. It is important to highlight that the composition and the quantity of the phosphor is responsible for determining characteristics such as the correlated color temperature (CCT), the color rendering index (CRI) as well as the luminous efficacy (RODRIGUES et al., 2011a).

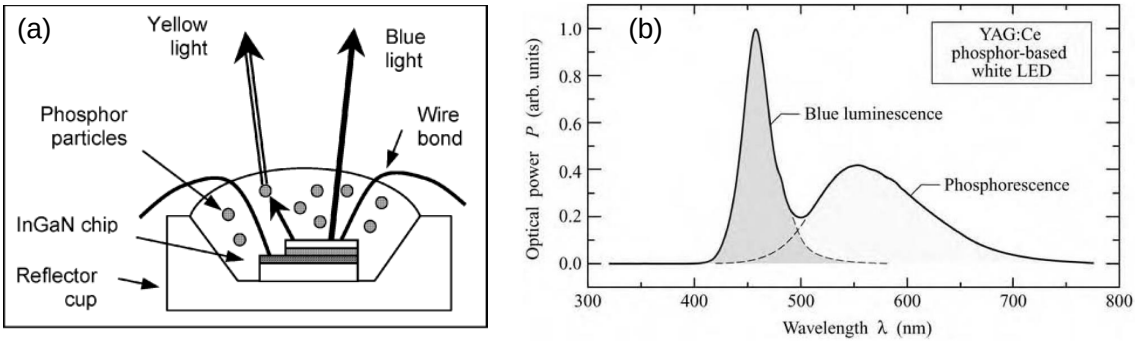


Figure 5: Phosphor-converted LED. (a) Working principle (SHUR & ZUKAUSKAS, 2005); (b) Emission spectrum (SCHUBERT; GESSMANN & KIM, 2005).

In general, the Phosphor-converted LED (PC-LED) technology has the potential of outperforming other lighting technologies (*e.g.*, High-pressure Sodium Lamps) and dominate the market. Globally, the Information Handling Services (IHS) Inc. estimates

[1]Electro-optic phenomenon in which a material emits light in response to the passage of an electric current or to a strong electric field.

that LED products accounted for 18 percent of lighting revenues in 2013, which corresponds to revenues of $16 billion (IHS, 2013). The main advantages of the LEDs over other technologies are the luminous efficacy, high CRI, several CCT values available, mechanical robustness and a long life span, which can reach 100,000 hours (SCHUBERT; GESSMANN & KIM, 2005)(TSAO, 2004)(RODRIGUES et al., 2011b).

1.2.2 Electrical Model

The use of an electrical model of the LED is quite suitable for designing an LED lighting system, since it allows for a theoretical prediction of the electrical behavior of the device. Bearing in mind that an LED is composed by a PN junction, its electrical behavior can be modeled in a similar way as a regular diode. Schubert, Gessmann and Kim (2005) shows the characteristic equation of an LED, which was derived from the Shockley equation as presented in (1.1).

$$V_{LED}\left(I_{LED}\right) = \frac{n_i k T_j}{q_e} \ln\left(\frac{I_{LED}}{I_s}\right) + R_s I_{LED}, \tag{1.1}$$

where:

n_i - ideality factor;

T_j - PN junction temperature;

R_s - parasitic series resistance;

I_s - saturation current;

k - Boltzmann constant($1.3806504 \cdot 10^{-23}$ J/K);

q_e - elementary charge of an electron ($1.602176487 \cdot 10^{-19}$ C).

Equation (1.1) presents a complete electrical model of an LED. Nevertheless, owing to the difficulty of obtaining the parameters of (1.1), it is more convenient to use a simplified model in some situations (*e.g.*, when designing an LED driver). This model can be obtained by linearizing (1.1) in the desired operating point. The resultant model can be represented as an ideal diode in series with a dc voltage source and a series resistance, as shown in Figure 6.

The model of Figure 6 can be described mathematically by

$$V_{LED}\left(I_{LED}\right) = V_T + r_d I_{LED}, \tag{1.2}$$

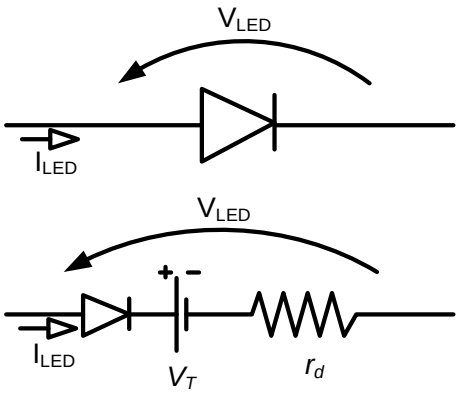


Figure 6: Piecewise linear model of an LED.

where:

V_T - threshold voltage;

r_d - dynamic resistance;

In order to compare the electrical models of the LED previously presented, a test with an LED OSRAM LUW W5PM-Golden Dragon was carried out. For this LED, the constant $(n_i \cdot k \cdot B \cdot T_j \cdot q_e^{-1})$ is equals to 165 mV, I_s has the value of 2.3 nA and R_s is 412 $m\Omega$ (ALMEIDA et al., 2011). Figure 7 shows the curves of the linear model (1.2) compared with the theoretical model (1.1) and the points obtained experimentally. For this LED, V_T and r_d are 2.96 V and 700 mΩ, respectively.

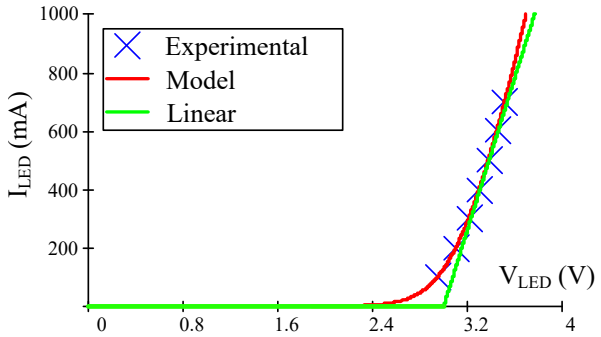


Figure 7: Comparison between the linear and the theoretical models of an LED as well as the points obtained experimentally.(ALMEIDA et al., 2011).

The next subsections deal with fundamental issues of SSL systems: the influence of the temperature, electrical power and the current waveform on the performance of the LEDs. Furthermore, a brief discussion regarding the human biologic effects of light flicker is presented.

1.2.3 Influence of the temperature and the electrical power on the optical performance of the LEDs

The heat sink shown in Figure 3 is the element responsible for managing the heat generated by the LEDs during the electroluminescence. The task performed by this component has a major importance for the performance of the whole SSL system, since the photometrical characteristics of the LEDs are closely related to the temperature in the PN junction.

Several works have reported the influence of the junction temperature in the photometric performance of the LEDs (GARCIA et al., 2008)(BIBER, 2008)(HUI & QIN, 2009)(YAN et al., 2011)(ALMEIDA et al., 2015a)(CHEN; TAO & HUI, 2012). Most of them have explored the drop of the luminous flux and luminous efficacy of the device according to the increase in the PN junction temperature. Additionally, Yan et al. (2011) reported that the phosphor temperature is also critical in determining the luminous efficacy.

The relationship between the luminous flux and the operating temperature of the devices is also reported in Garcia et al. (2008), in which an estimation of the luminous flux is developed based on measurements of the case and the ambient temperature. The experiments in this work shown good results of the proposed relationship, which proves the closer relationship between the photometric parameters and the operating temperature of the devices.

Biber (2008) presented a study of the relation between the heat sink parameters on the photometric performance of the LEDs. The aforementioned work showed several curves of the variation of the luminous flux according to the characteristics of the heat sink such as diameter, depth and volume. The results also shown that as the PN junction temperature decreases, the luminous flux of the devices increases.

Besides the temperature influence, the electric-optical conversion efficiency is also related to the average current that flows through the device. According to Chen, Tao and Hui (2012), the wall-plug efficiency[1] of an LED η_W depends on both the electrical power (P_d) and the PN junction temperature (T_j), as shown in (1.3).

$$\eta_W\left(T_j, P_d\right) = \frac{\left(\alpha T_j + \beta\right)\left(\chi P_d^2 + \delta P_d + \gamma\right)}{\mu}, \tag{1.3}$$

where α , β , χ, δ, γ and μ are constants that depend on the LED.

[1] conversion efficiency of a system that converts electrical power into optical power.

From (1.3), one can note that the wall-plug efficiency is linearly dependent on the PN junction temperature and has a quadratic relationship with the electrical power. Figure 8 shows an experimental evaluation of a Sharp 4.4 W LED (Model Number: GW5BNC15L02). Figure 8a shows the results of the variation in the heat sink temperature mantaining the electrical power constant and Figure 8b was gathered by varying the electrical power and keeping constant the heat sink temperature. One can see that both curves validate equation (1.3).

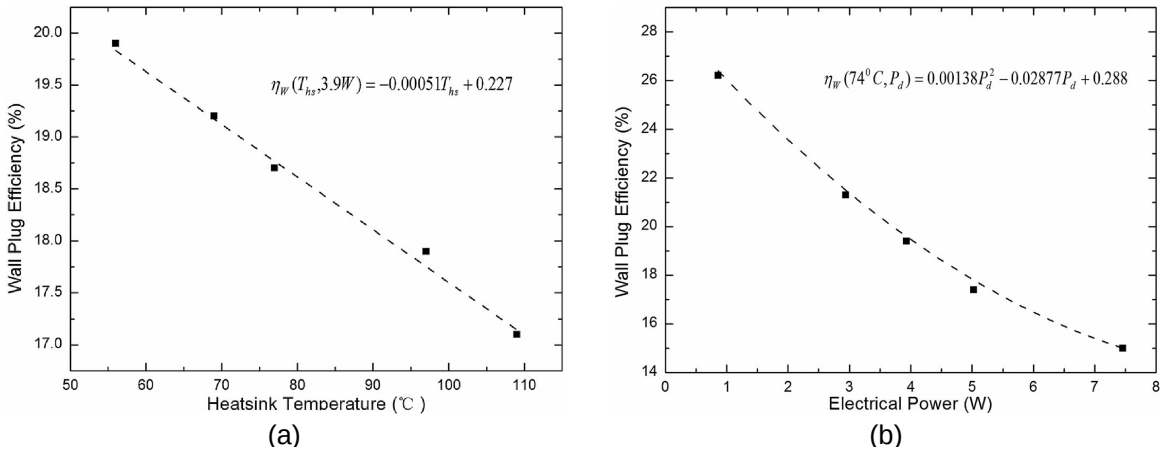


Figure 8: Wall-plug efficiency of a Sharp 4.4 W LED according to the heat sink temperature (at constant electrical power - 3.9 W) (a) and the electrical power (at constant heat sink temperature - 74 $°C$) (b). (CHEN; TAO & HUI, 2012).

Figure 9 shows the behavior of the flux and luminous efficacy according to variations in the average forward current of an LED Philips Lumileds LXML-PWN1 presented in Almeida et al. (2015a). For this experiment, six devices mounted on a heat sink with a thermal resistance of 4.39 $°C/W$ were used. Furthermore, the ambient temperature was controlled at 25 $°C$ by means of a heater inserted inside the experimental apparatus. One can note that the luminous flux saturates around 700 mA, indicating that, for the chosen heat sink, this current would be the maximum for ensuring a good relationship between the output flux and the electrical power.

1.2.4 Influence of the current waveform on the performance of the LEDs

Besides the average current and the temperature, the waveform of the LED's current also changes its photometrical performance (ALMEIDA; SOARES & BRAGA, 2013)(ALMEIDA et al., 2011)(ALMEIDA et al., 2015a).

Considering off-line applications, in which the driver is fed from the mains electricity, the current through the LEDs tends to assume a waveform similar to the one

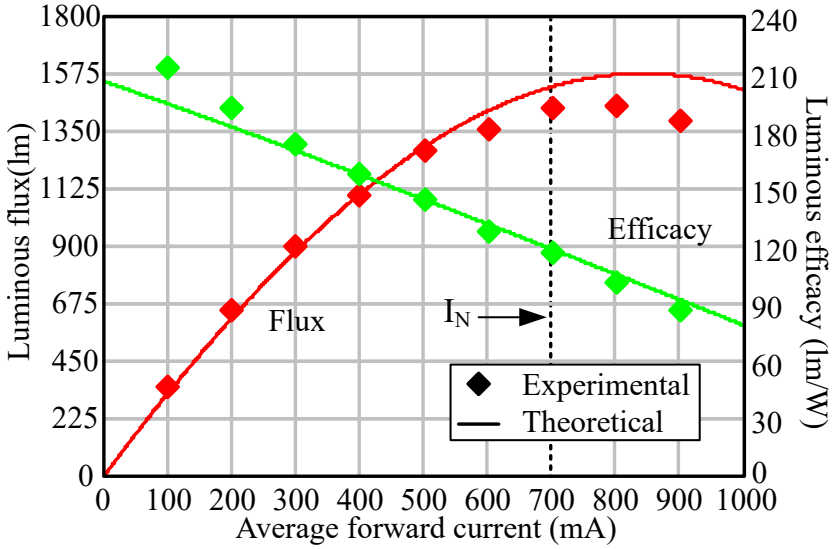


Figure 9: Behavior of the luminous flux and the efficacy of an LED Philips Limileds LXML-PWN1 according to variations in the average forward current. (ALMEIDA et al., 2015a)

presented in Figure 10, which was described in terms of a dc value I_o and a peak-to-peak ripple ΔI_o.

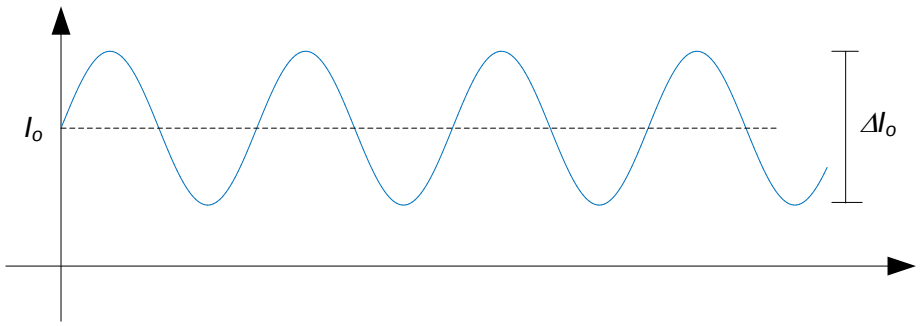


Figure 10: Typical current waveform at the LEDs in an off-line application.

The waveform shown in Figure 10 is characterized by a dc value and a Low Frequency Ripple (LFR) ΔI_o at twice the line frequency. Almeida, Soares and Braga (2013) and Almeida et al. (2015a) addressed the behavior of the luminous flux according the LFR. Figure 11 shows the photometrical performance of a Philips Lumileds LXK2-PWC4 LED string under such circumstances. One can note that a peak-to-peak ripple of 50% decreases the output luminous flux of the LEDs to about 98.5% of that of a pure dc current, a reduction that can be neglected in many LED applications.

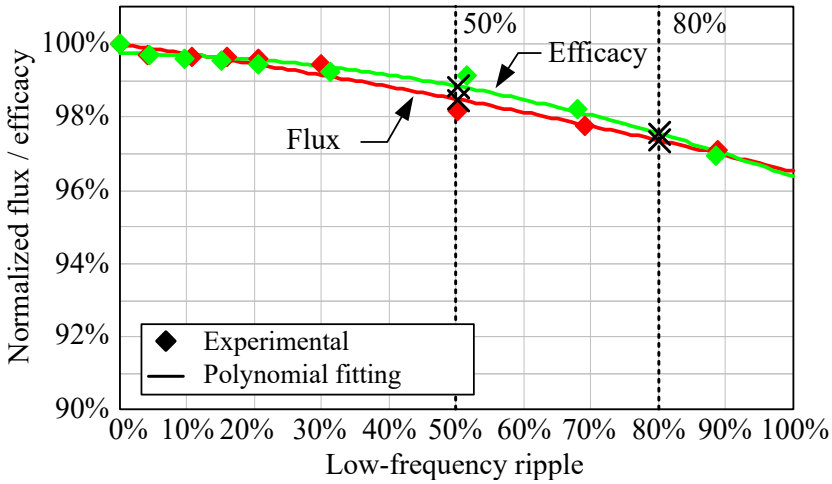


Figure 11: Degradation of the luminous flux and the efficacy of a Philips Lumileds LXK2-PWC4 LED string when a LFR is present. (ALMEIDA et al., 2015a).

1.2.5 Human biological effects of the light flicker

Some researchers have studied the human biological effects of the light flicker (LEHMAN & WILKINS, 2014; WILKINS; VEITCH & LEHMAN, 2010). In Lehman and Wilkins (2014), a literature review regarding the flicker effects is presented. The study showed that the if the flicker frequency is below 90 Hz, the luminance modulation can become hazard to health and can trigger headaches, migraines and even epileptic seizures. Furthermore, the aforementioned work also proposed that for flicker frequencies $f_{flicker}$ higher than 90 Hz, the percent flicker $Mod\%$ should satisfy the following:

- low-risk level: $Mod\% < 0.08 f_{flicker}$ - this choice will mitigate any distraction or negative biological effects caused by flicker;
- no-observable-effect level: $Mod\% < 0.033 f_{flicker}$

The percent flicker was defined in Wilkins, Veitch and Lehman (2010) as:

$$Mod\% = 100 \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \tag{1.4}$$

I_{max} and I_{min} represents the maximum and the minimum measured light intensities from the lamp. Since the light emitted by the LED is directly proportional to its current, the aforementioned conditions can be rewritten in terms of the peak-to-peak current ripple ΔI_{LED}, as shown in the following:

- low-risk level: $\Delta I_{LED} \leq 0.16 f_{flicker}$

- no-observable-effect level: $\Delta I_{LED} \leq 0.066 f_{flicker}$

For example, if $f_{flicker} = 120Hz$, the maximum peak-to-peak current ripple should be 19.2% and 7.9% for the low-risk and no-observable-effect levels, respectively.

Despite the fact that the aforementioned values can be used as a requisite for designing an LED lighting system, it is important to highlight that they are only a recommendation and, depending on the application, such limits could change. For example, High-pressure Sodium (HPS) lamps driven by magnetic ballasts has a percent flicker of approximately 100% and are often used without incidents regarding human health. According to Poplawski, Miller and FIES (2011), the flicker tolerance must be defined bearing in mind the characterisitcs of the application, such as the difficulty of the visual tasks.

1.3 LED DRIVERS

In order to maximize the benefits of the SSL technology, the LED driver must be designed to ensure a tightly-controlled current through the LEDs. This includes both the control of the average value and the limitation of the peak-to-peak current ripple. The latter could be a problem when the driver circuit is fed from the mains, since usually a large low-frequency ripple must be filtered to compensate the input-to-output instantaneous power imbalance (ALONSO et al., 2012). Other requirements for off-line LED driving include power factor correction and high efficiency.

It was shown in section 1.2 that the photometrical performance of the LEDs is not only directly related to the thermal management of the devices, but also to the nature and regime of the current that flows through them.

Therefore, for most applications, it is mandatory to keep the current ripple of the LEDs within a certain limit, thus guaranteeing that the light output achieves the desired performance whereas also avoiding stroboscopic and flickering effects, which could be noticeable to the human eye in some circumstances (LEHMAN & WILKINS, 2014).

The task of low-frequency ripple filtering is normally accomplished by using bulky storage elements, usually electrolytic capacitors, which are known to reduce the driver life span, or alternatively by using a bank of metalized film capacitors, which have better life span, but decrease the power density of the drivers (WANG & BLAABJERG, 2014). This could be a problem in applications where the available space for the

electronic driver is limited. Another solution consists in using higher temperature long-life electrolytic capacitors, which are much more expensive than conventional ones.

Therefore, the development of LED driving techniques aiming to the reduction in the required filtering capacitances is relevant and have recently been addressed by some researchers.

Despite the above-mentioned mandatory characteristics, the LED driver must be as simpler as possible in order to increase the economic attractiveness of the SSL systems. In fact, the reduction of the cost of the driver is a tendency among the manufacturers (BARDSLEY et al., 2014a).

Besides the use of a driver with a low component count, there are other ways to reduce the cost of this element. One of them is the reduction of the production costs by the use of products that cater to a wider range of applications, leading to a higher production scale (RASMUSSEN, 2012). Regarding the LED drivers, this characteristic can be achieved by designing the device to operate in a wider range of input voltages, since it allows for the application of the product in regions with different mains voltage characteristics. As can be seen in Figure 12, the domestic mains voltage in which the driver must operate varies dramatically worldwide. This variation can occur even in the same country, *e.g.,* Brazil.

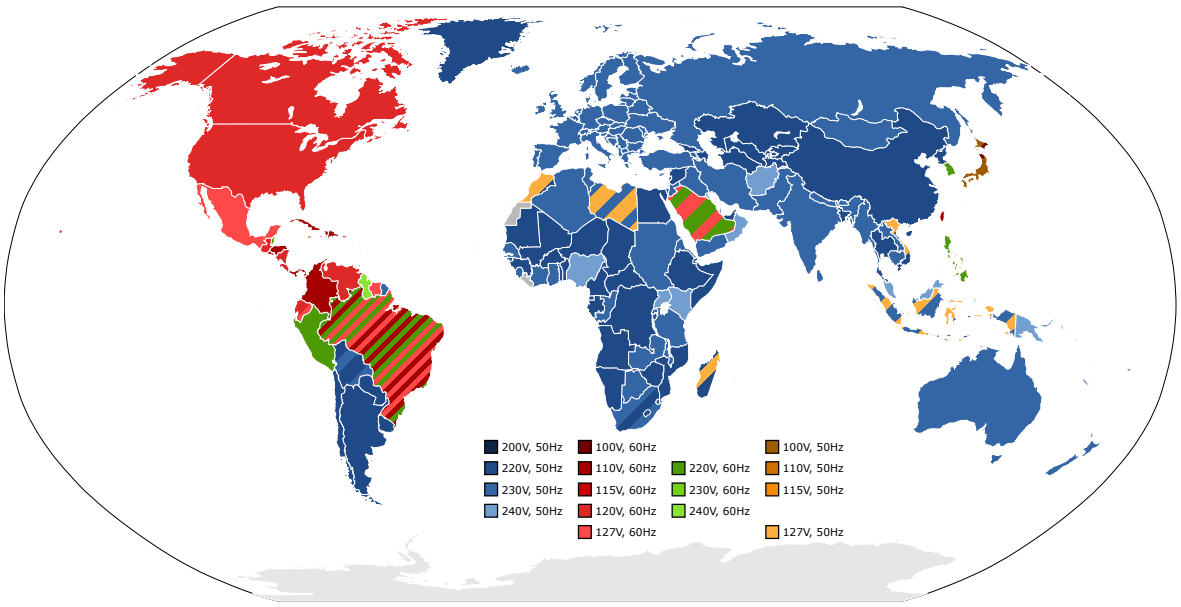


Figure 12: Countries of the world, colored according to their domestic nominal power net voltage and frequency. (SOMNUSDE, 2009)

1.4 CONTENT OF THE WORK

Based on the discussions of the last sections, this work proposes some contributions in LED driving, focusing on LED drivers with reduced storage capacitances.

However, before proposing an alternative for LED driving, some concepts regarding single phase power factor correction are addressed in chapter 2, in which some classical topologies and control techniques are discussed.

In chapter 3 some known capacitance reduction techniques are revisited. The characteristics of the technologies of capacitors are also outlined in this chapter.

Based on the requirements presented in chapter 1 and on the techniques shown in chapters 2 and 3, a novel strategy for capacitance minimization in off-line LED drivers, called Active Ripple Compensation (ARC), is presented in chapter 4. The technique is based on a controlled modulation of the duty cycle in a VMC converter so that the output LFR can be actively reduced. The proposed approach is applied to two converters: a single-stage topology (Flyback) and a two-stage converter (Double Buck-boost). For each case, a complete mathematical description as well as experimental results are presented.

Chapter 5 presents a generalization of the proposed technique by means of a design strategy based on an optimization approach. The generalized study comprises the application of the ARC technique in four different topologies for several design conditions.

An alternative implementation of the ARC technique is addressed in Chapter 6. In this strategy, the ripple compensation is performed by means of a classical proportional-integral controller, which must be designed simultaneously with the converter elements. As performed in Chapter 5, the design procedure was also modeled as an optimization problem so that all the requisites of the application could be met.

Finally, chapter 7 presents the final considerations of this work and discusses some proposals for future works.

2 SINGLE PHASE POWER FACTOR CORRECTION TECHNIQUES

As presented in the previous chapter, the LED is a direct current (dc) load. Therefore, in order to connect these devices to the distribution grid, it is necessary to use a driver performing the alternating current (ac) to dc conversion. However, depending on the technique used to design this driver, some problems arising from this conversion can appear. Most of them are related to harmonic pollution of the grid and low power factor, which are problems that could dramatically decrease the power quality of the distribution systems and increase the losses in the power transmission process.

In order to avoid such disadvantages, several organizations and institutes have been developing standards and recommendations that address this issue, establishing some criteria to design and analyze off-line converters. Most of them propose limits for the amplitudes of the input current harmonic components and even regulate about power factor of such devices. Regarding lighting equipments, it is possible to highlight the IEC-61000-3-2:2014 (IEC, 2014) as one of the most important publications on this topic, serving as a normative base for other several standards, such as the Brazilian NBR-16026 (ABNT, 2012). A brief review of these standards is presented in the next section of this chapter.

In order to ensure the compliance of the driver with the aforementioned standards, a power factor correction technique can be used. Therefore, it is suitable to revisit some power factor correction approaches applied to LED drivers. The analysis outlined in this chapter aims to present the main topologies, design strategies and even control techniques that can be applied to single phase PFC pre-regulators, addressing the characteristics and the main issues regarding each one.

2.1 POWER FACTOR CORRECTION STANDARDS

Recently, the Brazillian Association of Technical Standards (Associação Brasileira de Normas Técnicas) (ABNT) published a standard with recommended performance

parameters for LED drivers: the NBR-16026. This standard establishes that the power factor of the input current of the LED driver must be higher than 0.92 for devices whose the nominal power is greater than 25 W. Regarding the limits for harmonic current emissions, the NBR-16026 states that the input current of the driver must be in compliance with the limits established in the IEC-61000-3-2:2014 Class C: lighting equipment.

Table 1 shows the harmonic limits established by table 2 of the standard IEC-61000-3-2:2014. This table presents the limits for class C equipments, which is the classification assigned to lighting devices according to the aforementioned standard.

According to IEC-61000-3-2:2014 standard (IEC, 2014), there is a relaxation for high order harmonics that can be applied to the odd harmonic currents from the 21st to the 39th. It allows these high order harmonics to exceed the limits established in Table 1 but not exceeding 150 % of its individual limit. However, for these cases, the Partial Odd Harmonic Current (POHC), defined by (2.1), must be calculated. If the measured POHC is lower than the POHC limit, the relaxation is allowed, otherwise, it is not. The POHC limit can be calculated by applying the values of Table 1 in (2.1), which yields about 9.5 % of the fundamental current.

Table 1: Limits of harmonic emission of Class C equipment according to the IEC-61000-3-2:2014.

Order	Maximum allowable current (Normalized to the fundamental)
2	2 %
3	30λ[1] %
5	10 %
7	7 %
9	5 %
$11 < n < 39$	3 %

$$POHC = \sqrt{\sum_{n=21,23}^{39} I_n^2}. \tag{2.1}$$

where:

I_n - magnitude of the nth harmonic component.

[1]Measured power factor

In Brazil, the government has published several ordinances in order to prevent the commercialization of low quality products. Regarding the street lighting devices, the Instituto Nacional de Metrologia, Qualidade e Tecnologia (INMETRO) ordinance number 20 (INMETRO, 2017) determines that the LED drivers must comply with IEC-61000-3-2:2014 and must have a power factor greater than 0.92. On the other hand, the ordinance number 144 (INMETRO, 2015) states that lamps with an input power between 5 and 25 W must have a power factor greater than 0.70 whereas the devices with less than 5 W do not have any power factor constraint.

Therefore, the use of a power factor correction technique in LED drivers is mandatory. Some techniques are presented in the next sections of this chapter.

2.2 PASSIVE POWER FACTOR CORRECTION TECHNIQUES

Among the most simple PFC techniques are the strategies involving the use of passive pre-regulators. Such approaches rely on topologies which have only inductors, capacitors and diodes.

The advantages of passive power factor correction is the simplicity of the circuits and sometimes the robustness. However, all of them presents a relevant drawback: the size of the capacitors and the magnetic components are normally much larger than the active PFC converters. Furthermore, since the passive PFC converters normally operate in open-loop, the output variable (*e.g.*, output current) is unregulated and can dramatically vary with the input voltage and the values of the elements of the circuit.

2.2.1 Applications of passive pre-regulators in HPF LED drivers

Several works have addressed the use of passive HPF LED drivers (HUI et al., 2010)(LEE et al., 2011)(LEE et al., 2015). The main advantages cited by the authors are the high efficiency, simplicity, long lifetime and low cost of the passive topologies. However, the use of bulky passive elements can be verified in those works. This occurs because the passive drivers operate in low frequencies (normally twice the line frequency). Therefore, the inductors and capacitors of the converter must be sized to filter low-frequency currents and voltages, which dramatically increases the size of such elements.

An example of the use of HPF passive circuits in LED drivers can be seen in Hui et al. (2010), which presents a high power factor passive LED driver based on a modified

valley-fill structure. The topology of this driver is shown in Figure 13. Experimental results were presented in the aforementioned work showing a good performance of the circuit for driving a 50-W LED load. Some waveforms can be observed in Figure 2. The results showed that a power factor of 0.99 and a efficiency of 93% can be achieved with the passive LED driver. Despite these good results, the usage of this approach could be unfeasible in applications in which the available space is limited, since the converter needs bulky inductors ($L_s = 1.47$ H and $L = 1.9$ H).

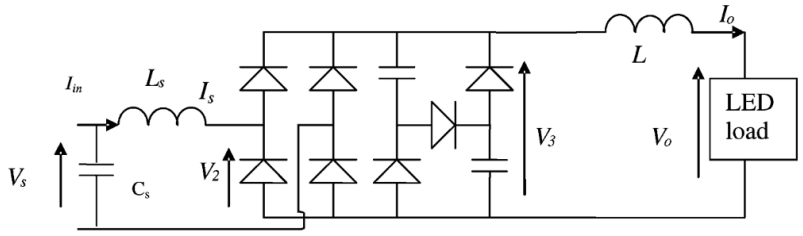


Figure 13: Passive LED driver proposed in (HUI et al., 2010).

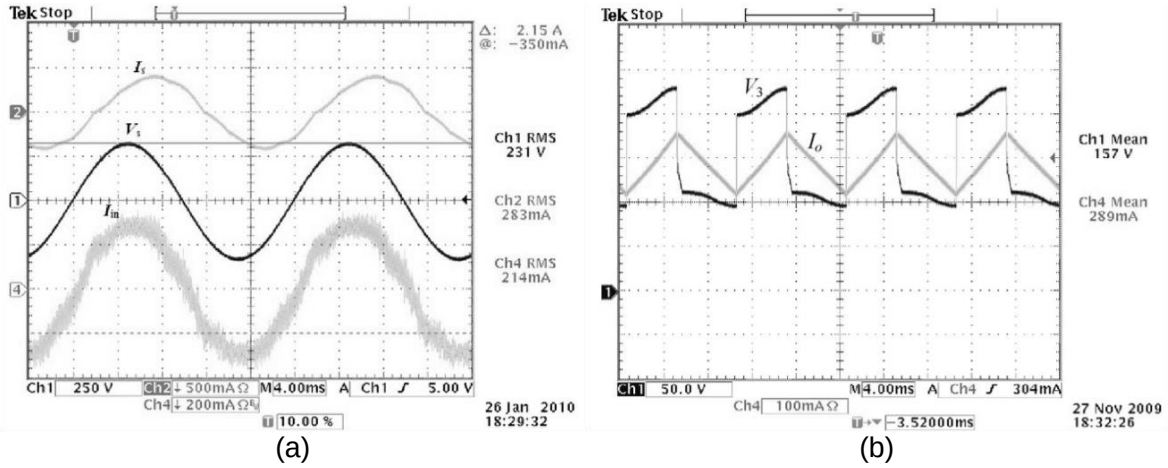


Figure 14: Some waveforms of the passive LED driver proposed in (HUI et al., 2010).(a) Input waveforms: I_s(CH2 - 0.5A/div), Vs(CH1 - 250V/div) and I_in(CH2- 0.5A/-div);(b)Output waveforms: I_o(CH4 - 0.1A/div), V_3(CH1 - 50V/div).Timescale:4ms.

2.3 ACTIVE POWER FACTOR CORRECTION TECHNIQUES

Although the use of passive PFC pre-regulators is suitable for some applications, the majority of LED lighting systems require the use of an active power converter, which allows a tight output voltage or current regulation as well as a reduced size. Regarding the active PFC pre-regulators, there are different techniques presented in the literature, and each one has advantages and drawbacks that must be analyzed by the designer.

Considering only PFC strategies for LED lighting applications, the use of a DC-DC converter is suitable in most cases, since the nominal power of the luminaires is normally lower than 500 W. Regarding the conventional DC-DC PFC pre-regulators, there are two control topologies: current-mode control (CMC) and voltage-mode control (VMC). Each of these control approaches has different characteristics that provides advantages for some applications and disadvantages for others. The next topics present each one of these PFC approaches, focusing on their application in off-line LED drivers.

2.3.1 Power factor correction with current-mode controlled converters

The current-mode controlled PFC pre-regulators are based on the direct control of the converter input current. The CMC techniques can be classified in two types: fixed switching frequency and variable switching frequency. The first one is normally applied in converters operating in Continuous Conduction Mode (CCM) whereas the second is used in converters operating in the Boundary Conduction Mode (BCM).

2.3.1.1 Fixed-frequency CMC

The main implementations of the fixed-frequency CMC are the average CMC and the peak CMC. Figures 15 and 16 shows the control topologies of each one applied to a Boost PFC.

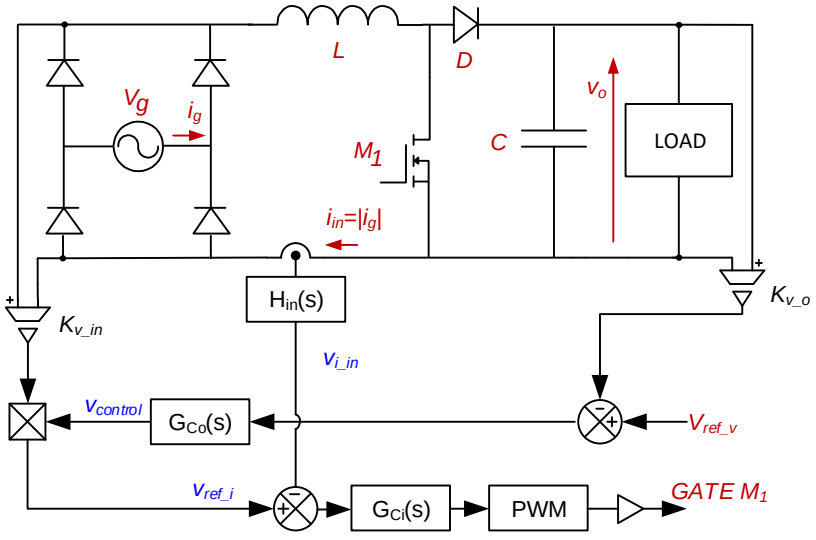


Figure 15: Typical schematic of a PFC boost with average CMC.

As can be seen in the schematics, both control topologies rely on two control loops. The inner loop (also known as current loop) is responsible for controlling the input

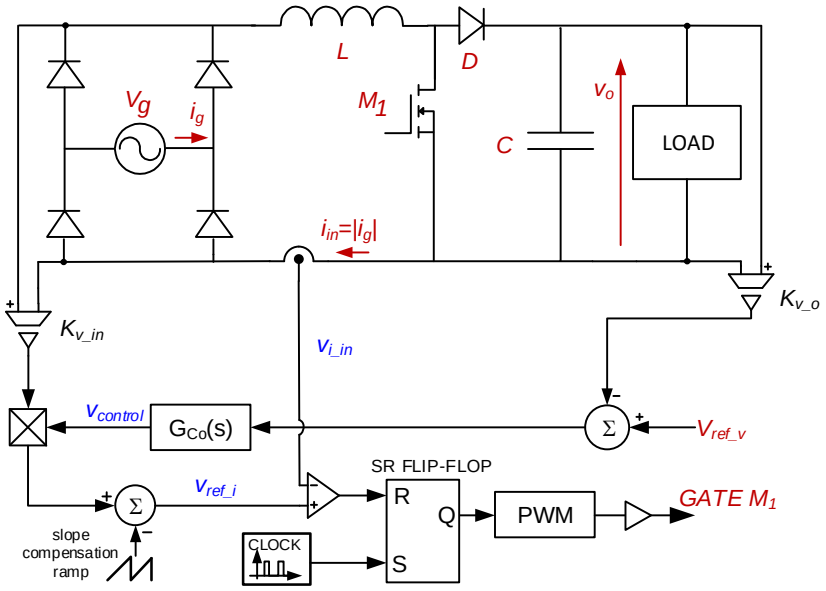


Figure 16: Typical schematic of a PFC boost with peak CMC.

current of the converter. In PFC converters, this loop must ensure that the input current of the converter follows the line voltage so that a HPF can be achieved. On the other hand, the outer loop (also known as voltage loop) controls the output variable so that it remains in the desired value and is immune to disturbances.

In order to achieve a HPF, the reference signal for the inner loop is normally synthesized from the multiplication of the measured input voltage of the converter and the output of the outer loop. This strategy makes the inner loop reference directly related to the input voltage waveform, which in this case is a rectified sinusoid. On the other hand, the outer loop controls the amplitude of such reference signal and consequently the power processed by the converter.

The differences between the two CMC approaches rely on the current loop. The average CMC uses a classical control structure in the inner loop, in which a compensator $G_{Ci}(s)$ is used to nullify the current error. The name average CMC derives from the fact that the control variable of the current loop is the average value of the measured current (obtained from a sensor $H_{iin}(s)$) in the inner loop.

On the other hand, the peak CMC is based on a circuit that forces the peak of the measured current to be equal to the current reference. In this case the control variable is the instantaneous value of the input current. The main components of the peak CMC are a clock source, a comparator and a Set-Reset flip-flop. As can be observed in Figure 16, the clock signal is responsible for turning on the main switch of the converter whereas the comparator turns the MOSFET off when the measured current is equals

to v_{ref_i}. Owing to this operating principle, in which the peak of the measured current is forced to be equal the reference current, this strategy is called peak CMC.

One can note that the peak CMC circuit have a slope compensation ramp, as shown in Figure 16. This scheme is used to prevent subharmonic oscillations on the current of the inductor and to ensure the circuit stability (ERICKSON & MAKSIMOVIC, 2001).

Despite the differences of the inner loop, both strategies have the same mechanism for correcting the power factor of the converter. By analyzing the outer loop of Figures 15 and 16, the value of v_{ref_i} can be found. This value is presented in (6.20).

$$v_{ref\_i} = v_{control} \times K_{v\_in}|v_g| \tag{2.2}$$

where:

$v_{control}$ - output signal of the outer loop;

K_{v_in} - gain of the input voltage sensor;

v_g - input voltage, defined in (2.3) in terms of its peak value V_G and the line frequency ω_L.

$$v_g(t) = V_G \sin(2\omega_L t) \tag{2.3}$$

Considering that the controller $G_{Ci}(s)$ is tunned properly, the input current i_g can be considered equal to v_{ref_i}, as stated in (2.4). The same statement can be done for the peak CMC if the high-frequency current ripple of i_g is small, which is a reasonable consideration since the converter is operating in CCM. Equation (2.4) also considers that the current sensor has a unity gain.

$$|i_g| = v_{ref\_i}. \tag{2.4}$$

In order to evaluate the PFC performance, it is suitable to define the emulated resistance of the boost converter:

$$R_{boost} = \frac{|v_g|}{|i_g|}. \tag{2.5}$$

By replacing (6.20) and (2.4) in (2.5), one can obtain the emulated resistance for a CMC boost PFC pre-regulator:

$$R_{boost\_cmc} = \frac{1}{K_{v\_in} v_{control}}. \tag{2.6}$$

Therefore, if the signal $v_{control}$ is constant within a line period, the converter will emulate a pure resistance, providing a high power factor for the system.

The assumption that $v_{control}$ is constant within a line period can be implemented by tunning the voltage loop controller with a limited bandwidth, so that the high-order harmonics of the error signal are filtered by the compensator and do not appear in $v_{control}$. Therefore, the design of the outer loop, which is originally devised to control the output variable, also has a direct impact on the PFC performance.

2.3.1.2 Variable-frequency CMC

The use of PFC pre-regulators operating in BCM is suitable for powers lower than 300W. Among the advantages of this operation mode in relation to the CCM, one can highlight the zero current switching (ZCS) feature, which could provide a higher efficiency level for the system (KIM; YI & CHO, 2014). Figure 17 presents a typical implementation of the CMC in a PFC boost operating in BCM. Some theoretical waveforms regarding the input variables are shown in Figure 18.

The schematics of the variable-frequency CMC presented in Figure 17 is similar to the one shown in Figure 16. The main difference is that the controlled switch is turned on by a zero cross detector (ZCD) circuit instead of a clock signal. This characteristic implies that the switching frequency varies according to the line voltage and also with the load.

One can note in Figure 17 that the peak of the input current $i_{g\_pk}(t)$ is controlled by the outer loop. Therefore:

$$i_{g\_pk} = K_{v\_in} |v_g| v_{control}. \tag{2.7}$$

The instantaneous average value of the input current $\langle i_g \rangle_{T_s}(t)$ is defined in (2.8).

$$\langle i_g \rangle_{T_s}(t) = \frac{1}{T_s} \int_0^{T_s} i_g(t) dt = \frac{1}{T_s} \left(\frac{i_{g\_pk}(t) \cdot T_s}{2} \right) = \frac{1}{2} i_{g\_pk}(t). \tag{2.8}$$

The emulated resistance can be calculated using (2.5), (2.7) and (2.8), yielding(2.9).

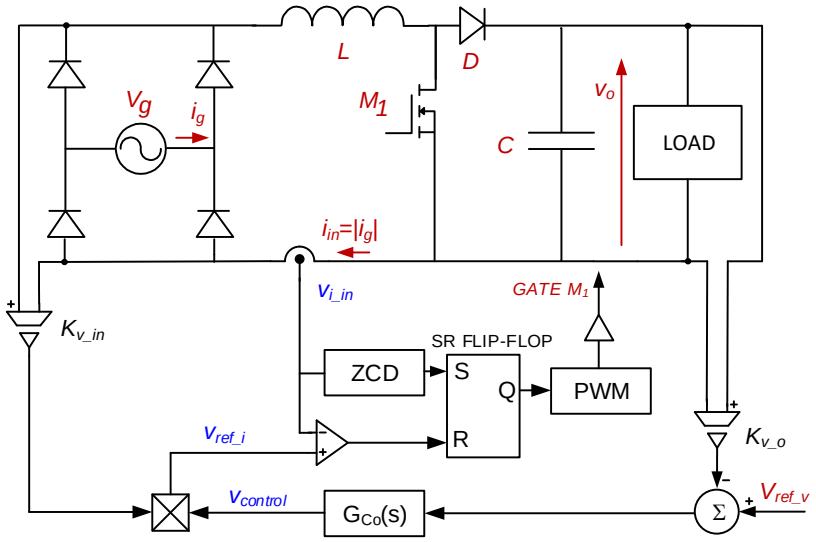


Figure 17: Typical schematic of a PFC boost operating in BCM with CMC.

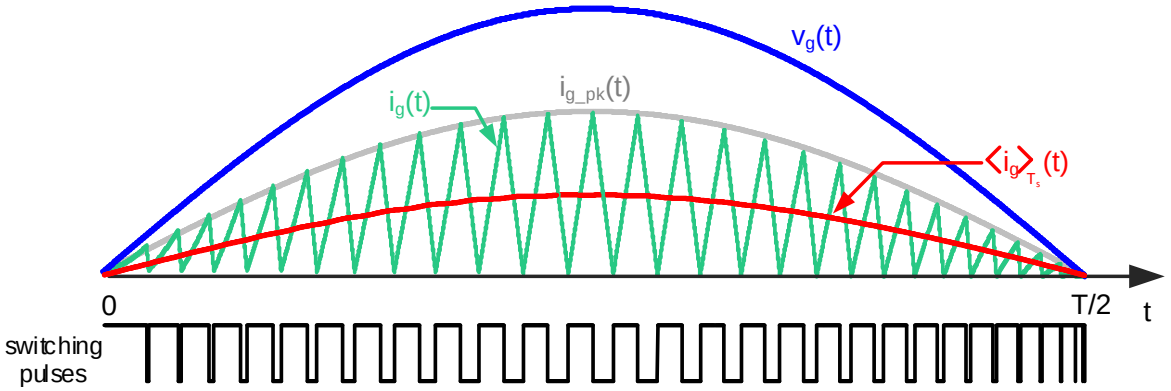


Figure 18: Theoretical waveforms of the BCM boost PFC.

$$R_{boost\_bcm} = \frac{2}{K_{v\_in} v_{control}}. \tag{2.9}$$

Equation (2.9) is similar to (2.6), therefore, the considerations of section 2.3.1.1 regarding the bandwidth of the outer control loop are also valid.

2.3.1.3 Applications of CMC pre-regulators in LED drivers

The use of CMC PFC pre-regulators in LED lighting applications have been related in some works (YIM et al., 2013)(JIA; LIU & FANG, 2015)(QU; WONG & TSE, 2010)(CHIU et al., 2010). Owing to the characteristics of the LED drivers, in which the wattage is normally lower than 300W, the most common CMC technique is the variable-frequency.

The aforementioned strategy is normally used in the PFC stage of two-stage LED drivers. Furthermore, there are several commercial products that are based on BCM current-mode controlled PFC pre-regulators (FAIRCHILD, 2011)(STMICROELECTRONICS, 2012)(NXP, 2012).

Chiu et al. (2010) presents an LED driver based on a BCM current-controlled SEPIC pre-regulator and linear current equalizers. Figure 19 shows the schematics of the proposed driver. In the aforementioned work, the outer loop has an adaptive voltage reference. This strategy is used to minimize the losses in the linear current regulators so that if the voltage drop on these devices rises, the voltage reference for the PFC pre-regulator is decreased. This approach ensures that the voltage drop on the current regulators stay controlled and the global efficiency of the circuit is maximized.

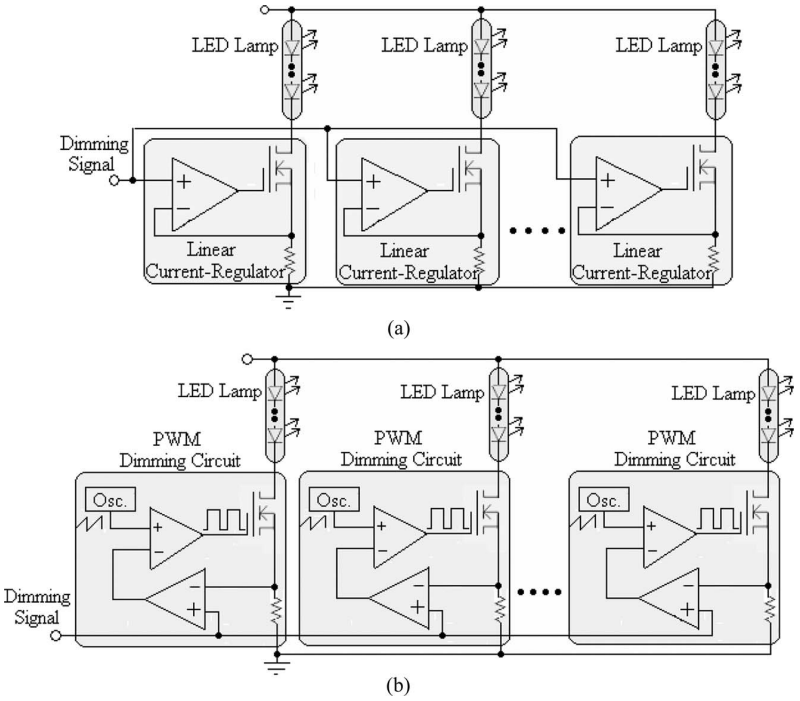


Figure 19: Schematics of an LED driver based on a BCM current-controlled SEPIC pre-regulator and linear current equalizers (CHIU et al., 2010).

Figure 20 shows some experimental results of the PFC pre-regulator, in which is possible to observe that the BCM current-controlled SEPIC pre-regulator meets the requirements of the IEC-61000-3-2:2014 standard.

2.3.2 Power factor correction with voltage-mode controlled converters

The VMC power factor pre-regulators are characterized by the simplicity of their control system, since a single control loop is used. However, since there is no current

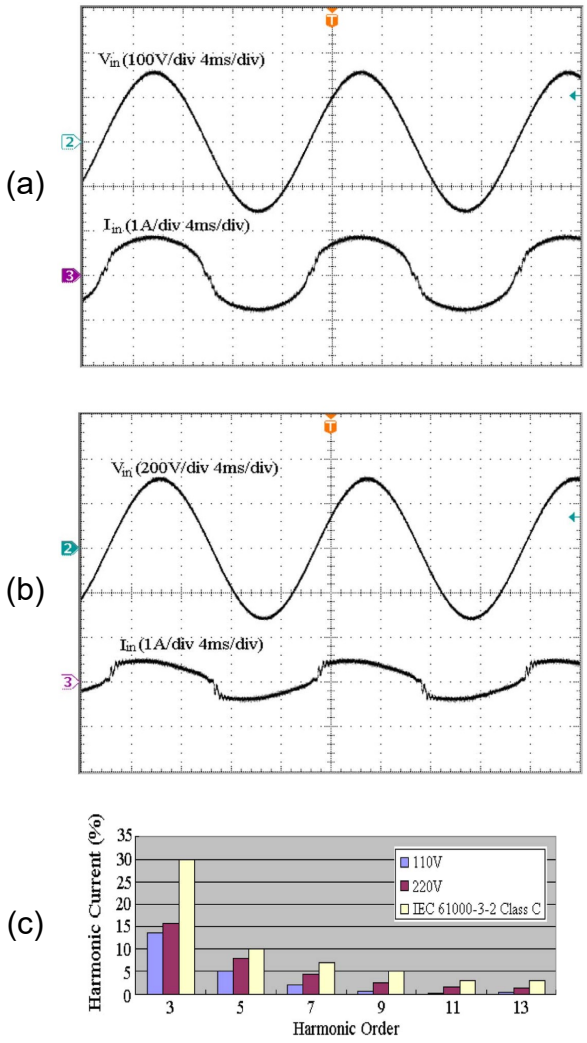


Figure 20: Experimental results of the PFC pre-regulator presented in Chiu et al. (2010). Measured input current waveforms at (a) 110V and (b) 220V. (c) Measured input current harmonic.

loop, these pre-regulators are designed to operate in DCM so that an intrinsic power factor correction can be obtained.

The drawbacks of the VMC PFCs are related to the disadvantages of the DCM, which are the high current stresses on the semiconductors and the demand of a bulky electromagnetic interference (EMI) filter in order to comply with standards such as the CISPR22 (IEC, 2008). However, these drawbacks do not represent major problems in low-to-mid power applications, in which the majority of the LED drivers are situated.

The PFC pre-regulators that operate in DCM behave like voltage-followers and this characteristic allows them to have a HPF in their input. However, depending on the topology, it is not possible to have a sinusoidal current at the converter input. On the other hand, there are converters that can theoretically achieve a perfect sinusoidal

current at its input. Among the topologies that have not a sinusoidal current at the input when operating in DCM are the boost and the buck-type topologies. On the other hand, the buck-boost type topologies can achieve a unity power factor when operating in DCM. The aforementioned topologies are outlined in the next subsections.

2.3.2.1 VMC boost PFC pre-regulator

The voltage-mode controlled boost PFC is shown in Figure 21. As can be observed in the figure, the VMC used in this PFC pre-regulator is much simpler than the CMC approach, shown in subsection 2.3.1, mainly because it operates in DCM.

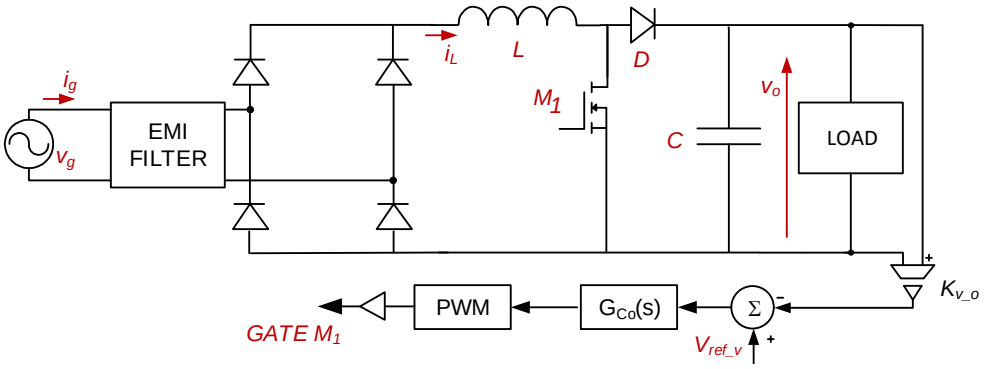


Figure 21: VMC boost PFC pre-regulator

According to Wei and Batarseh (1998), the input current i_g of the PFC boost operating in DCM is given by (2.10). This expression considers that the EMI filter suppress all the switching components of $i_g(t)$. This consideration will be assumed for all the analyses outlined in this section.

$$i_g(t) = \begin{cases} \frac{D^2 T_s}{2L}\left(\frac{|v_g(t)|V_o}{V_o - |v_g(t)|}\right), if\ v_g(t) > 0 \\ -\frac{D^2 T_s}{2L}\left(\frac{|v_g(t)|V_o}{V_o - |v_g(t)|}\right), if\ v_g(t) \leq 0 \end{cases}, \tag{2.10}$$

where:

D - duty-cycle;

T_s - switching period ;

L - inductance;

V_o - output voltage;

$v_g(t)$ - mains voltage.

Equation (2.10) is valid only if the boost converter is operating in DCM. This

condition is fulfilled if the duty cycle of the converter is lower than the critical duty cycle, defined in (2.11).

$$D_{c\_boost} = 1 - \frac{V_G}{V_o}. \tag{2.11}$$

By analyzing (2.10) considering the switching period and the duty-cycle constant, it is possible to note that the input current of the boost converter tends to a pure sinusoid as the output voltage increases and become distorted as this variable get closer to the input voltage. Therefore, the amplitude of the harmonic components of the boost converter depends on the value of the output voltage.

Figure 22 shows typical waveforms of the PFC boost operating in DCM. Almeida (2014) showed that the harmonic components of the input current of the boost PFC operating in DCM can be modeled as function of a static gain $M_{boost} = V_o/V_G$. Figure 23 shows the behavior of some parameters of the input current according to variations in M_{boost}.

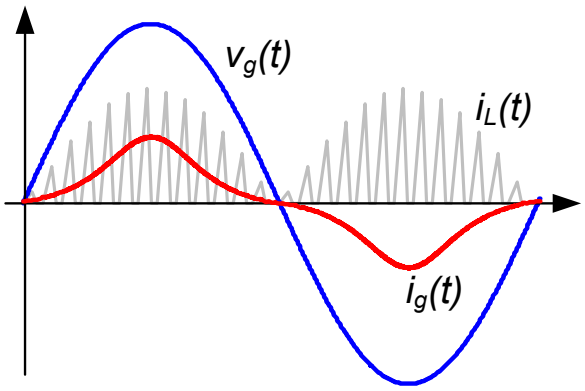


Figure 22: Typical waveforms of the boost PFC operating in DCM

Figure 23a shows the behavior of the THD and the PF according to M_{boost} whereas Figure 23b shows the behavior of the harmonic content of the input current and the limits regarding the IEC-61000-3-2:2014 standard. As can be observed in Figure 23b, the converter only meets the requirements of the aforementioned standard if the static gain M_{boost} is larger than 1.27. This means that the output voltage must be at least 395 V when the mains voltage is 220V (*i.e.*, $V_G = 311$) to ensure the compliance with the IEC-61000-3-2:2014 standard.

It is important to highlight that the output voltage ripple can influence the power factor correction performance of the boost-type PFC pre-regulators. Therefore, such influence must be taken into account for the analysis of the circuit if the voltage ripple

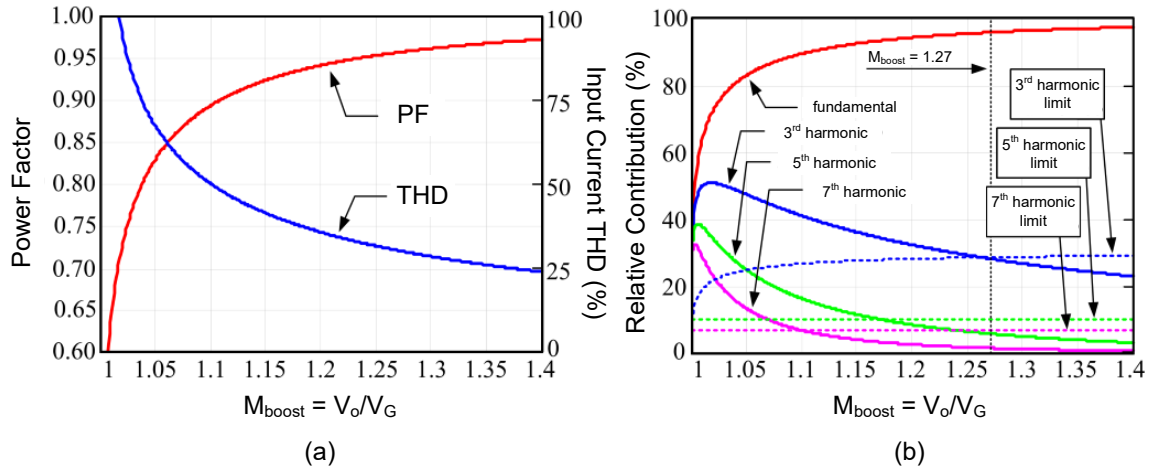


Figure 23: Curves of the input parameters of the PFC boost operating in DCM according to variations in the static gain M_{boost}. (a) Curves of PF and THD. (b) Curves of the harmonic components of the input current. Adapted from Almeida (2014).

is high, a typical condition in applications that aims capacitance reduction.

2.3.2.2 *VMC buck-type PFC pre-regulators*

The buck-type pre-regulators include the buck converter and its derivatives, such as the forward converter. Figure 24 shows a voltage-mode controlled buck PFC system.

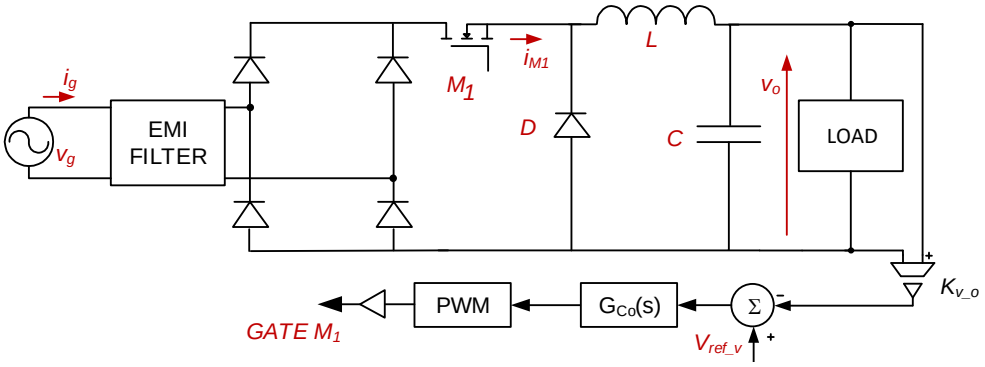


Figure 24: VMC buck PFC pre-regulator

The input current i_g of the buck converter operating in DCM is given by (2.12)(WEI & BATARSEH, 1998). This equation is valid only if the converter is operating in DCM, that is, its duty-cycle must be lower than D_{c_buck}, defined in (2.13).

$$i_g(t) = \begin{cases} \frac{D^2 T_s}{2L}\left(|v_g(t)| - V_o\right), \; if \; |v_g(t)| > V_o \; and \; v_g(t) > 0 \\ -\frac{D^2 T_s}{2L}\left(|v_g(t)| - V_o\right), \; if \; |v_g(t)| > V_o \; and \; v_g(t) < 0 \\ 0 \qquad\qquad\qquad\qquad\qquad , \; if \; |v_g(t)| \leq V_o \end{cases}, \tag{2.12}$$

$$D_{c\_buck} = \frac{V_o}{V_G}. \tag{2.13}$$

As verified in the boost converter, the input current of the buck topology operating in DCM also depends on its output voltage. As can be seen in (2.12), the smaller the value of V_o, closer to a pure sinusoidal the input current i_g is. Furthermore, since the output voltage of a buck converter never exceeds its input voltage, when the $|v_g(t)|$ falls below the output voltage V_o, the input current is zero. Figure 25 shows typical waveforms of the PFC buck operating in DCM.

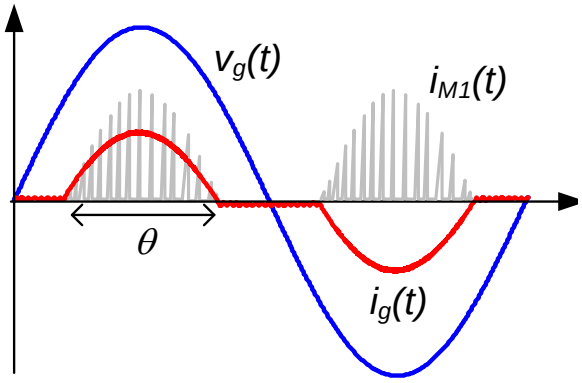


Figure 25: Typical waveforms of the buck PFC operating in DCM

As can be observed in Figure 25, the period in which the input current is not zero was defined as θ (conduction angle). As shown in DALLA COSTA et al. (2008), it is possible to evaluate the input power factor and the THD in terms of the angle θ, whose definition is given by (2.14). Figure 26 shows the behavior of these parameters for several values of θ.

According to DALLA COSTA et al. (2008), the DCM buck pre-regulator must have a conduction angle of $\theta = 130^o$ to meet the requirements of the IEC-61000-3-2:2014 Class C, leading to a PF = 0.96 and a THD = 29%. This means that if the mains voltage is 220 V (*i.e.*, $V_G = 311$), the maximum output voltage must be 130 V in order to ensure the compliance with the aforementioned standard. It is important to highlight that, as in the boost PFC converters, the voltage ripple can influence the performance of the buck-type PFC pre-regulators.

$$\theta = \pi - 2\sin^{-1}\left(\frac{V_o}{V_G}\right). \tag{2.14}$$

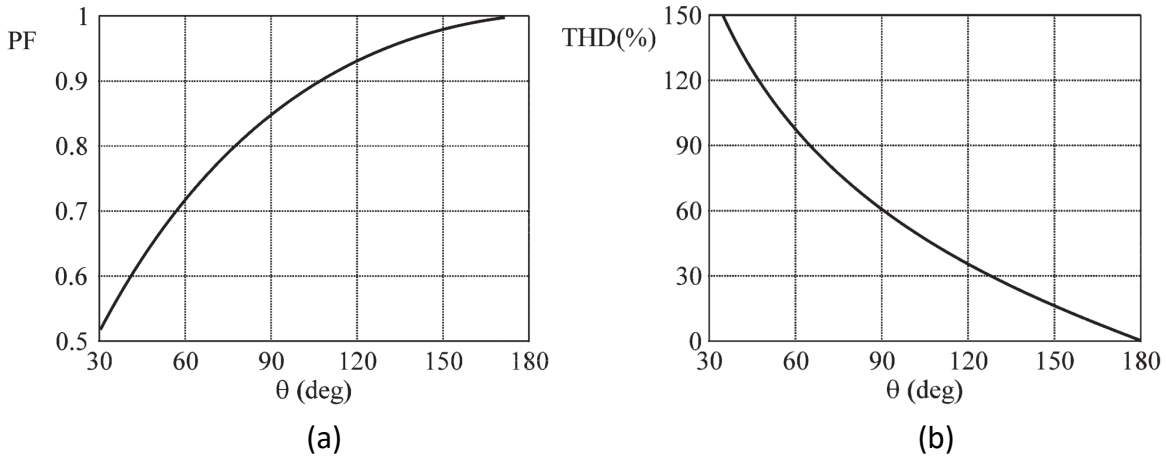


Figure 26: Behavior of (a)PF and (b)THD according the conduction angle θ. (DALLA COSTA et al., 2008)

2.3.2.3 VMC buck-boost-type PFC pre-regulators

The family of the buck-boost-type PFC pre-regulators includes the buck-boost converter and its derivatives, such as the Flyback converter. Figure 27 shows a voltage-mode controlled buck-boost PFC.

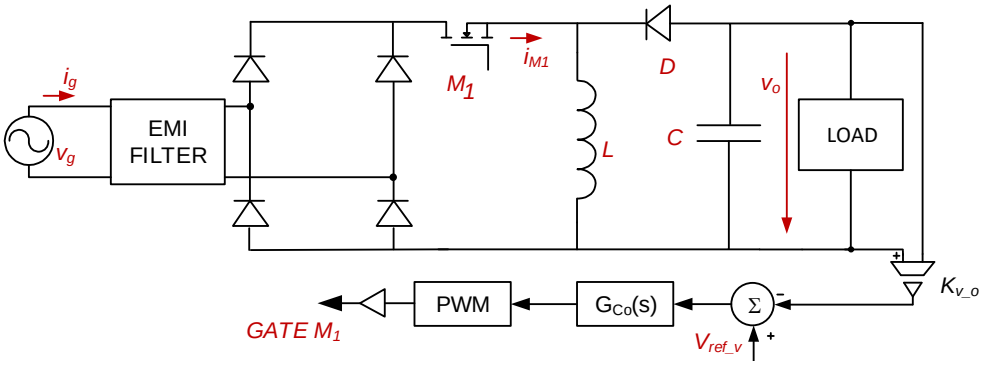


Figure 27: VMC buck-boost PFC pre-regulator

According to Wei and Batarseh (1998), the input current i_g of the PFC buck-boost operating in DCM is given by (2.15).

$$i_g(t) = \frac{D^2 T_s}{2L} v_g(t). \tag{2.15}$$

As can be seen in (2.15), differently from the boost and the buck-type pre-regulators, the input current of the buck-boost converter operating in DCM does not depend on the output voltage. Therefore, if the duty cycle and the switching frequency of the converter are kept constant, the input current waveform is theoretically sinusoidal. Figure 28 shows typical waveforms of the PFC buck-boost operating in DCM.

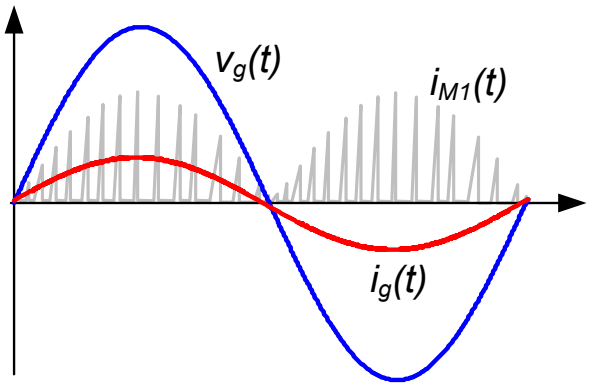


Figure 28: Typical waveforms of the buck-boost PFC operating in DCM

Thus, in terms of power factor correction capability, the buck-boost-type pre-regulators have the best performance among the basic VMC PFC converters. Furthermore, the output voltage ripple does not influence the power factor correction performance of the circuit.

2.3.2.4 Applications of VMC pre-regulators in LED drivers

The use of VMC PFC pre-regulators in LED drivers was extensively related in the literature (SOARES et al., 2012b)(ALMEIDA; SOARES & BRAGA, 2013)(ALONSO et al., 2011a)(GACIO et al., 2015), since those converters are suitable for low-to-medium power applications: the most common in LED lighting.

In Gacio et al. (2015), the behavior of a buck PFC pre-regulator for LED lighting applications was analyzed. The influence of the output voltage ripple in the input current waveform was addressed, showing that the LFR introduces an additional distortion in the line current of the buck PFC. Furthermore, the aforementioned work also presented the relation between the LFR and the conduction angle θ. A laboratory prototype of the Integrated buck-flyback converter for driving an LED string was built and the results showed the feasibility of the voltage-mode controlled PFC buck converter for lighting applications. Figure 29 shows the proposed topology.

2.4 SUMMARY OF THE CHAPTER

This chapter presented a brief review regarding the single-phase power factor correction techniques, focusing on the ones suitable for LED driving.

First, the main standards regarding power quality applicable to LED drivers were presented, highlighting the IEC-61000-3-2:2014 standard. Some Brazilian standards,

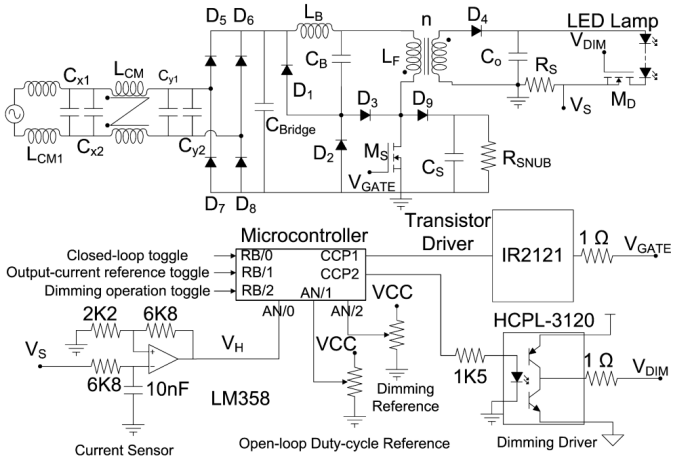


Figure 29: Integrated Buck-Flyback Converter presented in Gacio et al. (2015).

such as the NBR-16026 were also discussed.

As long as the importance of controlling the power quality parameters in LED drivers was addressed, some techniques devised to perform this task were discussed.

First, the power factor correction based on passive approaches was shown. The advantages of such techniques rely on the simplicity and sometimes on robustness. However, drivers based on passive PFCs tends to be bulky and are not suitable for applications in which the available space for the driver is limited.

Thereafter, some active strategies for correcting the power factor were revisited. These techniques were divided in two groups: those that are based on the current-mode control and the ones that rely on the voltage-mode control. It was shown that the current-mode control is normally used in converters operating in CCM or BCM whereas the VMC is normally applied for controlling PFC converters operating in DCM. Because of the operating mode, the voltage-controlled mode is usually preferred in applications of low-to-mid power, since the current stresses of the DCM are higher than the continuous conduction mode. On the other hand, the CMC converters have a more complex control structure, demanding additional control loops and consequently more components. Owing to these characteristics, the VMC PFCs are the most common approach in LED applications.

3 OFF-LINE LED DRIVERS WITH REDUCED STORAGE CAPACITANCE

As already commented in chapter 1, the LED driver is a fundamental element in the solid-state lighting system, since it is responsible for ensuring the benefits of this technology.

Furthermore, several works have shown that the LED driver must provide a tightly-controlled current through the LEDs in order to ensure the photometric performance of the devices as well as stability against temperature variations (ALMEIDA; SOARES & BRAGA, 2013)(HUI & QIN, 2009)(ALMEIDA et al., 2015a)(NOGUEIRA et al., 2012). Regarding the control of the current in the LEDs, this task includes both the stabilization of the average value and the limitation of the peak-to-peak current ripple. The latter could be a problem when the driver circuit is fed from the mains, since usually a large LFR must be filtered to compensate the input-to-output instantaneous power imbalance (ALONSO et al., 2012). Normally, the low-frequency ripple filtering is accomplished by using bulky storage elements, usually electrolytic capacitors, which are known to reduce the driver lifespan.

The US Departament of Energy carried out a study with more than 5400 LED luminaires which concluded that more than 59% of the catastrophic failures of such equipments occurred due to the driver (DOE, 2013). Moreover, it was shown in (ZHOU et al., 2012) that 50% of the failures in switched-mode power supplies (SMPS) are related to the malfunction of the electrolytic capacitors. Therefore, the electrolytic capacitors are directly related to the operational life of the LED luminaires so that avoiding them can improve the life span of the whole solid-state lighting system. An alternative is the use of metalized film capacitor, which can achieve more than 100,000-h lifetime (BUIATTI et al., 2009)(RODRIGUEZ & AMARATUNGA, 2008)

Despite the importance of the lifetime of the storage element, the capacitors in an LED driver must also be analyzed in terms of its power density, since there are some situations in which the available space for the electronic driver is limited. Regarding power density, the electrolytic capacitors are better when compared with film capac-

itors(WANG & BLAABJERG, 2014). Another option is the use of long-life electrolytic capacitors, which were devised so that their core withstands higher temperatures, leading to longer useful life when compared to conventional devices. However, similarly to film capacitors, the range of capacitances of the long-life electrolytic capacitors available in the market is limited.

In this context, several works have proposed different techniques to reduce the required filtering capacitances in off-line converters. Some of them are discussed in this chapter.

3.1 TECHNOLOGIES OF CAPACITORS

This section provides a study regarding the technologies of capacitors, focused mainly on the Aluminum Electrolytic Capacitors (Al-Caps) and the Metallized Polypropylene Film Capacitors (MPPF-Caps), which are present in the majority of SMPS. The aim of this analysis is to show the characteristics of such technologies, highlighting the advantages and drawbacks of each one. It is worth mentioning that there are other emerging technologies of capacitors that could also be employed in the design of LED drivers, such as the Multilayer Ceramic Capacitors (MLC-Caps) and the Aluminum Polymer Capacitors (AP-Caps), however, those technologies will not be discussed in this work.

3.1.1 Reliability

As already mentioned, the capacitors are one of the most critical elements in an LED driver, since that depending on the technology used, this component can affect dramatically the reliability of the system. Figure 30 shows a typical distribution of the capacitor's failure rate according to the time, also called "bath curve". One can note three different types of failures in capacitors: the early failures, which are related to the manufacturing process; the random failures, which occur within the lifetime (or service life) of the capacitor and are related to unexpected events(*e.g.*, a short-circuit between the leads of the component); and the wear-out failures, which occur due to electrochemical degradation of the capacitor.

The lifetime of a capacitor is limited by the electrochemical degradation of a single or a group of electrical parameters, such as the capacitance and the Equivalent Series Resistence (ESR). This parameter can be normally predicted taking into account the

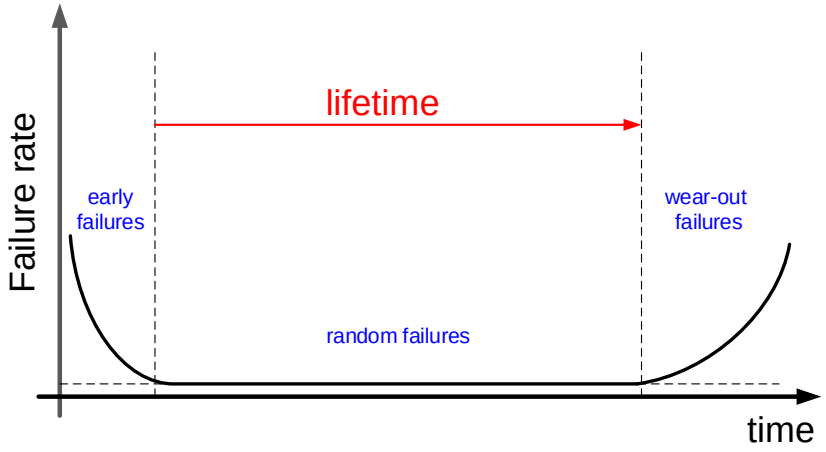


Figure 30: Capacitor 's failure rate vs time.

temperature and voltage stresses.

Some models for capacitors lifetime prediction have been proposed in the literature. Wang and Blaabjerg (2014) presents an empiric model derived from the Arrhenius equation and takes into consideration the influence of voltage and temperature stresses:

$$LT = L_{T0} \cdot \left(\frac{V_a}{V_r}\right)^{-n} \cdot \exp\left[\left(\frac{E_a}{K_B}\right)\left(\frac{1}{T} - \frac{1}{T_0}\right)\right]. \tag{3.1}$$

where:

LT - lifetime estimation;

L_{T0} - base lifetime;

V_a - applied voltage;

V_r - rated voltage;

T - temperature in Kelvin under use condition;

T_0 - temperature in Kelvin under testing condition;

E_a - activation energy;

K_B - Boltzmann's constant ($8.62 \cdot 10^{-}5eV/K$);

n - voltage stress exponent.

For the case of Al-Caps and film capacitors, a simplification of (3.1) was discussed in Jr and Dubilier (2004a), in which the activation energy was considered 0.94 eV, yielding

$$LT = L_{T0} \cdot \left(\frac{V_a}{V_r}\right)^{-n} \cdot 2^{\frac{T_0 - T}{10}}. \tag{3.2}$$

The value of n is between 7 and 9.4 for MPPF-Caps(POWER, 2012) whereas it ranges from 3 to 5 in Al-Caps(ALBERTSEN, 2010). This means that the degradation of the lifetime according to voltage stress is more severe in Al-Caps when compared to the MPPF-Caps.

The major failure mechanisms of Al-Caps can be found in Alwitt and Hills (1965), EPCOS (2012), Chemi-con (2013) and Dubilier (2002), which pointed out the electrolyte vaporization as the main cause of wear-out failures in snap-in-type Al-Caps.

In MPPF-Caps there is a phenomenon called "self-healing" in which breakdowns at local weak points in the dielectric material are fixed automatically at the cost of a small capacitance reduction (EPCOS, 2015). However, with the increase of these isolated weak points, the capacitance of the film capacitor is reduced towards its end-of-life (WANG & BLAABJERG, 2014).

As already mentioned, even within its service life, the capacitor is susceptible to random failures. These unexpected events normally are expressed in terms of the Failures in Time (FIT) λ or its reciprocal: the Mean-Time Between Failures (MTBF). Some documents have been presented techniques for modeling such failures for Al-Caps (USDOD, 1991)(JR & DUBILIER, 2004b). In USDoD (1991), a model for predicting λ was presented:

$$\lambda = \lambda_b \pi_C \pi_Q \pi_E \;\; Failures/10^6 hours \tag{3.3}$$

where:

λ_b - base lifetime, defined in (3.4) and (3.5) for the MPPF-Caps and Al-Caps, respectively. One can note that the base lifetime is a function of the capacitor ambient temperature T_a, the maximum applied voltage V_m (the ripple must be taken into account) and the rated voltage V_r;

π_C - capacitance factor, calculated from the capacitance of the capacitor in μF using (3.6) for MPPF-Caps and in (3.7) for Al-Caps;

π_Q - quality factor, which is related to quality of the component (informed by the manufacturer) - the values for this parameter can be found in USDoD (1991). For Non-Established Reliability capacitors, the value assigned to this factor is 3;

π_E - environment factor, which depends on the environment characteristic - the values for this parameter can be found in USDoD (1991). For fixed ground environment, the value is 1.

$$\lambda_{b\_MPPF} = 0.00051 \left[\left(\frac{V_m}{0.6V_r} \right)^5 + 1 \right] \exp \left[\frac{-0.15}{8.617 \times 10^{-5}} \left(\frac{1}{T_a + 273} - \frac{1}{298} \right) \right], \quad (3.4)$$

$$\lambda_{b\_Al} = 0.00012 \left[\left(\frac{V_m}{0.6V_r} \right)^5 + 1 \right] \exp \left[\frac{-0.35}{8.617 \times 10^{-5}} \left(\frac{1}{T_a + 273} - \frac{1}{298} \right) \right], \quad (3.5)$$

$$\pi_{C\_MPPF} = C^{0.09}, \quad (3.6)$$

$$\pi_{C\_Al} = C^{0.23}. \quad (3.7)$$

From the analysis of (3.2), (3.4) and (3.5), one can note that the voltage and temperature derating can dramatically improves the reliability of the capacitor. However, this strategy implies the oversizing of the element, which normally leads to a higher cost and volume. Furthermore, equations (3.6) and (3.7) show that if the total capacitance of the circuit is reduced, the number of failures in time tends to be lower. In order to verify this characteristic, the value of the FIT was plotted as a function of the capacitance for the MPPF-Caps and Al-Caps, as shown in Figure 31. This graph was obtained by considering a voltage derating of 10% (*i.e.,* $V_m/V_r = 0.9$) and an ambient temperature of 80 °C.

3.1.2 Power density

Power density is a quite important issue for the LED driver in several applications, mainly those in which the available space is limited, *e.g.*, LED bulbs.

Along with the magnetic elements, the storage capacitors are key elements when the power density of a circuit is under discussion and, sometimes, the application can limit the range of possible technologies depending on this characteristic.

März et al. (2010) discussed the power density of some capacitor technologies. It was shown that this parameter depends mostly on the relative permittivity and the

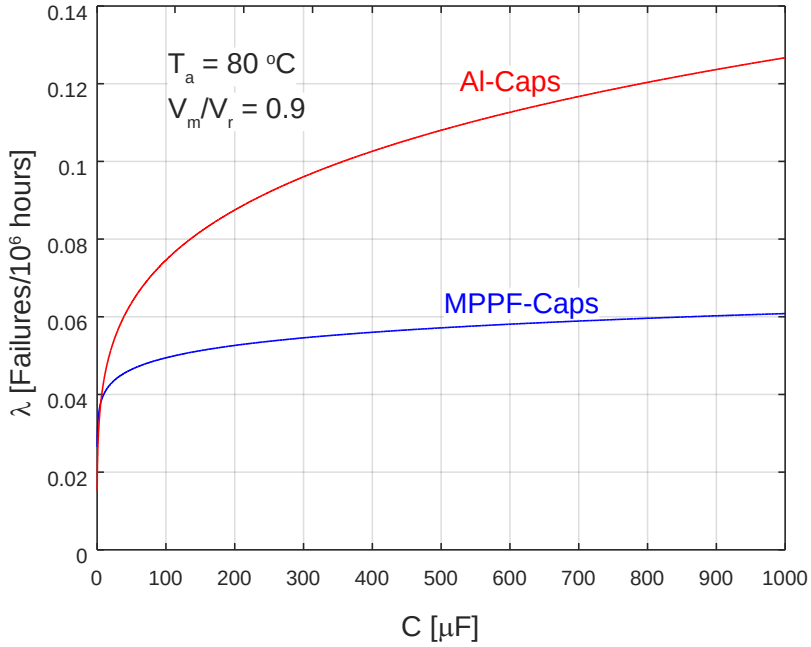


Figure 31: Behavior of the FIT as a function of the capacitance for for the MPPF-Caps and Al-Caps.

operational field strength of the dielectric material. Figure 32 shows the energy storage density of some dielectrics.

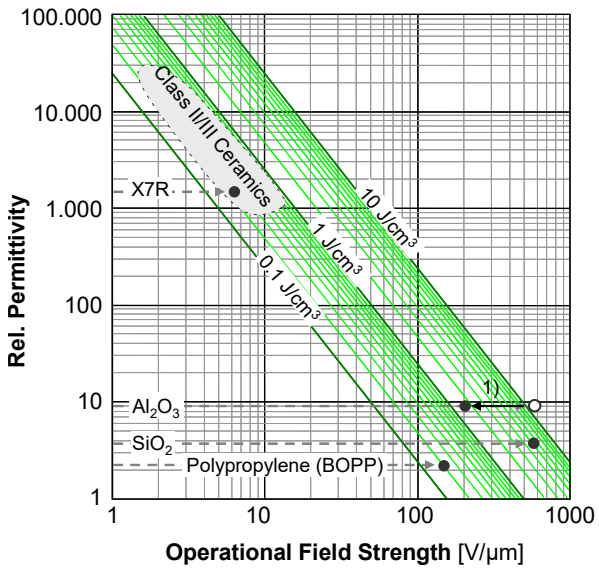


Figure 32: Energy storage density according to the dielectric material. März et al. (2010)

As can be seen in the graph shown in Figure 32, the capacitors based on polypropylene dielectric (*i.e.*, MPPF-Caps) can achieve about 0.2 J/cm^3 whereas the devices based on aluminum oxide (Al_2O_3), which is the case of Al-Caps, can reach an energy storage density of almost 2 J/cm^3. These values show that in terms of energy stor-

age density, Al-Caps are by far the best option. März et al. (2010) also related that currently Al-Caps lose about one order of magnitude in energy storage density in the winding construction, because of the overhead necessary to achieve the self-healing property (this point is highlighted as (1) in Figure 32).

Almeida (2014) also presented a comparison regarding the energy storage density between the Al-Caps and MPPF-Caps. Figure 33 shows a photograph comparing capacitors with similar nominal values. As can be noted in the picture, the energy storage density of the film technology is between 4 and 5 times lower than the capacitors that use aluminum oxide as dielectric material.

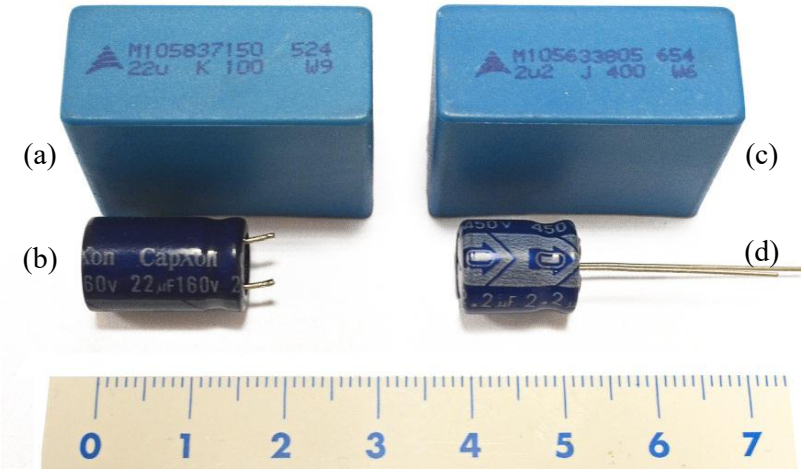


Figure 33: Comparison between capacitors with similar nominal values: (a) MPPF-Cap of 22 μF and 100 V - 10.5 cm^3 (0.0107 J/cm^3); b) Al-Cap of 22 μF and 160 V - 5.3 cm^3 (0.0531 J/cm^3); c) MPPF-Cap of 2.2 μF and 400 V - 10.5 cm^3 (0.0168 J/m^3) and d) Al-Cap of 2.2 μF e 450 V - 4.1 cm^3 (0.0543 J/cm^3). Ruler in centimeters. (ALMEIDA, 2014)

Once the characteristics of the mainly technologies of capacitors used in LED drivers were discussed, the next sections addresses some techniques used to reduce the filtering capacitances.

3.2 HIGH-VOLTAGE RIPPLE FILTERING (HVRF)

Some authors have proposed the strategy of filtering the LFR in higher voltages, in which the capacitor is operated in higher voltage levels. In Wong et al. (2016) it was shown that a general equation for the output voltage ripple in LED drivers can be approximated by:

$$\Delta v_o \approx \frac{P_{Load}}{\omega_L C V_{capacitor}}. \tag{3.8}$$

From (3.8) it is possible to observe that the output is inversely proportional to both the capacitance and the average voltage across the capacitor. Therefore, if the voltage is increased, the required capacitance for the same ripple level is lower. In order to exemplify the volume reduction, a calculation was carried out taking into account a load of 100 W, a 60-Hz mains voltage ($\omega = 377\,rad/s$) and a ripple around 10 %. Table 2 compares two capacitors with different voltages for this application. As can be seen, the capacitor sized to a higher voltage has about 61% of the volume of the lower voltage capacitor.

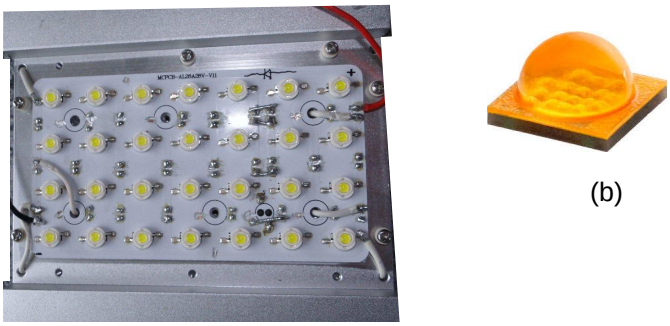
Table 2: Comparison of two capacitors from Panasonic with a different relationship between capacitance and voltage.

Capacitance	Voltage	Δv_o	Diameter	Length	Volume	Part Number
68 μF	200	9.75%	1.6 cm	2 cm	4.02 cm^3	EEU-EE2D680S
15 μF	400	11%	1.25 cm	2 cm	2.45 cm^3	EEU-ED2G150

In order to perform the low-frequency filtering in higher voltages there are basically two alternatives: by using a single-stage driver with a high voltage LED string or by using a two-stage driver.

Single-stage LED drivers presents good characteristics for driving LEDs owing their simplicity and high-efficiency. However, the design of those converters is quite inflexible, since a single converter must perform the functions of correcting the power factor and controlling the load's power. This characteristic normally leads to high filtering capacitances.

Nevertheless, the use of a high output voltage has been related in some works as a possible solution for decreasing the bulky capacitances of the circuit. Wong et al. (2016) and Soares et al. (2012b) showed single-stage converters with reduced filtering capacitances driving an LED load. In those works it is important to observe the type of the loads: in Soares et al. (2012b), a series-connected LED string (Figure 34a) was used whereas in Wong et al. (2016), the load was a high voltage LED module(Figure 34b). It is important to highlight that the high-voltage filtering was only possible owing to the characteristic of those loads. Therefore, the use of the aforementioned capacitance reduction technique in single-stage converters is conditioned by the load features.



(a) (b)

Figure 34: (a)LED module composed by 28 devices from Epileds connected in series. (b) Cree high-voltage module CREE XM-L HVW.

A more flexible approach for filtering LFR in higher voltages is by using two-stage converters, in which a high voltage dc-link connects the PFC and the PC stages. Owing to the presence of the power control stage, the voltage of the bulkiest capacitance can differ from the output voltage, which allows for the use of the HVRF even for low-voltage LED modules.

Figure 35 presents the behavior of the output current ripple of a two-stage converter composed by a cascade connection of the converters SEPIC and a buck-boost (ALMEIDA; SOARES & BRAGA, 2013). This figure shows that as the average bus voltage increases, the lower is the LFR. In the aforementioned work, the chosen bus (*i.e.*, dc-link) voltage was 250 V whereas the LED string nominal voltage was 180 V.

In Alonso et al. (2012) it was introduced a figure of merit (FoM) called power per voltage ratio P_v, defined in (3.9), for analyzing the bus voltage ripple in integrated converters. It was shown that as this ratio decreases, the bus voltage ripple in the integrated converters also decreases, showing that the average value of the bus voltage is inversely proportional to the ripple.

$$P_v = \frac{P_g}{V_B}. \tag{3.9}$$

where:

P_g - power of the converter;

V_B - average bus voltage;

Despite the potential of decreasing the capacitance by using high-voltage ripple filtering, this is not the only advantage of two-stage drivers. As presented in next

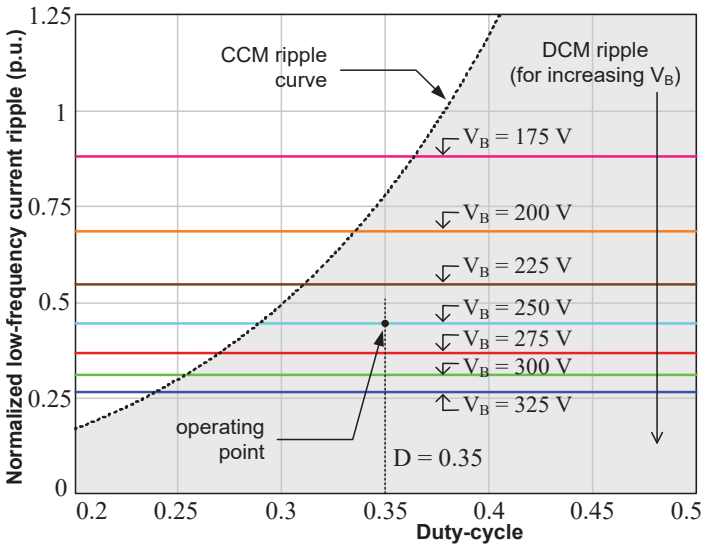


Figure 35: Normallized output current ripple of the integrated SEPIC buck-boost converter presented in Almeida, Soares and Braga (2013).

section, there are other mechanisms for ripple reduction in multi-stage converters.

3.3 MULTI-STAGE CONVERTERS

This section discusses the use of multi-stage converters for off-line LED driving, focusing in the mechanism of how these converters can reduce the LFR. As already mentioned, there are several advantages when using this type of converter in off-line LED drivers, mainly because the task of correcting the power factor and controlling the load's power is performed by two or more stages. This characteristic allows for a flexible design, i.e., there are more degrees of freedom that can be handled by the designer in order to achieve a better overall performance.

3.3.1 Converters based on the cascade connection of basic dc-dc topologies

The use of LED drivers based on the cascade connection of basic dc-dc topologies has been extensively related in the literature (ALONSO et al., 2012)(GACIO et al., 2011)(ALONSO et al., 2012)(ALONSO et al., 2011a)(ALONSO et al., 2011b)(SPIAZZI; BUSO & MENEGHESSO, 2005)(ALMEIDA; SOARES & BRAGA, 2013)(LUZ et al., 2014)(CHENG et al., 2011). The majority of those works rely on integrated converters, in which the PFC and PC stages are integrated in a single-active-switch topology so that the complexity of the control and the total number of components are decreased. On the other hand, Cheng et al. (2011) reported the use of a two-stage converter with independent stages, *i.e.*, both the PFC and the PC stages have an independent control loop. Figure 36

illustrates the difference between the aforementioned approaches.

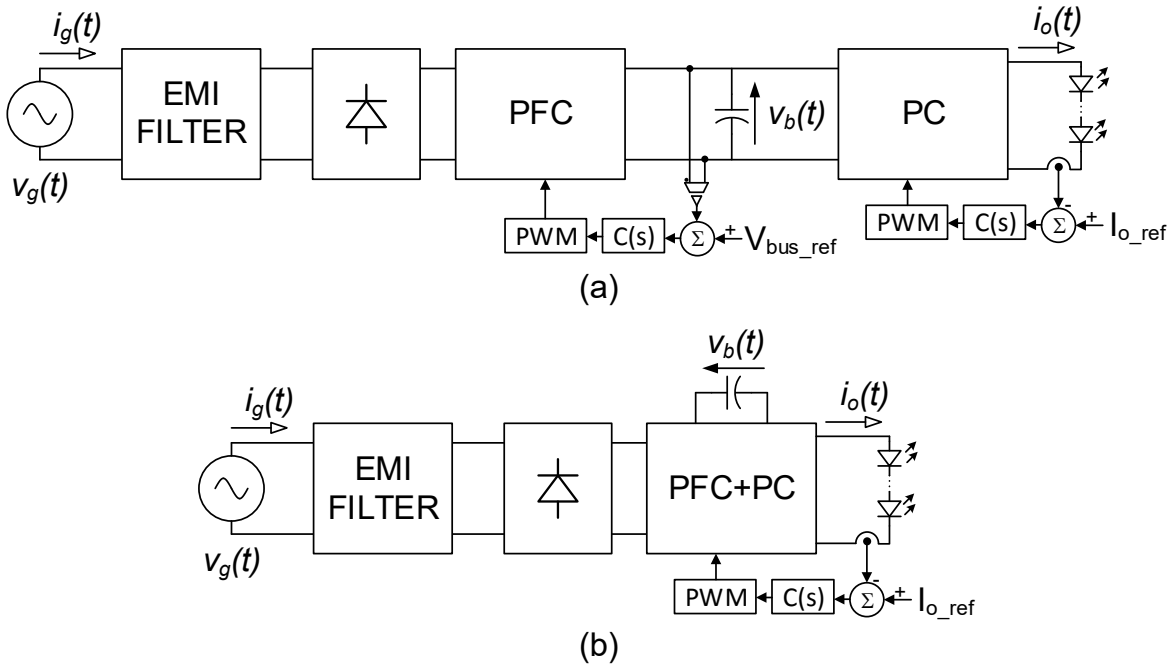


Figure 36: Two-stage converters: (a) with independent stages; (b) with integrated stages.

As can be observed, the strategy that relies on independent converters requires two control loops for its proper functioning whereas the integrated converter can work with only one control circuit. In this case it was considered that both the PFC and PC are voltage-mode controlled.

The independent operation of both converters brings more flexibility to the approach illustrated in Figure 36a. For example, the controller of the PC stage can be faster than the controller of the PFC, which provides a better dynamic performance. Regarding the integrated converter, this is not possible, since the controller of both stages is the same and it is generally tunned with a narrow bandwidth so that the power factor is not deteriorated. On the other hand, only one control loop means a small component count and therefore less cost and complexity.

According to Fraytag et al. (2015), there is not a major difference between the efficiency of integrated and nonintegrated converters if the PFC and the PC stages are designed with the same switching frequency.

As already mentioned, the use of a two-stage driver allows for the use of lower capacitances. In Alonso et al. (2012), it were addressed the mechanisms of ripple reduction of integrated converters. In the aforementioned work, the ripple in the LEDs was described as:

$$\widehat{I}_o = \frac{\nu \widehat{V}_B}{R_\gamma} \tag{3.10}$$

where:

$\widehat{I}_o$ - LED current ripple;

ν - voltage ripple transformation factor;

$\widehat{V}_B$ - bus voltage ripple;

R_γ - dynamic (or equivalent series) resistance of the LED string;

Therefore, in order to reduce the output current ripple, there are two ways: by reducing the ripple in the bus voltage or by reducing the voltage ripple transformation factor. The reduction of the ripple in the bus can be done by increasing the filtering capacitance or by increasing the bus voltage(ALONSO et al., 2012). Alternatively, the LED current ripple can be reduced by choosing a PC stage with a small value of ν. In Alonso et al. (2012),the values of the voltage ripple transformation factor for several converters were presented, showing that it is possible to obtain values of ν lower than one, which means that the second stage attenuates the low frequency ripple indeed. By comparison, if (3.10) was used to describe the ripple of a single-stage topology, the value of ν would be 1 and the only way to reduce the current ripple would be through the reduction in the output voltage ripple.

In Soares et al. (2012a) a comparative study between a Ćuk converter and an ISBB converter was carried out. The work showed that for the same load and ripple level, the bulkiest capacitor in the Ćuk converter was 45 μF/250V whereas the ISBB required a device of 10 μF/350V. Figure 37 shows both topologies. As expected, the two stage converter has a larger component count, however, the integration of the PFC and the PC stages minimizes this drawback since there is only one active switch.

3.3.2 Converters with a resonant stage

One of the drawbacks of the cascade connection of two basic topologies is that the overall efficiency of the drivers is limited and rarely is greater than 90% (ALONSO et al., 2012)(ALMEIDA; SOARES & BRAGA, 2013). In order to overcome this problem, some works have introduced the use of resonant converters as the PC stage (WANG et al., 2015a)(WANG et al., 2015b)(ALMEIDA et al., 2015b)(WANG et al., 2013). All of these works reported an overall efficiency higher than 90%.

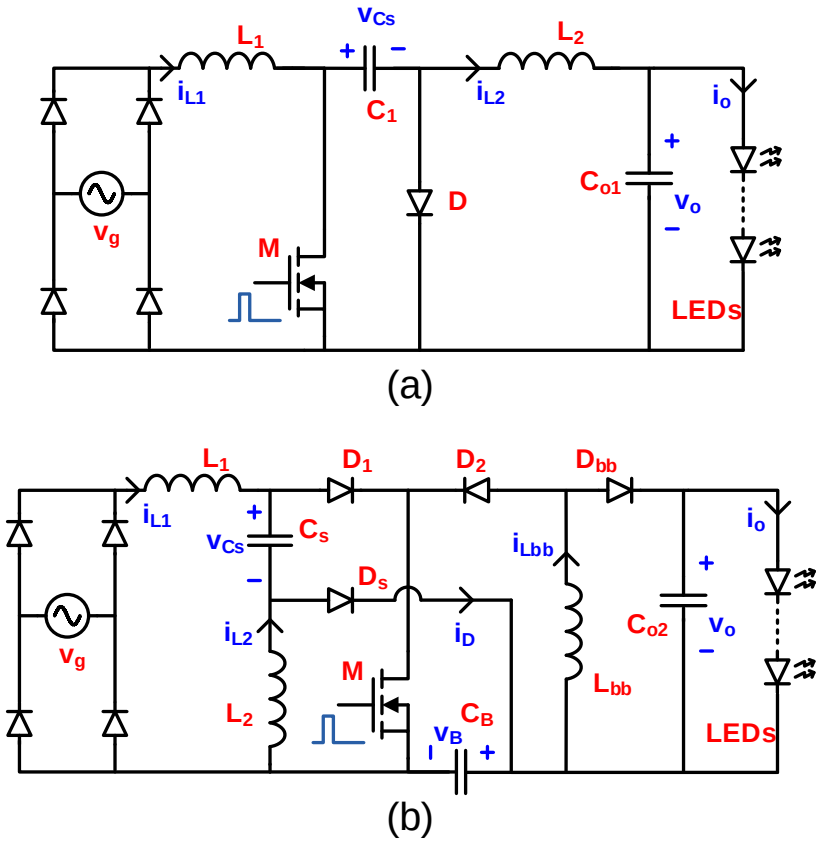


Figure 37: Topologies of two off-line LED drivers: (a) Ćuk converter; (b) ISBB converter. (SOARES et al., 2012a)

Besides promoting a significant improvement in the global efficiency of the converter, the resonant PC stage can also attenuate the low frequency ripple, as reported in Almeida et al. (2013) and Melo et al. (2015). Figure 38 shows the low-frequency attenuation capability of a Series Resonant Converter (SRC) operating as a PC stage. One can note that the use of a PC resonant stage provides an additional mechanism of capacitance reduction in off-line LED drivers.

Figure 39 presents the topology of an off-line LED driver with a resonant PC stage. One can note that the component count of this type of converter tends to be even larger than the conventional two-stage drivers (*i.e.*, composed by two simple dc-dc converter). This occurs because of the need of an inverter and an additional rectifier. Again, the integration of the PFC and PC stages can be used to simplify the topology.

3.3.3 Converters with reduced energy processing

Other solution for improving the efficiency in two-stage LED drivers was proposed in (CAMPONOGARA et al., 2013) and (CAMPONOGARA et al., 2015). The approach

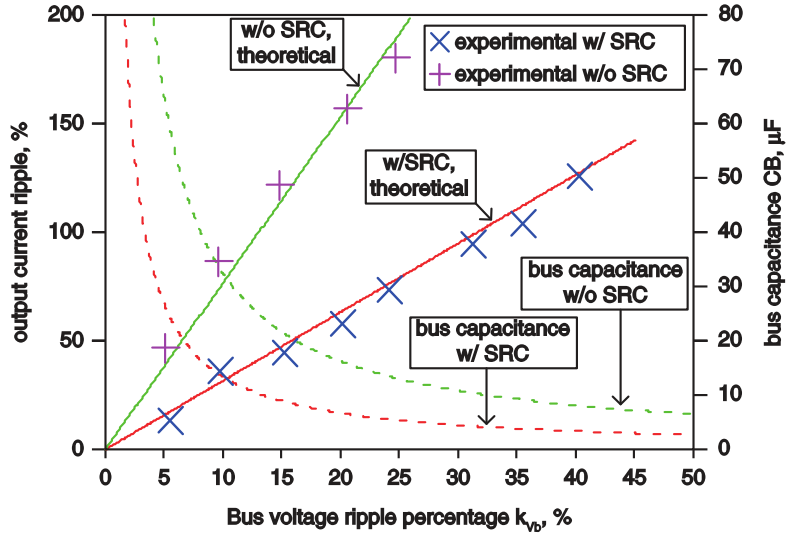


Figure 38: Ripple attenuation of a PC SRC. (ALMEIDA et al., 2013)

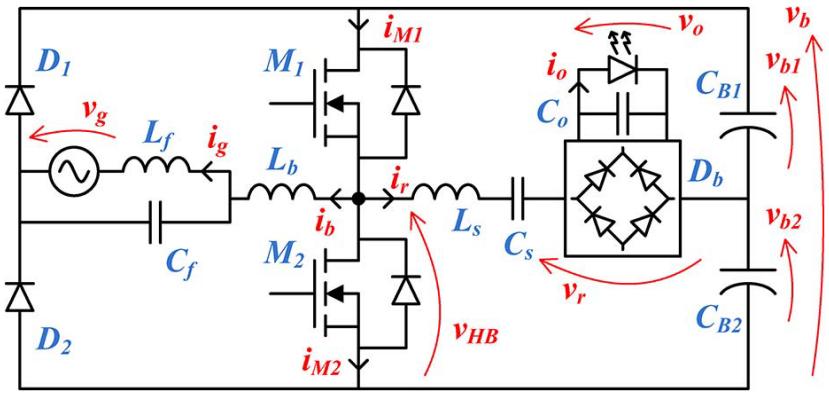


Figure 39: Integration between a Bridgeless Boost PFC and an Half-bridge Serie-Resonant Converter for LED driving. (ALMEIDA et al., 2015b)

presented in the aforementioned works is based on a converter with reduced energy processing, which means that only a part of the power delivered to the load is processed by the two stages of the converter so that the efficiency can be improved. Figure 40 illustrates the energy flow in a converter with reduced energy processing compared with a conventional two-stage driver. This comparison shows that the latter one tends to have a worse efficiency, since all the energy delivered to the load must be processed by both stages. Camponogara et al. (2013) reported an efficiency of 94 % with a driver whose topology is shown in Figure 41.

A control structure for the PC stage devised to attenuate the LFR was presented in (CAMPONOGARA et al., 2015).Figure 42 presents this control loop, which is composed by feedback and feedforward loops that are used both to regulate the current at the LEDs and to reduce the current ripple.

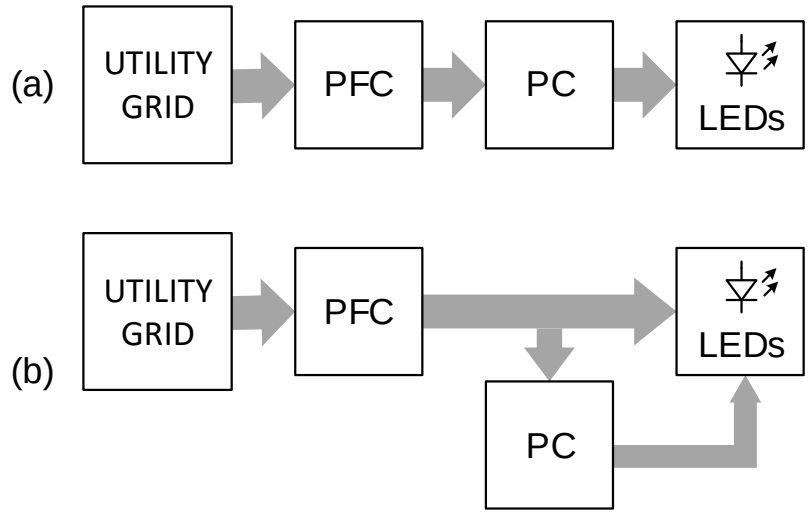


Figure 40: Comparison of the energy flow in: (a) a conventional two-stage converter; (b) a two-stage driver with reduced energy processing.

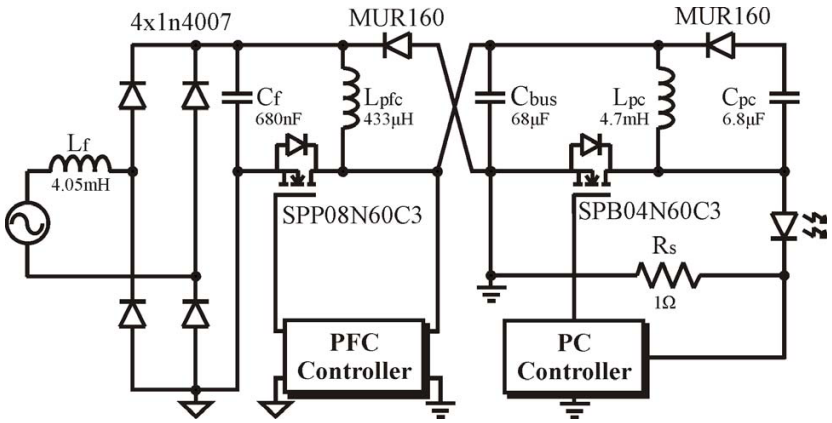


Figure 41: Schematics of the converter presented in Camponogara et al. (2013)

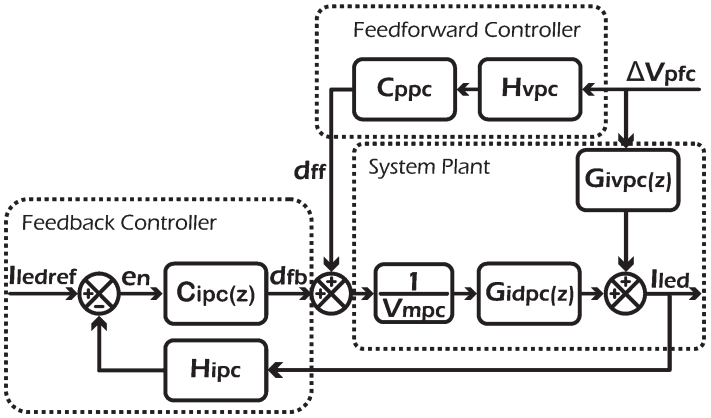


Figure 42: Control loop devised for the PC stage presented in Camponogara et al. (2015)

An alternative for LED driving with reduced power processing was presented in Pereira et al. (2017). In the aforementioned work, the current shaper technique

(ICS)(ALONSO et al., 1999; PEREIRA et al., 2015) was applied in order to achieve a topology with high power factor and reduced energy processing. The resultant topology, shown in Figure 43, is composed by a flyback converter, which implements the ICS, and a PC stage based on the buck topology, which is used for controlling the load power and helps to reduce the low-frequency ripple. The authors obtained an efficiency of 91.1% in the experimental evaluation of the proposed converter.

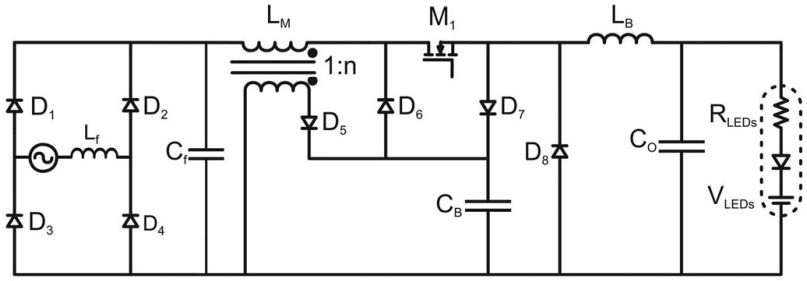


Figure 43: Converter proposed in Pereira et al. (2017).

3.4 HARMONIC CURRENT INJECTION

The output ripple in PFC pre-regulators occurs owing to the power imbalance between the input and the output of the converter. Considering a unity power factor PFC pre-regulator, the instantaneous input power has the following form:

$$P(t) = v_g(t) \cdot i_g(t) = V_G \sin(\omega_L t) \cdot I_G \sin(\omega_L t) = \frac{V_G I_G}{2} - \frac{V_G I_G}{2} \cos(2\omega_L t) . \qquad (3.11)$$

One can observe in (3.11) that the input power has an average value and an ac oscillating portion. The latter is the main cause of the LFR in off-line converters.

Some works have proposed the reduction of the amplitude of the ac portion of the instantaneous input power so that the LFR at the output of the converter can be reduced (WONG et al., 2016). Those techniques relies on the deliberated distortion of the input current (by injecting harmonic components) so that the peak-to-peak oscillation can be decreased. This approach is a trade-off between the increase in the THD of the input current and the reduction of the output low-frequency ripple.

In Gu et al. (2009), Wong et al. (2016) and Wang et al. (2010), the injection of harmonic components in the input current is proposed, aiming to the reduction of the peak-to-average ratio of the instantaneous input power. This task was accomplished by modifying the standard control loop of a current-mode controlled PFC converter in

order to provide a non-sinusoidal reference for the input current, including a certain amount of third (GU et al., 2009)(WONG et al., 2016) and fifth (WANG et al., 2010) harmonics so that the output ripple was decreased.

A similar strategy was outlined in Lamar et al. (2012), in which the technique also used a current-mode controlled PFC converter with a non-sinusoidal input current reference. However, differently from Gu et al. (2009), Wong et al. (2016) and Wang et al. (2010), the analysis presented in Lamar et al. (2012) took into account the limits of harmonic injection imposed by the IEC-61000-3-2 standard (IEC, 2014) in order to generate the reference for the input current.

One drawback of the harmonic injection techniques presented in Gu et al. (2009), Wang et al. (2010) and Lamar et al. (2012) is that two control-loops are needed. Furthermore, the complexity of the control structure is increased when compared to the conventional current-control mode. Figure 44 shows the circuits proposed in Wong et al. (2016) (Figure 44a) and Lamar et al. (2012)(Figure 44b).

3.5 SUMMARY OF THE CHAPTER

This chapter presented some issues related to the low-frequency ripple filtering in off-line converters.

Firstly, a brief review regarding the main technologies of capacitors was outlined showing that the MPPF-Caps are more reliable than the Al-Caps, being more suitable for long-lifetime applications. On the other hand, the Al-Caps are the best option in terms of energy density.

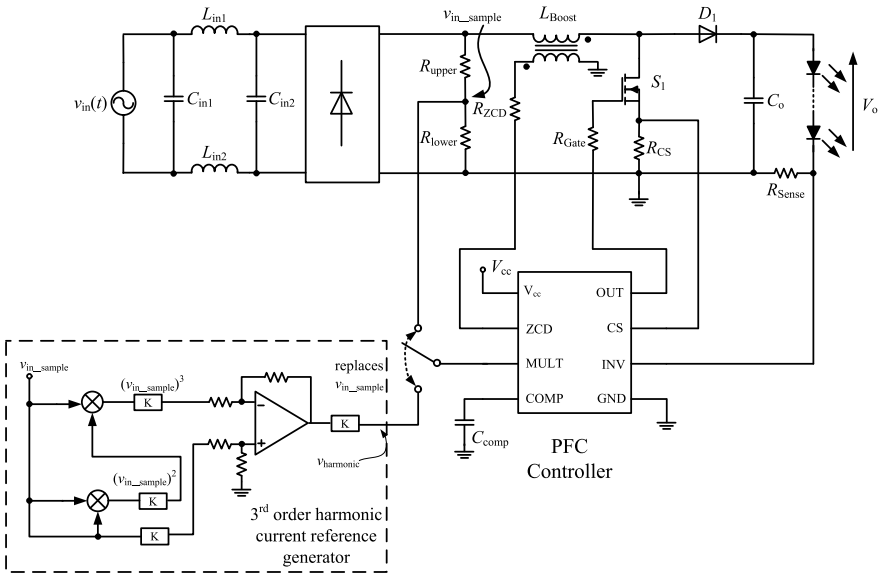
The remaining of the chapter addressed some techniques that allow for the reduction of the filtering capacitances in off-line converters. Three types of capacitance reduction techniques were discussed: the high voltage ripple filtering (HVRF), the use of multi-stage converters and the harmonic injection approach.

The HVRF technique is based on circuits in which the bulkiest capacitor is subjected to higher voltages, allowing for the reduction of the volume of the capacitor by decreasing the required capacitance of the application. It was shown that the use of this approach in two-stage drivers is more common since these topologies are more flexible than single-stage converters, in which the application of the HVRF is conditioned to the load's characteristics.

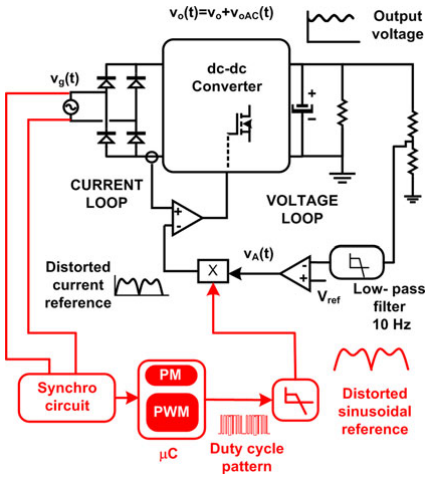
The use of multi-stage converters as a solution for attenuating the LFR was then

discussed. Three types of multi-stage converters were described in section 3.3 so that the advantages and drawbacks of each one were highlighted. In summary, the main mechanism of the multi-stage converters for reducing the LFR relies on the use of the PC stage to attenuate the ripple.

Finally, the use of harmonic injection techniques were presented in section 3.4. The works that are based on this approach, which are normally applied to CMC converters, showed that by distorting the input current of the PFC pre-regulator it is possible to attenuate the peak-to-peak value of the instantaneous input power, which allows for the reduction of the LFR of the output of the converter.



(a)



(b)

Figure 44: Control structures aiming the harmonic injection for reducing the output low-frequency ripple proposed in: (a) Wong et al. (2016); (b) Lamar et al. (2012).

4 REDUCING THE LOW FREQUENCY RIPPLE IN OFF-LINE LED DRIVERS BY USING LARGE SIGNAL DUTY CYCLE MODULATION

The previous chapter addressed some techniques devised to reduce the low-frequency filtering capacitances in off-line LED drivers. Several mechanisms were analyzed, each one with its advantages and drawbacks. Among the discussed techniques, one can highlight the use of two-stage converters and also control methods for reducing the instantaneous power imbalance between the input and the output of the driver. Regarding the alternative control techniques, the main approaches found in the literature are devised to topologies in which the current-mode control (CMC) is used. Therefore, the study of control techniques aiming to the capacitance reduction in VMC LED drivers rises as an interesting topic for investigation.

Figure 45 presents the simplified diagram of a VMC LED driver. In such circuits, there is a single compensation network for controlling the converter, which is responsible for generating the duty cycle $d(t)$ (*i.e.,* the control signal) from measurements of the output current.

In conventional approaches, the compensation network is designed only to ensure zero steady-state error of the average output current. In other words, the modulation of the converter duty cycle does not have a major influence upon the large signal behavior of the circuit. Thus, for sizing the main elements of a VMC driver, such as the inductors and capacitors, the conventional design strategies consider the duty cycle a constant variable.

The analysis presented in Chapter 2 showed that the duty cycle has a direct influence on the input current shape of a VMC PFC pre-regulator. On the other hand, the results obtained by Gu et al. (2009), Wang et al. (2010) and Lamar et al. (2012) attested that the controlled distortion of the converter input current can contribute to the capacitance reduction in off-line converters.

Therefore, the proposal of this work is to consider the duty cycle as a function

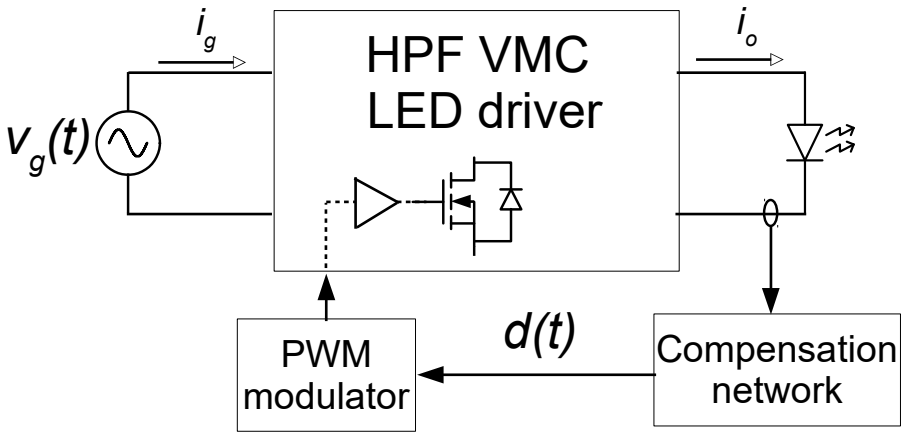


Figure 45: Basic diagram of a voltage-mode controlled LED driver.

that can have, besides the dc level, a set of harmonic components. This definition of the signal $d(t)$ allows it to influence not only the power processed, but also the large-signal behavior of the converter main variables. For the rest of this text, the proposed strategy will be called Active Ripple Compensation (ARC) technique.

Since the duty cycle signal can assume different forms in order to meet the design directives (*e.g.*, capacitance reduction), it is suitable to describe this variable in terms of its Fourier series components, as in the following:

$$d(t) = D_0 + \sum_{n=2,4,..}^{N} D_n \sin\left(n\omega_L t + \phi_n\right). \tag{4.1}$$

As can be seen in (4.1), the signal $d(t)$ is composed by a dc level an ac component, which was represented as a sum of N even harmonics multiple of the line frequency f_L. The odd harmonics are not considered because they impact on sub-harmonic components of the converter variables, whose fundamental is at twice the line frequency owing to the diode bridge.

Therefore, the proper selection of the $n-th$ harmonic components of $d(t)$, their amplitude D_n and phase ϕ_n allows the duty cycle signal to influence in the large-signal behavior of the converter. It will be shown along this chapter that the capacitance reduction provided by this strategy is based only on the modification of the control signal characteristic and is not related to topological changes.

Nevertheless, it is important to highlight that although the proposed approach is not related to topological changes, its performance can vary depending on the converter,

since the impact of the duty cycle modulation varies according to the topology.

Therefore, the ARC technique will be applied to different off-line LED drivers in order to evaluate its performance and feasibility.

Firstly, the proposed approach will be studied in an off-line flyback-based converter. Thereafter, the application of the ARC technique to an Integrated Double Buck-Boost Converter (IDBB) converter will be discussed. In both cases, the analysis will consider that the ac part of the duty cycle is composed only by one harmonic component. This consideration simplifies the theoretical analysis and allows for the sizing of the converter elements by means of design abacuses.

After this first evaluation, a more general analysis will be presented in next chapter, considering the use of more harmonic components in the duty cycle function, other topologies and several operating conditions.

4.1 INVESTIGATION OF THE ARC TECHNIQUE IN A FLYBACK CONVERTER

This section gives the mathematical description of a flyback-based LED driver with the ARC technique. The converter was devised to operate in the Discontinuous Conduction Mode (DCM), since in this operating mode, the circuit behaves like a voltage follower and can achieve a high power factor at the driver ac input. Figure 46 presents the basic diagram of an off-line flyback-based LED driver with a switching frequency f_s and a duty cycle $d(t)$.

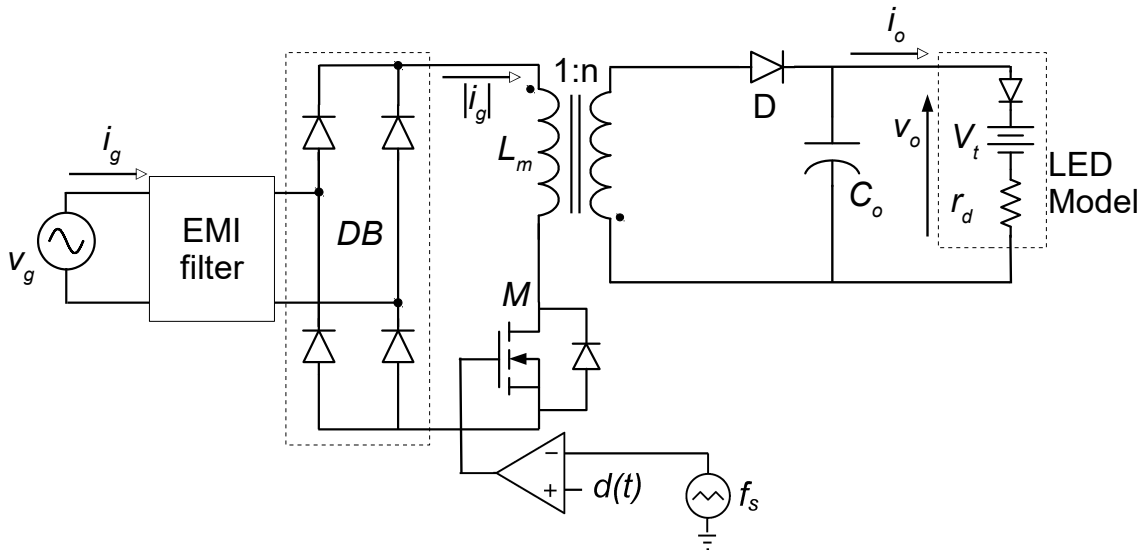


Figure 46: Basic diagram of an off-line flyback LED driver.

It is important to highlight that the design of the flyback driver with ARC must meet the requirements regarding the input current, so that it complies with the IEC-61000-3-2:2014 standard, and the output current, which must ensure that its average value and ripple stay within the desired values in order to assure the lighting quality. Therefore, the mathematical analysis presented in this section focuses on these two aspects.

According to (MARCHESAN et al., 2007), the input current of the flyback converter operating in DCM can be written as (4.2) in terms of the mains voltage $v_g(t)$, the duty cycle function $d(t)$, the flyback transformer magnetizing inductance of the flyback transformer L_m and the converter switching frequency f_s.

$$|i_g(t)| = \frac{|v_g(t)|\, d(t)^2}{2L_m f_s}. \tag{4.2}$$

On the other hand, the mains voltage can be defined by its RMS value V_G and frequency f_L:

$$v_g(t) = \sqrt{2}V_G \sin\left(2\pi f_L t\right). \tag{4.3}$$

Since the main variables of the converter will oscillate at twice the line frequency, a duty cycle function containing a harmonic with this frequency has been selected for this first analysis. This choice allows the control signal to influence the large-signal behavior of the converter. In this way, the duty cycle can be expressed as (4.4). Note that the modulation function is composed by three parameters: a dc component D_0, the duty cycle modulation amplitude D_2 and the modulation phase ϕ_2. The implementation of the duty cycle function will be discussed in Section 4.1.1.2.

$$d(t) = D_0 + D_2 \sin(2\omega_L t + \phi_2). \tag{4.4}$$

By using (4.4) in (4.2), the converter input current under the proposed modulation strategy can be derived as follows:

$$i_g\left(t\right) = I_1 \sin\left(\omega_L t + \theta_1\right) + I_3 \sin\left(3\omega_L t + \theta_3\right) + I_5 \sin\left(5\omega_L t + \theta_5\right), \tag{4.5}$$

in which the magnitudes and phases of the harmonic components are given by (4.6)-(4.11). The mathematical proof of the aforementioned equations is outlined in Ap-

pendix A.1.

$$I_1 = \frac{\sqrt{2}V_G}{2L_m f_s}\left[\left({D_0}^2 + \frac{{D_2}^2}{2} - D_0 D_2 \sin(\phi_2)\right)^2 + (D_0 D_2 \cos(\phi_2))^2\right]^{\frac{1}{2}}, \tag{4.6}$$

$$\theta_1 = tg^{-1}\left(\frac{2D_0 D_2 \cos(\phi_2)}{2{D_0}^2 + {D_2}^2 - 2D_0 D_2 \sin(\phi_2)}\right), \tag{4.7}$$

$$I_3 = \frac{\sqrt{2}V_G}{4L_m f_s}\left[\begin{pmatrix} 2D_0 D_2 \sin(\phi_2) + \\ \frac{{D_2}^2}{2}\cos(2\phi_2) \end{pmatrix}^2 + \begin{pmatrix} \frac{{D_2}^2}{2}\sin(2\phi_2) \\ -2D_0 D_2 \cos(\phi_2) \end{pmatrix}^2\right]^{\frac{1}{2}}, \tag{4.8}$$

$$\theta_3 = tg^{-1}\left(\frac{\frac{{D_2}^2}{2}\sin(2\phi_2) - 2D_0 D_2 \cos(\phi_2)}{2D_0 D_2 \sin(\phi_2) + \frac{{D_2}^2}{2}\cos(2\phi_2)}\right), \tag{4.9}$$

$$I_5 = \frac{\sqrt{2}V_G {D_2}^2}{8L_m f_s}, \tag{4.10}$$

$$\theta_5 = 2\phi_2 + \pi. \tag{4.11}$$

As can be seen, with the proposed duty-cycle signal, given by (4.4), the input current of the converter is composed only by the harmonics 1st, 3rd, and 5th. For the sake of simplicity, the analysis presented in this section will consider that the EMI input filter is designed to eliminate all the switching harmonics.

One can observe from (4.6) that the superposed modulation (D_2, ϕ_2) affects the first harmonic component of input current. Therefore, in order to achieve a good accuracy in the theoretical analysis, it is important to consider the influence of the ac part of $d(t)$ upon the power processed by the converter. This analysis will be shown in section 4.1.1.2.

With regard to the output current, it can be obtained by evaluating the low-frequency equivalent model of the converter's output, which is depicted in Figure 47. This analysis yields:

$$i_o(t) = \frac{v_o(t) - V_t}{r_d}, \tag{4.12}$$

in which V_t and r_d are the threshold voltage and the dynamic resistance of the LED string. The instantaneous output voltage $v_o(t)$ can be calculated by means of (4.13) in

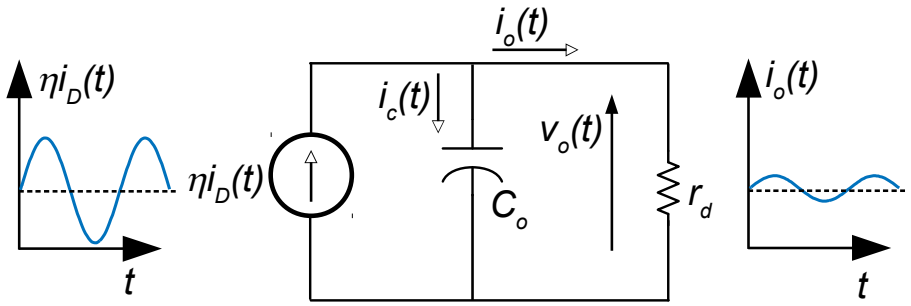


Figure 47: Low-frequency equivalent model of the flyback converter output.

terms of the diode current, which is given by (4.14). In equation (4.13), η represents the estimated efficiency of the circuit whereas C_o is the output capacitance.

$$\frac{dv_o(t)}{dt} = \frac{1}{C_o}\left(\eta i_D(t) - \frac{v_o(t) - V_t}{r_d}\right). \tag{4.13}$$

$$i_D(t) = \frac{v_g(t)^2 d(t)^2}{2 f_s L_m v_o(t)} \tag{4.14}$$

The lack of a closed-form solution for (4.13) implies that both the output voltage and the output current must be solved numerically. The instantaneous output voltage $v_o(t)$ must be found by using a numerical integration technique. In this work, the composite midpoint rule (LEVY, 2010) was chosen, which yields:

$$v_o(t_f) = \int_{t_1}^{t_f} \frac{dv_o(t)}{dt} dt \approx \sum_{k=0}^{N_s - 1} s_t \frac{\Delta v_o(t_k)}{\Delta t}, \tag{4.15}$$

where:

t_1 - initial time of the solution procedure;

t_f - final time of the solution procedure;

s_t - time step size;

N_s - number of steps, defined in (4.16);

t_k - k$^{\text{th}}$ time step, defined in (4.17).

$$N_s = \frac{t_f - t_1}{s_t}, \tag{4.16}$$

$$t_k\,(k) = t_1 + ks_t. \tag{4.17}$$

In this work, a step size s_t of one thousandth of the line period was used, the initial time t_1 was zero and the final time t_f was equal to five line periods.

The solution of the output current was then obtained simultaneously with the output voltage. In other words, for each $v_o(t_n)$, an output current value $i_o(t_n)$ is calculated by using (4.43). A MATLAB pseudo-code of a function that performs this calculation is shown in Figure 48.

```
function io = CalcIo(Co, D0, D2, φ2, Lm, fs, fL, VG, rd, Vt, η)

% Auxiliary parameters
ts = 1/(fL * 1000);
tf = 5/fL;
ωL = 2 * π * fL;
T = 0 : ts : tf;
vo = zeros(size(T));
io = zeros(size(T));
N = length(T) − 1;
vo(1) = Vt;

% Solution of the output current
for k = 1 : N
    t = T(k);
    d = D0 + D2*sin(2*ωL*t+φ2);
    vg = √2*VG*sin(ωL*t);
    vo(k + 1) = vo(k) + ts*1/(Co)*(d²*vg²/(2*fs*Lm*vo(k)) - (vo(k) - Vt)/rd));
    io(k) = (vo(k + 1) − Vt)/rd;
end
```

Figure 48: MATLAB pseudo-code for calculating the output current of the flyback-based LED driver.

4.1.1 Design Example

The design of the flyback-based LED driver with active ripple compensation must be performed in two steps. First, the passive elements (L_m and C_o) and the parameters of the duty cycle function (D_0, D_2 and ϕ_2) must be obtained. Thereafter, the control loop is designed so that $d(t)$ assumes the form defined in the previous step.

4.1.1.1 Design of the passive elements and the parameters of the duty cycle function

Since the values of D_0, D_2 and ϕ_2 affect the large signal behavior of the circuit, the passive elements must be designed simultaneously with the definition of the duty cycle function.

Table 3 summarizes the design parameters. The load, whose equivalent model presented in Table 3 is described in terms of V_{t0}, r_d and k_v, comprises 16 LED modules connected in series. Each module consists of the parallel association of four branches, which are composed by the series-connection of three Nichia NFSL757DT-V devices.

Table 3: Design Parameters

Symbol	Description	Value
V_G	Mains Voltage	220 V ±10%
f_L	Line frequency	60 Hz
V_{t0}	Nominal threshold voltage of the LED lamp	128.27 V at 25 ^{o}C
k_v	Temperature coefficient of the threshold voltage	-0.0816 V/^{o}C
ΔT_j	LED Junction temperature range	0 ^{o}C - 100 ^{o}C
$T_{j25^\circ C}$	Nominal LED junction temperature	25 ^{o}C
r_d	Dynamic resistance of the LED lamp	44.38 Ω
η	Estimated efficiency	90%
I_o	Average output current	350 mA
V_o	Average output voltage	143.81 V
P_o	Output power	50 W
$\Delta I_{o\%}$	Maximum current ripple	10%
f_s	Switching frequency	50 kHz

The criterion for choosing the current ripple level was based on the directives presented in Chapter 1, which showed that a ripple level of 10% is strict enough to prevent problems regarding flicker in human beings if the light modulation is at 120 Hz (typical in off-line LED drivers supplied by a 60-Hz mains voltage). It is important to highlight that one can use a higher value of $\Delta I_{o\%}$ for reducing the filtering capacitance depending on the application.

The first step is to define the maximum duty cycle, which ensures the DCM operation. As shown in (MARCHESAN et al., 2007), this parameter can be calculated by (4.18) in terms of the line RMS voltage V_G, the output voltage V_o and the flyback transformer relationship defined by n.

$$D_{crit}\left(V_o,V_G,n\right) = \frac{V_o}{V_o + n\sqrt{2}V_G}. \tag{4.18}$$

On the other hand, the output voltage of the circuit can be estimated by means of (4.19), as shown in Chapter 1.

$$V_o = V_t + r_d \times I_o, \tag{4.19}$$

in which V_t is the threshold voltage, defined in (4.20) as a function of the LED P-N junction temperature T_j.

$$V_t = V_{t0} + k_v \times \left(T_j - T_{j25^\circ C}\right). \tag{4.20}$$

Since the output voltage varies according to the temperature, D_{crit} must be calculated for the operating condition in which V_o is maximum. By analyzing (4.19) and (4.20), this situation occurs when the junction temperature is the lowest and can be calculated using the data presented in Table 3, yielding $V_{o\_max} = 145.9V$. Therefore, the constraint for ensuring the DCM when the converter is operating with the ARC technique is given by:

$$D_0 + D_2 \leq D_{crit}\left(V_{o\_max},V_G,n\right). \tag{4.21}$$

Once the condition for the DCM operation is defined, the design of the main parameters of the driver can be done. This task can be accomplished by adopting a graphical evaluation of the input and output current behaviors according to variations of the output capacitance and the parameters of the duty cycle function.

The design of the driver presented in the following will consider the nominal operating point, *i.e.*, $V_G = 220V$ and $T_j = T_{j25^\circ C}$. Furthermore, the chosen transformation relationship was $n = 1$, which results in a critical duty cycle of $D_{crit}\left(V_{o\_max}, 220, 1\right) = 0.319$ for this operating condition. Therefore, in order to ensure the DCM operation and allow for the large-signal modulation of the duty cycle signal, a value of $D_0 = 0.225$ was defined.

Figure 49 shows the behavior of the third and the fifth harmonic components of the input current as a function of the modulation angle ϕ_2 for different values of the modulation amplitude D_2. The graphs of the third and the fifth harmonic components were obtained using (4.8) and (4.10), respectively.

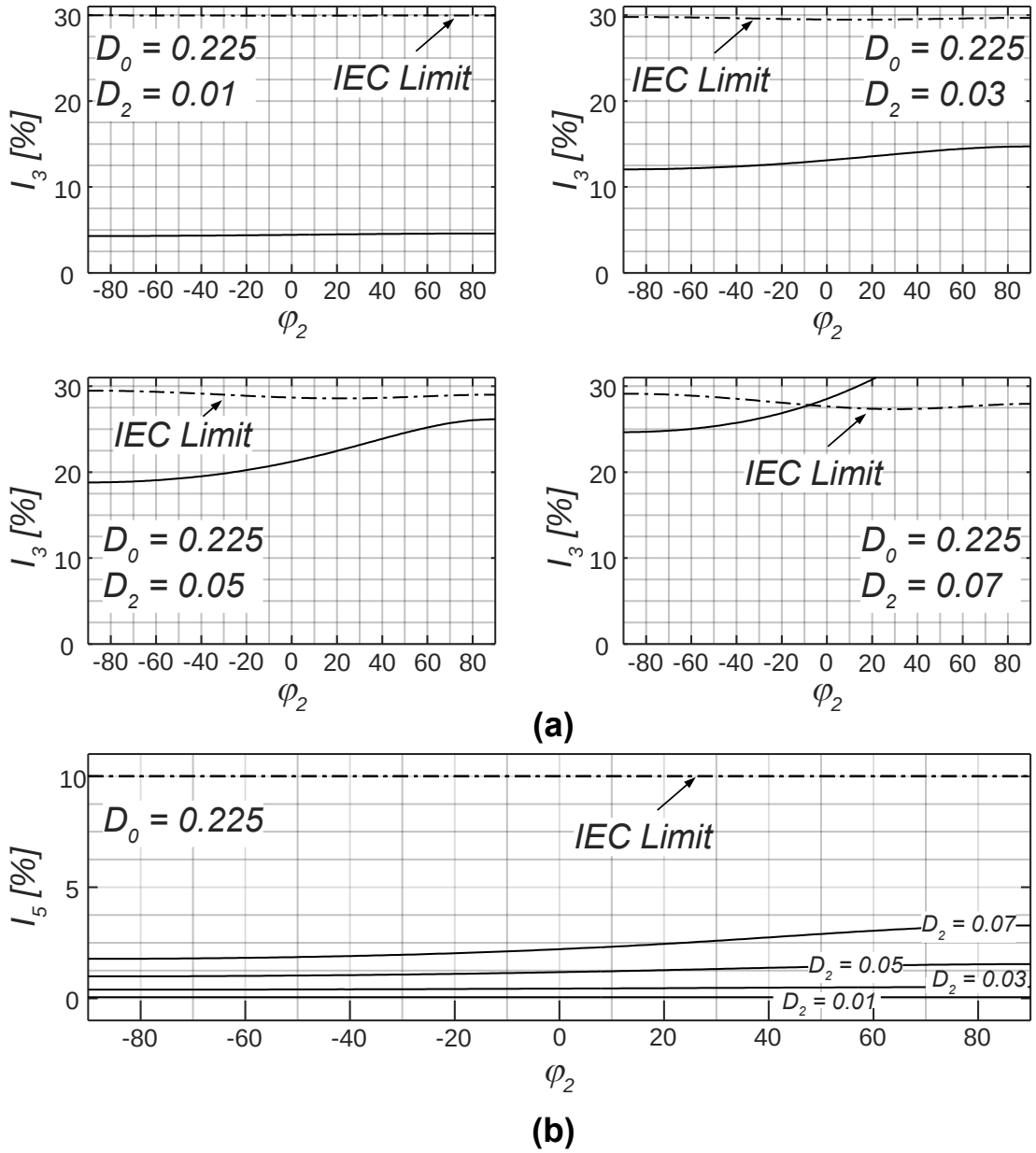


Figure 49: Behavior of the input current according to variations on the duty cycle parameters: (a) third harmonic component; (b) fifth harmonic component.

In Figure 49a, one can see that for $D_2 \leq 0.05$, the third harmonic component of the input current is within the limits established by the IEC 61000-3-2:2014 standard regardless the value of ϕ_2. Nevertheless, if $D_2 = 0.07$, the aforementioned standard is not met when the angle ϕ_2 is greater than -8^o. On the other hand, the fifth harmonic component (Figure 49b) remained within the limits of the IEC 61000-3-2:2014 standard regardless the values of the duty cycle parameters.

As can be noted from (4.6), the fundamental harmonic of the input current is also affected by D_2 and ϕ_2, so that the power processed by the converter is also modified according to the values of such parameters. Therefore, in order to ensure the power bal-

ance of the converter, for each pair (D_2, ϕ_2) a new value of the magnetizing inductance must be calculated so that the power delivered to the load remains constant.

The inductance L_m can be designed by means of power balance between the input and the output of the converter, as stated in (4.22) and (4.23). Thus, the flyback transformer magnetizing inductance can be obtained by using (4.2) and (4.23), which yields (4.24).

$$P_{in} = \frac{P_o}{\eta}. \tag{4.22}$$

$$\frac{1}{T}\int_0^T v_g(t) i_g(t) dt = \frac{P_o}{\eta}. \tag{4.23}$$

$$L_m = \frac{1}{T}\frac{\eta \int_0^T v_g(t)^2 d(t)^2 dt}{2 P_o f_s}, \tag{4.24}$$

where T is the line period ($T = 1/f_L$).

Figure 50 shows the behavior of the relative output current ripple for some values of C_o. For each capacitance, a set of curves was generated, being each one characterized by a certain value of D_2, ranging from $D_2 = 0$ up to $D_2 = 0.07$, and plotted for several values of ϕ_2. The graphs were obtained by solving (4.12), (4.13) and (4.14) using the values of D_2, ϕ_2 and C_o as well as the parameters presented in Table 3.

As can be noted in Figure 50, if $\phi_2 \geq 0$, the large-signal modulation of $d(t)$ decreases the output current ripple, achieving the maximum reduction when ϕ_2 is around 90^o. The graphs also show that if ϕ_2 is positive, the output current ripple decreases as D_2 increases. Nevertheless, when $D_2 \geq 0.05$, the driver lose the compliance with the IEC-61000-3-2:2014 standard, so that this represents the limit for the parameter D_2, as already addressed in Figure 49a.

Therefore, by choosing $D_2 = 0.05$ and $\phi_2 = 90^o$, the desired ripple criterion is achieved for an output capacitance of $C_o = 470\mu F$, which yields an output current ripple of 9.8% (34.3 mA).

In Figure 50, it can be noted that if the ARC technique was not used (*i.e.*, $D_2 = 0$), this capacitance would be insufficient for meeting the design requirements. In such case, a capacitance of 620 μF is required for achieving a similar ripple level. Thus, the modulation of the duty cycle provided a capacitance reduction of 150 μF (24.2 %)

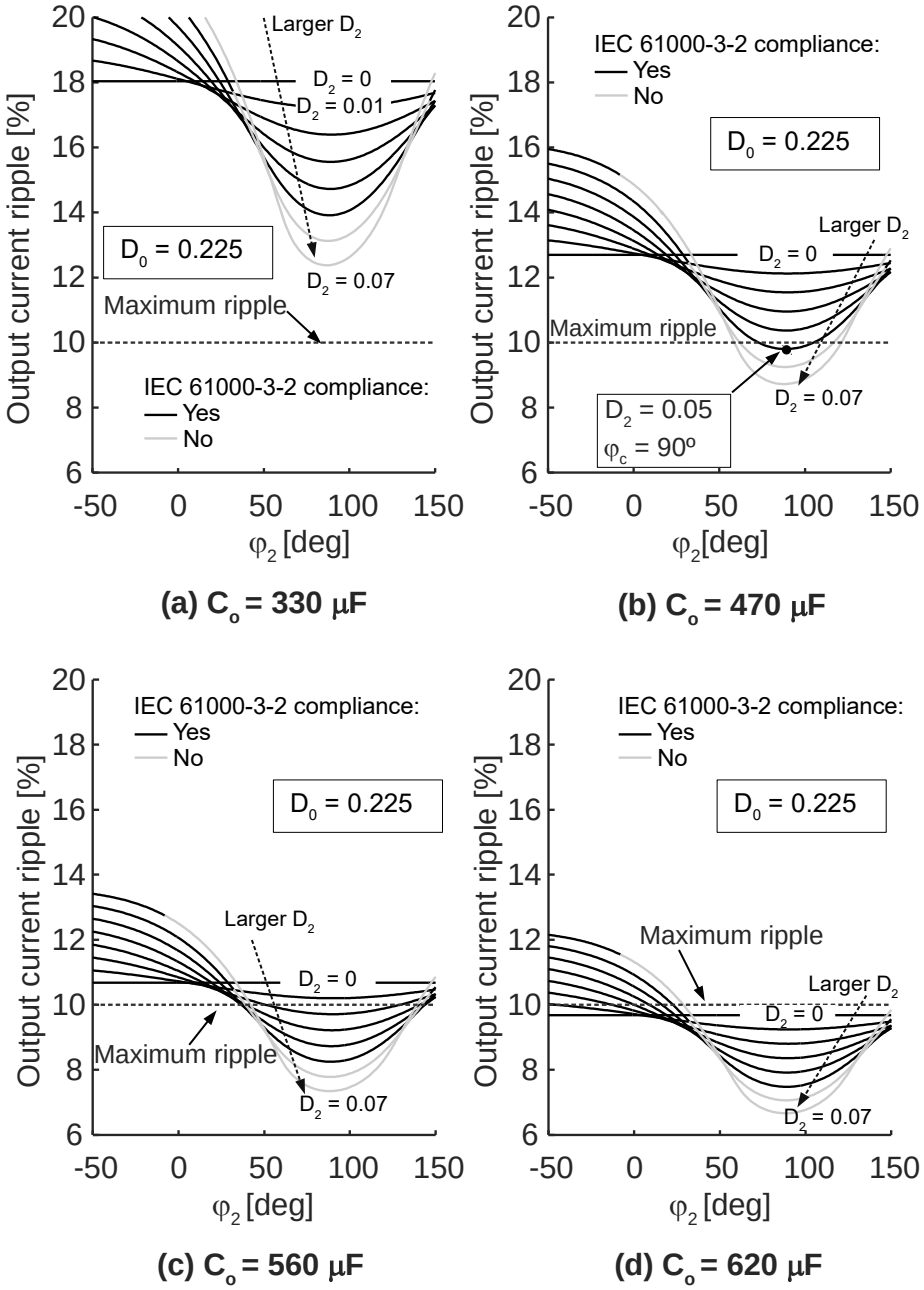


Figure 50: Behavior of the peak-to-peak output current ripple according to D_2 and ϕ_2 for several values of C_o.

when compared to the conventional approach without modulation.

Analogously to Figure 49, for each point of Figure 50, a magnetizing inductance L_m must be obtained to ensure the average power balance. Figure 51 shows the behavior of the magnetizing inductance as a function of ϕ_2 for several values of D_2. In Figure 51, it can be seen that for positive values of ϕ_2, the required value of the inductance L_m decreases as the amplitude of the ac portion of $d(t)$ increases. Furthermore, the graph also shows that for the chosen operating point (*i.e.*, $D_2 = 0.05$ and $\phi_2 = 90^o$), the value

of the inductance L_m must be 352 μH.

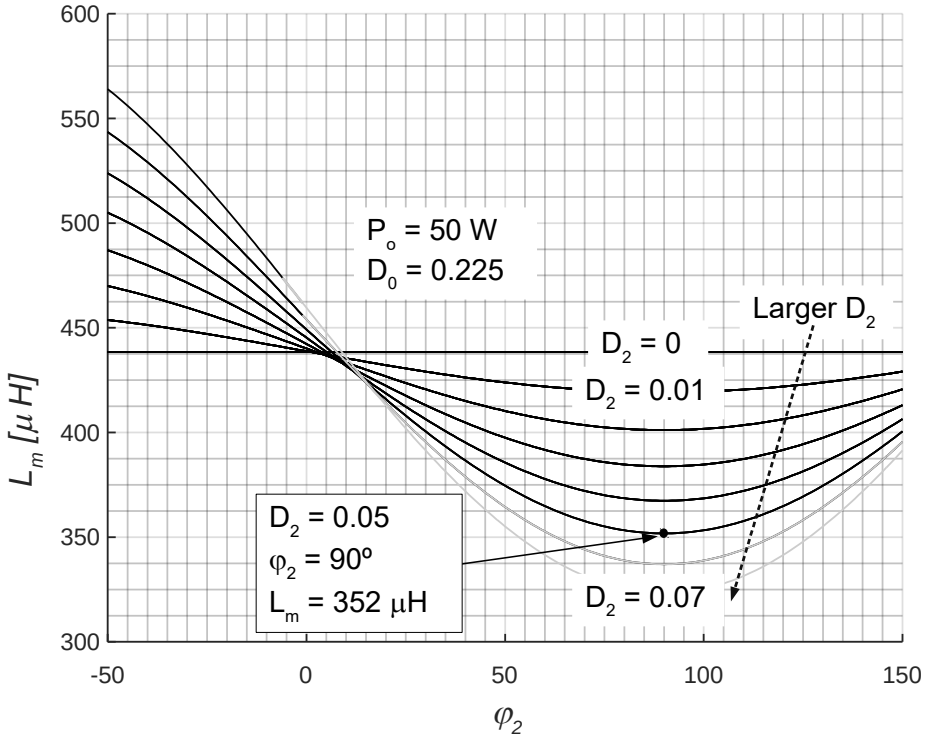


Figure 51: Variation of the magnetizing inductance according to the duty cycle parameters

4.1.1.2 Design of the control loop

Owing to the characteristic of the duty-cycle signal, it is necessary to derive a special structure for the control loop, which must be able to produce the signal described by (4.4), that is, both the average value D_0 and the ac portion, defined in terms of D_2 and ϕ_2.

A control circuit structure that is able to synthetize the two terms of the duty-cycle signal has been developed, meeting the performance parameters of the application. Figure 52 shows the diagram of the proposed closed-loop system, which is able to provide the desired duty-cycle function, solely from the output current error.

As can be seen, no extra sensor or control loop is required for this system. Some symbols in the Figure 52 were written in lower case indicating that these variables vary according to the operating conditions (*e.g.*, d_0 varies with the load). It is important to highlight that in this work, the current sensor circuit was based on the HCPL-7840 IC, tuned with a cut-off frequency of 2.5 kHz and a gain of 1 V/A. Therefore, the measured value presents a negligible phase-shift at $2\omega_L$.

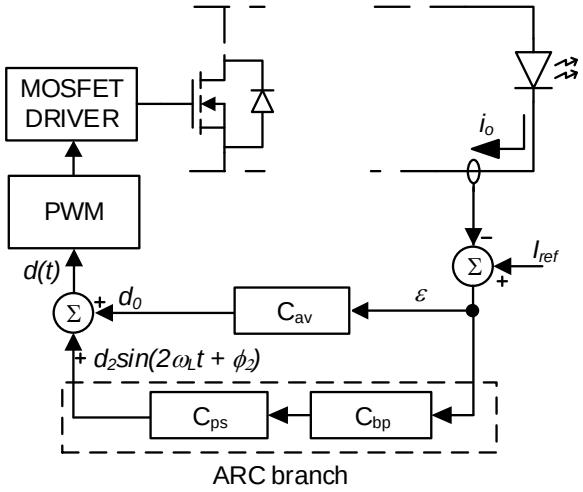


Figure 52: Diagram of the proposed closed-loop system.

In this control structure, a band-pass filter C_{bp} was used to isolate the ripple portion at $2\omega_L$, so that the control loop was composed by two frequency-independent branches. Because of this characteristic, each branch is responsible for synthetizing one portion of the whole duty-cycle function. The d_0 component is generated by C_{av}, which must ensure that the output average current follows the reference with null steady state error. This controller must be tuned to be slow enough to compensate only the average value of the error signal. It could be a classical proportional-integral (PI) controller or even a pure integrator.

The band-pass filter C_{bp} is tuned at twice the line frequency in order to obtain the $2\omega_L$ component of the error signal. It is important to highlight that this component is present in the error signal because the output current also oscillates at twice the line frequency due to the inherent input-to-output instantaneous power imbalance. The C_{ps} block is an phase-shifting filter, which provides the oscillating component of the duty-cycle by giving the correct gain and phase-shift to the $2\omega_L$ component of the error signal.

Figure 53 shows the theoretical waveforms in the ARC branch of the proposed control structure. As can be seen, the output of the band-pass filter is the $2\omega_L$ component of the error signal. Therefore, the input of the phase-shifting filter is directly related to the $2\omega_L$ component of the output current: the magnitude is multiplied by the gain of the band-pass filter and the phase is shifted by 180° (the phase shift of the band pass filter is zero at $2\omega_L$). One can note that C_{ps} is responsible for conditioning the output of the band-pass filter in order to yield the desired ac component of the duty cycle (*i.e.*, D_2 and ϕ_2).

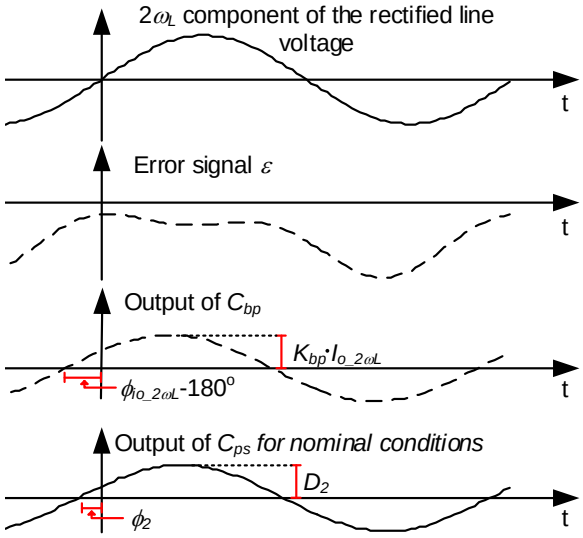


Figure 53: Theoretical waveforms of the ARC branch of the control structure.

One of the advantages of the proposed approach is that both control branches operate independently so that they can also be designed separately. However, the calculation of the elements of these two branches differs from the conventional design procedure of control loops (*e.g.*, the one employing phase and gain margins criteria). The blocks C_{av}, C_{bp} and C_{ps} can be understood as filters that are responsible for conditioning the "input" signal, which in this case is the current error signal ϵ, to generate a desired output signal, *i.e.*, the duty-cycle function $d(t)$, as described by (4.4) and indicated in Figure 52.

The transfer function of C_{av} is shown in (4.25). As can be noted, this compensator is an integrator, which ensures that the system have null steady-state error (OGATA & YANG, 1970). Furthermore, the crossover frequency of this transfer function must be tuned so that the output of the C_{av} block does not present any ac component in steady-state, *i.e.*, C_{av} must attenuate all the oscillating components of the error signal.

$$C_{av}(s) = K_a \frac{1}{s}. \tag{4.25}$$

In order to ensure a good attenuation at 120 Hz, a $K_a = 30$ was chosen, resulting in a crossover frequency of *ca.* 5 Hz.

The expression for $C_{bp}(s)$ was designed based on a narrow-band second-order band-pass filter (HUELSMAN & ALLEN, 1980). This element was tuned with a center angular frequency of $2\omega_L$ ($4\pi f_L$), which ensures that the oscillating component of the duty-cycle presents the desired frequency. Thus, the transfer function of C_{bp} is given by (4.26), in

which K_{bp} is the gain at center frequency and B is the filter bandwidth.

$$C_{bp}(s) = K_{bp}\frac{Bs}{s^2 + Bs + 4{\omega_L}^2}. \tag{4.26}$$

Finally, the design of the phase-shifting filter C_{ps} was based on the lead-lag compensator (OGATA & YANG, 1970). It must be calculated by considering the amplitude and phase of the output current at the frequency of interest ($2\omega_L$). These values can be obtained from (4.12) by using the Fourier series. Thus, the transfer function of $C_{ps}(s)$ is shown in (4.27) and its parameters must be chosen so that the output waveform of this filter is the desired oscillating component of the duty cycle signal. This condition is fulfilled by equations (4.28) and (4.29), which were devised from the analysis of the control diagram of Figure 52.

$$C_{ps}(s) = K_{ps}\frac{s + z_{ps}}{s + p_{ps}}, \tag{4.27}$$

$$|C_{ps}(2\omega_L)| = \frac{D_2}{I_{o\_2\omega L}K_{bp}}, \tag{4.28}$$

$$\angle C_{ps}(2\omega_L) = \phi_c - \phi_{io\_2\omega L} - 180^\circ, \tag{4.29}$$

in which $I_{o\_2\omega L}$ and $\phi_{io\_2\omega L}$ are the amplitude and phase of the $2\omega_L$ component of the output current, respectively.

By using the design results obtained in the subsection 4.1.1.1 in equations (4.12), (4.13) and (4.14) for calculating the output current $i_o(t)$ and thereafter using the Fourier series, the amplitude and phase of the $2\omega_L$ component of the output current is found as $17.2mA$ and -175.9^o, respectively. Therefore, those values can be used in equations (4.28) and (4.29) to find the parameters of C_{ps}.

Table 4 summarizes the design results of the control loop.

4.1.1.3 Digital implementation

In this work, the control system was implemented digitally by means of a TIVA C-Series microcontroller. The discretization of elements of the control loop was performed using the bilinear transformation (TUSTIN, 1947). The difference equations that represents the compensator $C_{av}(s)$, the band-pass filter $C_{bp}(s)$ and the phase-shifting

Table 4: Control circuit parameters

Parameter	Value
K_a	30 Hz
K_{bp}	1
B	125.66 rad/s
K_{ps}	27.88
z_{ps}	27.04 rad/s
p_{ps}	$21.02 \cdot 10^3$ rad/s

filter $C_{ps}(s)$ are given by (4.30), (4.31) and (4.32), respectively. Finally, the duty-cycle of the discrete-time system at the k^{th} instant is calculated by (4.33).

$$y_{avg}(k) = N_{a1}\varepsilon(k) + N_{a2}\varepsilon(k+1) - N_{a3}y_a(k+1), \tag{4.30}$$

$$y_{bp}(k) = N_{bp1}\varepsilon(k) + N_{bp2}\varepsilon(k+2) - N_{bp3}y_{bp}(k+1) - N_{bp4}y_{bp}(k+2), \tag{4.31}$$

$$y_{ps}(k) = N_{ps1}y_{bp}(k) + N_{ps2}y_{bp}(k+1) - N_{ps3}y_{ps}(k+1), \tag{4.32}$$

$$d_k(k) = y_a(k) + y_{ps}(k), \tag{4.33}$$

where y_{avg} , ε, y_{bp}, y_{ps} and d_k are the discrete variables representing the output of the average current compensator, the error signal, the band-pass filter, the phase-shifting filter and the duty-cycle, respectively. The integer k is the index of the k^{th} sample of the discrete system.

In order to calculate the coefficients in (4.30), (4.31) and (4.32), a sampling frequency f_{sam} of 5 kHz was considered. According to (BUSO & MATTAVELLI, 2015), this choice ensures that the discretization error for the bilinear transformation is lower than 3%, since the largest noticeable frequency in the output current is a decade below the sampling frequency. Moreover, since the cut-off frequency of the current sensor was tuned at 2.5 kHz, the aliasing errors in the digital system are mitigated because any noise with frequencies larger than the half of the sampling frequency will be attenuated.

The definition and values for each coefficient in (4.30), (4.31) and (4.32) are compiled in Table 5.

Table 5: Coefficients used in the discrete implementation

Coefficient	Definition	Value
N_{a1}	$\frac{K_a}{2f_{sam}}$	0.003003
N_{a2}	$\frac{K_a}{2f_{sam}}$	0.003003
N_{a3}	-1	-1
N_{bp1}	$\frac{K_{bp} \cdot B \cdot f_{sam}}{2{f_{sam}}^2 + B \cdot f_{sam} + 2{\omega_L}^2}$	0.012341
N_{bp2}	$-\frac{K_{bp} \cdot B \cdot f_{sam}}{2{f_{sam}}^2 + B \cdot f_{sam} + 2{\omega_L}^2}$	-0.012341
N_{bp3}	$\frac{4{\omega_L}^2 - 4{f_{sam}}^2}{2{f_{sam}}^2 + B \cdot f_{sam} + 2{\omega_L}^2}$	-1.953
N_{bp4}	$\frac{2{f_{sam}}^2 + 2{\omega_L}^2 - B \cdot f_{sam}}{2{f_{sam}}^2 + B \cdot f_{sam} + 2{\omega_L}^2}$	0.97532
N_{ps1}	$\frac{K_{ps}(2f_{sam} + z_{ps})}{2f_{sam} + p_{ps}}$	26.2043
N_{ps2}	$\frac{K_{ps}(z_{ps} - 2f_{sam})}{2f_{sam} + p_{ps}}$	-26.063
N_{ps3}	$\frac{p_{ps} - 2f_{sam}}{2f_{sam} + p_{ps}}$	0.35528

The flowchart of the algorithm implemented in the microcontroller is shown in Figure 54. The first two steps concern the configuration of the peripherals of the microcontroller, such as PWM and ADC, and then the initialization of the control variables. Thereafter, the main loop is executed periodically at 5 kHz. The control algorithm is performed in only six straightforward steps, which are the direct implementation of the equations shown in subsubsection 4.1.1.3. Owing to its simplicity, the proposed strategy can be implemented using low-cost microcontrollers, increasing the economic attractiveness of the proposal.

4.1.2 Experimental results

In order to verify the theoretical analysis presented in Section 4.1.1, a laboratory prototype was built. Table 6 presents the main elements used in the experiment. Figure 55 shows a photograph of the prototype boards. The schematic of the control board can be seen in Appendix A.2.

Figure 56 presents some experimental results of the flyback-based LED driver with ARC (Figure 56a) compared with the same circuit without the large-signal modulation of the duty cycle (Figure 56b), and also with the conventional approach with an additional output capacitance of 150 μF, *i.e.*, C_o = 620 μF (Figure 56c). As can be

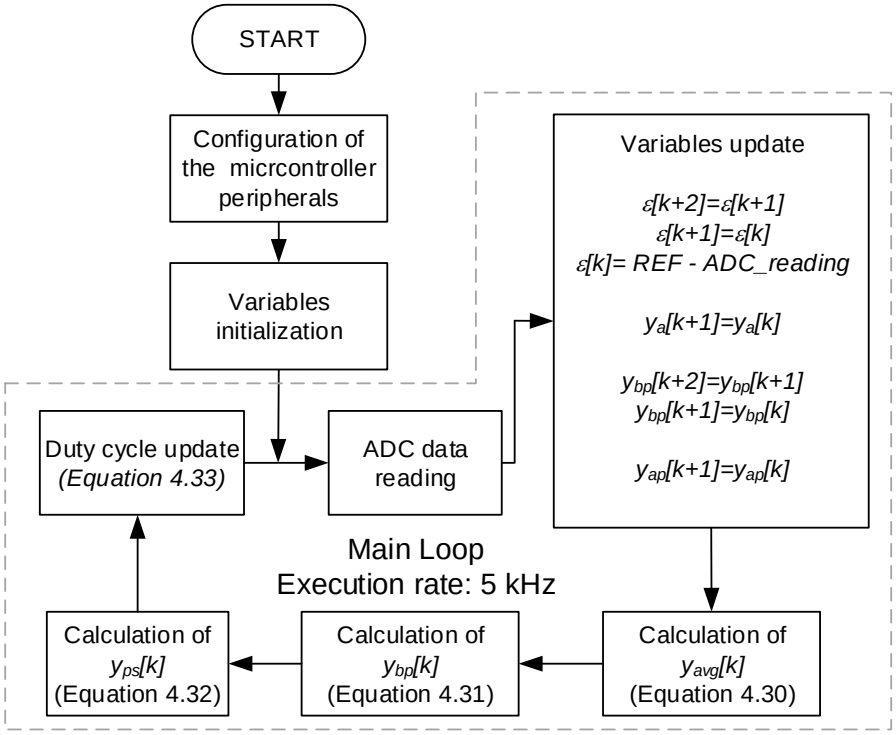


Figure 54: Flowchart of the control algorithm.

Table 6: Main Prototype Components

Item	Value
Diode Bridge DB	4 x HER156G
MOSFET M	IRF840
Diode D	HFA04SD60S
Capacitor Co	470 μ F / tanδ = 0.12/ 2000h@105^o (Electrolytic)
Flyback transformer	L_m = 355 μH / Leakage inductance = 15.4 μH/ ETD34 3C90 / Primary: 43T / Secondary: 43T / gap = 0.315 mm /Litz wire 66x38AWG
EMI Filter	CM:5.2 mH / DM: 3mH /2 x 220nF
MOSFET RCD Snubber	R = 180 kΩ / C = 2.2nF /D = MUR160
Microcontroller	TI TM4C123G

seen, these experimental results are in agreement with the theoretical analysis, since the ripple of 36 mA found in the experiment is close to the 34.3 mA predicted theoretically. Furthermore, Figure 56b shows that when the ARC technique is not used, the capacitance of 470 μF results in a larger ripple, being necessary an additional value of 150μF (Figure 56c) to decrease the output current ripple to a similar level to that in which the ARC is employed.

The results presented in Figure 56 show that the output current ripple of the circuit

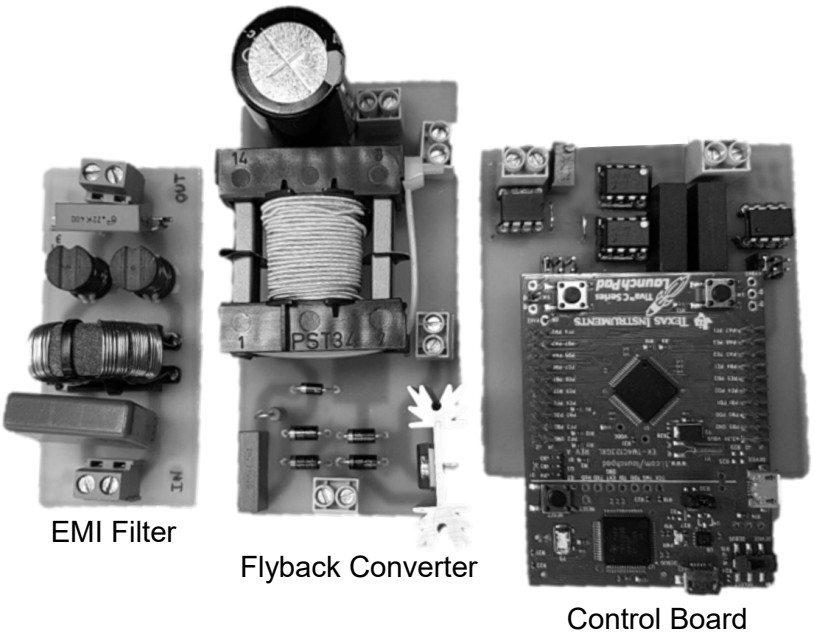


Figure 55: Photograph of the prototype

with duty cycle large-signal modulation is lower than the conventional approach (i.e, without ARC) at the cost of an increase of the input current distortion. Nevertheless, this distortion was predicted during the design procedure so that the harmonic content of the input current remains in compliance with the IEC-61000-3-2:2014 standard, as shown in Figure 57. The other harmonics were not depicted in Figure 57 because their values were negligible. As can be noted, the experimental results of the input current are also close to the values obtained in the theoretical analysis. The measured THD was 25.54%.

The efficiency of the converter with ARC technique was 90.1 % and 90.2 % with the conventional approach (*i.e.*, without ARC). This means that the effect of the large-signal modulation of the duty cycle upon the efficiency of the converter is negligible. Table 7 shows the measured losses distribution in the prototype, which was obtained by using a Tektronix DPO3014 oscilloscope.

The modulated duty cycle signal at steady-state operation can be seen in Figure 58. The measurement of this signal was carried out from the MOSFET gate-to-source voltage by using an IIR lowpass filter tuned at 1 kHz, which was embedded in the digital oscilloscope. The results show that the ARC branch is operating properly, since the ac portion of the duty cycle function is similar to the calculated value (*i.e.,* $D_2 =$ 5% and $\phi_2 = 90^o$).

The waveforms obtained from the MOSFET M and diode D can be observed in

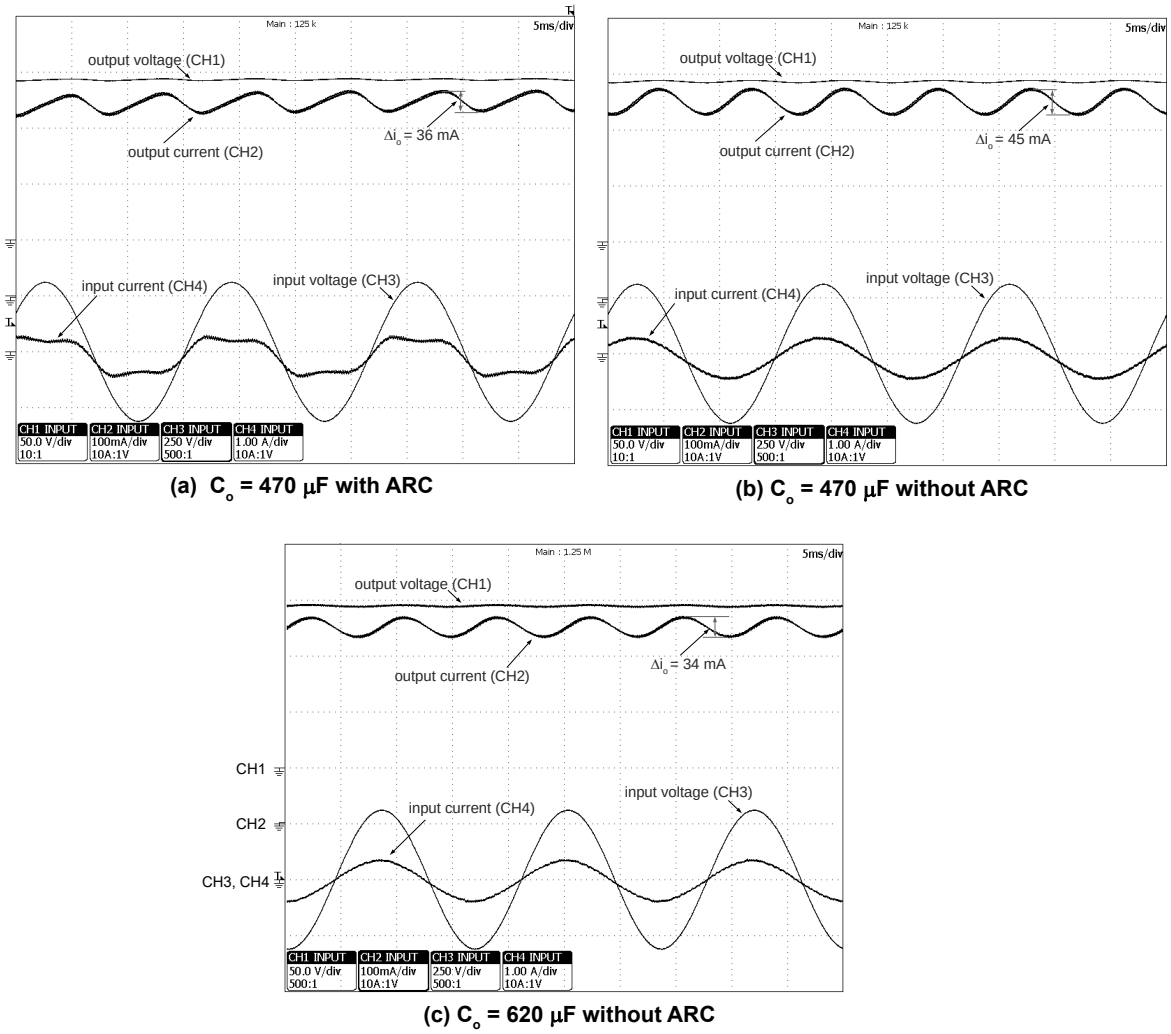


Figure 56: (a) Experimental waveforms obtained with ARC, (b) without ARC and (c) results without ARC with $C_o = 620$ μF. Output voltage (CH1 - 50V/div), output current(CH2 - 100 mA/div), input voltage (CH3 - 250V/div) and input current (1A/div). Horiz. scale: 5 ms/div.

Table 7: Measured Loss Distribution

Component	Value
EMI Filter	0.24 W
Diode Bridge	1.03 W
Flyback Transformer	0.79 W
MOSFET M	2.75 W
MOSFET snubber	0.20 W
Diode D	0.37 W
Output Capacitor	0.23 W
Total	5.61 W

Figure 59. As can be seen, the active switch is turned on with zero current, thus proving the DCM operation of the converter. One can note that during the turn-off of the active switch, the MOSFET entered in the avalanche mode. However, owing to

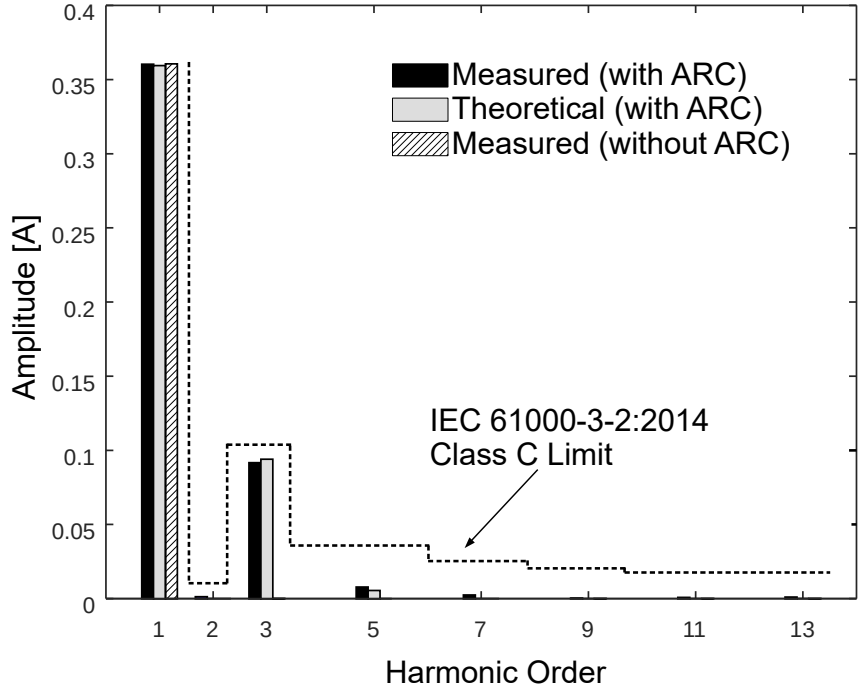


Figure 57: Harmonic content of the input current

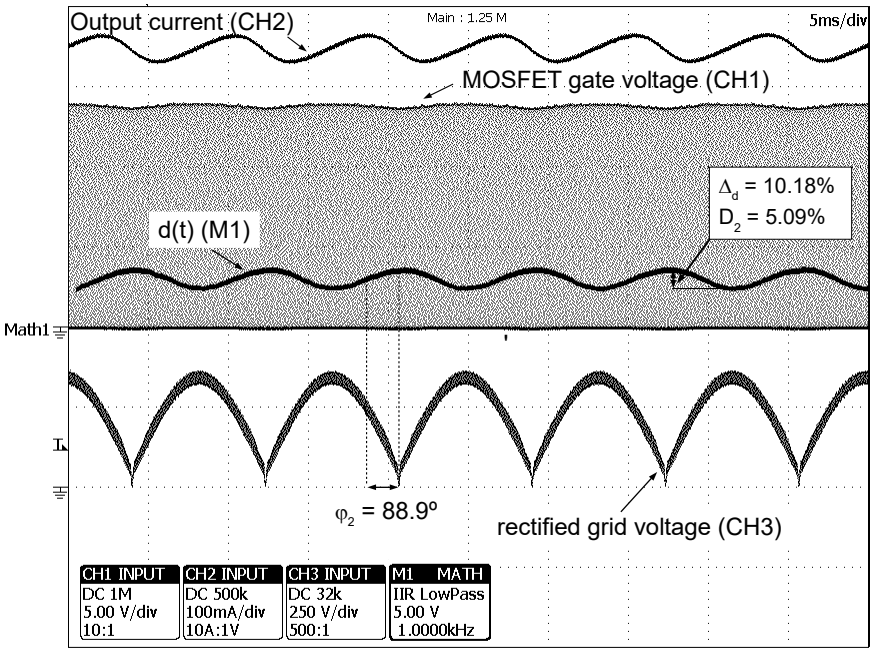


Figure 58: Behavior of the duty cycle in steady-state. MOSFET gate voltage (CH1 - 5V/div); duty cycle (M1 - IIR Lowpass filter with a cut-off frequency of 1 kHz - 5V/div) output current (CH2 - 100 mA/div); rectified grid voltage (CH3 - 250 V/div). Horizontal scale: 5 ms/div.

the small leakage inductance of the flyback transformer (4.3 %), the duration of the voltage spike was short and did not affect the circuit operation.

Figure 60 shows some results related to the closed-loop operation of the converter

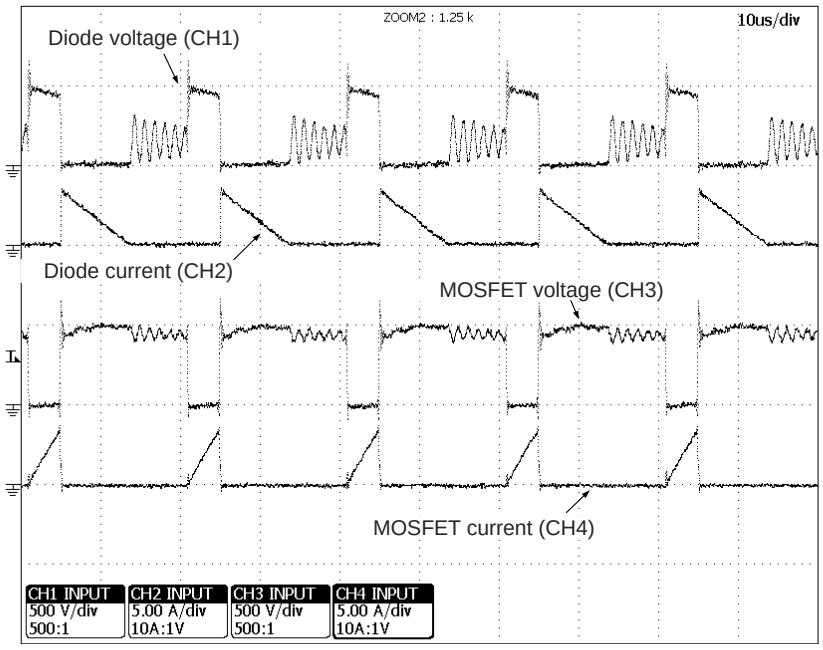


Figure 59: MOSFET voltage (CH3 - 500 V/div) and current (CH4 - 5A/div). Diode D voltage (CH1 - 500 V/div) and current (CH2 - 5A/div). Waveforms measured at the peak of the rectified voltage. Horiz. scale: 10 μs/div.

against input voltage and load variations. Figs. 60a and 60b demonstrate that the control loop was able to ensure a good output current regulation. In both cases, the output current remained very close to its nominal value for the whole operating range, so that the system was able to deal with variations in the input voltage, and also for changes in the output voltage, which can occur owing to alterations in the LED junction temperature.

Figure 60c presents the behavior of the efficiency of the converter owing to load variations. As can be seen, the maximum efficiency was 92.7% when the load is about 60 % and decreases for higher power levels.

Finally, Figure 61 shows the dynamic performance of the converter during steps of the input voltage and the load. In Figure 61a, two steps in the input voltage were carried out: from $V_G = 220V$ to $V_G = 240V$ and after from $V_G = 240V$ to $V_G = 200V$. As can be seen, in both cases the steady-state error of the average output current was approximately null, indicating the proper operation of the compensator C_{av}. On the other hand, the dynamic behavior of the converter for a short-circuit of 2 modules (12.5% of the load) can be observed in Figure 61b. In this case, the control system was also able to deal with the load variation and ensured null-steady state error. It is important to highlight that when part of the load was short-circuited, the excess of energy stored in the output capacitor caused a current overshoot. Nevertheless, it is

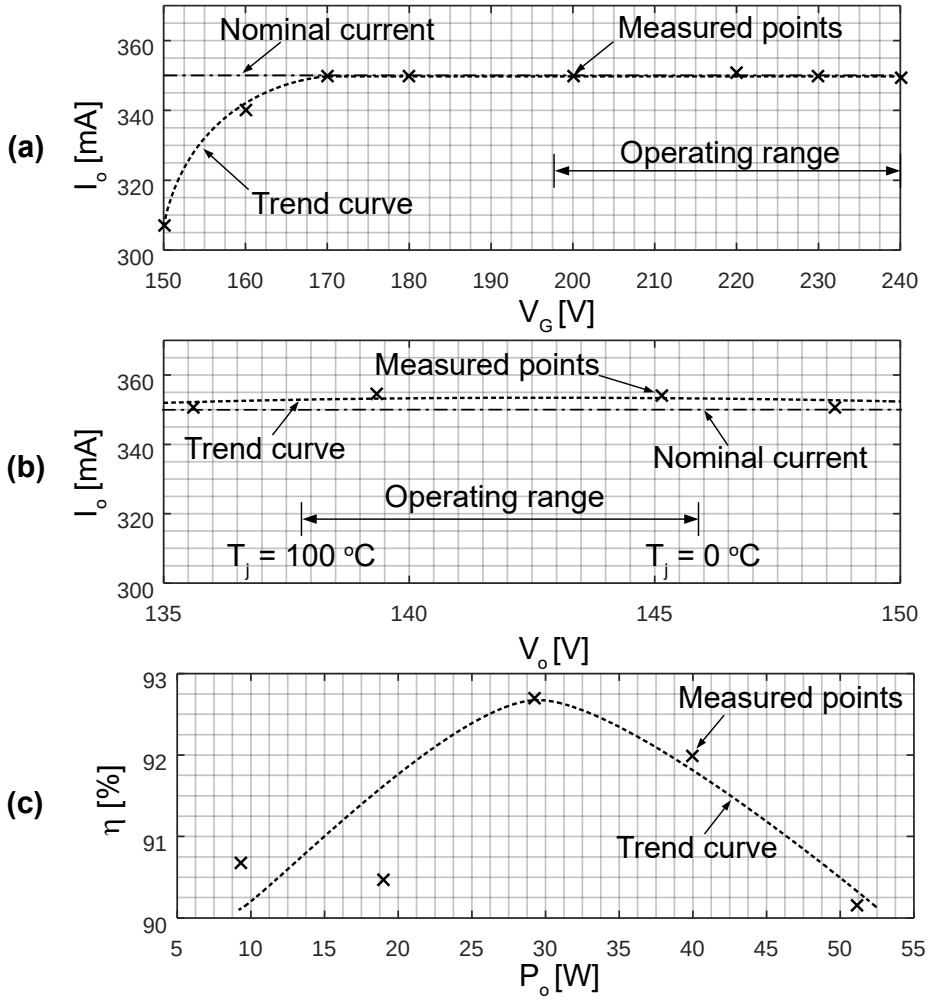


Figure 60: Behavior of the converter owing to variations of the input voltage and the load. (a) Output current regulation for input voltage variations; (b) Output current regulation for output voltage variations; (c) Efficiency of the converter for several load levels (dimming).

possible to see in Figure 61b that the input current decreases to zero in less than a half line cycle, indicating the quick action of the control system.

4.2 INVESTIGATION OF THE DUTY CYCLE MODULATION IN AN INTEGRATED TOPOLOGY

Section 4.1 presented the investigation of the ARC technique in an off-line Flyback based LED drivers. The results showed that the proposed technique was able to reduce the required filtering capacitance about 24 %.

Alonso et al. (2012) showed that the use of integrated converters in LED driving is a quite effective approach for reducing the low-frequency ripple filtering capacitances.

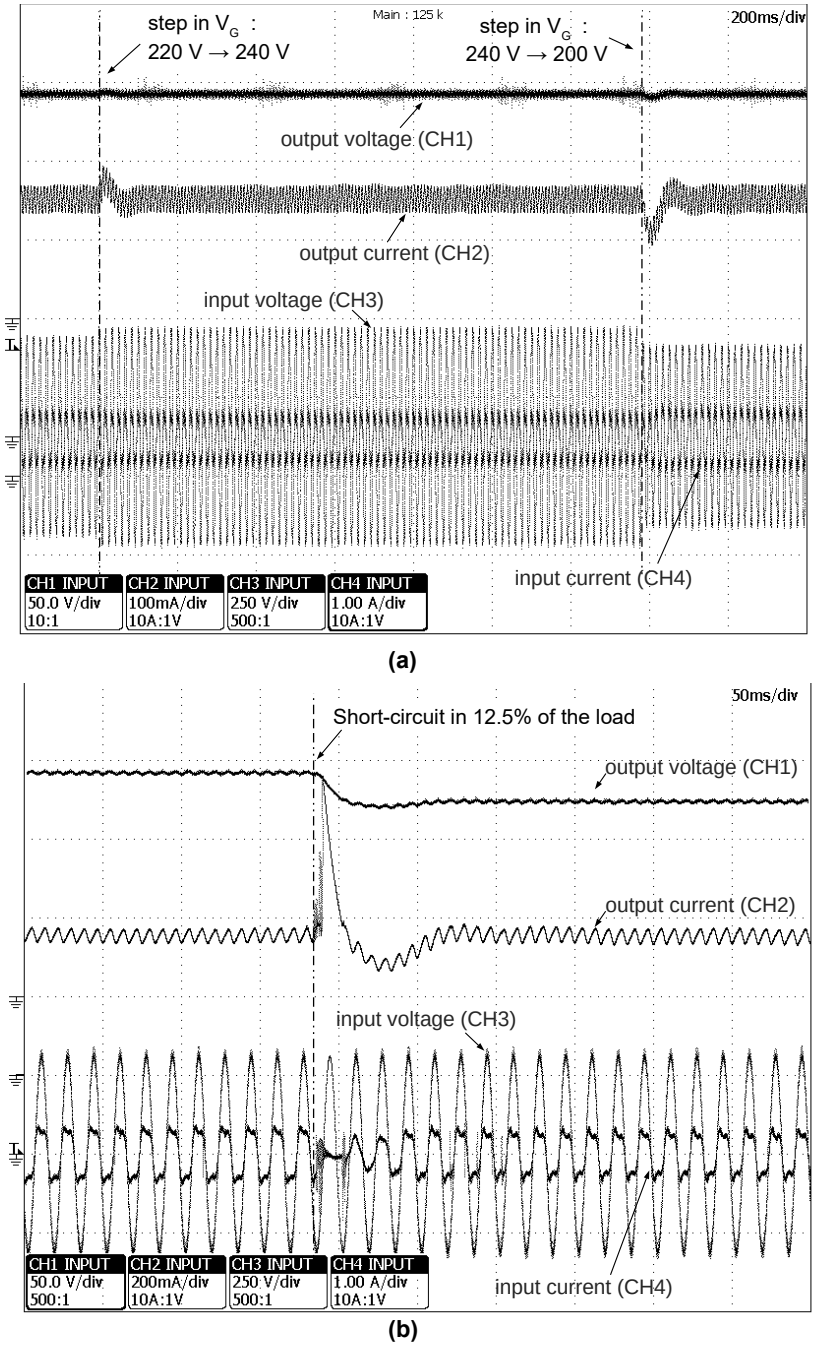


Figure 61: Dynamic behavior of the converter during steps of the input voltage (a) and the load(b). Output voltage (CH1: 50V/div), output current(CH2: 100 mA/div in (a) - 200 mA/div in(b)), input voltage (CH3: 250V/div) and input current (1A/div). Horiz. scale: 200 ms/div in (a) and 50 ms/div in (b).

This section presents the investigation of the ARC technique in an integrated topology in order to show the impact of the duty cycle modulation in this kind of converter.

The cascade connection of two buck-boost converters (ALONSO et al., 2011a)(ALONSO et al., 2012) is one of the simplest two-stage LED drivers. One advantage of this topology is that the input current of each stage does not depend on the output voltage,

which simplifies the converter analysis.

In order to reduce the number of controlled switches, the PFC and the PC stages can be integrated by applying a technique called "graft-scheme"(WU & CHEN, 1999) from the series connection of two buck-boost converters (Figure 62a). In the resultant topology, a single controlled switch is responsible for performing the functions of the main switches of both stages.

The integration technique presented in Wu and Chen (1999) ensures that the electrical characteristics of the new converter are the same as the topology composed by independent stages. However, both the PFC and the PC stages must have the same duty cycle and switching frequency. The integrated converter is obtained by identifying the connection between the active switches of both stages and then replacing them by a single one and some diodes. Based on Wu and Chen (1999), one can identify the connection type between the switches of the double buck-boost as the "i-T" (Figure 62b), in which the current stress of the new switch is the sum of the currents of the active switches of both stages (MARCHESAN, 2007). The resultant topology, called IDBB converter, is shown in Figure 62c.

For the analysis carried out in this section, the operating mode chosen for the converter was the full-DCM (*i.e.*, both stages in DCM), which allows for a further capacitance reduction when compared with the same converter with the PC stage operating in CCM (ALONSO et al., 2011a).

4.2.1 Analysis of the IDBB converter with duty cycle modulation

Since the driver is defined and the operating mode of both stages is also established, it is possible to evaluate the behavior of its main variables (*e.g.*, the output current). In off-line converters, it is well-known that those variables oscillate at twice the line frequency.

Therefore, it is suitable to derive a low-frequency large-signal circuit model in order to analyze the IDBB converter. This model can be seen in Figure 63, in which it is possible to observe that the energy transfer in the converter is performed in two stages. At first, the input power $p(t)$ is delivered to the dc bus via the PFC stage and then the PC stage transfers the dc bus power to the output. The losses in the power conversion process are represented by the efficiencies of the input and the output stages, which are η_{PFC} and η_{PC}, respectively. For the sake of simplicity, the analysis carried out on this chapter does not take into consideration the influence of the capacitor C_{out} for

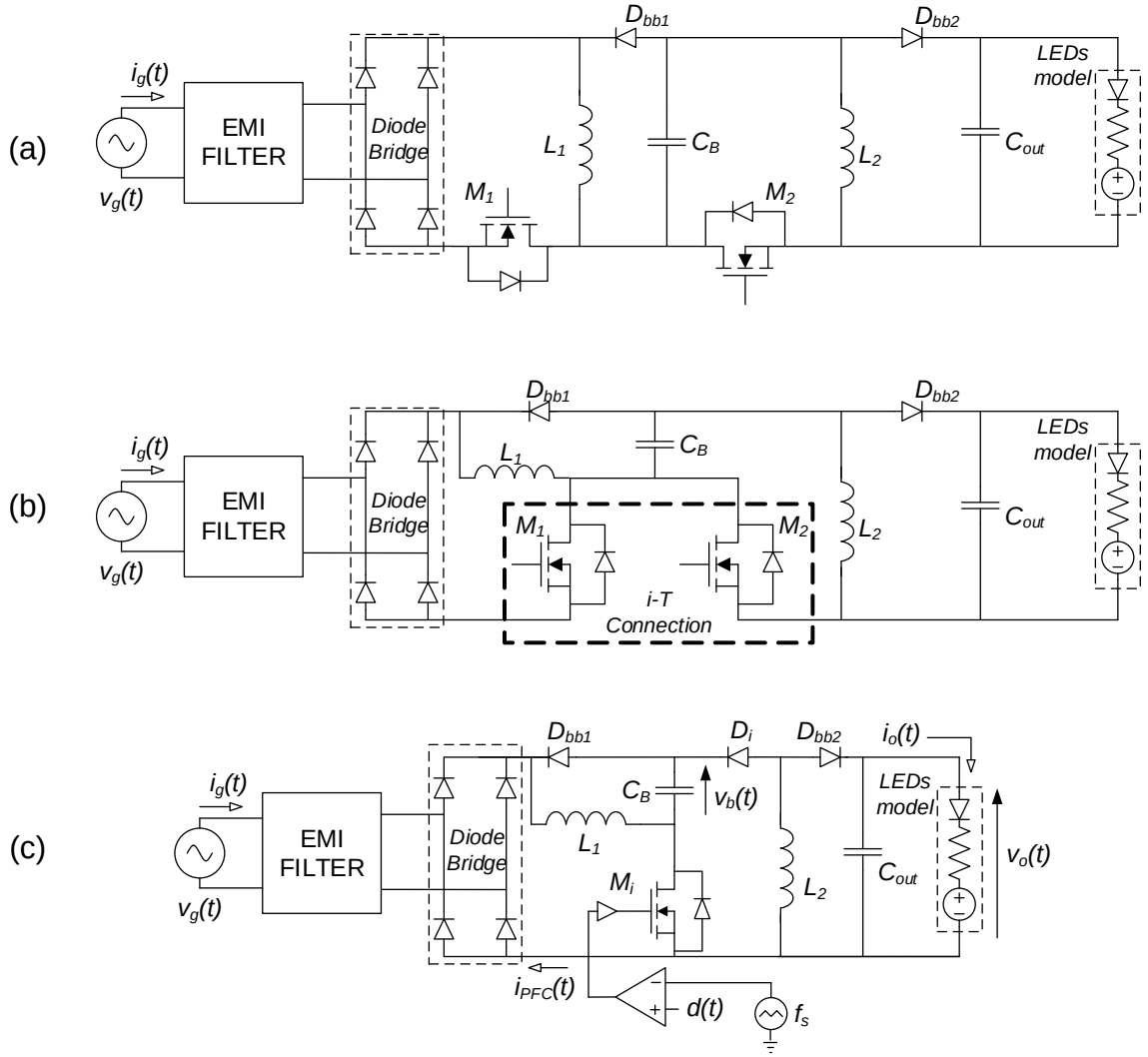


Figure 62: Two-stage converter based on the cascade connection of two buck-boost topologies. (a) independent stages; (b) i-T connection; (a) IDBB converter

the low-frequency ripple filtering, since this element is normally sized only to filter the high-frequency ripple (ALONSO et al., 2011a).

The instantaneous power at the input of the converter $p(t)$ is defined in (4.34) as the multiplication of the rectified input voltage, $|v_g(t)|$, defined in (4.3), by the input current $|i_g(t)|$, whose definition is stated in (4.35) (ALONSO et al., 2011a).

$$p(t) = |v_g(t)|\, i_{PFC}(t), \tag{4.34}$$

$$|i_g(t)| = i_{PFC}(t) = \frac{|v_g(t)|\, d(t)^2}{2L_1 f_s}, \tag{4.35}$$

in which L_1 is the inductance of the PFC stage.

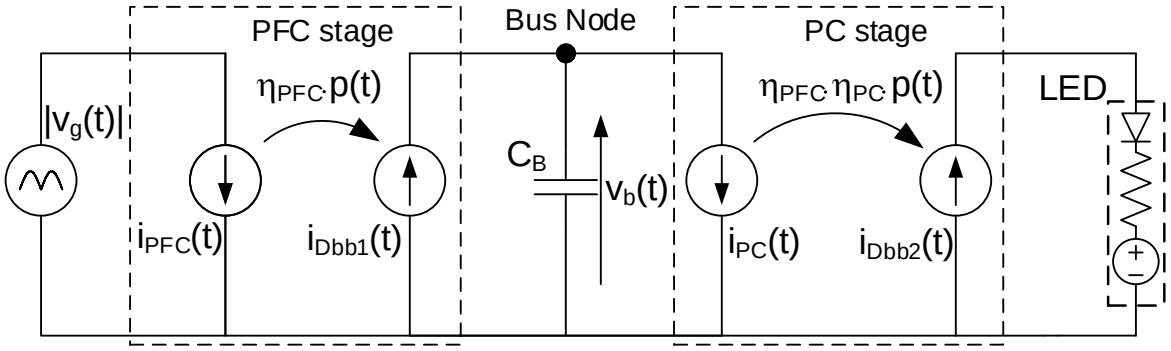


Figure 63: Large-signal low-frequency model of the IDBB converter.

Similarly of Section 4.1, for this analysis, the duty cycle signal will have the form defined by (4.4).

Since the input stage of the IDBB converter is based on the buck-boost topology, the expression of its input current is similar to the flyback converter. Therefore, equations (4.6)-(4.11) can be used to evaluate the input current of the IDBB converter under the duty cycle modulation just by replacing the magnetizing inductance L_m by the inductance L_1.

The current sources $i_{Dbb1}(t)$ and $i_{PC}(t)$ of the model presented in Figure 63 can be obtained by analyzing the current through D_{bb1} and the current at the input of the PC stage. These variables are defined in (4.36) and (4.37), respectively.

$$i_{Dbb1}(t) = \eta_{PFC}\frac{v_g(t)^2 d(t)^2}{2L_1 f_s v_b\,(t)}, \tag{4.36}$$

$$i_{PC}(t) = \frac{v_b\,(t)\,d(t)^2}{2L_2 f_s}, \tag{4.37}$$

where v_b is the instantaneous bus voltage and L_2 is the inductance of the PC stage.

The current through C_B can be calculated as follows:

$$i_{C_B}(t) = C_B\frac{dv_b}{dt} = i_{Dbb1}(t) - i_{PC}(t). \tag{4.38}$$

By manipulating (4.36), (4.37) and (4.38), the differential equation of the bus voltage is found, as shown in

$$\frac{dv_b(t)}{dt} = \frac{1}{2C_B f_s}\left(\eta_{PFC}\frac{v_g(t)^2 d(t)^2}{L_1 v_b(t)} - \frac{v_b(t)\, d(t)^2}{L_2}\right). \tag{4.39}$$

Regarding the output current of the IDBB converter, it can be found by evaluating the instantaneous power balance in the second stage of the LED driver, which is described by

$$p_b(t) = \frac{p_o(t)}{\eta_{PC}}. \tag{4.40}$$

The instantaneous bus power is obtained by multiplying the bus voltage and the input current of the second stage, which yields

$$p_b(t) = \frac{v_b(t)^2 d(t)^2}{2L_2 f_s}. \tag{4.41}$$

Thus, the expression of the power delivered to the LEDs is found by means of the equivalent load model, thus resulting in

$$p_o(t) = V_t i_o(t) + r_d i_o(t)^2. \tag{4.42}$$

By replacing (4.42) and (4.41) in (4.40) and solving for the output current, the expression of the current through the LED string is found, as shown in

$$i_o(t) = \sqrt{\left(\frac{V_t}{2r_d}\right)^2 + \eta_{PC}\frac{v_b(t)^2 d(t)^2}{2L_2 f_s r_d}} - \frac{V_t}{2r_d}. \tag{4.43}$$

In order to obtain the output current, the numerical method outlined in Section 4.1.1 was used, since there is not a closed-form solution for (4.39). A MATLAB pseudo-code for a function that performs this calculation is shown in Figure 64.

4.2.2 Design procedure

This section outlines the design procedure of the IDBB converter with the large-signal duty cycle modulation proposed in this work.

The input parameters for this design example are shown in Table 8. Differently of the design of the flyback converter addressed in Section 4.1, the IDBB converter will be sized considering a wide input voltage range, since this is suitable for improving the

```
function io = CalcIo(CB, D0, D2, φ2, L1, L2, fs, fL, VG, rd, Vt, ηPC)

% Auxiliary parameters
ts = 1/(fL * 1000);
tf = 5/fL;
ωL = 2 * π * fL;
T = 0 : ts : tf;
vb = zeros(size(T));
N = length(T) - 1;
vb(1) = 1;

% Solution of the output current
for k = 1 : N
    t = T(k);
    d = D0 + D2*sin(2*ωL*t+φ2);
    vg = √2*VG*sin(ωL*t);
    vb(k + 1) = vb(k) + ts*1/(2*CB*fs)*d^2*(vg^2/(L1*vb(k)) - (vb(k)/L2));
    io(k) = sqrt((Vt/(2 * rd))^2 + (ηPC * vb(k)^2 * d^2)/(2 * L2 * fs * rd)) − Vt/(2 * rd);
end
```

Figure 64: MATLAB pseudo-code for calculating the output current of the IDBB converter.

economic attractiveness of the proposal, as already commented in chapter 1. However, considering that the output current ripple varies with the input voltage, the converter must be designed under worst-case conditions, which occur for the lowest mains voltage (90 V in this case). Thus, the analysis in this section will consider this voltage level.

The LED luminaire, devised for street lighting purposes in this case, is composed by a module of LUXEON Rebel LEDs connected in series. It is important to highlight that for street lighting applications, the effects of flicker upon the human health are less hazardous (LEHMAN & WILKINS, 2014). Therefore, a ripple level of 50% was chosen in order to allow a minimization of the requiring filtering capacitances. Furthermore, for the sake of simplicity, the effects of the junction temperature variation are not taken into account in this design example.

4.2.2.1 Definition of the duty cycle function and calculation of the passive elements

In order to design the IDBB converter, the first step is to define the critical duty cycle D_{crit} for ensuring the full-DCM operation. This parameter can be calculated by means of:

$$D_{crit} = \min\left(D_{C\_PFC}, D_{C\_PC}\right), \tag{4.44}$$

Table 8: Parameters for the design of the IDBB converter

Item	Description	Value
V_G	RMS value of the input voltage	90 - 260 V
f_L	frequency of the mains voltage	60 Hz
f_s	switching frequency	50 kHz
I_o	average output current	500 mA
V_o	average output voltage	139.9 V
P_o	average output power	70 W
V_t	threshold voltage of the LED string	130.2 V
r_d	dynamic resistance of the LED string	19.34 Ω
ΔIo_{LF_max}	maximum peak-to-peak ripple of the output current	250 mA (50%)
ΔIo_{HF_max}	maximum high frequency ripple of the output current	30 mA
V_{B_max}	Maximum bus voltage	330 V
η_{PFC}	Efficiency of the PFC stage	0.922
η_{PC}	Efficiency of the PC stage	0.922

where D_{C_PFC} and D_{C_PC} are the values of the critical duty cycle of the PFC and the PC stage, respectively. According to Alonso et al. (2011a), those variables can be calculated by (4.45) and (4.46).

$$D_{C\_PFC} = \frac{V_{B\_\min}}{V_{B\_\min} + \sqrt{2}V_{G\_\min}}, \tag{4.45}$$

$$D_{C\_PC} = \frac{V_o}{V_o + V_{B\_\min}}, \tag{4.46}$$

where:

V_{G_min} - lowest value of the input voltage (*i.e.*, 90 V);

V_o - output voltage, defined in (4.47);

V_{B_min} - minimum bus voltage, defined in (4.48).

$$V_o = V_t + r_d I_o. \tag{4.47}$$

$$V_{B\_\min} = V_{B\_\max}\frac{V_{G\_\min}}{V_{G\_\max}}, \tag{4.48}$$

in which V_{G_max} is the input voltage (*i.e.*, 260 V).

Equation (4.48) states that the bus voltage varies linearly with the input voltage. As shown in (ALONSO et al., 2011a), this characteristic is a result of the integration

of the PFC and the PC stages when the converter is operating in full-DCM. In this case, the bus voltage of the IDBB converter depends only on a relationship between the inductances of both stages and the efficiency of the PFC stage, as shown in (4.49).

$$V_B = \sqrt{\frac{\eta_{PFC} L_2}{L_1}} V_G, \tag{4.49}$$

Similarly to the analysis performed in Section 4.1, in order to ensure the full-DCM operation, the sum of the dc level and the amplitude of the ac portion of $d(t)$ must be lower than the critical duty cycle for the whole operating range. By using the values of Table 8 in (4.44)-(4.48), it is possible to obtain $D_{crit} = 0.473$.

In this section, the calculation of the inductance is performed differently of Section 4.1.1: it is considered that the modulation of the duty cycle does not influence the active power processed by the converter. The error related to this assumption can be estimated by means of (4.50), which was derived comparing the average power P_{in} with and without the modulation of $d(t)$.

$$\begin{aligned} error &= \frac{P_{in}\left[D_0 + D_2 \sin\left(2\omega_L t + \phi_2\right)\right]}{P_{in}\left(D_0\right)} - 1 \\ &= \frac{2}{D_0} \times \frac{2}{T} \int_0^{2/T} \sin^2\left(\omega_L t\right) \times \left(D_0 + D_2 \sin\left(2\omega_L t + \phi_2\right)\right) dt - 1 \end{aligned} \tag{4.50}$$

Figure 65 presents the relative error of the input power as a function of the angle ϕ_2 for several values of D_2. One can note that as the relative amplitude of D_2 increases, the error also grows. However, if $D_2 < 20\% D_0$, the error is lower than 10% regardless the value of ϕ_2.

Therefore, by choosing $D_0 = 0.36$ and assuming that the maximum value of the amplitude of the ac portion of $d(t)$ is $D_{2\_max} = 0.05$, the inductance L_1 can be calculated by means of (4.51)[1] with an error lower than 10%. It is important to highlight that if a close loop system like the one presented in Figure 52 is used, the value of D_0 will be compensated in order to null the steady state error.

$$L_1 = \eta_G \frac{{D_0}^2 {V_{G\_\min}}^2}{4 V_o I_o f_s}, \tag{4.51}$$

where $\eta_G = \eta_{PFC} \times \eta_{PC}$ is the global efficiency of the converter.

[1]Equation (4.51) does not consider the ac portion of the duty cycle for calculating the average input power.

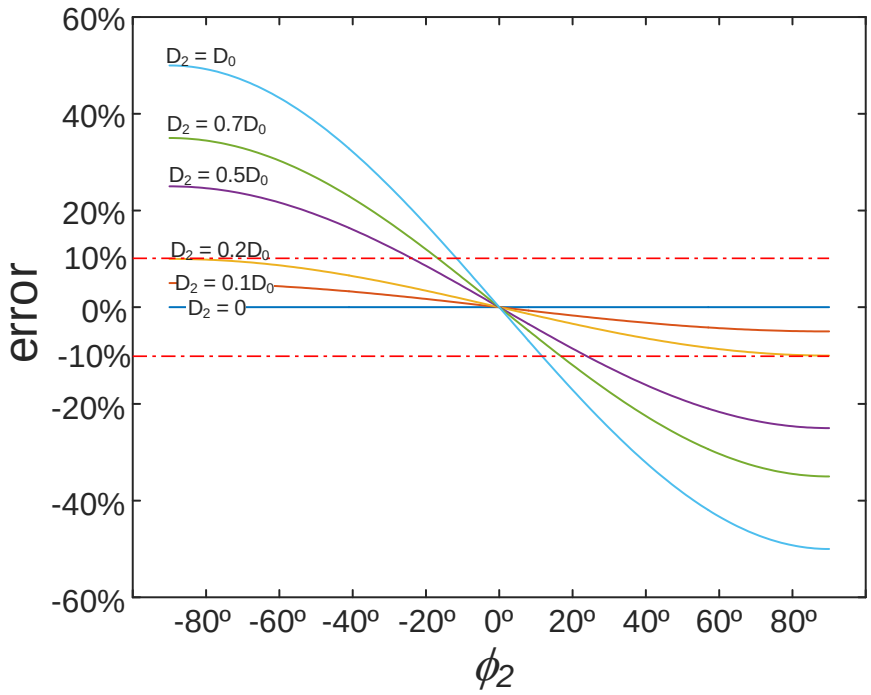


Figure 65: Relative error of the IDBB converter input power with ARCT considering only the average value of the duty cycle.

Since all the design parameters are chosen, the calculation of the inductances can be performed by using the values of Table 8 in (4.51) and then by using (4.49) considering $V_G = V_{G\_min}$ and $V_B = V_{B\_min}$. Moreover, the calculated global efficiency is 85%, yielded from the product of the efficiencies of the PC and the PFC stages stated in Table 8. The described calculation procedure yields $L_1 = 127$ μH and $L_2 = 204$ μH.

Owing to the duty cycle modulation, the output ripple of the IDBB converter is directly affected. Therefore, it is necessary to design the parameters D_2 and ϕ_2 together with the capacitor C_B so that the value of this component is calculated taking into account the effects of the duty cycle modulation.

As performed in Section 4.1.1.1, the calculation of the ac component of the duty-cycle signal must be accomplished in two steps. The first one is the evaluation of the behavior of the input current owing to variations of the magnitude and phase of the oscillating portion of $d(t)$. This analysis yields the allowable limits for D_2 and ϕ_2 based on the constraints imposed by the IEC-61000-3-2:2014 standard.

After the definition of the allowable values for the ARC parameters, the calculation of such quantities is performed simultaneously with the bus capacitor C_B so that the output ripple is below the desired limits, constrained in Table 8 (*i.e.*, 50% peak-to-peak), whereas the value of C_B is chosen to be the lowest possible.

Since the input current waveform does not depend on the bus capacitance, the behavior of its harmonic content according to the variations in D_2 and ϕ_c can be graphically visualized. By using the parameters defined in Table 8 and also the calculated values of D_0, L_1 and L_2, the input current 3rd and 5th harmonics can be plotted, as shown in Figure 66. This illustration shows that the 3rd harmonic component is closer to its IEC limit than the 5th and, therefore, it restricts the range of D_2 and ϕ_2. Nevertheless, if D_2 is kept below D_{2_max}, the converter will comply with the IEC-61000-3-2:2014 regardless the value of ϕ_c, as clearly seen in Figure 66a.

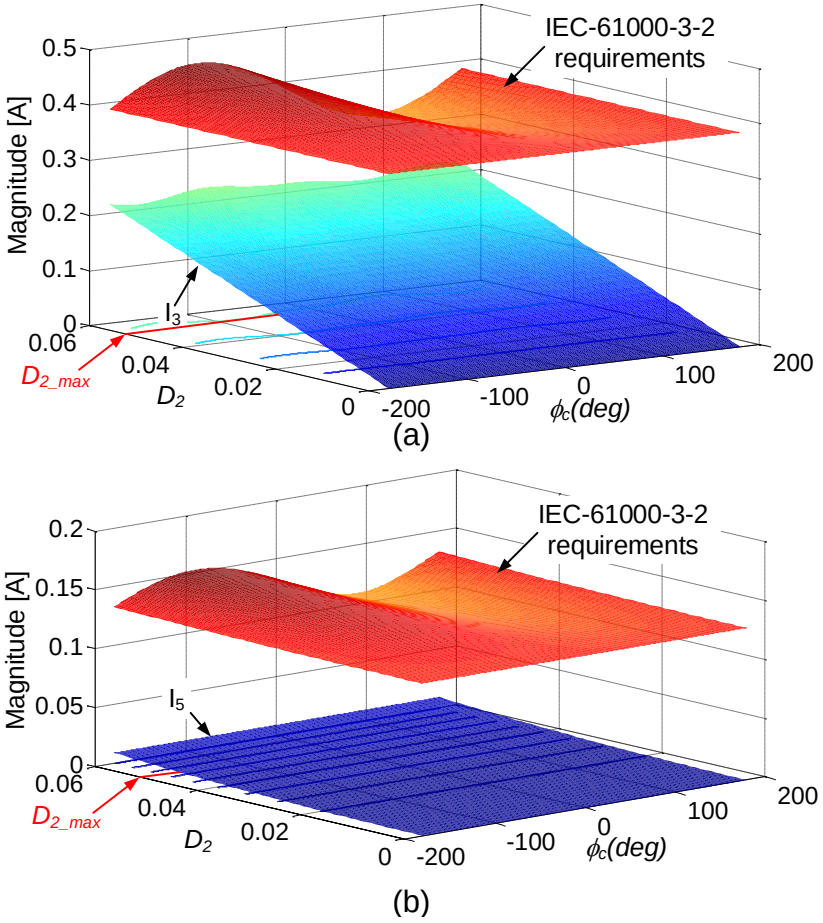


Figure 66: Harmonic content of the input current according to the oscillating component of the duty-cycle: (a) third harmonic component.; (b) fifth harmonic component.

The design of C_B, D_2 and ϕ_c must be performed simultaneously so that the output current ripple is lower than ΔIo_{LF_max}, which was stated in Table 8. Since the output current ripple can be obtained from (4.43) by using a numerical solution (Figure 64), the capacitor can be chosen through a graphical analysis of a design abacus plotting C_B against D_2 and ϕ_c parameterized.

Figure 67 shows these curves. The low-frequency output current ripple behavior according variations in D_2 and ϕ_c for several values of C_B are plotted. As can be seen,

for each value of C_B, a family of curves is generated, being each one parameterized by a certain value of D_2, with values ranging from $D_2 = 0$ up to $D_2 = D_{2\_max}$ in steps of 0.005.

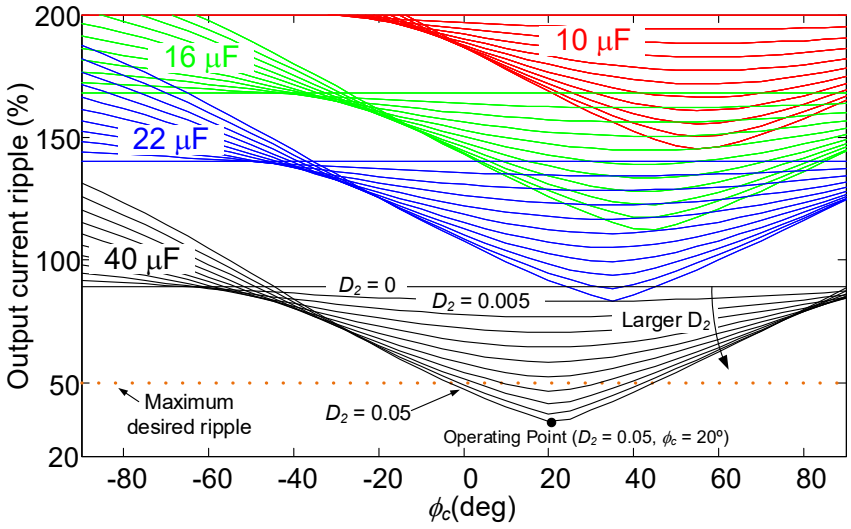


Figure 67: Behavior of the peak-to-peak output current ripple according to the ARC parameters for several values of C_B.

From Figure 67 it is possible to observe that the ARC parameters have a high influence on the output current ripple value, as expected. Furthermore, one can also notice the behavior of the converter without the ARC technique, analyzing those curves in which D_2 value is zero (no large-signal modulation whatsoever). As can be seen, if C_B is chosen to be equal to 10 μF, 16 μF or 22 μF, the ripple criterion will not be met regardless of the ARCT parameters. However, if a capacitance of 40 μF is selected, the output ripple will be lower than ΔIo_{LF_max} if $D_2 \geq 0.04$ and $0^o \leq \phi_c \leq 40^o$.

By using this graphical analysis, the chosen ARC parameters were $D_2 = 0.05$ and $\phi_c = 20^o$ because this operating point makes the output current ripple to be at its minimum for $C_B = 40$ μF. Furthermore, this choice maximizes the robustness of the system: even if D_2 decreases by 20% and ϕ_c varies by $\pm$ 20^o, the output ripple will remain below the maximum desired value of 50%. The theoretical value of the output ripple for the chosen parameters is 34.3%.

Figure 67 also shows that without employing the ARC (*i.e.*, $D_2 = 0$), a 40 μF bus capacitor would be insufficient to meet the ripple requirements. This shows that such effectiveness of the proposed technique.

It is important to highlight that the bus capacitance value can be further decreased if a larger value of V_B is chosen. However, such choice would affect negatively the

efficiency of the converter, since the voltage stress in the semiconductors would be higher.

By analyzing these results, it is possible to note that the ARC technique provides an advance towards capacitance reduction in two-stage converters. This mechanism becomes quite important when the others cannot be fully applied. For example, in converters with universal input voltage it is not possible to choose a high value for V_B for the lowest input voltage (*e.g.*, 90 V), since it would lead to an extremely high voltage stress in the semiconductors when the input voltage is at its maximum value (*e.g.*, 260 V). Therefore, the mechanism of high voltage ripple filtering is not suitable for such applications whereas the ARCT can be used for minimizing the required filtering capacitance in such situations.

Finally, the output capacitor of the PC stage must be designed to filter the high-frequency component of the output current, which is described by (4.52) for the buck-boost converter (ALMEIDA; SOARES & BRAGA, 2013). Taking into account this equation, the constraints stated in Table 8 (*i.e.*, $\Delta I_{o\_HF} < 30$ mA) and the laboratory availability, the chosen output capacitor was 16 μF.

$$\Delta I_{o\_HF} = \frac{1}{f_s C_{out} r_d} \left(I_o + \frac{\Delta I_{o\_LF}}{2} \right) \left(1 - D_0 \frac{V_{B\_\min}}{V_o} \right). \tag{4.52}$$

4.2.2.2 Design of the control loop

The design of the control loop for the IDBB converter was carried out using the same directives presented in Section 4.1.1.2. Table 9 summarizes the parameters of the control circuit and the coefficients of the difference equations are shown in Table 10.

Table 9: Control circuit parameters

Parameter	Value
K_a	20 Hz
K_{bp}	1
B	125.66 rad/s
K_{ps}	$6.33 \cdot 10^{-1}$
z_{ps}	$8.72 \cdot 10^{2}$ rad/s
p_{ps}	$6.52 \cdot 10^{2}$ rad/s

Table 10: Coefficients used in the discrete implementation

Coefficient	Value	Coefficient	Value	Coefficient	Value
N_{a1}	0.002	N_{bp1}	0.012341	N_{ps1}	0.646
N_{a2}	0.002	N_{bp2}	-0.012341	N_{ps2}	-0.5424
N_{a3}	-1	N_{bp3}	-1.953	N_{ps3}	-0.8776
		N_{bp4}	0.97532		

4.2.3 Simulation results

This section presents some simulation results of the proposed system. This analysis was carried out by means of the software PSIM. The circuit used in the simulation is presented in Figure 68. One can note that a "C block" component was added to the circuit in order to simulate also the digital control system. The program embedded in this block is based on the flowchart presented in Figure 54 except that the error signal is calculated externally. Moreover, a resistor *R_loss* was placed in parallel with the capacitor C_B in order to emulate the losses of the converter. The code used in the C-block can be seen in Appendix A.3.

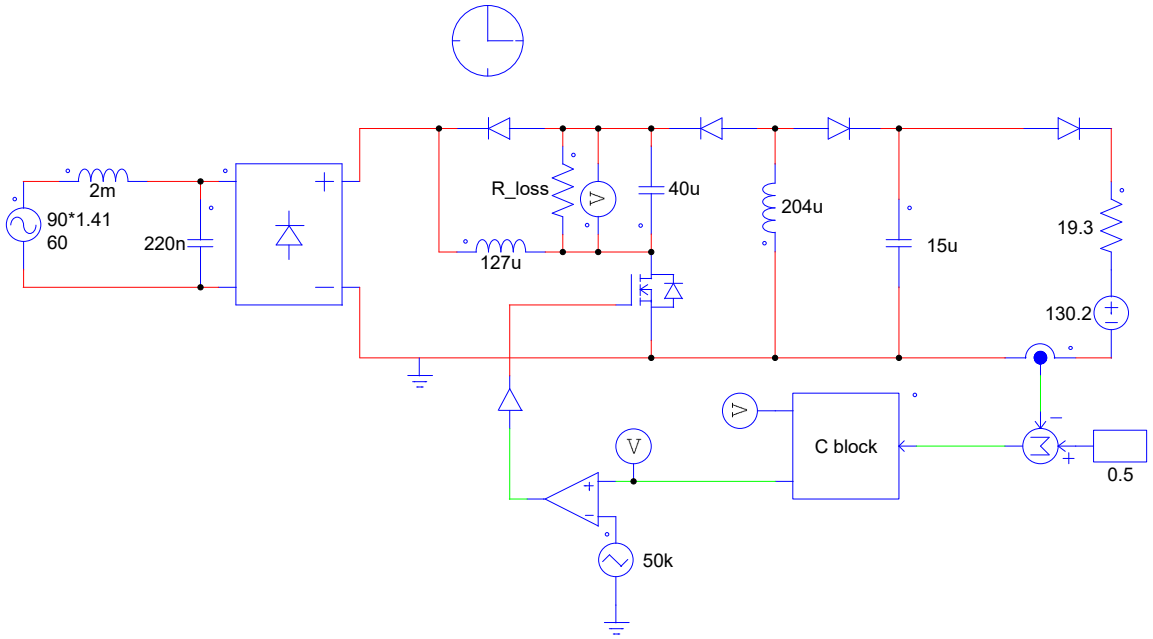


Figure 68: Circuit used in the simulation of the IDBB converter with ARCT.

Figures 69, 70 and 71 show some simulation results for $V_G = \sqrt{2} \cdot 90\,V$. In this simulation, $R\_loss = 904\,\Omega$ so that the efficiency of the converter was 85%, which was the value used in the calculations.

Figure 69a shows the input waveforms of the converter. The power factor of the

circuit was 0.971 and the THD of the input current was 18%. Regarding the bus voltage and the output waveforms, they can be observed in Figure 69b. The average value of $v_b(t)$ is 113.7 V, which is quite similar to the theoretical value calculated by (4.49) (114 V). Figure 69b also shows the characteristic of the output current, whose LFR was 177 mA (35.4%), which is also close to the predicted value (34.3%).

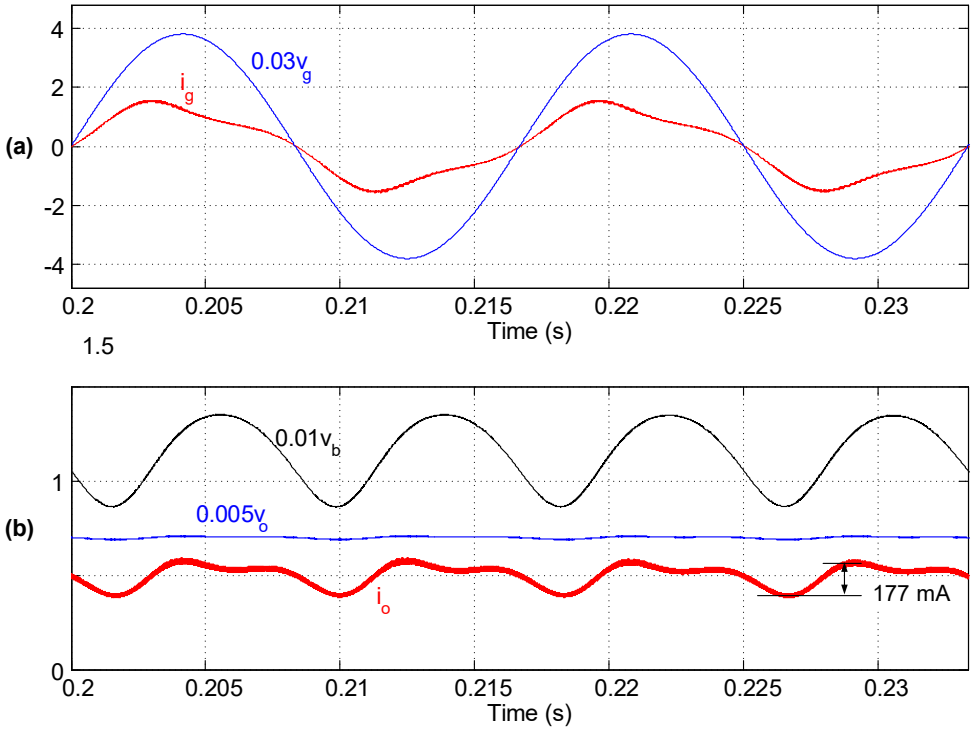


Figure 69: Simulation results for $V_G = \sqrt{2} \cdot 90\,V$. (a) Input variables; (b) bus voltage and output variables.

Figure 70 shows the behavior of the signal $d(t)$, which is also very similar to the theoretical value (*i.e.*, $D_0 = 0.36, D_2 = 0.05$ and $\phi_c = 20°$). Note that dc portion (*i.e.*, 0.337) differs a little from its calculated value (*i.e.*, 0.36). This occurs because the assumption that the ac portion of $d(t)$ does not influence in the active power. However, as commented in subsection 4.2.2.1, the control loop was able to compensate D_0 so that the steady-state error of the output current was null.

The full DCM operation can be verified by means of Figure 71, in which it is possible to observe that the inductors of both stages are operating in DCM.

Figure 72 shows some simulated waveforms for $V_G = \sqrt{2} \cdot 260\,V$. In this case, the resistor *R_loss* was changed to $8.825\,k\Omega$ to keep the same efficiency of the converter (*i.e.*, 85%). One can note that the output current low-frequency ripple when $V_G = \sqrt{2} \cdot 260\,V$ is almost null. This occurs because the bus voltage increases linearly with the line voltage, achieving 310 V in this situation and, consequently, the LFR reduces.

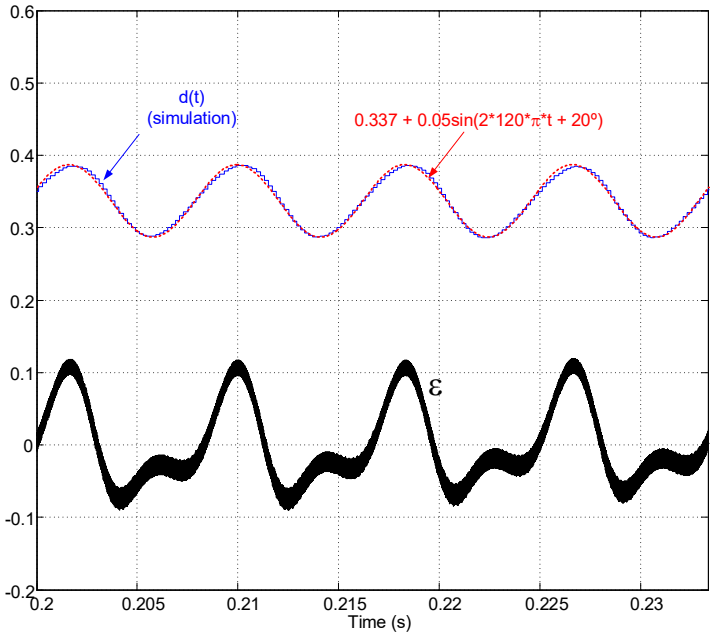


Figure 70: Simulation of the signal $d(t)$ and the error signal ϵ.

This ripple reduction shows the high-voltage ripple filtering capability of the IDBB converter. On the other hand, owing to the control structure, once the ripple decreases, the ARCT branch output also reduces and the signal $d(t)$ tends to a pure dc signal (Figure 70), that is, the circuit operates like a conventional IDBB converter. The power factor of the converter at $V_G = \sqrt{2} \cdot 260V$ was 0.995 and the THD of the input current was 4.3 %.

These results show that the proposed technique is effective when the LFR is high by the cost of increasing the THD of the input current. On the other hand, the the ARC branch is "automatically disabled" for the small ripple conditions, reestablishing the good performance of the PFC stage. Therefore, these characteristics makes the ARC technique an interesting solution for reducing the filtering capacitances in off-line integrated converters.

4.2.4 Experimental results

In order to attest the performance of the ARC technique in the IDBB converter, a laboratory prototype was built. The prototype's components values are given in Table 11 and a photograph of it is shown in Figure 74. As can be seen, only metalized film capacitors were employed in the power circuitry, thanks to the ARCT ability to reduce the capacitances needed to achieve the desired output ripple level.

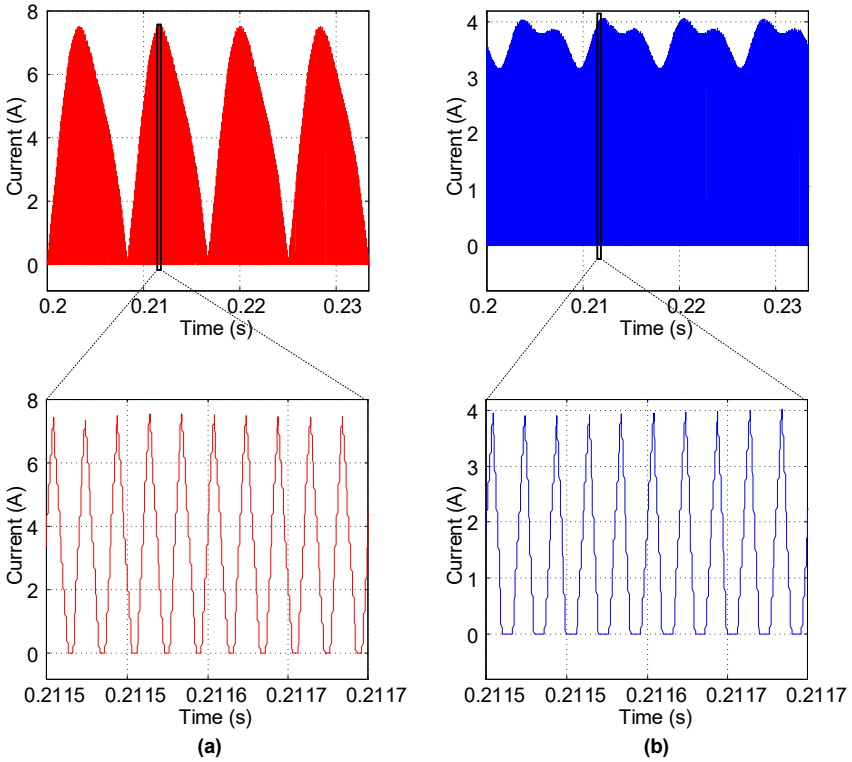


Figure 71: Simulation of the low-frequency and high-frequency behavior of the inductors's current: (a)Inductor L_1 ; (a)Inductor L_2.

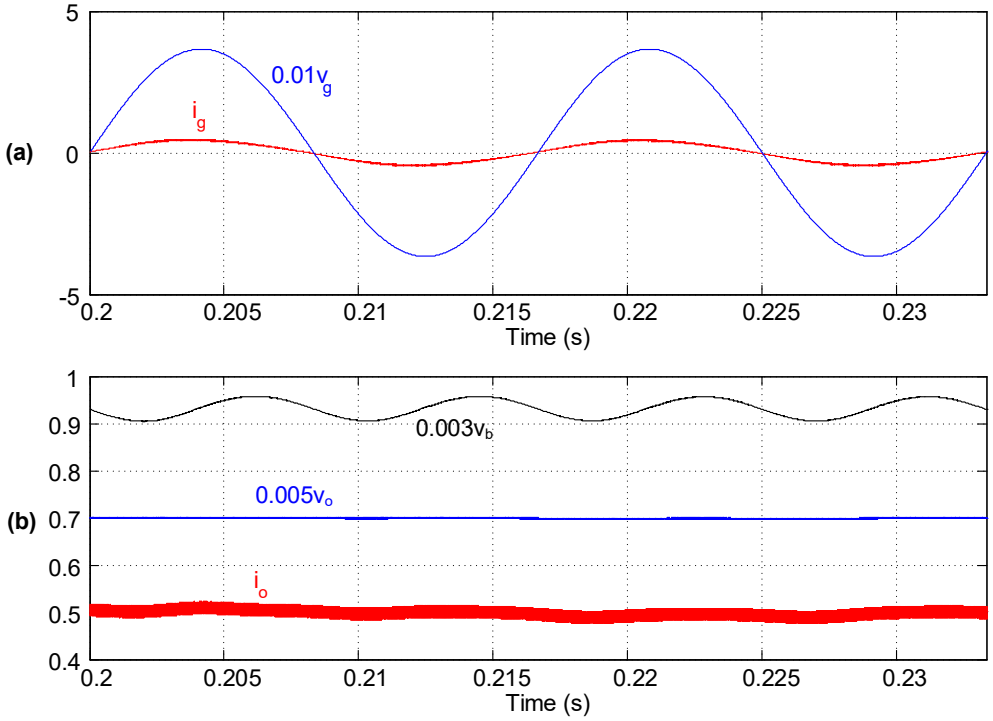


Figure 72: Simulation results for $V_G = \sqrt{2} \cdot 260V$. (a) Input variables; (b) bus voltage and output variables.

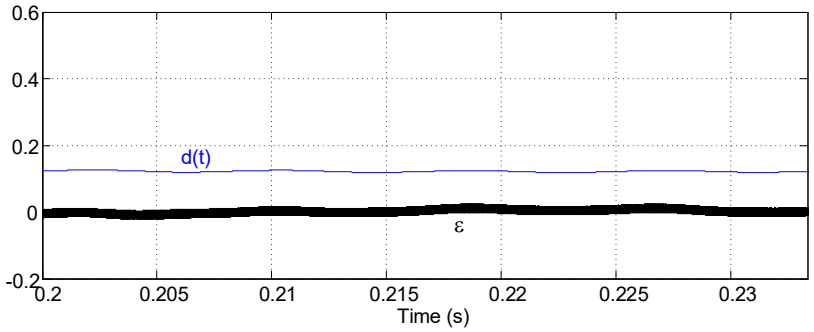


Figure 73: Simulation of the signal $d(t)$ and the error signal ϵ for $V_G = \sqrt{2} \cdot 260V$.

Table 11: Prototype parameters

Item	Description	Value
L_{DM1}, L_{DM2}	differential-mode inductors of the EMI filter	1 mH
C_{f1}, C_{f2}	capacitors of the EMI filter	33 nF/400V (polyester film)
L_{CM}	common-mode choke	10 mH
DB	diode bridge	GBU4J
L_1	PFC inductor	127 μH (E30 core)
L_2	PC inductor	204 μH (E30 core)
C_B	bus capacitor	40 μF/ 450V (polypropylene film)
C_{out}	output capacitor	16 μF/ 450V (polypropylene film)
M_i	main switch	SPP08N80C3
D_{bb1}	PFC diode	MUR 460
D_{bb2}	PC diode	MUR 460
D_i	diode of the integrated stages	MUR 460
$U1$	microcontroller	TM4C123G

As can be seen, the capacitance reduction provided by the ARC approach allowed for the use of polypropylene film capacitors, which are commercially available in the required values. However, if the application is cost-sensitive, the use of long-life electrolytic capacitors could be suitable, since they are cheaper than film ones. However, even in such applications, the ARC technique improves the cost-effectiveness of the system by reducing the value of capacitance and consequently the price. Furthermore, the proposed technique also enlarges the reliability of the driver, since lower capacitance leads to a higher MTBF (mean time between failures), as already addressed in section 3.1.

Figure 75a shows some selected experimental results for 90 V RMS, which is the worst case in terms of output current ripple. The theoretical behavior, predicted from the analytical analysis of subsection 4.2.2.1, for the input and the output currents has been sketched in dashed lines, as a reference, on top of the oscillograms. There is only a slight deviation between the theoretical and the experimental waveforms, which

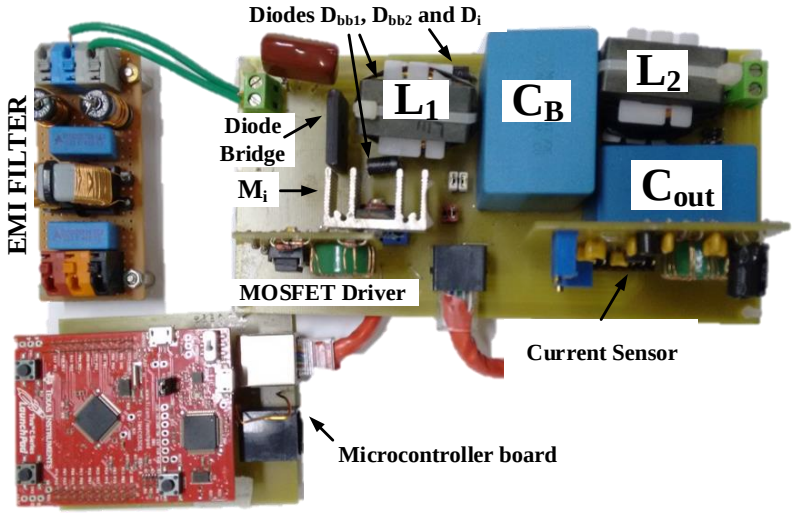


Figure 74: Top-view of the complete prototype, showing both power and digital control circuitry, along with the MOSFET driver and current sensor boards (mounted vertically).

could be attributed in part to the simplifications that might have been adopted in part of the mathematical modeling. However, the general behavior is very similar, proving the validity of the presented technique and analysis. In order to compare the proposed control technique with the conventional approach, Figure 75b shows the same experimental results for the converter without the ARCT. The low-frequency ripple in Figure 75a was 44% while in Figure 75b it was 80%. This means that an IDBB converter with the same elements, but without using the ARCT, have an output ripple 36% higher.

Figure 76 shows the same waveforms of Figure 75 for an input voltage of 260 V RMS. One can note that a similar result of the one presented in subsection 4.2.3 was obtained, in which the LFR is negligible and the converter behaves as a conventional IDBB with a high power factor.

Figure 77 shows the efficiency of the converter according to variations in both the input voltage (Figure 77a) and the output load (Figure 77b). The curve of Figure 77a was obtained for the nominal load and the values of Figure 77b were gathered at an input voltage of 115 V RMS. These curves show that the efficiency of the converter improves when the input current of the converter is lower, which occur for higher input voltages or light load conditions. This behavior is expected since the integration scheme used to derive the IDBB converter leads to higher current stress in the main switch (WU & CHEN, 1999), increasing the losses in this semiconductor. Furthermore, owing

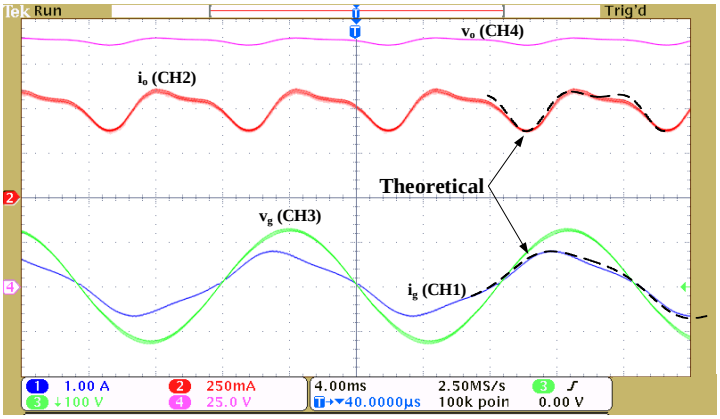


Figure 75: Experimental waveforms obtained with ARCT (a) and without ARCT (b) for an input voltage of 90 V RMS. Input current (CH1 - 1A/div), output current (CH2 - 250 mA/div), mains voltage (CH3 - 100/div) and output voltage (CH4 - 25 V/div). Horiz. Scale: 4 ms/div.

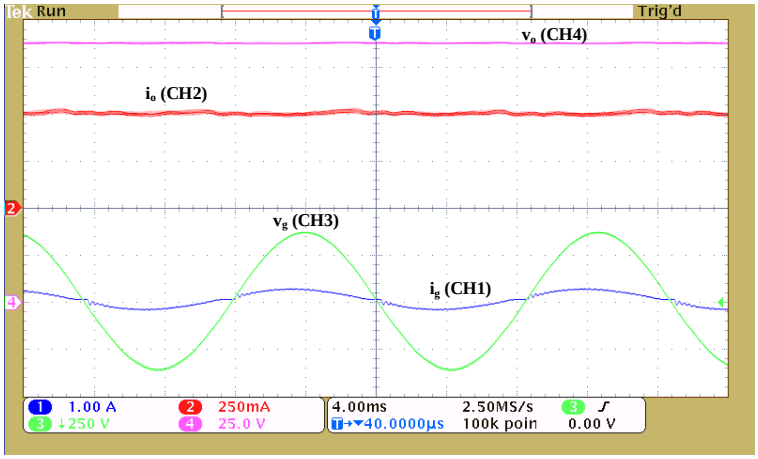


Figure 76: Experimental waveforms obtained for an input voltage of 260 V RMS. Input current (CH1 - 1 A/div), output current (CH2 - 250 mA/div), mains voltage (CH3 - 250/div) and output voltage (CH4 - 25 V/div). Horiz. Scale: 4 ms/div.

to the chosen bus voltage for this application, the voltage stress at this input voltage level do not have a major impact on the efficiency as the current stress does.

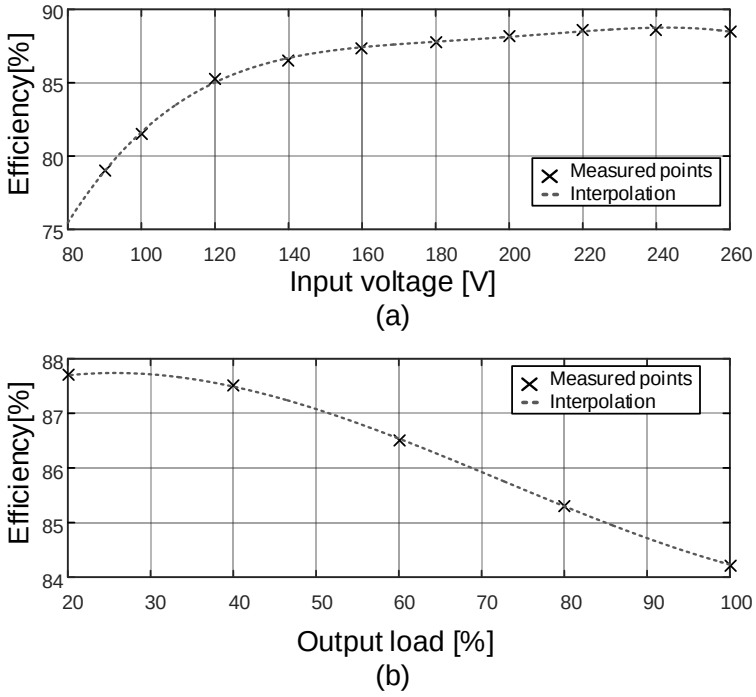


Figure 77: Efficiency of the converter. (a) Behavior for variations of the input voltage at full-load;(b) behavior for variations of the output load with $V_G = \sqrt{2} \cdot 115\,V$.

Figure 78 shows the harmonic content of the input current of the converter in two distinct cases: the behavior when the ARCT is used and when no modulation of the duty-cycle is present (*i.e.*, without ARCT). As it can be seen, the input current is in compliance with the IEC-61000-3-2:2014 for both cases, and the magnitudes of the harmonic components are also similar to those predicted. Note that the harmonics from 21^{st} to 39^{th} were omitted in this graph since their values were negligible.

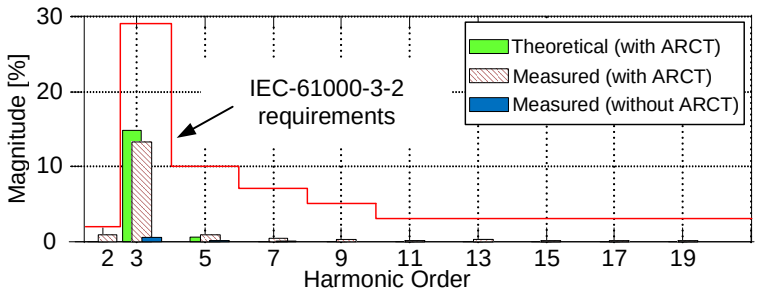


Figure 78: Harmonic content of the input current compared to the limits imposed by the IEC-61000-3-2:2014 standard (class C equipment). $V_G = \sqrt{2} \cdot 90$ V

Figure 79 shows the variation of the power factor and THD with the input voltage. As can be seen, the performance of the PFC stage improves as the input voltage

increases because the output of the ARC branch becomes negligible for higher input voltages, as already discussed. Nevertheless, one can also note that both the PF and the THD undergoes a deterioration for input voltages above 180 V RMS. This phenomenon is not related to the ARC but to the EMI filter, which was empirically tunned to 90 V RMS and presents a worsening of its performance for higher input voltages.

Although a lower harmonic content on input current is obtained when the ARC is not used (classical solution), not modulating the duty-cycle in a controlled manner (as the ARC does) leads to undesirably high output current ripple, as shown in Figure 75.

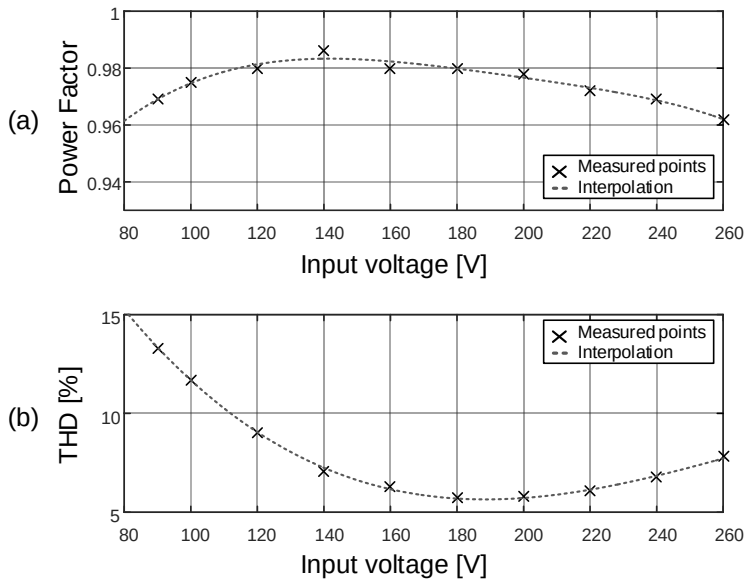


Figure 79: Variation of the power factor (a) and THD (b) with the line voltage.

The behavior of the output current ripple for the desired input voltage range (90-260 V) is shown in Figure 80 also for both conditions, with and without the proposed ARC technique. The theoretical characteristic of the converter if only the average current compensator (C_{avg}) is present was also plotted along, *i.e.*, when using a conventional control scheme. The results show that the output current ripple is lower when the ARC is used regardless the input voltage.

By using the theoretical analysis as presented in subsection 4.2.2.1, if one choses $D_2 = 0$ (no ARC whatsoever), it is possible to demonstrate that a capacitance of *c.a.* 76 μF would be necessary at the bus for the conventional system to achieve an output current ripple lower than 50%. This result means that the proposed system provided a reduction of 46.3% in the required filtering capacitance when compared to a conventional system.

The differences between the theoretical prediction and the experimental results

occur mainly due to the efficiency of the converter, which varies according to the input voltage (Figure 77), whereas it was considered constant in the theoretical analysis (*i.e.*, 85%). Another source of error is the discrete implementation of the band-pass and phase-shift filters, which can generate values of D_2 and ϕ_c a little different from those calculated. Nevertheless, the output ripple was kept below the maximum desired level for the whole operating range, which shows the robustness of the proposed system even when considering some typical implementation demeanors.

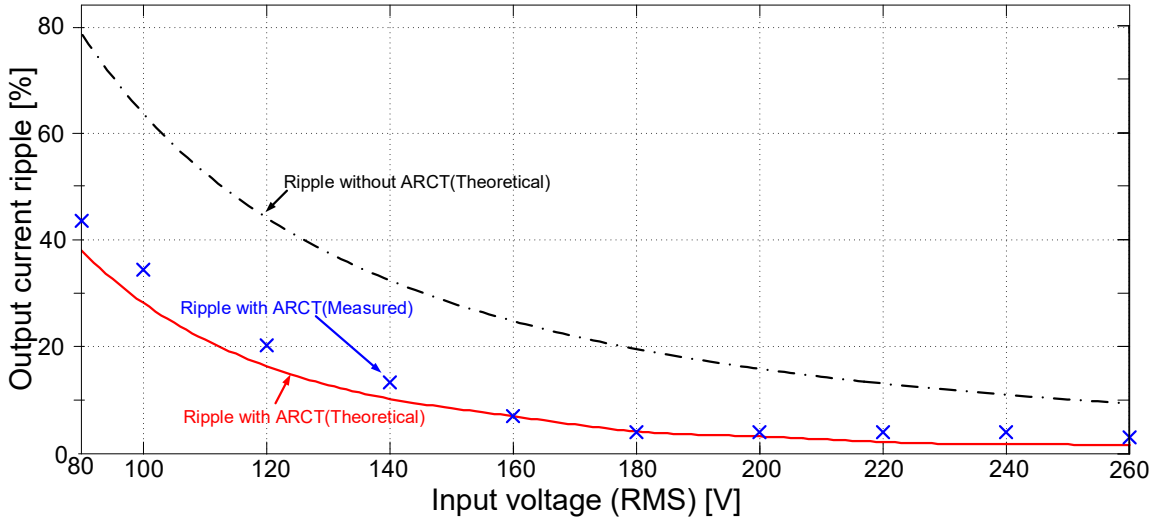


Figure 80: Behavior of the output current ripple for variations in the mains voltage magnitude.

Figure 81 shows the bus voltage for two load conditions. In order to analyze the ripple behavior, these waveforms were obtained for the lowest value of the input voltage (90 V), for which the higher ripple should be expected. In Figure 81, both conditions were compiled in a single picture by using the memory function of the oscilloscope. As can be seen, the average value of the bus voltage was similar in both cases (about 98 V), which a little below the theoretical value (*i.e.*, 114 V). This occurs because equation (4.49) does not consider the losses of the converter, which have an effect of decreasing the bus voltage. The figure also shows that the low-frequency ripple of the bus voltage dramatically reduces with light loads.

Figure 82 shows the current and voltage waveforms of the main switch M_i, in which the MOSFET current ramps up from zero, reducing the switching losses. Finally, the full-DCM can be verified by means of Figure 83, which shows a similar behavior of the simulated results presented in Figure 71.

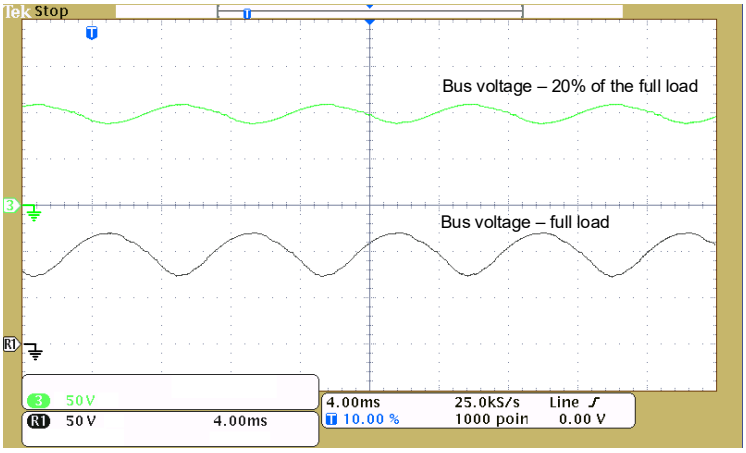


Figure 81: Behavior of the bus voltage according to load variations for an input voltage of 90 V. Bus voltage for 20% of the full load (CH3 - 50 V/div); Bus voltage for full load (R1 - 50 V/ div). Time scale: 4 ms.

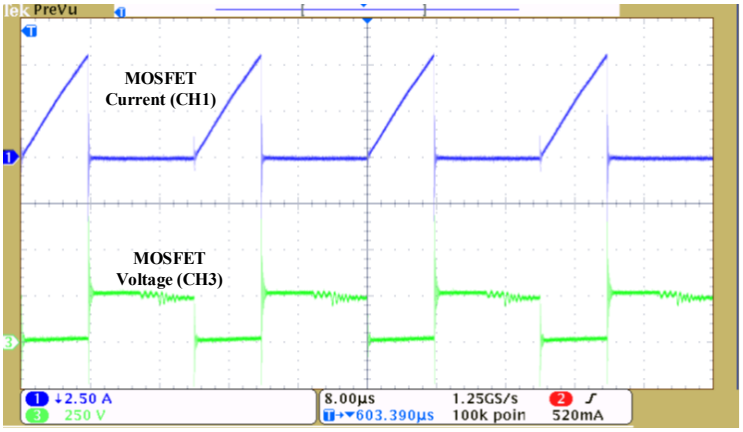


Figure 82: Current (CH1, 2.5 A/div) and voltage (CH3, 250 V/div) measured at the MOSFET in the peak of the rectified voltage.Time scale: 8μs/div.

4.3 SUMMARY OF THE CHAPTER

This chapter introduced Active Ripple Compensation (ARC) technique: an approach devised to reduce the LFR in off-line VMC LED drivers by means of the proper modulation of the converter duty cycle. A parametric duty-cycle function $d(t)$ was proposed, whose characteristic allowed for the change of the conventional low-frequency behavior of the studied converters. The mathematical analysis showed that by using the proposed modulation scheme it is possible to reduce the required filtering capacitances while still maintaining the harmonic content of the input current in compliance with the IEC-61000-3-2:2014 Class C.

The proposal was investigated in the off-line flyback-based LED driver and also

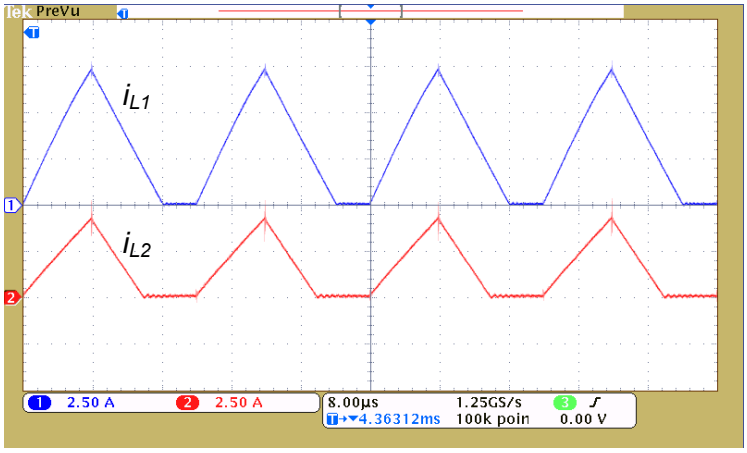


Figure 83: High frequency behavior of the current of the inductors L_1 (CH1, 2.5 A/div) and L_2 (CH2, 2.5 A/div) measured at the peak of the rectified voltage ($V_G = \sqrt{2} \cdot 90$). Time scale: 8 μs/div.

in an Integrated Double Buck-boost converter. In both cases, design examples were presented in detail, highlighting the sizing of the passive elements based on design abacuses. Since there is no parallel with classical VMC control, a novel control loop scheme has been proposed for the converter and its implementation aspects were addressed.

Experimental results attested the theoretical analysis, showing that the ARC technique allowed for a capacitance reduction of 24.2 % in the flyback converter and 46.3% in the IDBB topology at the cost of an increase in the THD of 25.54% and 14%, respectively.

The next chapter will present a more general study regarding the ARC technique by considering other harmonics in the duty cycle function, other topologies and also different design conditions.

5 OPTIMIZED DESIGN OF LED DRIVERS WITH ACTIVE RIPPLE COMPENSATION CONTROL

The previous chapter introduced the use of low-frequency duty cycle modulation for capacitance reduction in off-line LED drivers. Two cases were investigated using the flyback converter and the Integrated Double Buck-boost (IDBB) topology. It was possible to note from the first analysis that the modulation of the duty cycle can lead to a large capacitance reduction. Furthermore, its implementation requires just an additional branch in the conventional control structure of the converter.

This chapter expands the analysis to other cases and topologies in order to show the effectiveness of the Active Ripple Compensation Technique for several design conditions. Furthermore, an investigation regarding the use of more harmonic components in the duty cycle will be presented in order to verify if the performance of the system can be improved.

Differently from Chapter 4, the analysis carried out in the following will use an optimization approach for designing the converter instead of design abacuses, since this method allows for the consideration of more variables and design conditions at the same time. Furthermore, by means of the optimization approach it is possible to program the design procedure, allowing for a systematic evaluation of several design conditions.

For the analysis carried out in this chapter, four topologies were chosen:

- Flyback;
- Integrated Buck Flyback Converter (IBuFly);
- Integrated Boost Buck Converter (IBoBu);
- Integrated Double Buck Boost Converter (IDBB).

One can note that the proposed study includes one sole topology and three integrated converters. Moreover, each one of the integrated topologies has a different PFC

stage. This choice allows for an evaluation of the impact of the duty cycle modulation on converters that presents a different input current shape.

In order to present the generalized study, the chapter was divided in seven sections. The first one presents the directives for designing LED drivers by means of a non-linear constrained optimization problem. The second section outlines the design procedure based on the presented directives. Sections 3, 4 , 5 and 6 present the mathematical modeling, simulations and the optimization results of the Flyback, IBuFly, IBoBu and IDBB converters, respectively. Finally, a summary is discussed in section 7.

5.1 DESIGN OF LED DRIVERS BASED ON A CONSTRAINED OPTIMIZATION PROBLEM

As presented in the previous chapter, the modulation of the duty cycle affects the behavior of the main waveforms of the converter. Therefore, the design of the elements of the circuit must also take into account the modulation.

Furthermore, owing to the modulation of $d(t)$, some equations of the converter must be solved numerically (*e.g.*, the bus voltage of the IDBB converter - see (4.39)), since there is not a closed-form solution or this solution would be too complex and useless for analyzing the converter behavior.

Bearing in mind this characteristic, the design of an LED driver with ARC approach could be modeled as an optimization problem, so that all the elements and variables could be sized numerically in order to achieve some performance parameters. Since the main goal of this work is to minimize the filtering capacitances, the optimization problem can be stated as

$$\begin{aligned} &\min && f(x) = W_1 C_{LF} + W_2 \Delta I_{LF} \\ &subject\,to && H(x) \leqslant 0_{9x1} \end{aligned} \tag{5.1}$$

where:

C_{LF} - value of the capacitor sized to filter the low-frequency ripple of the output current in Farads;

x - a vector containing a possible solution for the optimization problem. The vector x compiles all the optimization variables, which are the parameters of the duty cycle function and the value of C_{LF}.

ΔI_{LF} - low-frequency ripple of the LEDs current in amperes;

W_1, W_2 - weights of the capacitance and the output current ripple, respectively.

H - vector containing the constraints, defined in (5.2);

0_{9x1} - null vector with 9 rows and 1 column.

$$H(x) = \begin{pmatrix} \Delta Io_{LF} - \Delta Io_{LF\_max} \\ d(t) - 0.9D_{crit} \\ -PF + 0.92 \\ I_3 - 0.3PFI_1 \\ I_5 - 0.1I_1 \\ I_7 - 0.07I_1 \\ I_9 - 0.05I_1 \\ I_{11} - 0.03I_1 \\ I_{13} - 0.03I_1 \end{pmatrix}, \tag{5.2}$$

where the power factor PF is described by (5.3) in terms of the phase shift of the fundamental ϕ_1 and the THD, defined in (5.4). The constraints defined in matrix $H(x)$ will be detailed in the following.

$$PF = \frac{\cos(\phi_1)}{\sqrt{1 + THD^2}}, \tag{5.3}$$

$$THD = \frac{\sqrt{\sum_{m=3,5,..}^{13} I_m^2}}{I_1}, \tag{5.4}$$

In (5.4), I_m is the amplitude of the $m-th$ harmonic component of the converter input current and can be calculated by means of (5.5) as a function of the Fourier coefficients a_m and b_m and I_1 - the amplitude of the fundamental. The Fourier coefficients are given by (5.6) and (5.7).

$$I_m = \sqrt{a_m^2 + b_m^2} \tag{5.5}$$

$$a_m = \frac{2}{T}\int_{-T/2}^{T/2} i_g(t)\cos(m\omega t)\,dt \tag{5.6}$$

$$b_m = \frac{2}{T}\int_{-T/2}^{T/2} i_g(t)\sin(m\omega t)\,dt \tag{5.7}$$

It is important to highlight that the low-frequency capacitance C_{LF} is a discrete variable, which means that for a given value, several ripple conditions could be verified (see Figure 67). Thus, the ripple term was added in $f(x)$ so that the algorithm could find the minimum ripple condition for a certain capacitor. In this work, the values used for the weights are $W_1 = 10^6$ $[F^{-1}]$ and $W_2 = 1$ $[A^{-1}]$. This choice gives a major importance for the minimization of the low-frequency capacitor.

The constraints compiled in the matrix H were defined in order to ensure that the performance of the LED driver is within the requirements for the application, which were outlined in Chapters 1, 2 and 3. Note that using this numerical design approach, the designer can introduce additional constraints in order to obtain the best parameters for the application. For example, limits for the MOSFET or bus voltage levels could be added as a constraint in matrix H.

For this design, nine constraints were introduced. The first one limits the output current ripple so that a good photometric performance of the LEDs is ensured. For this analysis, only the low-frequency ripple is being considered.

The second constraint is an operational condition that guarantees the operating mode of the converter. It is important to highlight that a safety margin of 10% was considered. Moreover, it was considered that all the stages of the converter must operate in DCM.

The third row of the matrix H assures that the power factor of the converter meets the INMETRO ordinance number 478 (**?**) whereas the six last constraints treats the compliance of the input current harmonic content with the IEC-61000-3-2 standard (Class C). For the sake of simplicity and to reduce the computational cost, the harmonics above the thirteenth were not considered.

As already mentioned, the vector x compiles the data of the duty cycle function and the capacitor C_{LF}. As presented in Chapter 4, the signal $d(t)$ was defined so that it could be interpreted as a parameterized function whose parameters are the coefficients of the Fourier series (see (4.1)). On the other hand, all the development carried out in

the previous chapter considered only one harmonic component in the duty cycle signal.

In order to expand the analysis, the optimization problem defined in (5.1) will be solved considering four harmonic components, so that the vector x is defined as:

$$x = \begin{bmatrix} D_2 & \phi_2 & D_4 & \phi_4 & D_6 & \phi_6 & D_8 & \phi_8 & C_{LF} \end{bmatrix}. \tag{5.8}$$

By summarizing, the optimization problem stated in this section was defined so that it selects the optimum vector x^* from a search-space $\mathbb{S}$ that minimizes the low-frequency filtering capacitances while meeting the constraints defined in H. The search-space $\mathbb{S}$ comprises all the possible combinations of the variables that compose the vector x. A further discussion regarding the search space will be provided in the next sections. Besides the vector x^*, the optimization algorithm also return the values of the inductors of the circuit and the capacitor sized to filter the high-frequency ripple of the output current.

It is important to highlight that for designing the converter (*i.e.,* to solve the optimization problem), it is necessary to define the design parameters *a priori*, which is a set of values that comprises the main data of the application, such as the mains voltage and the load features. Since the set of design parameters depends on the topology, they will be presented in sections 5.3, 5.4, 5.5 and 5.6, in which the converters studied in this chapter are discussed.

5.2 DESIGN PROCEDURE

Since the design of the LED driver was modeled as a constrained optimization problem, several techniques can be used to solve it, such as genetic algorithms, heuristic methods or exhaustive-search. Each approach has advantages and drawbacks, so that its performance normally depends on the characteristics of the problem and the search-space. The algorithm used in this work was based on the Exhaustive Search (ES) method, which is robust against the local minima problem although it has the drawback of demanding a large computational effort.

Although four different topologies will be studied in this chapter, the design procedure on the ES method is similar for all the converters and can be summarized by means of the flowchart presented in Figure 84. One can note that the solution procedure of (5.1) was described in the flowchart as an iterative process composed by eight steps, which are explained in the following.

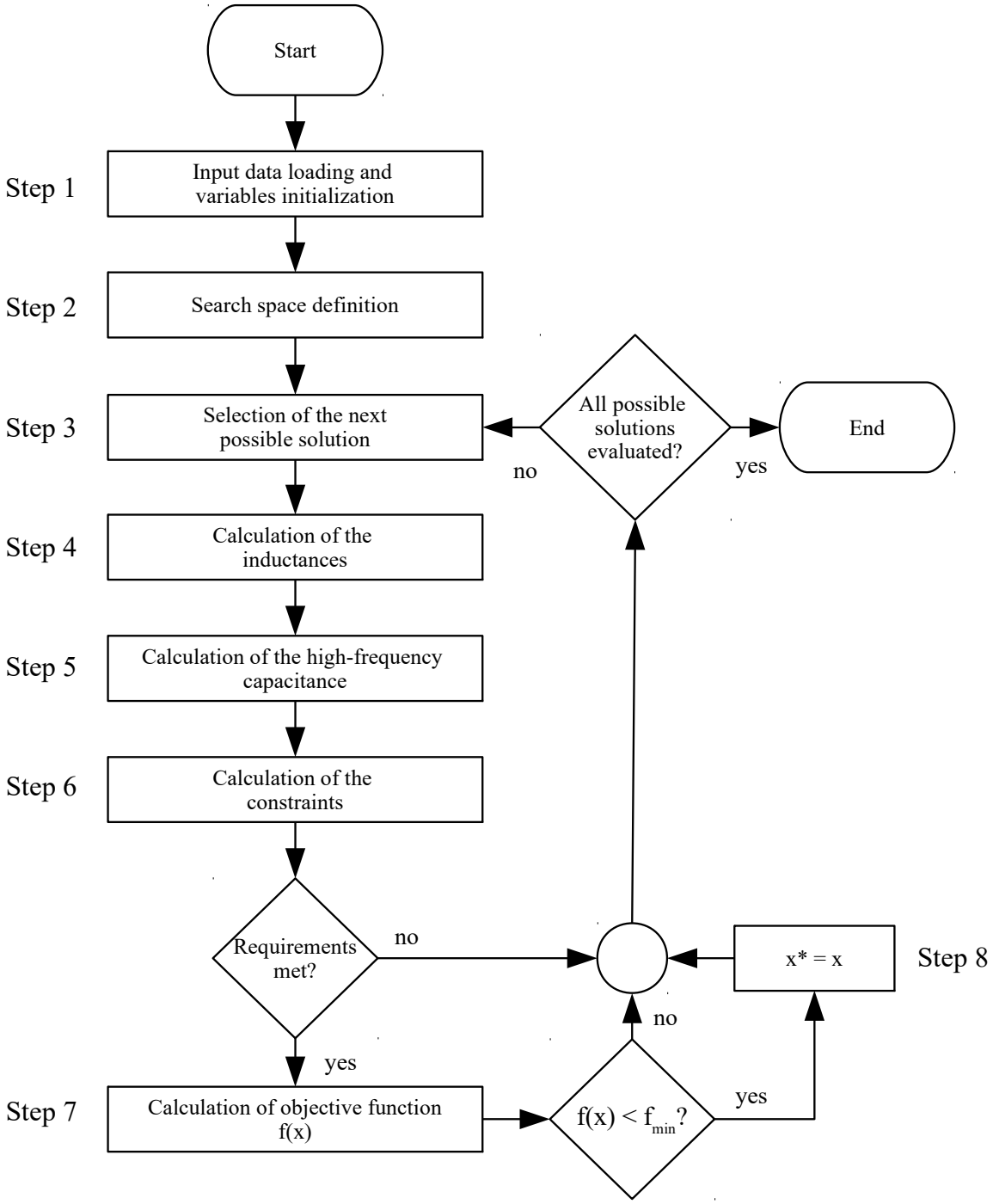


Figure 84: Design steps flowchart.

Step 1: variables initialization and input data reading. In this step the design parameters such as the mains voltage and the load characteristics are loaded. Furthermore, some parameters for the converter design are also calculated, such as the critical duty cycle.

Step 2: the search-space is defined as the combination of all the possibilities of the optimization variables. It is important to highlight that the search-space is generated

considering the second constraint of the matrix H, *i.e.,* all the possible duty cycle functions are defined so that the converter always operates in DCM. More details regarding the procedure of the search-space generation can be found in Appendix B, where all the MATLAB codes used for the optimization routine are presented and explained.

Step 3: choose the next possible solution x.

Step 4: Calculation of the inductances of the circuit. Since for the analysis carried out in this chapter considers that all the power stages of the converters are operating in DCM, the inductances of the topologies can be obtained using the expressions of power balance in each stage of the converter.

Step 5: Calculation of the capacitance sized to filter the high-frequency ripple of the output current. This step is only required when a two-stage converter is being analyzed, since in sole topologies the capacitance sized to filter the low-frequency component of the output current ripple also attenuates the high-frequency components.

Step 6: Calculation of the constraints of the optimization problem, *i.e.*, evaluate the matrix H.

Step 7: Evaluation of $f(x)$ in order to be compared with the variable f_{min}, which is initialized with a large value in *Step 1* and represents the actual minimum value of the objective function.

Step 8: Store the values of the parameters that yielded f_{min}, which includes the input data x and also the design results of the converter, such as the inductances and capacitances. As already commented, the variable x^* represents the set of input variables that lead the solution of (5.1) to the optimum point.

The equations used in the steps of the optimization routine depend on the topology and are presented in the next sections.

5.3 FLYBACK CONVERTER

Since the operation and design of the flyback converter with duty cycle modulation was addressed in Chapter 4, this section will highlight only some small differences that must be taken into account for analyzing the circuit owing to the inclusion of more harmonic components in the duty cycle signal.

5.3.1 Main equations

- Critical duty cycle D_{crit}

As commented in previous section, all the converters analyzed in this chapter will be designed to operate in DCM. Therefore, for the flyback converter, the expression of the critical duty cycle remains the same as the one presented in Chapter 4, *i.e.*, (4.18). This expression must be used in the design step 2 (see Figure 84) for defining the search-space.

- Input current i_g

The input current of the flyback converter can be evaluated by means of (5.9), which is repeated here for the reader's convenience.

$$i_g(t) = \frac{v_g(t)d(t)^2}{2L_m f_s}. \tag{5.9}$$

Differently from Chapter 4, the harmonic components of the input current will be obtained numerically by means of (5.5)-(5.7). This procedure is suitable for this case since the ac part of the duty cycle function could have more than one harmonic component, leading to complex expressions if i_g was evaluated analytically. Moreover, by using the numerical approach, the procedure becomes more systematic and straightforward to program. It is important to highlight that the calculation of the harmonic components of the input current is necessary for the evaluation of the constraints defined in the rows 3 to 9 of the matrix H, a procedure that is performed during the step 6 of the design algorithm.

- Inductance L_m

For the calculation of the inductance L_m, the expression (4.24) remains valid, since this equation takes into account all the harmonic components of $d(t)$ for calculating the magnetizing inductance of the flyback transformer. This calculation is performed during step 4 of the design algorithm.

- Low-frequency output current ripple ΔIo_{LF}

Regarding the output current ripple, the procedure is the same as the one outlined in Chapter 4, since it was based on a numeric evaluation of the output current that considered the whole duty cycle function $d(t)$. As the input current harmonics, the calculation of ΔIo_{LF} is necessary in step 6 for evaluating the constraints of the design procedure.

5.3.2 Simulation results

Before discussing the optimization results, it is important to validate the equations used in the design procedure. In this work, such validation was carried out by comparing the results provided by the theoretical equations of the converter (discussed in the last subsection) with simulations using the software PSIM. It is important to highlight that the equations of the flyback converter with duty cycle modulation were also validated by means of experiments, as shown in Chapter 4. Nevertheless, the following simulations address the behavior of the converter with $d(t)$ being defined with four harmonic components, instead of only one, which was the case studied in the last chapter.

Figure 85 presents the circuit and Table 12 define the values used in the simulation of the flyback converter. The simulation step defined in Table 12 was chosen in order to avoid numerical errors.

Since the mathematical model developed in this work deals only with the low- frequency behavior, a low-pass filter tuned at 5 kHz was used to obtain the low-frequency waveform of the input current, excluding the switching harmonics from this signal. This strategy was used because it allows for an evaluation of the low-frequency behavior of the input current regardless the characteristics of the circuit. It is important to highlight that if an EMI filter was used, it would be necessary to size this element for each load condition, which is not the aim of the analysis carried out in this chapter. The same strategy will be used for the simulation of the other converters.

Figure 86 presents a comparison between the waveforms gathered from the PSIM simulation and the ones obtained from the mathematical model. From the simulation results it is possible to verify that the differences between the theoretical and simulated waveforms are negligible, which could also be verified by analyzing the simulation results in Table 13. The MATLAB function used to calculate the theoretical waveforms of the flyback converter was named *calc_fly* and is presented in Appendix B.4.

The calculation routine for evaluating the converter behavior by means of the low-

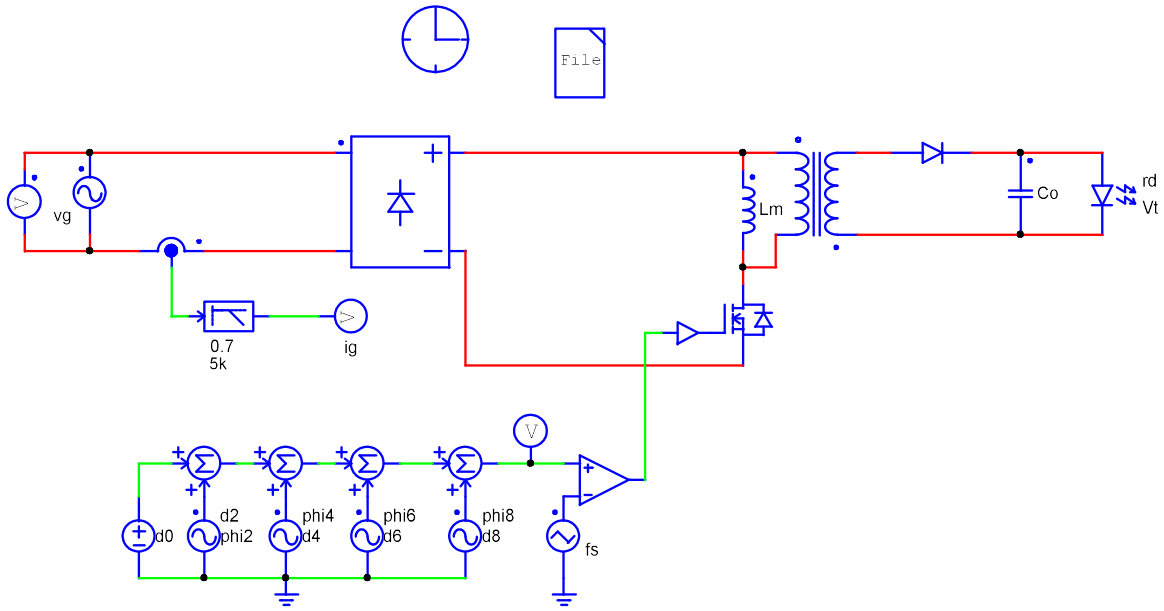


Figure 85: Circuit used in the simulation of the flyback converter

Table 12: Values used in the simulation of the flyback converter

Item	Value
v_g	$127\sqrt{2}\sin(2\pi 60t)$ V
d	$d_0 = 0.2188$, $d_2 = 0.06$, $d_4 = 0.01$, $d_6 = 0.01$, $d_8 = 0.01$, $phi2 = 90°$, $phi4 = 100°$,$phi6 = 0°$,$phi8 = 0°$
f_s	50 kHz
L_m	83.94 μH
C_o	200 μF
r_d	19.34 Ω
V_t	130.18 V
I_o	500 mA (nominal)
Simulation step	0.1 μs

frequency mathematical model has an important advantage when compared to softwares like PSIM: the execution speed. Since the proposed set of equations was devised to provide directly the low-frequency behavior of the converter, this approach allows for the evaluation of the numeric equations with a somewhat large time step, which was defined as 16.67 μs (i.e., 1000 points per cycle of the line voltage) in the MATLAB routine. On the other hand, the simulation executed in PSIM must have a time step much smaller, since the simulation also have to evaluate the high-frequency behavior of the circuit.

It is important to mention that the execution speed of the algorithm is a quite important parameter in this work, since the evaluation of the converter variables is part of an iterative optimization routine. This means that the calculation of the flyback

converter quantities will be carried out thousand of times during the optimization procedure, having a direct impact on the total time spent by the optimization routine. By way of comparison, the simulation of the PSIM demands approximately 1.33 seconds[1] to evaluate one line voltage cycle whereas the MATLAB function *calc_fly* can perform[2] the same task in less than 6 ms. Those measurements were carried out by executing both the PSIM simulation and the MATLAB routine on a notebook with the following hardware configuration: Intel Core i7-3610QM CPU @ 2.3 GHz, 8GB RAM and a Solid State Disk (SSD) of 256 GB.

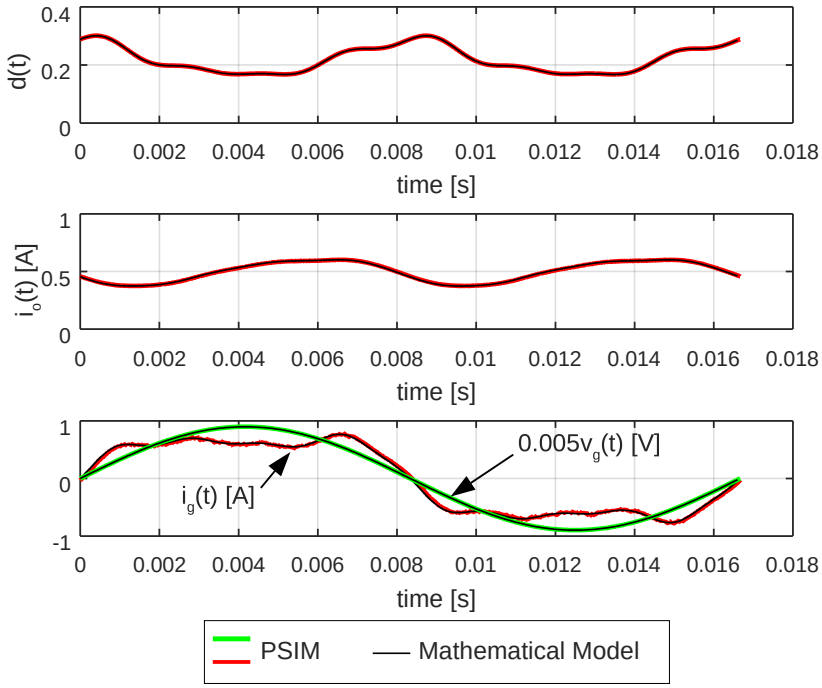


Figure 86: Comparison between the simulated waveforms with the theoretical model of the flyback converter.

Table 13: Simulation results of the flyback converter.

Item	Description	PSIM Result	Mathematical Model
I_o	Average output current	499 mA	499 mA
ΔIo_{LF}	Low-frequency output current ripple	226 mA	228 mA
THD	Total Harmonic Distortion	31.38 %	30.97%
PF	Power Factor	0.954	0.955

5.3.3 Description of the design conditions and the search space

Since the main equations of the flyback converter were validated and the design procedure is established, a MATLAB program based on the flowchart presented in

[1] with a time step of 0.1 μs.
[2] with a time step of 16.67 μs

Figure 84 was developed in order to solve the optimization problem. The source code of this program can be seen in Appendix B.

In order to reduce the time for solving the optimization routine and to allow for a wider analysis of the ARC technique performance (*i.e.*, to consider more design conditions), the MATLAB code was executed on the computer cluster of the post-graduation program in electrical engineering of the Federal University of Juiz de Fora (PPEE-UFJF), whose configuration is shown in Table 14. As can be seen in the table, the cluster allows for the execution of 256 simultaneous processes, which is 64 times more than a conventional personal computer (PC)[3]. Nevertheless, owing to the number of MATLAB licenses of the PPEE-UFJF, only 96 processes can be executed simultaneously (24 times more than a conventional PC).

Table 14: Specification of the PPEE-UFJF cluster

Item	Value
Number of nodes	32
Processes per node	8
CPU	2 Intel Xeon per node
RAM	16 GB per node

The first step for running the program is to define the input parameters for the design and also the search space.

In order to evaluate the performance of the ARC technique for several design conditions, a set of cases were chosen by varying some of the main design parameters, as described in the following:

- RMS input voltage: 127 V and 220 V;
- Line frequency: 60 Hz
- Average value of the duty cycle: 0.5 D_{crit} and 0.75D_{crit}
- Parameters of the LED: Threshold voltage $V_T = 2.7120$ V and dynamic resistance $r_d = 0.4030\Omega$.
- Nominal output current I_o: 500 mA;
- Number of LEDs: 48 (70 W) and 72 (105 W);
- Switching frequency: 50 kHz;

[3]equipped with a quad-core CPU

- Flyback transformer turn ratio: 1;
- Estimated efficiency: 1 (ideal converter);
- Maximum low-frequency output current ripple ΔIo_{LF_max}: 250 mA and 50 mA;
- Maximum high-frequency output current ripple ΔIo_{HF_max}: 100 mA and 25 mA;

The combination of the parameters listed above yields 16 cases, which are defined in Table 15. Note that the critical duty cycle for each one is also highlighted in the table.

The search space $\mathbb{S}$ is composed by the combination of all the possible values of the vector x variables, which are summarized in Table 16. As can be seen, the amplitudes of the duty cycle harmonic components can vary from zero to 90 % of D_{crit}. However, this is an initial search space, since the routine *GenSS* (see Appendix B.3), which generates $\mathbb{S}$, evaluates if the duty cycle function formed by the elements of the vector x complies with the second constraint of the matrix H (*i.e.,* $d(t) < 0.9D_{crit}$). Thanks to this constraint, the size of $\mathbb{S}$ will be lower than the initial search space. One can note from Table 16 that the search space of the low-frequency capacitor is defined in terms of the variable C_{def}, which represents the capacitance required for solving the optimization problem when no ARC is employed, *i.e.,* $D_2 = D_4 = D_6 = D_8 = 0$. Therefore, this is the theoretical limit for this variable.

Table 15: Cases studied in the flyback converter

Case	$D_{0\%}$	D_{crit}	V_G	f_L	f_s	I_o	r_d	V_t	n	η	ΔIo_{LF_max}	ΔIo_{HF_max}
1	50 %	0.44	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.17 V	1	1	50 mA	25mA
2	50 %	0.54	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	1	1	50 mA	25mA
3	50 %	0.31	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.17 V	1	1	50 mA	25mA
4	50 %	0.40	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	1	1	50 mA	25mA
5	75 %	0.44	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.17 V	1	1	50 mA	25mA
6	75 %	0.54	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	1	1	50 mA	25mA
7	75 %	0.31	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.17 V	1	1	50 mA	25mA
8	75 %	0.40	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	1	1	50 mA	25mA
9	50 %	0.44	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.17 V	1	1	250 mA	100mA
10	50 %	0.54	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	1	1	250 mA	100mA
11	50 %	0.31	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.17 V	1	1	250 mA	100mA
12	50 %	0.40	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	1	1	250 mA	100mA
13	75 %	0.44	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.17 V	1	1	250 mA	100mA
14	75 %	0.54	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	1	1	250 mA	100mA
15	75 %	0.31	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.17 V	1	1	250 mA	100mA
16	75 %	0.40	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	1	1	250 mA	100mA

By analyzing Table 16, it is possible to see that the number of possibilities depends on the characteristics of the application, which changes the value of D_{crit}. For example, if $D_{crit} = 0.4$, the size of $\mathbb{S}$ would be approximately 1.0339×10^{22} [4]. Considering a hy-

[4]this value was obtained by using the fundamental principal of counting.

Table 16: Range of the optimization variables.

Variable	Range
D_n (n = 2,4,6 and 8)	from 0 to $0.9D_{crit}$ in steps of 0.01
ϕ_n (n = 2,4,6 and 8)	from -180° to 180° in steps of 10°
C_{LF}	from $0.01C_{def}$ to C_{def} in steps of $C_{def}/50$

pothesis that the search space reduction mechanism could shrink $\mathbb{S}$ to 10% of its initial size, the number of possibilities that the optimization algorithm should evaluate would be 1.1×10^{13}. Additionally, taking into account that the average time for evaluating one possible solution is 12 ms [5] and that the cluster can evaluate 96 possibilities simultaneously, the total time for solving the optimization problem would be approximately 3.85×10^5 hours. This means that is not possible to solve the optimization problem stated in (5.1) considering simultaneously 4 harmonics in the duty cycle signal and using the exhaustive search algorithm.

Table 17 shows the time prediction for solving the optimization problem as a function of the number of harmonics of the duty cycle signal. The calculation procedure was the same of the one explained above.

Table 17: Estimation of the time spent for solving the optimization routine

Number of harmonics of d(t)	Prediction of time spent
4	3.85×10^5 hours (≈ 44 *years*)
3	316 hours
2	15.53 minutes
1	less than one second

It is important to highlight that the values presented in Table 17 are estimated and can vary according to the application. However, the table presents the order of magnitude for each case. Therefore, the analysis presented in this work will not consider more than two simultaneous harmonics in the duty cycle signal. This means that $d(t)$ can assume ten configurations, with the following harmonic components: only 2^{nd}; only 4^{th};only 6^{th};only 8^{th}; 2^{nd} and 4^{th}; 2^{nd} and 6^{th};2^{nd} and 8^{th};4^{th} and 6^{th};4^{th} and 8^{th};6^{th} and 8^{th}.

5.3.4 Optimization results

This section discusses the results of the optimization problem for all the 16 studied design cases. Those results were obtained by means of the MATLAB script presented

[5] time measured on PPEE-UFJF cluster.

in Appendix B.1, which was the same for all the converters.

The analysis presented in this chapter will focus mainly on the capacitance reduction and also on the THD for each design case. Other variables, such as the converter inductance and also the amplitudes and phases of the duty cycle function, can be visualized in the supplementary material of this chapter, which is described in Appendix D.

Table 18 presents the results of the optimization process regarding the value of the output capacitance for each studied case. One can note that beside each value of capacitance is the amount of capacitance reduction $\Delta C_{\%}$, defined by:

$$\Delta C_{\%} = 100\frac{C_{def} - C_{opt}}{C_{def}}, \tag{5.10}$$

in which C_{def} is the capacitance required for meeting the design requirements of the studied case without ARC and C_{opt} is the capacitance obtained from the optimization routine for such design condition. The color scale used in the table is based on the value of $\Delta C_{\%}$, as indicated below the table.

From the results, it is possible to note that the presence of the second harmonic in the duty cycle led to the best results in terms of capacitance reduction. On the other hand, one can see that the lack of this harmonic in $d(t)$ decreases dramatically the potential of the ARC technique for reducing the filtering capacitance. As already commented in Chapter 4, this characteristic was expected since the low-frequency ripple is at twice the line frequency. Moreover, the optimization results also showed that the combination of the second harmonic with the fourth one or even with the sixth could improve the results. For example, in the studied case no. 11, the inclusion of the fourth harmonic in the duty cycle signal allowed for a capacitance reduction of 9.8 % when compared with the situation in which only the second harmonic is considered.

In order to verify the impact of the duty cycle modulation on the input current of the converter, the THD will be considered since it characterizes the input current distortion. Table 19 presents the THD of the studied cases. Furthermore, the ΔTHD for each design condition is also shown between parentheses. Such quantity, defined in (5.11), is a good figure to measure the influence of the ARC upon the input current distortion.

Table 18: Output capacitance and $\Delta C_{\%}$ of the flyback converter with ARC for all the studied cases

Case	*Default*	2^{nd}	4^{th}	6^{th}	8^{th}	2^{nd} and 4^{th}	2^{nd} and 6^{th}	2^{nd} and 8^{th}	4^{th} and 6^{th}	4^{th} and 8^{th}	6^{th} and 8^{th}
1	1373 μF	1068 μF (22.2%)	1318 μF (4.0%)	1345 μF (2.0%)	1373 μF (-0.0%)	1012 μF (26.3%)	1040 μF (24.3%)	1068 μF (22.2%)	1262 μF (8.1%)	1318 μF (4.0%)	1318 μF (4.0%)
2	916 μF	712 μF (22.3%)	879 μF (4.0%)	897 μF (2.1%)	916 μF (-0.0%)	675 μF (26.3%)	694 μF (24.2%)	694 μF (24.2%)	860 μF (6.1%)	879 μF (4.0%)	879 μF (4.0%)
3	1373 μF	1123 μF (18.2%)	1345 μF (2.0%)	1318 μF (4.0%)	1373 μF (-0.0%)	1040 μF (24.3%)	1068 μF (22.2%)	1123 μF (18.2%)	1262 μF (8.1%)	1345 μF (2.0%)	1318 μF (4.0%)
4	916 μF	731 μF (20.2%)	879 μF (4.0%)	897 μF (2.1%)	916 μF (-0.0%)	694 μF (24.2%)	712 μF (22.3%)	731 μF (20.2%)	842 μF (8.1%)	879 μF (4.0%)	879 μF (4.0%)
5	1373 μF	1123 μF (18.2%)	1318 μF (4.0%)	1345 μF (2.0%)	1373 μF (-0.0%)	1096 μF (20.2%)	1068 μF (22.2%)	1123 μF (18.2%)	1234 μF (10.1%)	1318 μF (4.0%)	1318 μF (4.0%)
6	916 μF	731 μF (20.2%)	879 μF (4.0%)	897 μF (2.1%)	916 μF (-0.0%)	731 μF (20.2%)	712 μF (22.3%)	731 μF (20.2%)	842 μF (8.1%)	879 μF (4.0%)	879 μF (4.0%)
7	1373 μF	1151 μF (16.2%)	1318 μF (4.0%)	1345 μF (2.0%)	1373 μF (-0.0%)	1123 μF (18.2%)	1096 μF (20.2%)	1123 μF (18.2%)	1262 μF (8.1%)	1318 μF (4.0%)	1318 μF (4.0%)
8	916 μF	731 μF (20.2%)	879 μF (4.0%)	879 μF (4.0%)	916 μF (-0.0%)	731 μF (20.2%)	712 μF (22.3%)	731 μF (20.2%)	823 μF (10.2%)	879 μF (4.0%)	879 μF (4.0%)
9	265 μF	201 μF (24.2%)	249 μF (6.0%)	260 μF (1.9%)	265 μF (-0.0%)	190 μF (28.3%)	190 μF (28.3%)	201 μF (24.2%)	233 μF (12.1%)	249 μF (6.0%)	254 μF (4.2%)
10	177 μF	134 μF (24.3%)	170 μF (4.0%)	173 μF (2.3%)	177 μF (-0.0%)	123 μF (30.5%)	127 μF (28.2%)	131 μF (26.0%)	159 μF (10.2%)	166 μF (6.2%)	170 μF (4.0%)
11	265 μF	211 μF (20.4%)	254 μF (4.2%)	254 μF (4.2%)	265 μF (-0.0%)	185 μF (30.2%)	201 μF (24.2%)	211 μF (20.4%)	233 μF (12.1%)	254 μF (4.2%)	254 μF (4.2%)
12	177 μF	138 μF (22.0%)	166 μF (6.2%)	173 μF (2.3%)	177 μF (-0.0%)	127 μF (28.2%)	127 μF (28.2%)	138 μF (22.0%)	156 μF (11.9%)	166 μF (6.2%)	166 μF (6.2%)
13	265 μF	211 μF (20.4%)	249 μF (6.0%)	254 μF (4.2%)	265 μF (-0.0%)	195 μF (26.4%)	201 μF (24.2%)	211 μF (20.4%)	233 μF (12.1%)	249 μF (6.0%)	249 μF (6.0%)
14	177 μF	138 μF (22.0%)	166 μF (6.2%)	173 μF (2.3%)	177 μF (-0.0%)	131 μF (26.0%)	134 μF (24.3%)	138 μF (22.0%)	156 μF (11.9%)	166 μF (6.2%)	166 μF (6.2%)
15	265 μF	217 μF (18.1%)	249 μF (6.0%)	260 μF (1.9%)	265 μF (-0.0%)	201 μF (24.2%)	206 μF (22.3%)	217 μF (18.1%)	238 μF (10.2%)	249 μF (6.0%)	254 μF (4.2%)
16	177 μF	138 μF (22.0%)	166 μF (6.2%)	170 μF (4.0%)	177 μF (-0.0%)	131 μF (26.0%)	134 μF (24.3%)	138 μF (22.0%)	156 μF (11.9%)	166 μF (6.2%)	166 μF (6.2%)

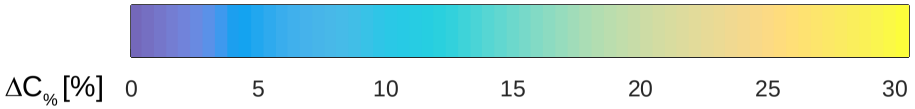
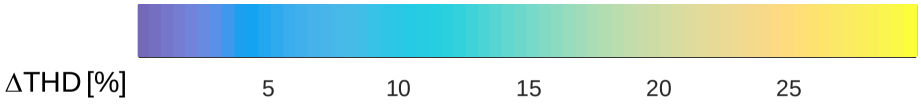


Table 19: THD and ΔTHD of the flyback converter with ARC for all the studied cases

Case	*Default*	2^{nd}	4^{th}	6^{th}	8^{th}	2^{nd} and 4^{th}	2^{nd} and 6^{th}	2^{nd} and 8^{th}	4^{th} and 6^{th}	4^{th} and 8^{th}	6^{th} and 8^{th}
1	0.0%	27.1% (+27.0%)	12.9% (+12.9%)	6.5% (+6.5%)	6.5% (+6.5%)	29.6% (+29.6%)	28.9% (+28.9%)	27.1% (+27.0%)	17.4% (+17.4%)	14.2% (+14.2%)	12.0% (+12.0%)
2	0.0%	26.3% (+26.3%)	10.5% (+10.5%)	5.2% (+5.2%)	5.2% (+5.2%)	29.9% (+29.9%)	27.6% (+27.6%)	26.9% (+26.9%)	14.1% (+14.1%)	11.6% (+11.6%)	10.5% (+10.5%)
3	0.0%	22.3% (+22.3%)	9.1% (+9.1%)	9.1% (+9.1%)	0.0% (-0.0%)	29.6% (+29.6%)	24.6% (+24.6%)	22.3% (+22.3%)	16.3% (+16.3%)	9.1% (+9.1%)	9.1% (+9.1%)
4	0.0%	23.0% (+23.0%)	14.0% (+14.0%)	7.0% (+7.0%)	7.0% (+7.0%)	29.1% (+29.1%)	25.1% (+25.1%)	23.0% (+23.0%)	18.9% (+18.9%)	15.4% (+15.4%)	13.0% (+13.0%)
5	0.0%	20.9% (+20.9%)	12.9% (+12.9%)	8.6% (+8.6%)	4.3% (+4.3%)	29.5% (+29.5%)	23.8% (+23.8%)	21.4% (+21.4%)	19.2% (+19.2%)	13.4% (+13.4%)	11.7% (+11.7%)
6	0.0%	22.9% (+22.9%)	13.9% (+13.9%)	7.0% (+7.0%)	7.0% (+7.0%)	29.5% (+29.5%)	25.0% (+25.0%)	22.9% (+22.9%)	18.8% (+18.8%)	15.3% (+15.3%)	13.0% (+13.0%)
7	0.0%	19.5% (+19.5%)	12.1% (+12.1%)	6.1% (+6.1%)	6.1% (+6.1%)	29.4% (+29.4%)	21.2% (+21.2%)	20.6% (+20.6%)	16.4% (+16.4%)	13.4% (+13.4%)	11.7% (+11.7%)
8	0.0%	23.0% (+23.0%)	14.0% (+14.0%)	9.3% (+9.3%)	4.7% (+4.7%)	29.4% (+29.4%)	24.1% (+24.1%)	23.0% (+23.0%)	16.7% (+16.7%)	14.5% (+14.5%)	12.5% (+12.5%)
9	0.0%	26.9% (+26.9%)	12.9% (+12.9%)	6.5% (+6.5%)	6.5% (+6.5%)	29.6% (+29.6%)	28.4% (+28.4%)	26.9% (+26.9%)	17.6% (+17.6%)	14.8% (+14.8%)	12.0% (+12.0%)
10	0.0%	26.2% (+26.2%)	10.5% (+10.5%)	5.2% (+5.2%)	5.2% (+5.2%)	29.9% (+29.9%)	27.3% (+27.3%)	26.9% (+26.9%)	15.2% (+15.2%)	12.0% (+12.0%)	10.5% (+10.5%)
11	0.0%	22.3% (+22.3%)	9.1% (+9.1%)	9.1% (+9.1%)	0.0% (+0.0%)	29.6% (+29.6%)	23.8% (+23.8%)	22.3% (+22.3%)	17.5% (+17.5%)	9.1% (+9.1%)	9.1% (+9.1%)
12	0.0%	23.0% (+23.0%)	14.0% (+14.0%)	7.0% (+7.0%)	7.0% (+7.0%)	29.1% (+29.1%)	29.4% (+29.4%)	23.0% (+23.0%)	18.8% (+18.8%)	15.7% (+15.7%)	13.0% (+13.0%)
13	0.0%	20.9% (+20.9%)	12.9% (+12.9%)	8.6% (+8.6%)	4.3% (+4.3%)	29.3% (+29.3%)	23.7% (+23.7%)	20.9% (+20.9%)	19.3% (+19.3%)	13.8% (+13.8%)	11.7% (+11.7%)
14	0.0%	22.9% (+22.9%)	13.9% (+13.9%)	7.0% (+7.0%)	7.0% (+7.0%)	29.2% (+29.2%)	24.9% (+24.9%)	22.9% (+22.9%)	18.8% (+18.8%)	14.6% (+14.6%)	13.0% (+13.0%)
15	0.0%	19.5% (+19.5%)	12.1% (+12.1%)	6.1% (+6.1%)	6.1% (+6.1%)	27.4% (+27.4%)	21.1% (+21.1%)	19.5% (+19.5%)	16.9% (+16.9%)	13.9% (+13.9%)	11.7% (+11.7%)
16	0.0%	23.0% (+23.0%)	14.0% (+14.0%)	9.3% (+9.3%)	4.7% (+4.7%)	28.5% (+28.5%)	24.1% (+24.1%)	23.0% (+23.0%)	17.5% (+17.5%)	14.9% (+14.9%)	12.5% (+12.5%)



$$\Delta THD = THD_{opt} - THD_{def}, \tag{5.11}$$

where THD_{opt} and THD_{def} are the THD of the circuit with and without the ARC technique, respectively.

It is important to highlight that although the analyses carried out in this chapter are based on the THD, each harmonic component of the input current is limited according to the IEC 61000-3-2 standard thanks to the constraints established in the definition of the optimization problem (see Equation 5.2).

By comparing the results of Tables 18 and 19, it is possible to note that the best results in terms of capacitance reduction are related to a higher THD, which achieved values up to 29.9 %, as in the cases number 2 and 10.

Table 20 presents a summary with the results obtained from the optimization procedure. In order to compile the data of all the studied cases, the one-sample Kolmogorov-Smirnov test (Massey Jr. & Frank J., 1951), also known as *K-S test*, was applied to the data of each column of tables 18 and 19. This procedure returns the test decision for the null hypothesis that the data in each column of the aforementioned tables comes from a standard normal distribution characterized by the mean and standard deviation indicated in Table 20. If the result of the test is *true*, it means that the *K-S test* rejects the null hypothesis with a significance level of 5%. In other words, if the result is *true*, there are grounds to believe that the mean and the standard deviation indicated in Table 20 are good parameters for representing the behavior of the studied cases. Therefore, as can be seen in the table, the capacitance reduction $\Delta C_{\%}$ and the ΔTHD can be represented as normal distributions.

By analyzing Table 20, it is possible to see a relationship between the capacitance reduction and the ΔTHD. In order to evaluate quantitatively such relationship, it is proposed a Figure of Merit (FoM) described by (5.12) in terms of $\Delta C_{\%}$, ΔTHD and the parameters K_1 and K_2, which represents the importance levels of the amount of capacitance reduction and of the additional current distortion caused by the duty cycle modulation, respectively. One can note that the default FoM is 1. Values lower than one indicate that to employ the duty cycle modulation with such configuration is worse than the default strategy (*i.e.,* no ARC). On the other hand, if the calculated value is greater than one, the ARC technique provides better results compared to the conventional approach. In this work, the values assigned to the parameters of the FoM were $K_1 = 2$ and $K_2 = 1$.

Table 20: Summary of the optimization results of the Flyback converter with ARC

Harmonic	Capacitance Reduction $\Delta C_{\%}$			ΔTHD			Average FoM
	Mean	STD	K-S test	Mean	STD	K-S test	($K_1 = 2$ and $K_2 = 1$)
2^{nd}	20.7%	2.2%	true	23.1%	2.4%	true	1.15
4^{th}	4.7%	1.2%	true	12.4%	1.7%	true	0.97
6^{th}	2.7%	1.0%	true	7.4%	1.4%	true	0.98
8^{th}	0.0%	0.0%	true	5.1%	2.2%	true	0.95
2^{nd} and 4^{th}	25.0%	3.7%	true	29.3%	0.6%	true	1.16
2^{nd} and 6^{th}	24.0%	2.4%	true	25.2%	2.5%	true	1.18
2^{nd} and 8^{th}	21.0%	2.4%	true	23.3%	2.4%	true	1.15
4^{th} and 6^{th}	9.9%	1.9%	true	17.5%	1.5%	true	1.02
4^{th} and 8^{th}	4.8%	1.3%	true	13.5%	2.0%	true	0.97
6^{th} and 8^{th}	4.6%	1.0%	true	11.7%	1.3%	true	0.98

$$FoM = \frac{100 + K_1 \Delta C_{\%}}{100 + K_2 \Delta THD} \tag{5.12}$$

The average value of the proposed FoM for each configuration of the duty cycle signal is presented in Table 20. One can note that the best harmonic configuration for the flyback converter with ARC is the one that uses the modulation of $d(t)$ with the second and the sixth harmonics. Nevertheless, it is also possible to see that the alternative that consists only of the second harmonic achieved a similar result with the advantage of requiring a less complicated control structure[6].

It is worth mentioning that in the experimental evaluation shown in Chapter 4, the values of $\Delta C_{\%}$ and ΔTHD were 24.2% and 25.54%, respectively, yielding a FoM of 1.18. Those results are similar to the ones presented in this section, showing a good agreement between the generalized analysis presented in this chapter and the case studied in Chapter 4.

5.4 INTEGRATED BUCK FLYBACK CONVERTER

The second converter studied in this chapter is the Integrated Buck Flyback converter (GACIO et al., 2011), whose circuit is shown in Figure 87. As can be seen, the converter has a DCM buck-type PFC and a flyback-based PC stage. Next subsection addresses the main equations of this converter, which will be used by the optimization routine to calculate the objective function and the constraints.

[6]each harmonic component demands an additional branch in the control structure, as shown in Chapter 4.

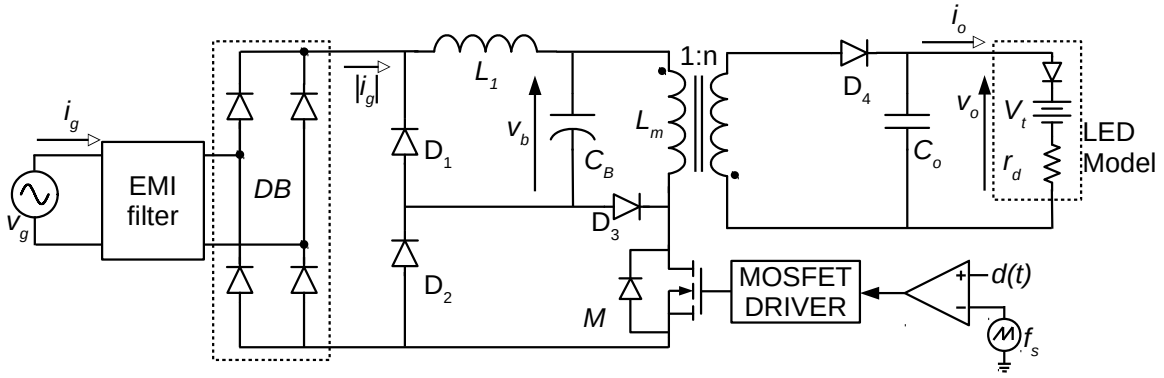


Figure 87: Integrated Buck Flyback Converter.

5.4.1 Main equations

- Critical duty cycle D_{crit}

In order to ensure that both stages of the Integrated Buck Flyback Converter (IBuFly) converter operate in DCM, the instantaneous duty cycle $d(t)$ must be lower than the critical duty cycle value D_{crit}, which is given by (5.13). As already mentioned in Section 5.2, this expression must be used in the design step 2 (see Figure 84) for defining the search-space.

$$D_{crit} = \min\left(D_{c\_PFC}, D_{c\_PC}\right), \tag{5.13}$$

in which D_{c_PFC} and D_{c_PC} are the critical duty cycle values of the PFC and the PC stages of the IBuFly converter, given by (5.14) and (5.15), respectively.

$$D_{crit} = \frac{V_B}{\sqrt{2}V_G}, \tag{5.14}$$

$$D_{crit} = \frac{V_o}{nV_B + V_o}, \tag{5.15}$$

where:

V_G - RMS value of the input voltage;

V_B - average value of the bus voltage;

V_o - average value of the output voltage;

n - transformer relationship.

- Input current i_g

The equation used by the optimization routine for evaluating the input current of the IBuFly converter is given by:

$$i_g(t) = \begin{cases} \frac{d(t)^2}{2L_1 f_s} \left(|v_g(t)| - v_b(t)\right), \; if \; |v_g(t)| > v_b(t) \; and \; v_g(t) > 0 \\ -\frac{d(t)^2}{2L_1 f_s} \left(|v_g(t)| - v_b(t)\right), \; if \; |v_g(t)| > v_b(t) \; and \; v_g(t) < 0 \\ 0 \qquad\qquad\qquad\qquad\qquad , \; if \; |v_g(t)| \leq v_b(t) \end{cases} \tag{5.16}$$

One can note that (5.16) differs from (2.12), shown in Chapter 2 for the buck PFC, since it considers the instantaneous value of the duty cycle as well as the instantaneous bus voltage $v_b(t)$. This approach allows for a larger precision in the calculation of the input current of the IBuFly converter, as long as it takes into account the effects of the ARC and also the bus voltage ripple.

Analogously to the procedure explained in Section 5.3, the harmonic components of the input current will be obtained numerically by means of (5.5)-(5.7).

- Inductances L_1 and L_m

Since the IBuFly converter was designed to operate in DCM, its inductances can be sized by means of the power balance relationship in each stage of the circuit. Therefore, the values of L_1 and L_m can be calculated by means of (5.17) and (5.18), respectively.

$$L_1 = \frac{\eta_{PFC}\eta_{PC}}{TP_o f_s} \int_{t_1}^{t_2} v_g(t) \left[v_g(t) - V_B\right] d(t)^2 dt, \tag{5.17}$$

$$L_m = \frac{\eta_{PC}}{TP_o f_s} \int_0^{T/2} V_B^2 d(t)^2 dt, \tag{5.18}$$

where:

η_{PFC} - efficiency of the PFC stage;

η_{PC} - efficiency of the PC stage;

T - period of the line voltage;

ω_L - angular frequency of the line voltage

f_s - switching frequency of the converter

P_o - output power

t_1,t_2 - integration limits for calculating the inductance of the PFC stage, given by (5.19) and (5.20), respectively

.

$$t_1 = \frac{1}{\omega_L} \arcsin\left(\frac{V_B}{V_G}\right), \tag{5.19}$$

$$t_2 = \frac{T}{2} - t_1. \tag{5.20}$$

One can note that the calculation of the inductances uses the average value of the bus voltage instead of its instantaneous value. This approach is used in this case since it is not possible to calculate $v_b(t)$ before the calculation of the inductances.

- High-frequency capacitor

The output capacitor of the IBuFly converter must be sized to filter the high-frequency components of the output current (GACIO et al., 2011). The expression for designing this element can be obtained by evaluating the high frequency current waveforms in the output node of the converter, which are shown in Figure 88.

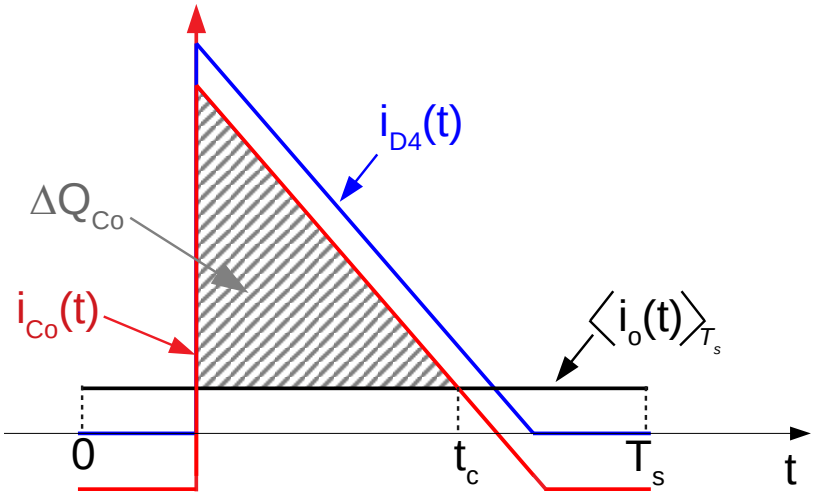


Figure 88: Theoretical high-frequency current waveforms in the output node of the IBuFly converter

The high-frequency voltage ripple can be obtained by means of:

$$\Delta V_{o\_HF} = \frac{\Delta Q_{Co}}{C_o} = \frac{1}{C_o}\int_0^{t_c} i_{Co}(t)dt = \frac{1}{C_o}\left(\frac{1}{2}t_c I_{Co\_pk}\right), \tag{5.21}$$

where t_c is the output capacitor charging time and I_{Co_pk} is the peak value of the output capacitor current.

The expression of the capacitor current during the diode D_4 conduction is given by (5.22) whereas the flyback diode current can be obtained by using (5.23).

$$i_{Co}(t) = i_{D4}(t) - \langle i_o(t)\rangle_{T_s} \tag{5.22}$$

$$i_{D4}(t) = \frac{V_B D_0}{nL_m f_s} - \frac{V_o}{L_m n^2}t \tag{5.23}$$

Since the instantaneous average value of the output current $\langle i_o(t)\rangle_{T_s}$ varies as a function of the low-frequency output current ripple, the design of the capacitor C_o must consider the worst case, *i.e.*, when the low-frequency component of the output current is at its peak. Therefore $\langle i_o(t)\rangle_{T_s}$ can be defined as:

$$\langle i_o(t)\rangle_{T_s} = I_o + \frac{\Delta I_{o\_LF}}{2}. \tag{5.24}$$

The values of t_c and I_{Co_pk} can be obtained by solving (5.25) and (5.26), respectively.

$$i_{Co}(t_c) = \langle i_o(t)\rangle_{T_s} \tag{5.25}$$

$$I_{Co\_pk} = i_{Co}(0) \tag{5.26}$$

Finally, by replacing (5.25) and (5.26) in (5.21), and also considering that $\Delta V_{o\_HF} = \Delta I_{o\_HF} r_d$, the expression for calculating the output capacitor of the IBuFly converter can be obtained, as shown in (5.27).

$$C_o = \frac{n\left[D_0 V_B - L_m f_s\left(\Delta I_{o\_LF} + I_o\right)\right]\left(\frac{D_0 V_B}{nL_m f_s} - \Delta I_{o\_LF} - I_o\right)}{2V_o \Delta I_{o\_HF} f_s r_d} \tag{5.27}$$

It is important to highlight that the analysis of the high-frequency frequency ripple considered only the average values of the $d(t)$ and $v_b(t)$, *i.e.,* D_0 and V_B, respectively. Furthermore, one can see in (5.27) that the output capacitor value depends on the

low-frequency output current ripple, which is an unknown variable *a priori*. For the sake of simplicity, in this work it was considered that ΔI_{o_LF} is equal to its maximum allowable value $\Delta I_{o\_LF\_max}$ for calculating the C_o. This assumption can be done since the optimization algorithm normally will lead the output current ripple to $\Delta I_{o\_LF\_max}$ in order to minimize the capacitance C_B, which is the element sized to filter the low-frequency output current ripple.

- Low-frequency output current ripple ΔIo_{LF}

In this chapter, the low-frequency output current ripple of the two-stage converters is calculated using an alternative approach in which the output capacitor C_o is also taken into account for evaluating ΔIo_{LF}. This strategy can be employed since the design procedure is completely numeric and allows for the introduction of this consideration without changing the structure of the optimization algorithm. It is important to highlight that the majority of the works that present the use of integrated converters for LED driving consider only the bus capacitance for low-frequency ripple filtering (ALONSO et al., 2012; GACIO et al., 2011; ALONSO et al., 2012; ALONSO et al., 2011a; ALONSO et al., 2011b; ALMEIDA; SOARES & BRAGA, 2013; LUZ et al., 2014). Nevertheless, in some applications, the requirements regarding the high-frequency filtering of the output current can make the output capacitance large enough to influence also the low-frequency behavior of the circuit. Therefore, since this chapter proposes a more general analysis, *i.e.*, several design conditions will be evaluated, the simplification assumed in the aforementioned works can lead to imprecise results.

Figure 89 depicts the large-signal low-frequency model of the IBuFly converter. As already mentioned, for this analysis the output capacitor is considered.

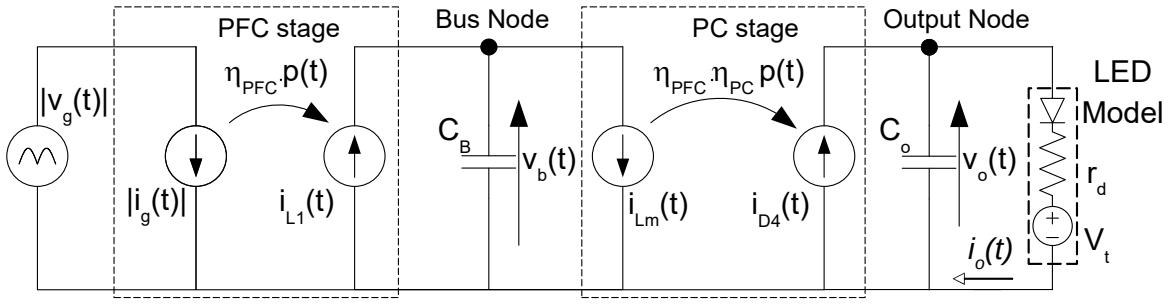


Figure 89: Large-signal low-frequency model of the IBuFly converter

From the analysis of the circuit presented in Figure 89, the expression for the output current can be calculated as:

$$i_o(t) = \frac{v_o(t) - V_t}{r_d}. \tag{5.28}$$

On the other hand, the instantaneous output voltage can be evaluated by equating the output node, which yields (5.29).

$$\frac{dv_o(t)}{dt} = \frac{1}{C_o}\left(\eta_{PC} i_{D4}(t) - \frac{v_o(t) - V_t}{r_d}\right), \tag{5.29}$$

The current through the diode D_4 is given by:

$$i_{D4}(t) = \frac{v_b(t)^2 d(t)^2}{2 f_s L_m v_o(t)} \tag{5.30}$$

As can be seen in (5.30), it is necessary to obtain the bus voltage for obtaining the current injected in the output node. This calculation can be performed by analyzing the bus node. Thus, v_b can be evaluated by means of (5.31) in terms of the inductor current $i_{L1}(t)$, which is given by (5.32).

$$\frac{dv_b(t)}{dt} = \frac{1}{C_B}\left(\eta_{PFC} i_{L1}(t) - \frac{d(t)^2 v_b(t)}{2 L_m f_s}\right), \tag{5.31}$$

$$i_{L1}(t) = \begin{cases} \frac{|v_g(t)| d(t)^2}{2 L_1 f_s v_b(t)} \left(|v_g(t)| - v_b(t)\right), \; if \; |v_g(t)| > v_b(t) \\ 0 \qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad , \; if \; |v_g(t)| \leq v_b(t) \end{cases} \tag{5.32}$$

Owing to the lack of a close-form solution for equations (5.29) and (5.31), the output current of the IBuFly could be obtained by using a numerical procedure analogous to the one outlined in section 4.1. Therefore, in order to evaluate the low-frequency output current ripple, the optimization algorithm solve the equation system formed by (5.28) - (5.32).

5.4.2 Simulation results

In order to validate the theoretical equations developed in the last section, a PSIM simulation of the IBuFly converter was carried out.Table 21 summarize the main simulation parameters whereas the circuit is shown in Figure 90. For the simulation of the IBuFly converter, the same directives presented in Subsection 5.3.2 were used, including the simulation time step and the measurements of the low-frequency variables, which were performed by means of low-pass filters. The MATLAB function used to

calculate the theoretical waveforms of the flyback converter was named *calc_ibufly* and is presented in Appendix B.5.

Table 21: Values used in the simulation of the IBuFly converter

Item	Value
v_g	$127\sqrt{2}\sin(2\pi 60t)$ V
d	$d_0 = 0.1690$, $d_2 = 0.04$, $d_4 = 0.01$, $d_6 = 0.01$, $d_8 = 0.01$, $phi2 = 20°$, $phi4 = 50°$,$phi6 = 0°$,$phi8 = 0°$
f_s	50 kHz
L_1	35.42 μH
L_m	15.49 μH
n	1
C_B	112 μF
C_o	5 μF
r_d	19.34 Ω
V_t	130.18 V
I_o	500 mA (nominal)
Simulation step	0.1 μs

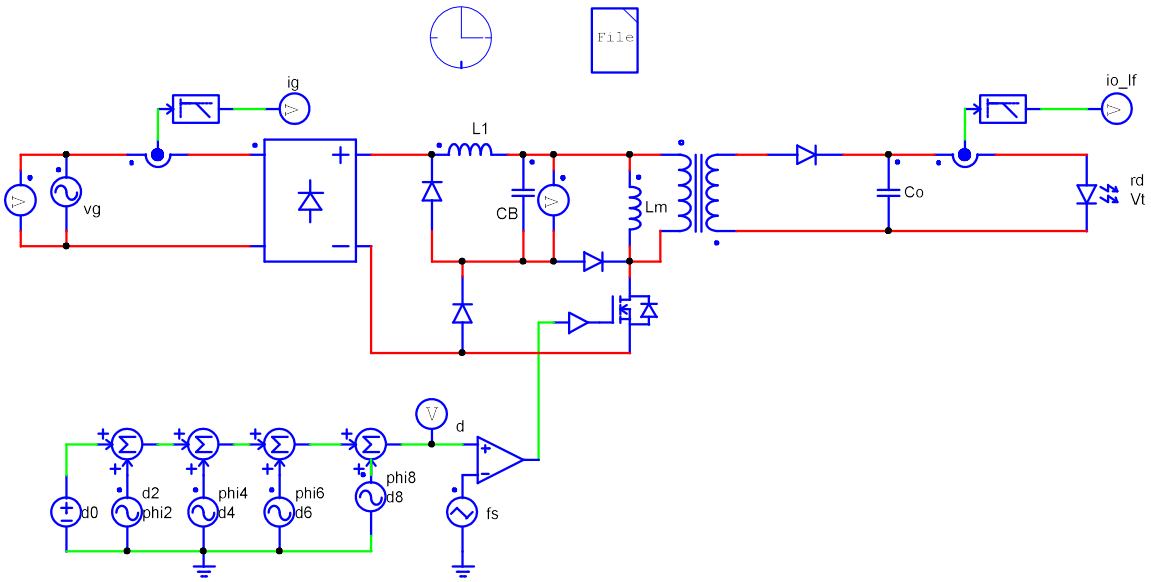


Figure 90: Circuit used in the simulation of the IBuFly converter

Figures 91 and 92 presents the main waveforms obtained from the simulation of the converter compared with the theoretical model. From Figure 91, it is possible to see that the simulation results regarding the bus voltage and the input current are quite similar to the waveforms predicted by the equations presented in subsection 5.4.1. Similarly, the output current waveform (Figure 92) obtained from the mathematical model also presents a good agreement with the PSIM results. The small differences between the theoretical waveforms and the simulated results in Figure 92 occurred owing

to the simplifications assumed in the theoretical analysis, however, the overall results show that the equations obtained in subsection 5.4.1 can be used by the optimization algorithm to evaluate the low-frequency behavior of the IBuFly converter.

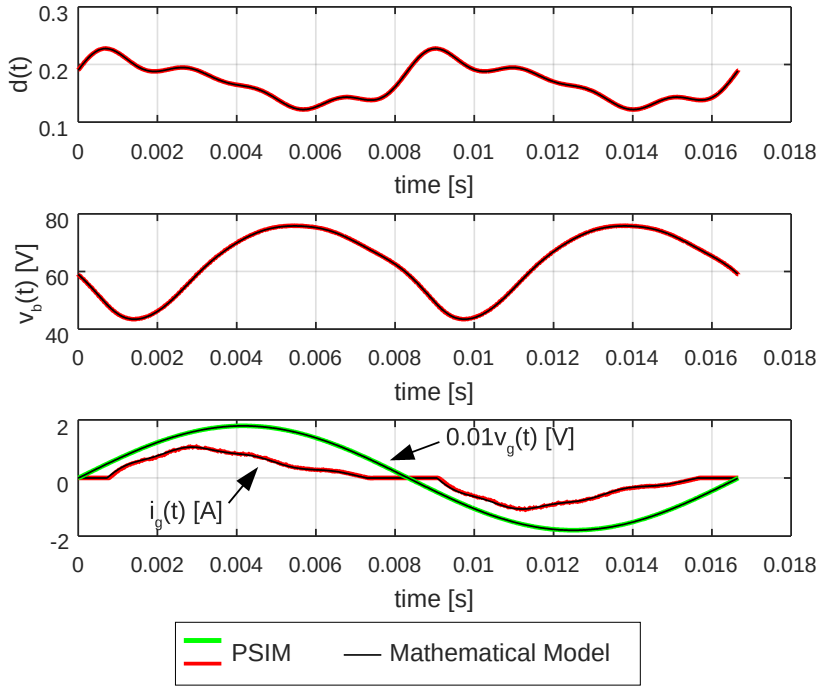


Figure 91: Comparison between the simulated waveforms with the theoretical model of the IBuFly converter.

Table 22 presents a comparison between some values gathered from the simulation and the theoretical values. The larger difference between the simulation results and the theoretical analysis is regarding the high-frequency ripple. Such divergence occurred because the high-frequency capacitor was sized considering $\Delta Io_{LF} = 250\text{mA}$ and this variable was slightly higher for the bus capacitance used in the simulation, which also lead the high-frequency output current ripple to a higher value. It is important to highlight that such divergence will be lower in the design routine, since the low-frequency output current ripple tends to be close to the specified value thanks to the optimization algorithm.

5.4.3 Optimization results

Similarly to the analysis carried out for the flyback converter, several design conditions were considered for evaluating the performance of the ARC technique in the IBuFly converter. Table 23 summarizes the parameters of the 32 evaluated cases. One can note that in this case, it is necessary to define the bus voltage as a design parameter. As already commented in Chapter 2, there is a constraint regarding the output

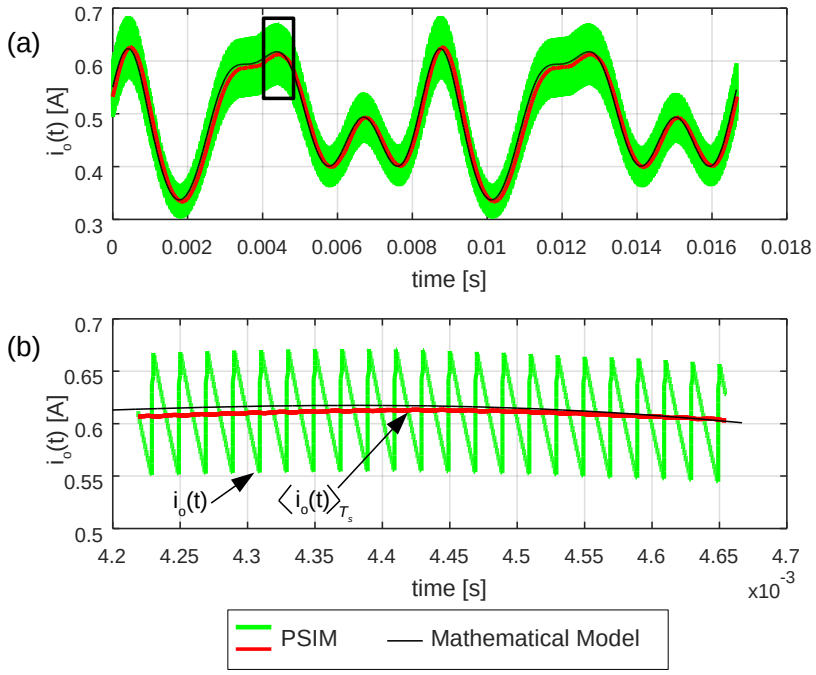


Figure 92: Comparison between the simulated waveforms of the IBuFly converter output current with the theoretical model. (a) Low-frequency behavior; (b) High-frequency waveforms

Table 22: Simulation results of the IBuFly converter.

Item	Description	PSIM Result	Mathematical Model
I_o	Average output current	490.3 mA	492.7 mA
ΔIo_{LF}	Low-frequency output current ripple	287 mA	286 mA
ΔIo_{HF}	High-frequency output current ripple	113 mA	100 mA
V_B	Average bus voltage	62.71 V	62.66 V
THD	Total Harmonic Distortion	31.23 %	31.07%
PF	Power Factor	0.9251	0.9211

voltage in a buck PFC: it must be lower than $V_G \sin(25)$ in order to meet the IEC 61000 3-2 standard requirements[7]. Therefore, the selected values for the bus voltage were $0.6V_G \sin(25)$ and $0.8V_G \sin(25)$. This choice was done bearing in mind that the injection of harmonic components in the duty cycle signal, as well as the bus voltage ripple, causes a further distortion of the input current. Thus, by selecting a bus voltage lower than the aforementioned constraint, the optimization algorithm would be able to add harmonic components in the duty cycle without violating the constraints defined in (5.2).

Table 24 presents the results of the optimization process regarding the value of the bus capacitance for each studied case. One can note that similarly to the flyback

[7]This value does not consider the bus voltage ripple

converter, the performance of the ARC technique is directly related to the injection of the second harmonic component in the duty cycle signal. Additionally, it is possible to see that the results in terms of capacitance reduction are much better than the ones obtained with the flyback converter, achieving high values such as 76.8% in some cases (*e.g.*, case n. 10 with second harmonic).

From the analysis of Table 24, it could be noted that the best performance in terms of capacitance reduction occurs for the cases in which the ripple requirement is stricter, *i.e.*, $\Delta Io_{LF} = 50mA$ and $\Delta Io_{HF} = 25mA$ (cases 1 to 16). Furthermore, for the aforementioned cases, the algorithm selected only the second harmonic, meaning that the impact of the other components upon the low-frequency ripple is negligible or that the inclusion of them in the duty cycle leads the design to the violation of some constraint. Another important observation from Table 24 is that for the cases in which $\Delta Io_{LF} = 250mA$, $\Delta Io_{HF} = 100mA$ and $V_B = 0.8V_G \sin(25)$, the combination of the 2^{nd} and the 4^{th} harmonic components led to best results in terms of capacitance reduction when compared with the strategy that uses only the second harmonic.

Table 25 presents the THD of the 32 studied cases and also the ΔTHD for each one. Again, it is possible to observe a difference between the cases 1 to 16 and 17 to 32. Nevertheless, differently from the flyback converter, the higher values of ΔTHD did not occur for the cases with the best performance in terms of capacitance reduction. The reason for this behavior comes from the analysis of the vector x^{*}[8] for each studied case.

[8]vector containing the optimum values of the optimization variables

Table 23: Cases studied in the IBuFly

Case	$D_{0\%}$	D_{crit}	V_G	f_L	f_s	I_o	r_d	V_t	V_B	n	η_{PFC}	η_{PFC}	ΔIo_{LF}	ΔIo_{HF}
1	50%	0.25	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	45.54 V	1	1	1	50 mA	25 mA
2	50%	0.34	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	60.72 V	1	1	1	50 mA	25 mA
3	50%	0.25	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	45.54 V	1	1	1	50 mA	25 mA
4	50%	0.34	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	105.19 V	1	1	1	50 mA	25 mA
5	50%	0.25	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	78.89 V	1	1	1	50 mA	25 mA
6	50%	0.34	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	105.19 V	1	1	1	50 mA	25 mA
7	50%	0.25	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	78.89 V	1	1	1	50 mA	25 mA
8	75%	0.34	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	60.72 V	1	1	1	50 mA	25 mA
9	75%	0.25	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	45.54 V	1	1	1	50 mA	25 mA
10	75%	0.34	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	60.72 V	1	1	1	50 mA	25 mA
11	75%	0.25	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	45.54 V	1	1	1	50 mA	25 mA
12	75%	0.34	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	105.19 V	1	1	1	50 mA	25 mA
13	75%	0.25	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	78.89 V	1	1	1	50 mA	25 mA
14	50%	0.34	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	60.72 V	1	1	1	50 mA	25 mA
15	75%	0.34	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	105.19 V	1	1	1	50 mA	25 mA
16	75%	0.25	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	78.89 V	1	1	1	50 mA	25 mA
17	50%	0.34	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	60.72 V	1	1	1	250 mA	100 mA
18	50%	0.25	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	45.54 V	1	1	1	250 mA	100 mA
19	50%	0.34	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	60.72 V	1	1	1	250 mA	100 mA
20	50%	0.25	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	45.54 V	1	1	1	250 mA	100 mA
21	50%	0.34	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	105.19 V	1	1	1	250 mA	100 mA
22	50%	0.25	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	78.89 V	1	1	1	250 mA	100 mA
23	50%	0.34	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	105.19 V	1	1	1	250 mA	100 mA
24	50%	0.25	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	78.89 V	1	1	1	250 mA	100 mA
25	75%	0.34	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	60.72 V	1	1	1	250 mA	100 mA
26	75%	0.25	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	45.54 V	1	1	1	250 mA	100 mA
27	75%	0.34	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	60.72 V	1	1	1	250 mA	100 mA
28	75%	0.25	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	45.54 V	1	1	1	250 mA	100 mA
29	75%	0.34	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	105.19 V	1	1	1	250 mA	100 mA
30	75%	0.25	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	78.89 V	1	1	1	250 mA	100 mA
31	75%	0.34	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	105.19 V	1	1	1	250 mA	100 mA
32	75%	0.25	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	78.89 V	1	1	1	250 mA	100 mA

Table 24: Bus capacitance and $\Delta C_{\%}$ of the IBuFly converter with ARC for all the studied cases

Case	*Default*	2^{nd}	4^{th}	6^{th}	8^{th}	2^{nd} and 4^{th}	2^{nd} and 6^{th}	2^{nd} and 8^{th}	4^{th} and 6^{th}	4^{th} and 8^{th}	6^{th} and 8^{th}
1	1117 μF	372 μF (66.7%)	1117 μF (-0.0%)	1117 μF (-0.0%)	1117 μF (-0.0%)	372 μF (66.7%)	372 μF (66.7%)	372 μF (66.7%)	1117 μF (-0.0%)	1117 μF (-0.0%)	1117 μF (-0.0%)
2	1870 μF	510 μF (72.7%)	1870 μF (-0.0%)	1870 μF (-0.0%)	1870 μF (-0.0%)	510 μF (72.7%)	510 μF (72.7%)	510 μF (72.7%)	1870 μF (-0.0%)	1870 μF (-0.0%)	1870 μF (-0.0%)
3	1670 μF	557 μF (66.6%)	1670 μF (-0.0%)	1670 μF (-0.0%)	1670 μF (-0.0%)	557 μF (66.6%)	557 μF (66.6%)	557 μF (66.6%)	1670 μF (-0.0%)	1670 μF (-0.0%)	1670 μF (-0.0%)
4	2795 μF	762 μF (72.7%)	2795 μF (-0.0%)	2795 μF (-0.0%)	2795 μF (-0.0%)	762 μF (72.7%)	762 μF (72.7%)	762 μF (72.7%)	2795 μF (-0.0%)	2795 μF (-0.0%)	2795 μF (-0.0%)
5	375 μF	125 μF (66.7%)	375 μF (-0.0%)	375 μF (-0.0%)	375 μF (-0.0%)	125 μF (66.7%)	125 μF (66.7%)	125 μF (66.7%)	375 μF (-0.0%)	375 μF (-0.0%)	375 μF (-0.0%)
6	624 μF	170 μF (72.8%)	624 μF (-0.0%)	624 μF (-0.0%)	624 μF (-0.0%)	170 μF (72.8%)	170 μF (72.8%)	170 μF (72.8%)	624 μF (-0.0%)	624 μF (-0.0%)	624 μF (-0.0%)
7	560 μF	187 μF (66.6%)	560 μF (-0.0%)	560 μF (-0.0%)	560 μF (-0.0%)	187 μF (66.6%)	187 μF (66.6%)	187 μF (66.6%)	560 μF (-0.0%)	560 μF (-0.0%)	560 μF (-0.0%)
8	932 μF	254 μF (72.7%)	932 μF (-0.0%)	932 μF (-0.0%)	932 μF (-0.0%)	254 μF (72.7%)	254 μF (72.7%)	254 μF (72.7%)	932 μF (-0.0%)	932 μF (-0.0%)	932 μF (-0.0%)
9	1121 μF	306 μF (72.7%)	1121 μF (-0.0%)	1121 μF (-0.0%)	1121 μF (-0.0%)	306 μF (72.7%)	306 μF (72.7%)	306 μF (72.7%)	1121 μF (-0.0%)	1121 μF (-0.0%)	1121 μF (-0.0%)
10	1870 μF	434 μF (76.8%)	1870 μF (-0.0%)	1870 μF (-0.0%)	1870 μF (-0.0%)	434 μF (76.8%)	434 μF (76.8%)	434 μF (76.8%)	1870 μF (-0.0%)	1870 μF (-0.0%)	1870 μF (-0.0%)
11	1679 μF	458 μF (72.7%)	1679 μF (-0.0%)	1679 μF (-0.0%)	1679 μF (-0.0%)	458 μF (72.7%)	458 μF (72.7%)	458 μF (72.7%)	1679 μF (-0.0%)	1679 μF (-0.0%)	1679 μF (-0.0%)
12	2795 μF	649 μF (76.8%)	2795 μF (-0.0%)	2795 μF (-0.0%)	2795 μF (-0.0%)	649 μF (76.8%)	649 μF (76.8%)	649 μF (76.8%)	2795 μF (-0.0%)	2795 μF (-0.0%)	2795 μF (-0.0%)
13	376 μF	103 μF (72.6%)	376 μF (-0.0%)	376 μF (-0.0%)	376 μF (-0.0%)	103 μF (72.6%)	103 μF (72.6%)	103 μF (72.6%)	376 μF (-0.0%)	376 μF (-0.0%)	376 μF (-0.0%)
14	626 μF	145 μF (76.8%)	626 μF (-0.0%)	626 μF (-0.0%)	626 μF (-0.0%)	145 μF (76.8%)	145 μF (76.8%)	145 μF (76.8%)	626 μF (-0.0%)	626 μF (-0.0%)	626 μF (-0.0%)
15	563 μF	154 μF (72.6%)	563 μF (-0.0%)	563 μF (-0.0%)	563 μF (-0.0%)	154 μF (72.6%)	154 μF (72.6%)	154 μF (72.6%)	563 μF (-0.0%)	563 μF (-0.0%)	563 μF (-0.0%)
16	937 μF	218 μF (76.7%)	937 μF (-0.0%)	937 μF (-0.0%)	937 μF (-0.0%)	218 μF (76.7%)	218 μF (76.7%)	218 μF (76.7%)	937 μF (-0.0%)	937 μF (-0.0%)	937 μF (-0.0%)
17	223 μF	133 μF (40.4%)	223 μF (-0.0%)	223 μF (-0.0%)	223 μF (-0.0%)	106 μF (52.5%)	133 μF (40.4%)	133 μF (40.4%)	223 μF (-0.0%)	223 μF (-0.0%)	223 μF (-0.0%)
18	373 μF	177 μF (52.5%)	373 μF (-0.0%)	373 μF (-0.0%)	373 μF (-0.0%)	177 μF (52.5%)	177 μF (52.5%)	177 μF (52.5%)	373 μF (-0.0%)	373 μF (-0.0%)	373 μF (-0.0%)
19	334 μF	199 μF (40.4%)	334 μF (-0.0%)	334 μF (-0.0%)	334 μF (-0.0%)	159 μF (52.4%)	199 μF (40.4%)	199 μF (40.4%)	334 μF (-0.0%)	334 μF (-0.0%)	334 μF (-0.0%)
20	559 μF	265 μF (52.6%)	559 μF (-0.0%)	559 μF (-0.0%)	559 μF (-0.0%)	265 μF (52.6%)	265 μF (52.6%)	265 μF (52.6%)	559 μF (-0.0%)	559 μF (-0.0%)	559 μF (-0.0%)
21	75 μF	45 μF (40.0%)	75 μF (-0.0%)	75 μF (-0.0%)	75 μF (-0.0%)	36 μF (52.0%)	45 μF (40.0%)	45 μF (40.0%)	75 μF (-0.0%)	75 μF (-0.0%)	75 μF (-0.0%)
22	125 μF	59 μF (52.8%)	125 μF (-0.0%)	125 μF (-0.0%)	125 μF (-0.0%)	59 μF (52.8%)	59 μF (52.8%)	59 μF (52.8%)	125 μF (-0.0%)	125 μF (-0.0%)	125 μF (-0.0%)
23	112 μF	67 μF (40.2%)	112 μF (-0.0%)	112 μF (-0.0%)	112 μF (-0.0%)	53 μF (52.7%)	67 μF (40.2%)	67 μF (40.2%)	112 μF (-0.0%)	112 μF (-0.0%)	112 μF (-0.0%)
24	186 μF	88 μF (52.7%)	186 μF (-0.0%)	186 μF (-0.0%)	186 μF (-0.0%)	88 μF (52.7%)	88 μF (52.7%)	88 μF (52.7%)	186 μF (-0.0%)	186 μF (-0.0%)	186 μF (-0.0%)
25	223 μF	133 μF (40.4%)	223 μF (-0.0%)	209 μF (6.3%)	223 μF (-0.0%)	110 μF (50.7%)	124 μF (44.4%)	124 μF (44.4%)	209 μF (6.3%)	223 μF (-0.0%)	209 μF (6.3%)
26	373 μF	177 μF (52.5%)	373 μF (-0.0%)	373 μF (-0.0%)	373 μF (-0.0%)	177 μF (52.5%)	177 μF (52.5%)	177 μF (52.5%)	373 μF (-0.0%)	373 μF (-0.0%)	373 μF (-0.0%)
27	334 μF	199 μF (40.4%)	334 μF (-0.0%)	314 μF (6.0%)	334 μF (-0.0%)	165 μF (50.6%)	186 μF (44.3%)	186 μF (44.3%)	314 μF (6.0%)	334 μF (-0.0%)	314 μF (6.0%)
28	559 μF	265 μF (52.6%)	559 μF (-0.0%)	559 μF (-0.0%)	559 μF (-0.0%)	265 μF (52.6%)	265 μF (52.6%)	265 μF (52.6%)	559 μF (-0.0%)	559 μF (-0.0%)	559 μF (-0.0%)
29	75 μF	45 μF (40.0%)	73 μF (2.7%)	70 μF (6.7%)	75 μF (-0.0%)	37 μF (50.7%)	42 μF (44.0%)	42 μF (44.0%)	70 μF (6.7%)	73 μF (2.7%)	70 μF (6.7%)
30	125 μF	59 μF (52.8%)	125 μF (-0.0%)	125 μF (-0.0%)	125 μF (-0.0%)	59 μF (52.8%)	59 μF (52.8%)	59 μF (52.8%)	125 μF (-0.0%)	125 μF (-0.0%)	125 μF (-0.0%)
31	112 μF	67 μF (40.2%)	112 μF (-0.0%)	105 μF (6.3%)	112 μF (-0.0%)	55 μF (50.9%)	62 μF (44.6%)	62 μF (44.6%)	105 μF (6.3%)	112 μF (-0.0%)	105 μF (6.3%)
32	186 μF	88 μF (52.7%)	186 μF (-0.0%)	186 μF (-0.0%)	186 μF (-0.0%)	88 μF (52.7%)	88 μF (52.7%)	88 μF (52.7%)	186 μF (-0.0%)	186 μF (-0.0%)	186 μF (-0.0%)

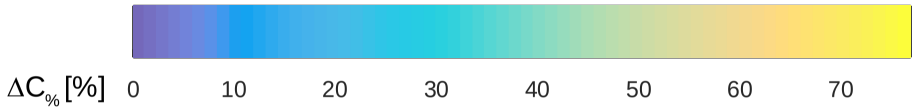


Table 25: THD and ΔTHD of the IBuFly converter with ARC for all the studied cases

Case	*Default*	2^{nd}	4^{th}	6^{th}	8^{th}	2^{nd} and 4^{th}	2^{nd} and 6^{th}	2^{nd} and 8^{th}	4^{th} and 6^{th}	4^{th} and 8^{th}	6^{th} and 8^{th}
1	22.6%	23.3% (+0.7%)	22.6% (-0.0%)	22.6% (-0.0%)	22.6% (-0.0%)	23.3% (+0.7%)	23.3% (+0.7%)	23.3% (+0.7%)	22.6% (-0.0%)	22.6% (-0.0%)	22.6% (-0.0%)
2	16.5%	18.3% (+1.9%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)	18.3% (+1.9%)	18.3% (+1.9%)	18.3% (+1.9%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)
3	22.6%	23.3% (+0.7%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)	23.3% (+0.7%)	23.3% (+0.7%)	23.3% (+0.7%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)
4	16.5%	18.3% (+1.9%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)	18.3% (+1.9%)	18.3% (+1.9%)	18.3% (+1.9%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)
5	22.6%	23.4% (+0.7%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)	23.4% (+0.7%)	23.4% (+0.7%)	23.4% (+0.7%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)
6	16.5%	18.3% (+1.9%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)	18.3% (+1.9%)	18.3% (+1.9%)	18.3% (+1.9%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)
7	22.6%	23.3% (+0.7%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)	23.3% (+0.7%)	23.3% (+0.7%)	23.3% (+0.7%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)
8	16.5%	18.3% (+1.9%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)	18.3% (+1.9%)	18.3% (+1.9%)	18.3% (+1.9%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)
9	22.6%	24.1% (+1.4%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)	24.1% (+1.4%)	24.1% (+1.4%)	24.1% (+1.4%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)
10	16.5%	19.8% (+3.4%)	16.5% (-0.0%)	16.5% (-0.0%)	16.5% (-0.0%)	19.8% (+3.4%)	19.8% (+3.4%)	19.8% (+3.4%)	16.5% (-0.0%)	16.5% (-0.0%)	16.5% (-0.0%)
11	22.6%	24.1% (+1.4%)	22.6% (-0.0%)	22.6% (-0.0%)	22.6% (-0.0%)	24.1% (+1.4%)	24.1% (+1.4%)	24.1% (+1.4%)	22.6% (-0.0%)	22.6% (-0.0%)	22.6% (-0.0%)
12	16.5%	19.8% (+3.4%)	16.5% (-0.0%)	16.5% (-0.0%)	16.5% (-0.0%)	19.8% (+3.4%)	19.8% (+3.4%)	19.8% (+3.4%)	16.5% (-0.0%)	16.5% (-0.0%)	16.5% (-0.0%)
13	22.6%	24.1% (+1.4%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)	24.1% (+1.4%)	24.1% (+1.4%)	24.1% (+1.4%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)
14	16.5%	19.8% (+3.4%)	16.5% (-0.0%)	16.5% (-0.0%)	16.5% (-0.0%)	19.8% (+3.4%)	19.8% (+3.4%)	19.8% (+3.4%)	16.5% (-0.0%)	16.5% (-0.0%)	16.5% (-0.0%)
15	22.6%	24.1% (+1.4%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)	24.1% (+1.4%)	24.1% (+1.4%)	24.1% (+1.4%)	22.6% (+0.0%)	22.6% (+0.0%)	22.6% (+0.0%)
16	16.5%	19.8% (+3.4%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)	19.8% (+3.4%)	19.8% (+3.4%)	19.8% (+3.4%)	16.5% (+0.0%)	16.5% (+0.0%)	16.5% (+0.0%)
17	21.8%	26.1% (+4.4%)	21.8% (-0.0%)	21.8% (-0.0%)	21.8% (-0.0%)	29.9% (+8.1%)	26.1% (+4.4%)	26.1% (+4.4%)	21.8% (-0.0%)	21.8% (-0.0%)	21.8% (-0.0%)
18	15.8%	21.8% (+6.0%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)	24.1% (+8.3%)	21.8% (+6.0%)	21.8% (+6.0%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)
19	21.7%	26.1% (+4.4%)	21.7% (+0.0%)	21.7% (+0.0%)	21.7% (+0.0%)	29.9% (+8.1%)	26.1% (+4.4%)	26.1% (+4.4%)	21.7% (+0.0%)	21.7% (+0.0%)	21.7% (+0.0%)
20	15.8%	21.8% (+6.0%)	15.8% (-0.0%)	15.8% (-0.0%)	15.8% (-0.0%)	24.1% (+8.3%)	21.8% (+6.0%)	21.8% (+6.0%)	15.8% (-0.0%)	15.8% (-0.0%)	15.8% (-0.0%)
21	21.8%	26.2% (+4.4%)	21.8% (-0.0%)	21.8% (-0.0%)	21.8% (-0.0%)	29.9% (+8.2%)	26.2% (+4.4%)	26.2% (+4.4%)	21.8% (-0.0%)	21.8% (-0.0%)	21.8% (-0.0%)
22	15.8%	21.8% (+6.0%)	15.8% (-0.0%)	15.8% (-0.0%)	15.8% (-0.0%)	24.1% (+8.3%)	21.8% (+6.0%)	21.8% (+6.0%)	15.8% (-0.0%)	15.8% (-0.0%)	15.8% (-0.0%)
23	21.8%	26.1% (+4.4%)	21.8% (+0.0%)	21.8% (+0.0%)	21.8% (+0.0%)	29.9% (+8.1%)	26.1% (+4.4%)	26.1% (+4.4%)	21.8% (+0.0%)	21.8% (+0.0%)	21.8% (+0.0%)
24	15.8%	21.8% (+6.0%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)	24.1% (+8.3%)	21.8% (+6.0%)	21.8% (+6.0%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)
25	21.8%	26.1% (+4.4%)	24.3% (+2.5%)	22.2% (+0.4%)	21.8% (+0.0%)	28.1% (+6.4%)	27.7% (+6.0%)	25.8% (+4.0%)	22.2% (+0.4%)	24.3% (+2.5%)	22.2% (+0.4%)
26	15.8%	21.8% (+6.0%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)	21.8% (+6.0%)	21.8% (+6.0%)	21.8% (+6.0%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)
27	21.7%	26.1% (+4.4%)	24.3% (+2.5%)	22.2% (+0.4%)	21.7% (+0.0%)	28.1% (+6.4%)	27.7% (+6.0%)	25.8% (+4.0%)	22.2% (+0.4%)	24.3% (+2.5%)	22.2% (+0.4%)
28	15.8%	21.8% (+6.0%)	15.8% (-0.0%)	15.8% (-0.0%)	15.8% (-0.0%)	21.8% (+6.0%)	21.8% (+6.0%)	21.8% (+6.0%)	15.8% (-0.0%)	15.8% (-0.0%)	15.8% (-0.0%)
29	21.8%	26.2% (+4.4%)	24.3% (+2.5%)	22.2% (+0.4%)	21.8% (+0.0%)	28.1% (+6.4%)	27.7% (+6.0%)	25.8% (+4.0%)	22.2% (+0.4%)	24.3% (+2.5%)	22.2% (+0.4%)
30	15.8%	21.8% (+6.0%)	15.8% (-0.0%)	15.8% (-0.0%)	15.8% (-0.0%)	21.8% (+6.0%)	21.8% (+6.0%)	21.8% (+6.0%)	15.8% (-0.0%)	15.8% (-0.0%)	15.8% (-0.0%)
31	21.8%	26.1% (+4.4%)	24.3% (+2.5%)	22.2% (+0.4%)	21.8% (+0.0%)	28.1% (+6.4%)	27.7% (+6.0%)	25.8% (+4.0%)	22.2% (+0.4%)	24.3% (+2.5%)	22.2% (+0.4%)
32	15.8%	21.8% (+6.0%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)	21.8% (+6.0%)	21.8% (+6.0%)	21.8% (+6.0%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)

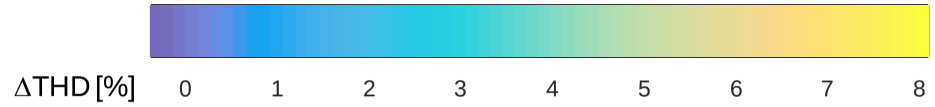


Table 26 presents the amplitudes of the second and fourth harmonic components of the duty cycle, gathered from the vector x^*, for the configuration with only the second harmonic and for the one with the second and fourth. For the sake of simplicity, only the results of the cases 1, 2, 3, 17, 18 and 19 were presented. It is important to highlight that the design parameters of the cases 1 and 17 are the same, with the exception of the ripple requirements, which are $\Delta Io_{LF} = 50mA$ and $\Delta Io_{HF} = 25mA$ for case 1 and $\Delta Io_{LF} = 250mA$ and $\Delta Io_{HF} = 100mA$ for the case 17. The same relationship is valid for the cases 2 and 18 as well as for the 3 and 19 ones.

By analyzing the Table 26 it is possible to see that the amplitudes of the harmonic components selected by the optimization routine were much larger for the cases with a relaxed ripple requirement. This occurs because in these cases the output current ripple is higher, demanding a larger duty cycle modulation for compensating the ripple, which consequently causes a further distortion in the input current.

Table 26: Results of the optimization procedure regarding the amplitudes of some harmonic components of the duty cycle function for the IBuFly converter

Harmonic components in $d(t)$	2^{nd}	2^{nd} and 4^{th}	
Case	D_2/D_0 (%)	D_2/D_0(%)	D_4/D_0(%)
1	5.9 %	5.9 %	0.0 %
2	7.9 %	7.9 %	0.0 %
3	5.9 %	5.9 %	0.0 %
17	11.8 %	23.7 %	5.9 %
18	15.8 %	23.7 %	7.9 %
19	11.8 %	23.7 %	5.9 %

An interesting aspect is that this characteristic was not verified in the case of the flyback converter, in which the THD remained in a same level regardless the ripple requirements. Table 27 shows the amplitudes of the harmonic components of the flyback converter for six cases (1,2 3 - $\Delta Io_{LF} = 50mA$ and $\Delta Io_{HF} = 25mA$ and 9, 10, 11 - $\Delta Io_{LF} = 250mA$ and $\Delta Io_{HF} = 100mA$). From this table it is possible to see that there is not a large difference between the amplitudes of the duty cycle for the cases with a relaxed ripple requirement. By comparing the tables Table 26 and Table 27, one can note that the amplitudes of the harmonic components of the sole topology is significantly higher than the integrated converter. These results show that the duty cycle modulation is less effective in a single-stage converter, since it is necessary a large low-frequency modulation of the duty for compensating the output current ripple.

The effectiveness difference of the ARC technique between single-stage topologies

Table 27: Results of the optimization procedure regarding the amplitudes of some harmonic components of the duty cycle function for the flyback converter

Harmonic components in $d(t)$	2^{nd}	2^{nd} and 4^{th}	
Case	D_2/D_0 (%)	D_2/D_0(%)	D_4/D_0(%)
1	22.8 %	27.4 %	4.6 %
2	22.3 %	26.0 %	7.4 %
3	19.3 %	25.8 %	6.4 %
9	22.8 %	27.4 %	4.6 %
10	22.3 %	26.0 %	7.4 %
11	19.3 %	25.8 %	6.4 %

and integrated converters is related with the frequency response characteristic of such converters. As shown in (WU & CHEN, 1999), the output-to-control transfer function (*i.e.*, $G_{iod} = i_o(s)/d(s)$) of an integrated converter depends only on the output stage. Therefore, the frequency response characteristic of the flyback and of the IBuFly converters have the same mathematical description, which can be obtained by using the procedure outlined in (ALONSO et al., 2013) and is given by:

$$G_{iod}(s) = \frac{i_o(s)}{d(s)} = K_{tf}\frac{1 + s/\omega_z}{1 + s/\omega_p}. \tag{5.33}$$

The dc gain of the transfer function K_{tf}, the zero defined by ω_z and the pole characterized by ω_p are defined in (5.34),(5.35) and (5.36), respectively.

$$K_{tf} = \frac{J_{Dd}}{1 - G_{Do}r_d} \tag{5.34}$$

$$\omega_z = \frac{1}{r_c C_o} \tag{5.35}$$

$$\omega_p = \frac{1 - G_{Do}r_d}{(r_d + r_c - G_{Do}r_d r_c)\, C_o} \tag{5.36}$$

where:

J_{Dd} - partial derivative of the flyback diode average current with respect to the duty cycle;

G_{Do} - partial derivative of the flyback diode average current with respect to the output voltage;

r_d - dynamic resistance of the LED string;

C_o - output capacitor;

r_c - equivalent series resistance of the output capacitor.

One can see that the frequency of the pole is highly dependent on the output capacitance. Therefore, since the output capacitance of the flyback converter is sized to filter the low-frequency ripple, this element will also attenuate the effect of the duty cycle modulation on the output current. On the other hand, the capacitance of the IBuFly converter is sized to filter the high-frequency ripple so that its influence upon the low-frequency modulation of the duty cycle is small.

Table 29 presents a summary with the results obtained from the optimization procedure. As can be seen, the standard deviation was high for some cases owing to the issue regarding the low-frequency ripple requirements. Nevertheless, the results show that the performance of the ARC technique in the IBuFly converter was significantly better than the ones obtained from the flyback topology, since the modulation of the duty cycle allowed for a huge capacitance reduction whereas the additional distortion of the input current was very small.

By analyzing the average value of the FoM for each configuration, the superior performance of the ARC technique in the IBuFly can be attested. The results of the FoM also indicate that the best configuration for the IBuFly converter is the injection of the second and the fourth harmonic components in the duty cycle signal. Nevertheless, if one choose the configuration with only the second harmonic component, the results would be similar, mainly for the cases in which the ripple requirements are stricter.

Figure 93 presents a simulation of case no. 15 comparing the default (without ARC) and the optimized design (with the 2nd harmonic). The circuit used in the simulation is the same as the one illustrated in Figure 90 and the parameters are summarized in Table 28. By analyzing the simulation results, one can observe that both designs meet the application requirements, since the current ripple is lower than 50 mA (10 %) and the input current harmonics comply with the IEC-61000-3-2 standard. As can be seen, the bus voltage ripple is higher for the case in which the bus capacitance is lower. Nevertheless, owing to the duty cycle modulation, the output current ripple was compensated and remained within the application requirements at the cost of a slight increase of the input current harmonic content.

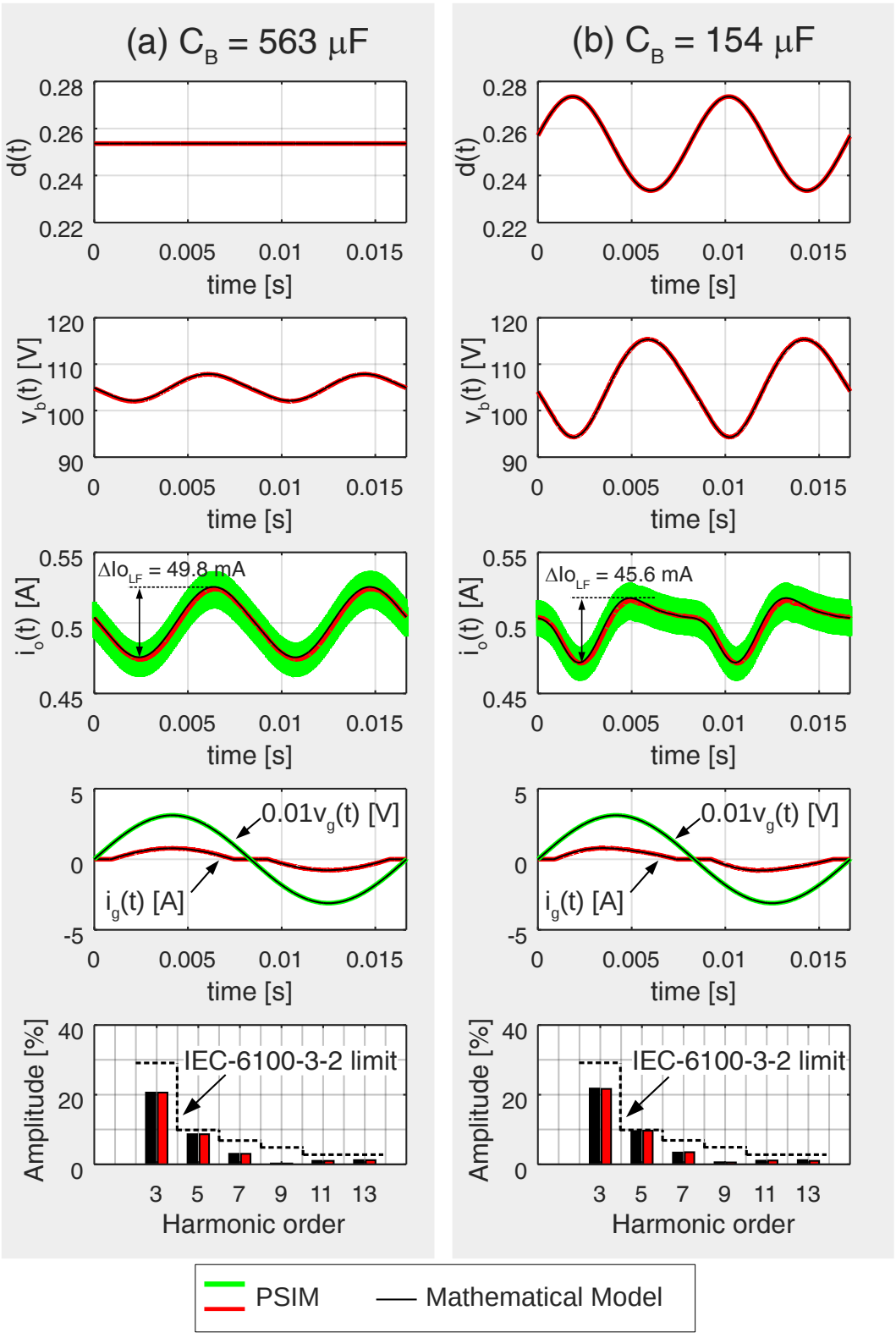


Figure 93: Comparison between the simulated waveforms with the theoretical model of the IBuFly converter for the case no. 15. (a) Default design ($C_B = 563\ \mu F$ - without ARC). (b) Optimized design ($C_B = 154\ \mu F$ - ARC with the 2nd harmonic).

Table 28: Values used in the simulation of the IBoBu converter for evaluating the optimization results of the case no. 15

Item	Default Design	Optimized Design (2^{nd})
v_g	$127\sqrt{2}\sin(2\pi 60t)$ V	$127\sqrt{2}\sin(2\pi 60t)$ V
d	$d_0 = 0.2536$, $d_2 = 0$, $d_4 = 0$ $d_6 = 0$, $d_8 = 0$ $\phi_2 = 0°$, $\phi_4 = 0°$ $\phi_6 = 0°$, $\phi_8 = 0°$	$d_0 = 0.2536$, $d_2 = 0.02$, $d_4 = 0$ $d_6 = 0$, $d_8 = 0$ $\phi_2 = 10°$, $\phi_4 = 0°$ $\phi_6 = 0°$, $\phi_8 = 0°$
f_s	50 kHz	50 kHz
L_1	171.45 μH	169.12 μH
L_m	67.56 μH	67.76 μH
N_e	1	1
C_B	563 μF	154 μF
C_o	12 μF	12 μF
r_d	29.01 Ω	29.01 Ω
V_t	195.26 V	195.26 V
I_o	500 mA (nominal)	500 mA (nominal)
Simulation step	0.1 μs	0.1 μs

5.5 INTEGRATED BOOST BUCK CONVERTER

The circuit of the Integrated Boost Buck converter (RODRIGUES, 2012) is presented in Figure 94. As can be seen, the converter has a boost-type input stage, which is designed to operate in DCM to achieve high-power factor, concatenated with a PC stage based on the buck topology, also designed to operate in DCM in this application. Next subsection addresses the main equations of this converter, which will be used by the optimization routine to evaluate the behavior of the circuit. It is important to highlight that the procedure for obtaining the equations is quite similar to the one presented in the previous section, so that the equations for the IBoBu converter will be presented in a more straightforward way.

5.5.1 Main equations

- Critical duty cycle D_{crit}

Similarly to the IBuFly converter, the critical duty cycle value D_{crit} of the IBoBu topology can be calculated by means of (5.13), just changing the values of D_{c_PFC} and D_{c_PC} to the expressions (5.37) and (5.38).

$$D_{crit} = 1 - \frac{\sqrt{2}V_G}{V_B}, \tag{5.37}$$

Table 29: Summary of the optimization results of the IBuFly converter with ARC

Harmonic	Capacitance Reduction $\Delta C_{\%}$			ΔTHD			Average FoM
	Mean	STD	K-S test	Mean	STD	K-S test	($K_1 = 2$ and $K_2 = 1$)
2^{nd}	59.3%	14.1%	true	3.4%	1.9%	true	2.12
4^{th}	0.1%	0.5%	true	0.2%	0.9%	true	1.00
6^{th}	0.8%	2.1%	true	-0.0%	0.3%	true	1.02
8^{th}	0.0%	0.0%	true	-0.1%	0.3%	true	1.00
2^{nd} and 4^{th}	62.2%	10.6%	true	4.4%	2.9%	true	2.15
2^{nd} and 6^{th}	59.8%	13.4%	true	3.6%	2.1%	true	2.12
2^{nd} and 8^{th}	59.8%	13.4%	true	3.4%	1.9%	true	2.13
4^{th} and 6^{th}	0.8%	2.1%	true	-0.0%	0.3%	true	1.02
4^{th} and 8^{th}	0.1%	0.5%	true	0.2%	0.9%	true	1.00
6^{th} and 8^{th}	0.8%	2.1%	true	-0.0%	0.3%	true	1.02

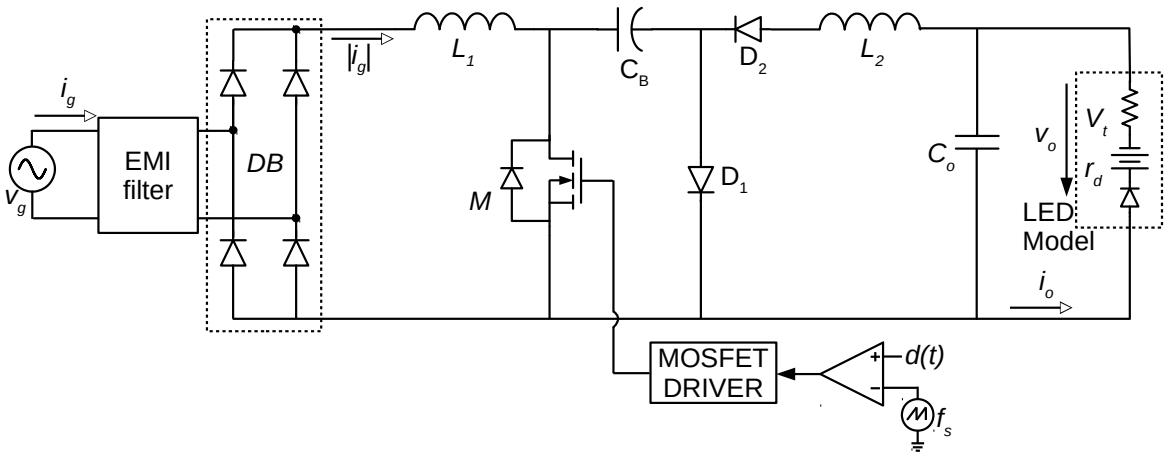


Figure 94: Integrated Boost Buck Converter

$$D_{crit} = \frac{V_o}{V_B}, \tag{5.38}$$

- Input current i_g

The equation used by the optimization routine for evaluating the input current of the IBoBu converter is given by (5.39).

$$i_g(t) = \begin{cases} \frac{d(t)^2}{2L_1 f_s}\left(\frac{|v_g(t)|v_b(t)}{v_b(t)-|v_g(t)|}\right), if\ |v_g(t)| > v_b(t) \\ -\frac{d(t)^2}{2L_1 f_s}\left(\frac{|v_g(t)|v_b(t)}{v_b(t)-|v_g(t)|}\right), if\ |v_g(t)| \leq v_b(t) \end{cases}, \tag{5.39}$$

As can be seen in (5.39), the expression of the input current of the IBoBu converter differs a little from (2.10), shown in Chapter 2 for the VMC boost PFC, since it considers the instantaneous value of the duty cycle as well as the instantaneous bus

voltage $v_b(t)$. This approach allows for a larger precision in the calculation procedure used by the optimization routine, as long as it takes into account the effects of the ARC and also the bus voltage ripple.

Analogously to the procedure explained in 5.3, the harmonic components of the input current will be obtained numerically by means of (5.5)-(5.7).

- Inductances L_1 and L_2

Similarly to the procedure presented in section 5.4, the design of the inductances of the IBoBu converter can be performed by equating the power balance in each stage of the circuit. Therefore, the values of L_1 and L_2 can be calculated by means of (5.40) and (5.41), respectively.

$$L_1 = \frac{\eta_{PFC}\eta_{PC}}{TP_o f_s} \int_0^{T/2} d(t)^2 v_g(t) \frac{v_g(t) V_B}{V_B - v_g(t)} dt, \tag{5.40}$$

$$L_2 = \frac{\eta_{PC}}{TP_o f_s} \int_0^{T/2} V_B \left(V_B - V_o\right) d(t)^2 dt, \tag{5.41}$$

One can note that the calculation of the inductances uses the average value of the bus voltage instead of the instantaneous value. This approach is used in this case since it is not possible to calculate $v_b(t)$ before the calculation of the inductances.

- High-frequency capacitor

In order to calculate the high-frequency capacitor of the IBoBu converter, the same procedure and directives presented in section 5.4 can be employed, which yields:

$$C_o = \frac{I_o + \frac{\Delta Io_{HF}}{2} - \frac{D_0(V_B - V_o)}{L_2 f_s}}{2\Delta Io_{HF} V_o f_s r_d \left(V_B - V_o\right)} \Bigg[V_o \left(D_0 V_B - \Delta Io_{HF} L_2 f_s\right) - D_0 V_B^2 + \frac{\Delta Io_{HF} L_2 V_B f_s}{2} + \left(I_o + \frac{\Delta Io_{LF}}{2}\right) L_2 V_B f_s \Bigg] \tag{5.42}$$

- Low-frequency output current ripple ΔIo_{LF}

The instantaneous output current of the IBoBu converter obtained using (5.43) in terms of the output voltage, which is given by (5.44).

$$i_o(t) = \frac{v_o(t) - V_t}{r_d}. \tag{5.43}$$

$$\frac{dv_o(t)}{dt} = \frac{1}{C_o}\left(\eta_{PC} i_{L2}(t) - \frac{v_o(t) - V_t}{r_d}\right). \tag{5.44}$$

The current through the inductor L_2 is given by:

$$i_{L2}(t) = \frac{v_b(t)d(t)^2}{2f_s L_m v_o(t)}\left(v_b(t) - v_o(t)\right). \tag{5.45}$$

On the other hand, the bus voltage can be obtained by means of:

$$\frac{dv_b(t)}{dt} = \frac{d(t)^2}{2C_B f_s}\left(\eta_{PFC}\frac{v_g(t)^2}{L_1\left(v_b(t) - |v_g(t)|\right)} - \frac{v_b(t) - v_o(t)}{L_2}\right), \tag{5.46}$$

Therefore, the value of the low-frequency output current ripple can be obtained by solving numerically the equation system formed by (5.43) - (5.46).

5.5.2 Simulation results

In order to verify the theoretical equations developed in the last section, a PSIM simulation of the IBoBu converter was carried out.Table 30 summarize the main simulation parameters whereas the circuit is shown in Figure 95. For the simulation of the IBuFly converter, the same directives presented in the previous sections were used. The MATLAB function used to calculate the theoretical waveforms of the flyback converter was named *calc_ibobu* and is presented in Appendix B.6.

Figures 96 and 97 present the main waveforms obtained from the simulation of the converter compared with the theoretical model. From Figure 96 it is possible to see that the simulation results regarding the bus voltage and the input current are quite similar to the waveforms predicted by the equations presented in subsection 5.5.1. Similarly, the output current waveform (Figure 97) obtained from the mathematical model also presents a good agreement with the PSIM results. The small differences between the theoretical waveforms and the simulated results in Figure 97 occurred owing to the simplifications assumed in the theoretical analysis, however, the overall results show that the equations obtained in subsection 5.5.1 can be used by the optimization

Table 30: Values used in the simulation of the IBoBu converter

Item	Value
v_g	$127\sqrt{2}\sin(2\pi 60t)$ V
d	$d_0 = 0.1667$, $d_2 = 0.04$, $d_4 = 0.01$, $d_6 = 0.01$, $d_8 = 0.01$, $phi2 = 20°$, $phi4 = 50°$,$phi6 = 0°$,$phi8 = 0°$
f_s	50 kHz
L_1	145.51 μH
L_2	143.37 μH
C_B	112 μF
C_o	4 μF
r_d	19.34 Ω
V_t	130.18 V
I_o	500 mA (nominal)
Simulation step	0.1 μs

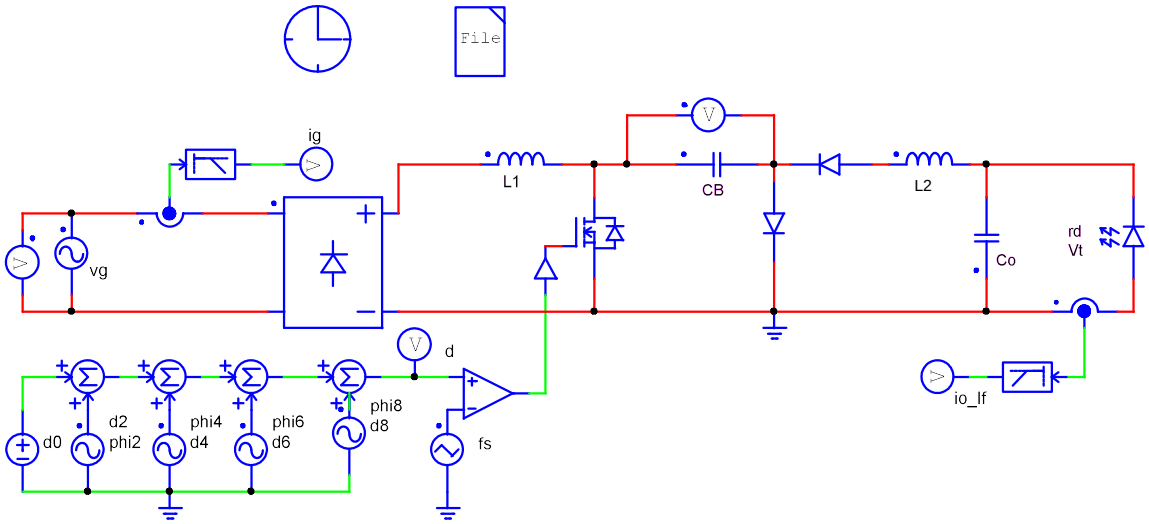


Figure 95: Circuit used in the simulation of the IBoBu converter

algorithm to evaluate the low-frequency behavior of the IBoBu converter.

Table 31 presents a comparison between some values gathered from the simulation and the theoretical values. As occurred in the IBuFly converter, the larger difference between the simulation results and the theoretical analysis is regarding the high-frequency ripple. Such divergence occurred because the high-frequency capacitor was sized considering $\Delta Io_{LF} = 250$mA and this variable was significantly higher in the simulation. It is important to highlight that the simulation parameters were chosen arbitrary and were not designed to meet any performance parameter. The main goal in this analysis was only to validate the theoretical low-frequency model.

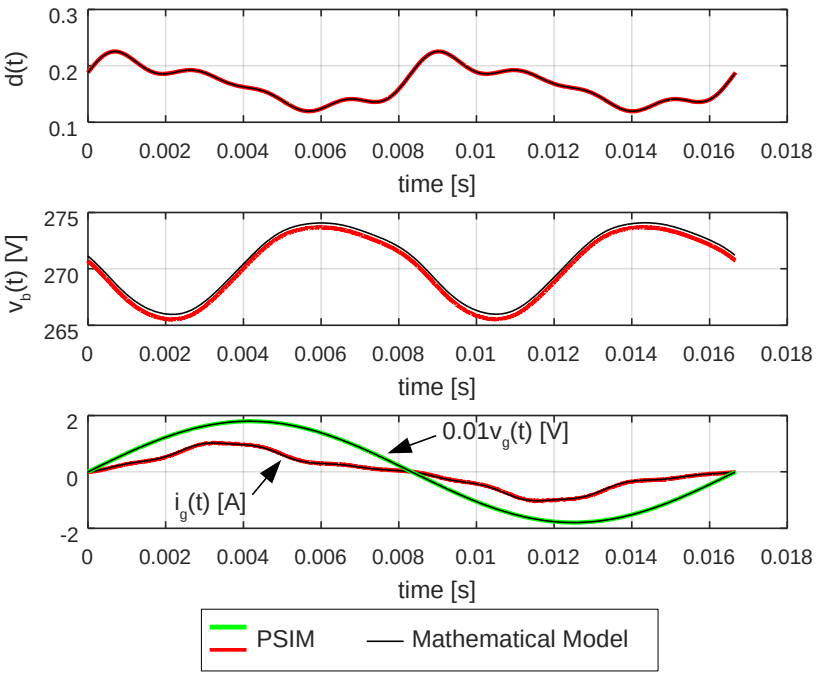


Figure 96: Comparison between the simulated waveforms with the theoretical model of the IBoBu converter.

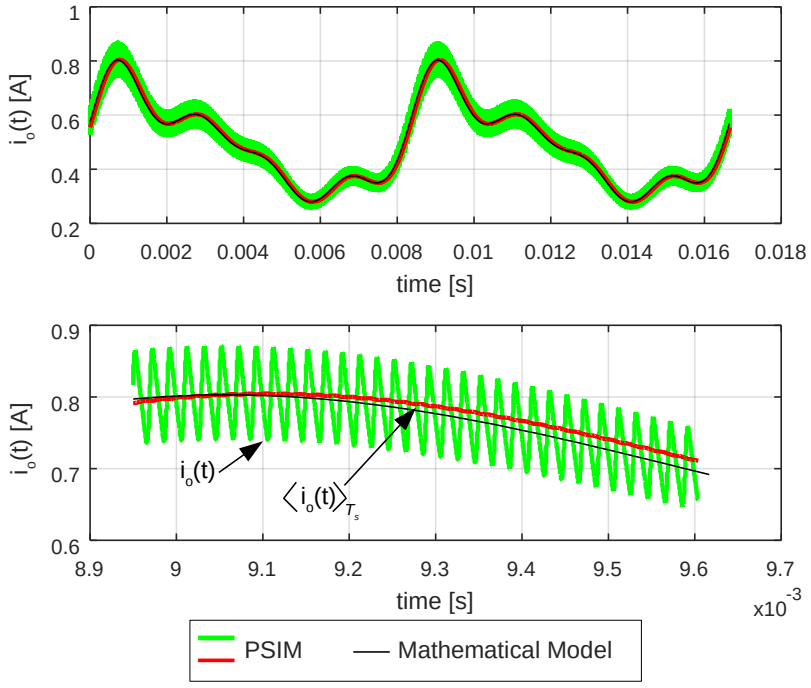


Figure 97: Comparison between the simulated waveforms of the IBoBu converter output current with the theoretical model. (a) Low-frequency behavior; (b) High-frequency waveforms

Table 31: Simulation results of the IBoBu converter.

Item	Description	PSIM Result	Mathematical Model
I_o	Average output current	495.3 mA	495.3 mA
ΔIo_{LF}	Low-frequency output current ripple	523.2 mA	523.2 mA
ΔIo_{HF}	High-frequency output current ripple	130 mA	100 mA
V_B	Average bus voltage	270.04 V	270.49 V
THD	Total Harmonic Distortion	27.39 %	27.31%
PF	Power Factor	0.9510	0.9482

5.5.3 Optimization results

In order to evaluate the performance of the ARC technique in the IBoBu converter, several design conditions were analyzed, as performed for the previous converters. Similarly to the IBuFly topology, the bus voltage of the IBoBu converter also influences in the input current distortion. Therefore, this parameter must be chosen using the directives presented in Chapter 2. Table 32 presents all the design parameters of the 32 studied cases.

Table 24 presents the results of the optimization process regarding the value of the bus capacitance for each studied case. The results show a good performance of the ARC technique to reduce the required filtering capacitances. Again, it is possible to see that the second harmonic component has a high influence in the overall behavior of the ARC technique. Furthermore, one can note that the use of the fourth harmonic combined with the second one improved the results in some cases, such as in case 3, in which the value of $\Delta C_{\%}$ was 74.6% for the ARC with only the second harmonic and 87 % (the highest value) for the strategy that comprises both, the second and the fourth ones.

Table 32: Cases studied in the IBoBu

Case	$D_{0\%}$	D_{crit}	V_G	f_L	f_s	I_o	r_d	V_t	V_B	η_{PFC}	η_{PFC}	ΔIo_{LF}	ΔIo_{HF}
1	50 %	0.33	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	269.41 V	1	1	50 mA	25 mA
2	50 %	0.41	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	305.33 V	1	1	50 mA	25 mA
3	50 %	0.33	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	269.41 V	1	1	50 mA	25 mA
4	50 %	0.41	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	305.33 V	1	1	50 mA	25 mA
5	50 %	0.30	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	466.69 V	1	1	50 mA	25 mA
6	50 %	0.26	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	528.92 V	1	1	50 mA	25 mA
7	50 %	0.33	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	466.69 V	1	1	50 mA	25 mA
8	50 %	0.40	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	528.92 V	1	1	50 mA	25 mA
9	75 %	0.33	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	269.41 V	1	1	50 mA	25 mA
10	75 %	0.41	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	305.33 V	1	1	50 mA	25 mA
11	75 %	0.33	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	269.41 V	1	1	50 mA	25 mA
12	75 %	0.41	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	305.33 V	1	1	50 mA	25 mA
13	75 %	0.30	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	466.69 V	1	1	50 mA	25 mA
14	75 %	0.26	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	528.92 V	1	1	50 mA	25 mA
15	75 %	0.33	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	466.69 V	1	1	50 mA	25 mA
16	75 %	0.40	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	528.92 V	1	1	50 mA	25 mA
17	50 %	0.33	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	269.41 V	1	1	250 mA	100 mA
18	50 %	0.41	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	305.33 V	1	1	250 mA	100 mA
19	50 %	0.33	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	269.41 V	1	1	250 mA	100 mA
20	50 %	0.41	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	305.33 V	1	1	250 mA	100 mA
21	50 %	0.30	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	466.69 V	1	1	250 mA	100 mA
22	50 %	0.26	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	528.92 V	1	1	250 mA	100 mA
23	50 %	0.33	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	466.69 V	1	1	250 mA	100 mA
24	50 %	0.40	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	528.92 V	1	1	250 mA	100 mA
25	75 %	0.33	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	269.41 V	1	1	250 mA	100 mA
26	75 %	0.41	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	305.33 V	1	1	250 mA	100 mA
27	75 %	0.33	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	269.41 V	1	1	250 mA	100 mA
28	75 %	0.41	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	305.33 V	1	1	250 mA	100 mA
29	75 %	0.30	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	466.69 V	1	1	250 mA	100 mA
30	75 %	0.26	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	528.92 V	1	1	250 mA	100 mA
31	75 %	0.33	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	466.69 V	1	1	250 mA	100 mA
32	75 %	0.40	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	528.92 V	1	1	250 mA	100 mA

Similarly to the IBuFly converter, the best results in terms of capacitance reduction occurred for the cases in which the ripple requirements were stricter. Another important observation is that the capacitances required for the IBoBu converter are, in general, much lower than the ones of the flyback converter and of the IBuFly topology. This characteristic was already expected since the bus voltage of the IBoBu converter is higher than the other mentioned topologies, which reduces the required capacitance by means of the high-voltage filtering mechanism, as explained in Chapter 3.

Table 34 presents the THD of the 32 studied cases and also the ΔTHD for each one. Again, it is possible to observe a difference between the cases 1 to 16 and 17 to 32, which occurred owing to the same reasons addressed in Section 5.4.3. Nevertheless, in general, the harmonic distortion of the input current due to the ARC technique is small.

An interesting behavior can be seen in tenth column of Table 34, in which the ARC technique provided a reduction of the THD instead of increasing it. In the case no. 28, for example, the solution of the optimization problem allowed for a capacitance and THD reduction of 13% and 2.8%, respectively.

Table 33: Bus capacitance and $\Delta C_{\%}$ of the IBoBu converter with ARC for all the studied cases

Case	*Default*	2^{nd}	4^{th}	6^{th}	8^{th}	2^{nd} and 4^{th}	2^{nd} and 6^{th}	2^{nd} and 8^{th}	4^{th} and 6^{th}	4^{th} and 8^{th}	6^{th} and 8^{th}
1	83 μF	19 μF (77.1%)	83 μF (-0.0%)	83 μF (-0.0%)	83 μF (-0.0%)	13 μF (84.3%)	19 μF (77.1%)	19 μF (77.1%)	83 μF (-0.0%)	83 μF (-0.0%)	83 μF (-0.0%)
2	58 μF	15 μF (74.1%)	58 μF (-0.0%)	58 μF (-0.0%)	58 μF (-0.0%)	8 μF (86.2%)	15 μF (74.1%)	15 μF (74.1%)	58 μF (-0.0%)	58 μF (-0.0%)	58 μF (-0.0%)
3	193 μF	49 μF (74.6%)	193 μF (-0.0%)	193 μF (-0.0%)	193 μF (-0.0%)	25 μF (87.0%)	49 μF (74.6%)	49 μF (74.6%)	193 μF (-0.0%)	193 μF (-0.0%)	193 μF (-0.0%)
4	119 μF	25 μF (79.0%)	119 μF (-0.0%)	119 μF (-0.0%)	119 μF (-0.0%)	18 μF (84.9%)	25 μF (79.0%)	25 μF (79.0%)	119 μF (-0.0%)	119 μF (-0.0%)	119 μF (-0.0%)
5	23 μF	7 μF (69.6%)	23 μF (-0.0%)	23 μF (-0.0%)	23 μF (-0.0%)	7 μF (69.6%)	7 μF (69.6%)	7 μF (69.6%)	23 μF (-0.0%)	23 μF (-0.0%)	23 μF (-0.0%)
6	17 μF	5 μF (70.6%)	17 μF (-0.0%)	17 μF (-0.0%)	17 μF (-0.0%)	5 μF (70.6%)	5 μF (70.6%)	5 μF (70.6%)	17 μF (-0.0%)	17 μF (-0.0%)	17 μF (-0.0%)
7	39 μF	9 μF (76.9%)	39 μF (-0.0%)	39 μF (-0.0%)	39 μF (-0.0%)	6 μF (84.6%)	9 μF (76.9%)	9 μF (76.9%)	39 μF (-0.0%)	39 μF (-0.0%)	39 μF (-0.0%)
8	28 μF	7 μF (75.0%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)	4 μF (85.7%)	7 μF (75.0%)	7 μF (75.0%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)
9	83 μF	19 μF (77.1%)	83 μF (-0.0%)	83 μF (-0.0%)	83 μF (-0.0%)	13 μF (84.3%)	19 μF (77.1%)	19 μF (77.1%)	83 μF (-0.0%)	83 μF (-0.0%)	83 μF (-0.0%)
10	59 μF	13 μF (78.0%)	59 μF (-0.0%)	59 μF (-0.0%)	59 μF (-0.0%)	9 μF (84.7%)	13 μF (78.0%)	13 μF (78.0%)	59 μF (-0.0%)	59 μF (-0.0%)	59 μF (-0.0%)
11	194 μF	49 μF (74.7%)	194 μF (-0.0%)	194 μF (-0.0%)	194 μF (-0.0%)	33 μF (83.0%)	49 μF (74.7%)	49 μF (74.7%)	194 μF (-0.0%)	194 μF (-0.0%)	194 μF (-0.0%)
12	119 μF	28 μF (76.5%)	119 μF (-0.0%)	119 μF (-0.0%)	119 μF (-0.0%)	20 μF (83.2%)	28 μF (76.5%)	28 μF (76.5%)	119 μF (-0.0%)	119 μF (-0.0%)	119 μF (-0.0%)
13	23 μF	6 μF (73.9%)	23 μF (-0.0%)	23 μF (-0.0%)	23 μF (-0.0%)	6 μF (73.9%)	6 μF (73.9%)	6 μF (73.9%)	23 μF (-0.0%)	23 μF (-0.0%)	23 μF (-0.0%)
14	17 μF	4 μF (76.5%)	17 μF (-0.0%)	17 μF (-0.0%)	17 μF (-0.0%)	4 μF (76.5%)	4 μF (76.5%)	4 μF (76.5%)	17 μF (-0.0%)	17 μF (-0.0%)	17 μF (-0.0%)
15	39 μF	9 μF (76.9%)	39 μF (-0.0%)	39 μF (-0.0%)	39 μF (-0.0%)	6 μF (84.6%)	9 μF (76.9%)	9 μF (76.9%)	39 μF (-0.0%)	39 μF (-0.0%)	39 μF (-0.0%)
16	28 μF	7 μF (75.0%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)	4 μF (85.7%)	7 μF (75.0%)	7 μF (75.0%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)
17	16 μF	6 μF (62.5%)	16 μF (-0.0%)	16 μF (-0.0%)	16 μF (-0.0%)	5 μF (68.8%)	6 μF (62.5%)	6 μF (62.5%)	16 μF (-0.0%)	16 μF (-0.0%)	16 μF (-0.0%)
18	11 μF	4 μF (63.6%)	11 μF (-0.0%)	11 μF (-0.0%)	11 μF (-0.0%)	4 μF (63.6%)	4 μF (63.6%)	4 μF (63.6%)	11 μF (-0.0%)	11 μF (-0.0%)	11 μF (-0.0%)
19	38 μF	16 μF (57.9%)	38 μF (-0.0%)	38 μF (-0.0%)	38 μF (-0.0%)	12 μF (68.4%)	16 μF (57.9%)	16 μF (57.9%)	38 μF (-0.0%)	38 μF (-0.0%)	38 μF (-0.0%)
20	23 μF	10 μF (56.5%)	23 μF (-0.0%)	23 μF (-0.0%)	23 μF (-0.0%)	7 μF (69.6%)	10 μF (56.5%)	10 μF (56.5%)	23 μF (-0.0%)	23 μF (-0.0%)	23 μF (-0.0%)
21	4 μF	2 μF (50.0%)	4 μF (-0.0%)	4 μF (-0.0%)	4 μF (-0.0%)	1 μF (75.0%)	2 μF (50.0%)	2 μF (50.0%)	4 μF (-0.0%)	4 μF (-0.0%)	4 μF (-0.0%)
22	3 μF	1 μF (66.7%)	3 μF (-0.0%)	3 μF (-0.0%)	3 μF (-0.0%)	1 μF (66.7%)	1 μF (66.7%)	1 μF (66.7%)	3 μF (-0.0%)	3 μF (-0.0%)	3 μF (-0.0%)
23	8 μF	3 μF (62.5%)	8 μF (-0.0%)	8 μF (-0.0%)	8 μF (-0.0%)	3 μF (62.5%)	3 μF (62.5%)	3 μF (62.5%)	8 μF (-0.0%)	8 μF (-0.0%)	8 μF (-0.0%)
24	5 μF	2 μF (60.0%)	5 μF (-0.0%)	5 μF (-0.0%)	5 μF (-0.0%)	2 μF (60.0%)	2 μF (60.0%)	2 μF (60.0%)	5 μF (-0.0%)	5 μF (-0.0%)	5 μF (-0.0%)
25	16 μF	7 μF (56.3%)	16 μF (-0.0%)	16 μF (-0.0%)	16 μF (-0.0%)	7 μF (56.3%)	7 μF (56.3%)	7 μF (56.3%)	15 μF (6.3%)	16 μF (-0.0%)	16 μF (-0.0%)
26	11 μF	5 μF (54.5%)	11 μF (-0.0%)	11 μF (-0.0%)	11 μF (-0.0%)	5 μF (54.5%)	5 μF (54.5%)	5 μF (54.5%)	10 μF (9.1%)	11 μF (-0.0%)	11 μF (-0.0%)
27	38 μF	17 μF (55.3%)	36 μF (5.3%)	36 μF (5.3%)	38 μF (-0.0%)	17 μF (55.3%)	17 μF (55.3%)	17 μF (55.3%)	33 μF (13.2%)	36 μF (5.3%)	36 μF (5.3%)
28	23 μF	10 μF (56.5%)	22 μF (4.3%)	22 μF (4.3%)	23 μF (-0.0%)	10 μF (56.5%)	10 μF (56.5%)	10 μF (56.5%)	20 μF (13.0%)	22 μF (4.3%)	22 μF (4.3%)
29	4 μF	2 μF (50.0%)	4 μF (-0.0%)	4 μF (-0.0%)	4 μF (-0.0%)	2 μF (50.0%)	2 μF (50.0%)	2 μF (50.0%)	4 μF (-0.0%)	4 μF (-0.0%)	4 μF (-0.0%)
30	3 μF	1 μF (66.7%)	3 μF (-0.0%)	3 μF (-0.0%)	3 μF (-0.0%)	1 μF (66.7%)	1 μF (66.7%)	1 μF (66.7%)	3 μF (-0.0%)	3 μF (-0.0%)	3 μF (-0.0%)
31	8 μF	3 μF (62.5%)	7 μF (12.5%)	7 μF (12.5%)	8 μF (-0.0%)	3 μF (62.5%)	3 μF (62.5%)	3 μF (62.5%)	7 μF (12.5%)	7 μF (12.5%)	7 μF (12.5%)
32	5 μF	2 μF (60.0%)	5 μF (-0.0%)	5 μF (-0.0%)	5 μF (-0.0%)	2 μF (60.0%)	2 μF (60.0%)	2 μF (60.0%)	5 μF (-0.0%)	5 μF (-0.0%)	5 μF (-0.0%)

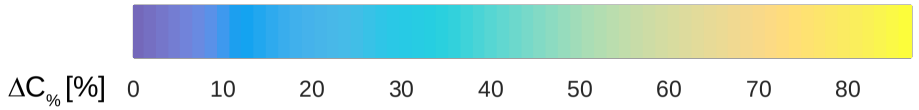
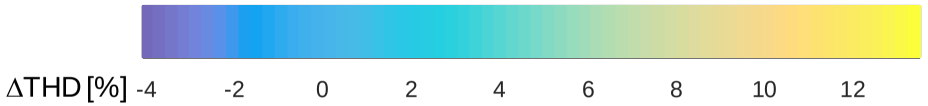


Table 34: THD and ΔTHD of the IBoBu converter with ARC for all the studied cases

Case	$Default$	2^{nd}	4^{th}	6^{th}	8^{th}	2^{nd} and 4^{th}	2^{nd} and 6^{th}	2^{nd} and 8^{th}	4^{th} and 6^{th}	4^{th} and 8^{th}	6^{th} and 8^{th}
1	20.7%	23.8% (+3.2%)	20.7% (+0.0%)	20.7% (+0.0%)	20.7% (+0.0%)	24.4% (+3.7%)	23.8% (+3.2%)	23.8% (+3.2%)	20.7% (+0.0%)	20.7% (+0.0%)	20.7% (+0.0%)
2	16.4%	19.1% (+2.7%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)	23.7% (+7.2%)	19.1% (+2.7%)	19.1% (+2.7%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)
3	20.7%	23.0% (+2.4%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)	26.3% (+5.6%)	23.0% (+2.4%)	23.0% (+2.4%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)
4	16.4%	20.1% (+3.7%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)	21.7% (+5.3%)	20.1% (+3.7%)	20.1% (+3.7%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)
5	20.7%	21.7% (+1.0%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)	21.7% (+1.0%)	21.7% (+1.0%)	21.7% (+1.0%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)
6	16.4%	18.2% (+1.8%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)	18.2% (+1.8%)	18.2% (+1.8%)	18.2% (+1.8%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)
7	20.7%	24.0% (+3.3%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)	24.8% (+4.1%)	24.0% (+3.3%)	24.0% (+3.3%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)
8	16.4%	19.4% (+3.0%)	16.4% (+0.0%)	16.4% (+0.0%)	16.4% (+0.0%)	23.7% (+7.3%)	19.4% (+3.0%)	19.4% (+3.0%)	16.4% (+0.0%)	16.4% (+0.0%)	16.4% (+0.0%)
9	20.7%	23.8% (+3.2%)	20.7% (+0.0%)	20.7% (+0.0%)	20.7% (+0.0%)	23.3% (+2.6%)	23.8% (+3.2%)	23.8% (+3.2%)	20.7% (+0.0%)	20.7% (+0.0%)	20.7% (+0.0%)
10	16.4%	21.2% (+4.7%)	16.4% (+0.0%)	16.4% (+0.0%)	16.4% (+0.0%)	21.4% (+5.0%)	21.2% (+4.7%)	21.2% (+4.7%)	16.4% (+0.0%)	16.4% (+0.0%)	16.4% (+0.0%)
11	20.7%	23.0% (+2.4%)	20.7% (+0.0%)	20.7% (+0.0%)	20.7% (+0.0%)	23.8% (+3.2%)	23.0% (+2.4%)	23.0% (+2.4%)	20.7% (+0.0%)	20.7% (+0.0%)	20.7% (+0.0%)
12	16.4%	20.5% (+4.1%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)	19.9% (+3.5%)	20.5% (+4.1%)	20.5% (+4.1%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)
13	20.7%	22.6% (+1.9%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)	22.6% (+1.9%)	22.6% (+1.9%)	22.6% (+1.9%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)
14	16.4%	19.7% (+3.3%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)	19.7% (+3.3%)	19.7% (+3.3%)	19.7% (+3.3%)	16.4% (-0.0%)	16.4% (-0.0%)	16.4% (-0.0%)
15	20.7%	24.0% (+3.3%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)	23.6% (+3.0%)	24.0% (+3.3%)	24.0% (+3.3%)	20.7% (-0.0%)	20.7% (-0.0%)	20.7% (-0.0%)
16	16.4%	19.4% (+3.0%)	16.4% (+0.0%)	16.4% (+0.0%)	16.4% (+0.0%)	22.8% (+6.3%)	19.4% (+3.0%)	19.4% (+3.0%)	16.4% (+0.0%)	16.4% (+0.0%)	16.4% (+0.0%)
17	19.9%	28.7% (+8.8%)	19.9% (+0.0%)	19.9% (+0.0%)	19.9% (+0.0%)	28.3% (+8.5%)	28.7% (+8.8%)	28.7% (+8.8%)	19.9% (+0.0%)	19.9% (+0.0%)	19.9% (+0.0%)
18	15.8%	27.8% (+12.0%)	15.8% (-0.0%)	15.8% (-0.0%)	15.8% (-0.0%)	28.9% (+13.1%)	29.5% (+13.7%)	27.8% (+12.0%)	12.5% (-3.3%)	15.8% (-0.0%)	15.8% (-0.0%)
19	20.1%	25.7% (+5.7%)	20.1% (+0.0%)	20.1% (+0.0%)	20.1% (+0.0%)	27.6% (+7.6%)	25.7% (+5.7%)	25.7% (+5.7%)	20.1% (+0.0%)	20.1% (+0.0%)	20.1% (+0.0%)
20	15.9%	25.8% (+9.9%)	20.7% (+4.8%)	15.9% (-0.0%)	15.9% (-0.0%)	27.7% (+11.8%)	28.0% (+12.1%)	25.8% (+9.9%)	12.8% (-3.1%)	20.7% (+4.8%)	15.9% (-0.0%)
21	19.8%	27.0% (+7.2%)	19.8% (-0.0%)	19.8% (-0.0%)	19.8% (-0.0%)	27.3% (+7.5%)	27.0% (+7.2%)	27.0% (+7.2%)	19.8% (-0.0%)	19.8% (-0.0%)	19.8% (-0.0%)
22	15.7%	27.5% (+11.7%)	15.7% (-0.0%)	15.7% (-0.0%)	15.7% (-0.0%)	24.1% (+8.4%)	27.5% (+11.7%)	27.5% (+11.7%)	15.7% (-0.0%)	15.7% (-0.0%)	15.7% (-0.0%)
23	19.8%	24.5% (+4.6%)	19.8% (+0.0%)	19.8% (+0.0%)	19.8% (+0.0%)	26.3% (+6.5%)	28.1% (+8.2%)	24.5% (+4.6%)	19.8% (+0.0%)	19.8% (+0.0%)	19.8% (+0.0%)
24	15.8%	24.5% (+8.7%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)	26.7% (+10.9%)	28.3% (+12.5%)	24.5% (+8.7%)	15.8% (+0.0%)	15.8% (+0.0%)	15.8% (+0.0%)
25	19.9%	25.4% (+5.6%)	23.9% (+4.0%)	20.9% (+1.1%)	19.9% (+0.0%)	25.4% (+5.6%)	25.4% (+5.6%)	25.4% (+5.6%)	16.3% (-3.5%)	23.9% (+4.0%)	20.9% (+1.1%)
26	15.8%	24.6% (+8.8%)	19.0% (+3.2%)	16.4% (+0.6%)	15.8% (+0.0%)	22.8% (+7.0%)	25.9% (+10.1%)	24.6% (+8.8%)	12.9% (-2.8%)	19.0% (+3.2%)	16.4% (+0.6%)
27	20.1%	22.8% (+2.7%)	23.9% (+3.8%)	21.5% (+1.4%)	20.1% (+0.0%)	22.8% (+2.7%)	22.8% (+2.7%)	22.8% (+2.7%)	16.7% (-3.4%)	23.9% (+3.8%)	21.5% (+1.4%)
28	15.9%	23.1% (+7.2%)	19.0% (+3.1%)	16.7% (+0.8%)	15.9% (-0.0%)	25.9% (+10.1%)	23.1% (+7.2%)	23.1% (+7.2%)	13.1% (-2.8%)	19.0% (+3.1%)	16.7% (+0.8%)
29	19.8%	25.2% (+5.4%)	24.4% (+4.6%)	19.8% (-0.0%)	19.8% (-0.0%)	25.2% (+5.4%)	25.2% (+5.4%)	25.2% (+5.4%)	15.9% (-3.9%)	24.4% (+4.6%)	19.8% (-0.0%)
30	15.7%	22.0% (+6.3%)	15.7% (-0.0%)	15.7% (-0.0%)	15.7% (-0.0%)	21.7% (+5.9%)	22.0% (+6.3%)	22.0% (+6.3%)	15.7% (-0.0%)	15.7% (-0.0%)	15.7% (-0.0%)
31	19.8%	26.0% (+6.2%)	23.8% (+4.0%)	20.8% (+0.9%)	19.8% (-0.0%)	26.0% (+6.2%)	26.0% (+6.2%)	26.0% (+6.2%)	16.2% (-3.6%)	23.8% (+4.0%)	20.8% (+0.9%)
32	15.8%	22.8% (+7.0%)	19.1% (+3.3%)	16.4% (+0.6%)	15.8% (+0.0%)	22.5% (+6.7%)	22.8% (+7.0%)	21.7% (+6.0%)	12.8% (-2.9%)	19.1% (+3.3%)	16.4% (+0.6%)



Finally, Table 35 presents a summary with the results obtained from the optimization procedure. From the analysis of the FoM values, one can see that the results of the ARC technique in the IBuFly converter were even better than the ones of the IBuFly topology. The table also shows that the best configuration for the IBoBu converter is the combination of the second and the fourth harmonic components. Nevertheless, if one choose a strategy in which the duty cycle modulates only at twice the line frequency, the results will be similar.

Table 35: Summary of the optimization results of the IBoBu converter with ARC

Harmonic	Capacitance Reduction $\Delta C_{\%}$			ΔTHD			Average FoM
	Mean	STD	K-S test	Mean	STD	K-S test	($K_1 = 2$ and $K_2 = 1$)
2^{nd}	67.1%	9.3%	true	5.1%	2.9%	true	2.23
4^{th}	0.7%	2.5%	true	0.9%	1.7%	true	1.00
6^{th}	0.7%	2.5%	true	0.1%	0.5%	true	1.01
8^{th}	0.0%	0.0%	true	-0.1%	0.3%	true	1.00
2^{nd} and 4^{th}	72.0%	11.7%	true	5.8%	2.9%	true	2.31
2^{nd} and 6^{th}	67.1%	9.3%	true	5.5%	3.4%	true	2.23
2^{nd} and 8^{th}	67.1%	9.3%	true	5.1%	2.8%	true	2.23
4^{th} and 6^{th}	1.7%	4.1%	true	-1.0%	1.6%	true	1.04
4^{th} and 8^{th}	0.7%	2.5%	true	0.9%	1.7%	true	1.00
6^{th} and 8^{th}	0.7%	2.5%	true	0.1%	0.5%	true	1.01

Figure 98 presents a simulation of case no. 3 comparing the default (without ARC) and the optimized design (with the 2nd and 4th harmonics). The circuit used in the simulation is the same as the one illustrated in Figure 95 and the parameters are summarized in Table 36.The simulation results attested that both designs meet the application requirements, since the current ripple is lower than 50 mA (10 %) and the input current harmonics comply with the IEC-61000-3-2 standard. Owing to the reduction of 87 % in the bus capacitance, the bus voltage ripple was higher for the case shown in Figure 98b. Nevertheless, thanks to the duty cycle modulation, the output current ripple was compensated and remained within the requirements at the cost of an increase of the input current harmonic content.

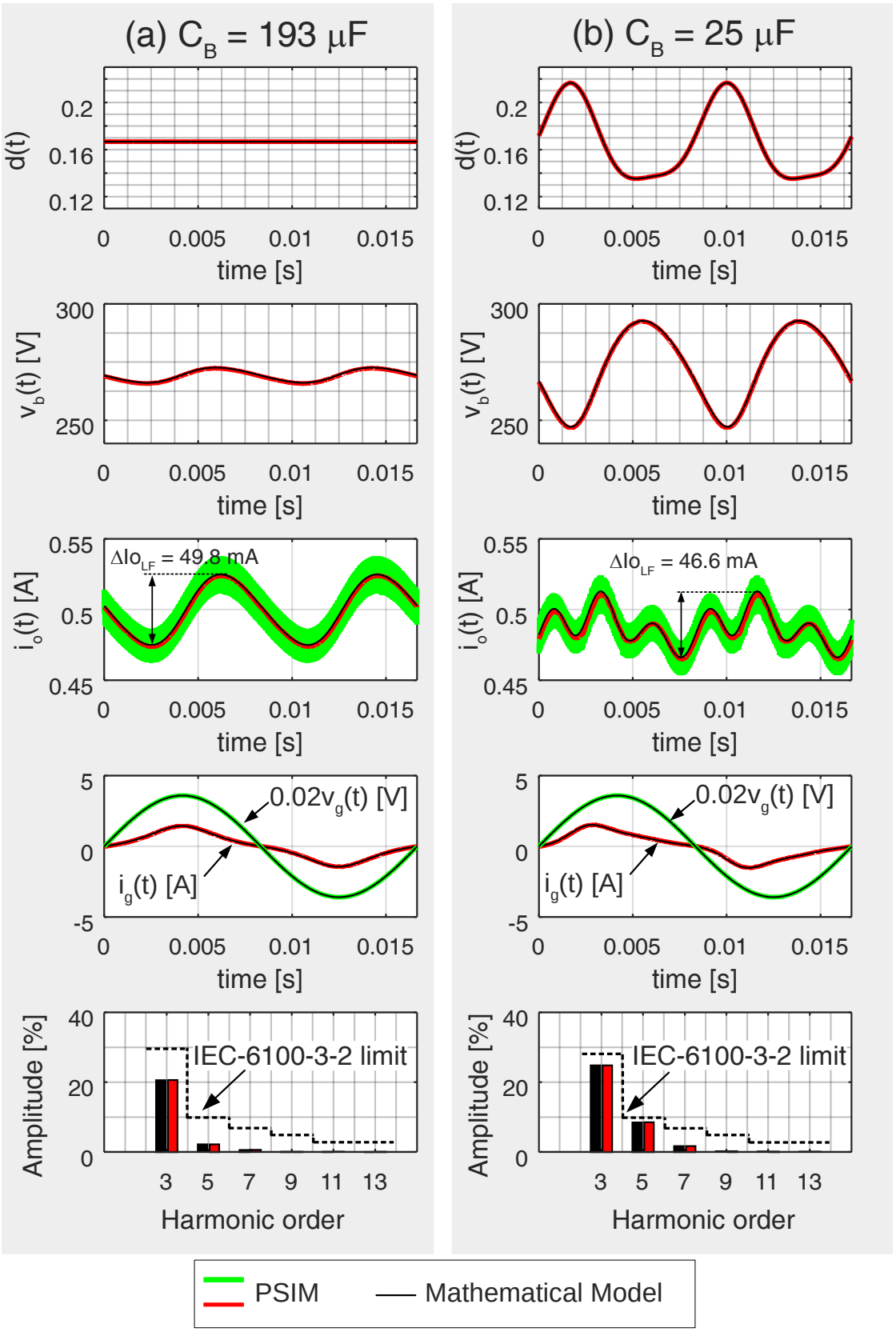


Figure 98: Comparison between the simulated waveforms with the theoretical model of the IBoBu converter for the case no. 3. (a) Default design ($C_B = 193\ \mu F$ - without ARC). (b) Optimized design ($C_B = 25\ \mu F$ - ARC with the 2nd and 4th harmonics).

Table 36: Values used in the simulation of the IBoBu converter for evaluating the optimization results of the case no. 3

Item	Default Design	Optimized Design (2^{nd} and 4^{th})
v_g	$127\sqrt{2}\sin(2\pi 60t)$ V	$127\sqrt{2}\sin(2\pi 60t)$ V
d	$d_0 = 0.1667$, $d_2 = 0$, $d_4 = 0$ $d_6 = 0$, $d_8 = 0$ $\phi_2 = 0°$, $\phi_4 = 0°$ $\phi_6 = 0°$, $\phi_8 = 0°$	$d_0 = 0.1667$, $d_2 = 0.04$, $d_4 = 0.01$ $d_6 = 0$, $d_8 = 0$ $\phi_2 = 20°$, $\phi_4 = -60°$ $\phi_6 = 0°$, $\phi_8 = 0°$
f_s	50 kHz	50 kHz
L_1	103.89 μH	95.16 μH
L_2	42.54 μH	43.84 μH
C_B	193 μF	25 μF
C_o	11 μF	11 μF
r_d	29.01 Ω	29.01 Ω
V_t	195.26 V	195.26 V
I_o	500 mA (nominal)	500 mA (nominal)
Simulation step	0.1 μs	0.1 μs

5.6 INTEGRATED DOUBLE BUCK BOOST CONVERTER

This section addresses the main equations of the IDBB converter considering the ARC with more than one harmonic component. The equations will be presented in a straightforward way, since the analysis of the IDBB converter was already presented in the previous chapter and the strategy for evaluating integrated converters with more than one harmonic via the optimization algorithm was outlined and the two previous sections.

5.6.1 Main equations

- Critical duty cycle D_{crit}

The methodology for calculating the critical duty cycle of the IDBB converter was already presented in section 4.2.2.1 and remains the same for the case with more than one harmonic component in the duty cycle signal.

- Input current i_g

The harmonic components of the IDBB converter input current can be calculated analogously to the procedure outlined in section 5.3.1, just by considering the inductor L_1 (see Figure 62) instead of the magnetizing inductance of the flyback transformer L_m.

- Inductances L_1 and L_2

In order to calculate the inductances L_1 and L_2, it will be considered a design technique slightly different from the one presented in section 4.2.2.1, since for the approach presented in this section, the effects of the duty cycle modulation upon the active power of the circuit will be taken into account. Therefore, the inductance L_1 and L_2 can be calculated by means of (5.47) and (5.48). Similarly to the analysis of the other integrated converters, the expressions for calculating the inductances of the IDBB converter were obtained from the power balance relationship of each power stage.

$$L_1 = \frac{\eta_{PFC}\eta_{PC}}{TP_o f_s}\int_0^{T/2} v_g(t)^2 d(t)^2 dt, \tag{5.47}$$

$$L_2 = \frac{2L_1}{\sqrt{\eta_{PFC}}\left(\frac{\sqrt{2}V_G}{V_B}\right)^2} \tag{5.48}$$

- High-frequency capacitor

The output capacitor of the IDBB converter can be calculated by means of (4.52).

- Low-frequency output current ripple ΔIo_{LF}

Regarding the output current ripple, the procedure is slightly different from the one outlined in Chapter 4, since the modeling presented in this chapter also takes into account the effect of the output capacitor for low-frequency ripple filtering.

Therefore, the output current of the IDBB converter can be calculated by means of:

$$i_o(t) = \frac{v_o(t) - V_t}{r_d}. \tag{5.49}$$

$$\frac{dv_o(t)}{dt} = \frac{1}{C_o}\left(\eta_{PC}\frac{v_b(t)^2 d(t)^2}{2f_s v_o(t) L_2} - \frac{v_o(t) - V_t}{r_d}\right). \tag{5.50}$$

On the other hand, the bus voltage can be obtained by means of:

$$\frac{dv_b(t)}{dt} = \frac{1}{2C_B f_s}\left(\eta_{PFC}\frac{v_g(t)^2 d(t)^2}{L_1 v_b(t)} - \frac{v_b(t)\, d(t)^2}{L_2}\right). \tag{5.51}$$

Therefore, the value of the low-frequency output current ripple can be obtained by solving numerically the equation system formed by (5.49) - (5.51).

5.6.2 Simulation results

In order to verify the theoretical equations developed in the last section, a PSIM simulation of the IDBB converter was carried out.Table 37 summarize the main simulation parameters whereas the circuit is shown in Figure 99. For the simulation of the IDBB converter, the same directives presented in subsection 5.3.2 were used. The MATLAB function used to calculate the theoretical waveforms of the flyback converter was named *calc_idbb* and is presented in Appendix B.7.

Table 37: Values used in the simulation of the IBuFly converter

Item	Value
v_g	$127\sqrt{2}\sin(2\pi 60t)$ V
d	$d_0 = 0.2186$, $d_2 = 0.04$, $d_4 = 0.01$, $d_6 = 0.01$, $d_8 = 0.01$, $phi2 = 20°$, $phi4 = 50°$,$phi6 = 0°$,$phi8 = 0°$
f_s	50 kHz
L_1	104.94 μH
L_m	210.81 μH
C_B	112 μF
C_o	5 μF
r_d	19.34 Ω
V_t	130.18 V
I_o	500 mA (nominal)
Simulation step	0.1 μs

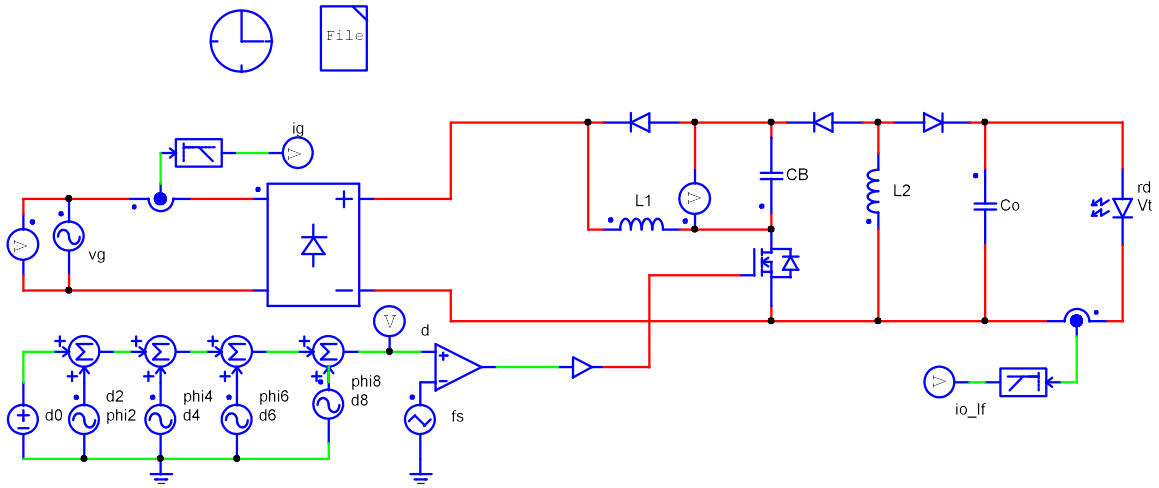


Figure 99: Circuit used in the simulation of the IDBB converter

Figures 100 and 101 presents the main waveforms obtained from the simulation of the converter compared with the theoretical model. From Figure 100 it is possible

to see that the simulation results regarding the bus voltage and the input current are quite similar to the waveforms predicted by the equations presented in subsection 5.6.1. Similarly, the output current waveform (Figure 101) obtained from the mathematical model presents also presents a good agreement with the PSIM results. The small differences between the theoretical waveforms and the simulated results in Figure 101 occurred owing to the simplifications assumed in the theoretical analysis, however, the overall results show that the equations obtained in subsection 5.6.1 can be used by the optimization algorithm to evaluate the low-frequency behavior of the IDBB converter.

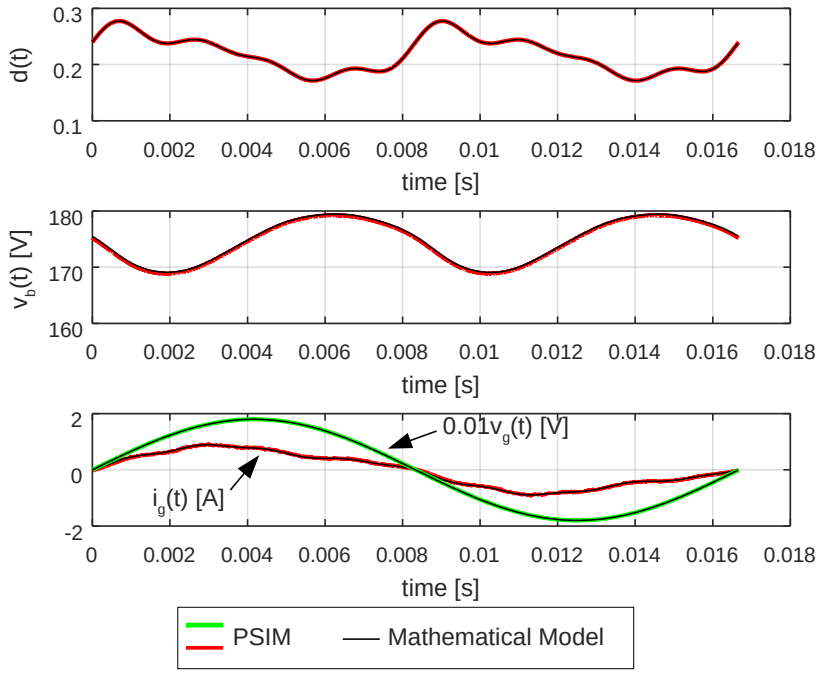


Figure 100: Comparison between the simulated waveforms with the theoretical model of the IDBB converter.

Table 38 presents a comparison between some values gathered from the simulation and the theoretical values. One can note that the mathematical model yielded a good prediction of the low-frequency behavior of the converter.

Table 38: Simulation results of the IDBB converter.

Item	Description	PSIM Result	Mathematical Model
I_o	Average output current	497.9 mA	498.6 mA
ΔIo_{LF}	Low-frequency output current ripple	413 mA	415 mA
ΔIo_{HF}	High-frequency output current ripple	106 mA	100 mA
V_B	Average bus voltage	174.12 V	174.79 V
THD	Total Harmonic Distortion	15.51 %	15.45%
PF	Power Factor	0.9758	0.9728

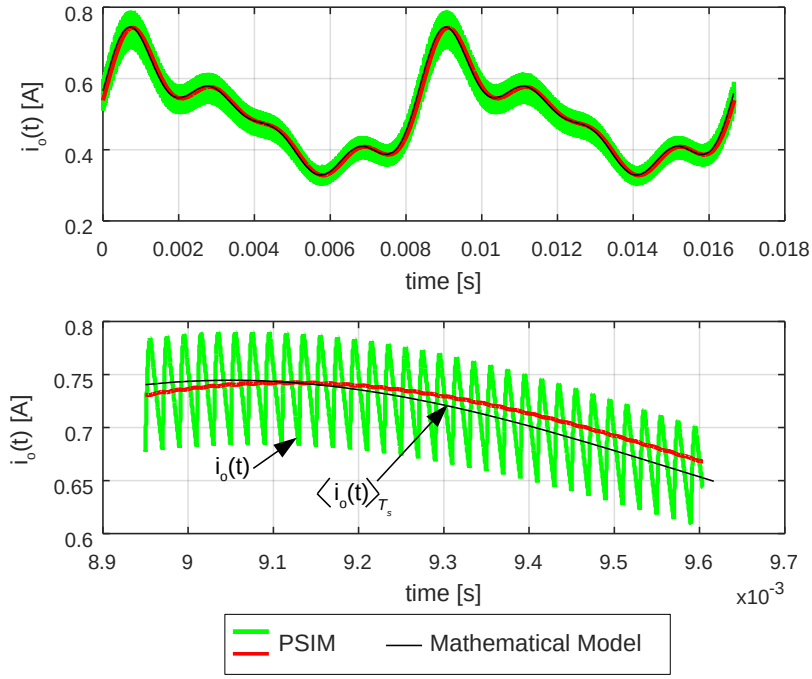


Figure 101: Comparison between the simulated waveforms of the IDBB converter output current with the theoretical model. (a) Low-frequency behavior; (b) High-frequency waveforms

5.6.3 Optimization results

This section presents the optimization results of the IDBB converter. Similarly to the other topologies, several design conditions were evaluated. Table 39 presents the parameters of the 32 studied cases.

Table 40 presents the results of the optimization process regarding the value of the bus capacitance for each studied case. As the other integrated converters, the results show that the ARC technique was able to reduce dramatically the required filtering capacitance. The maximum value of $\Delta C_{\%}$ was 84.8% in the first case for the configuration with the second and fourth harmonic components. Similarly to the other integrated converters, the best results in terms of capacitance reduction occurred for the cases in which the ripple requirements were stricter. Furthermore, one can note that the use of the fourth harmonic combined with the second one can improve the results in some cases, mainly in those in which the low-frequency ripple is higher (*i.e.*, cases 17 to 32).

The THD of the 32 studied cases and also the ΔTHD are presented in Table 41. Again, it is possible to observe a difference between the cases 1 to 16 and 17 to 32, which occurred owing to the same reasons addressed in Section 5.4.3.

Table 39: Cases studied in the IDBB converter

Case	$D_{0\%}$	D_{crit}	V_G	f_L	f_s	I_o	r_d	V_t	V_B	η_{PFC}	η_{PFC}	ΔIo_{LF}	ΔIo_{HF}
1	50 %	0.44	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	180 V	1	1	50 mA	25 mA
2	50 %	0.28	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	350 V	1	1	50 mA	25 mA
3	50 %	0.50	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	180 V	1	1	50 mA	25 mA
4	50 %	0.37	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	350 V	1	1	50 mA	25 mA
5	50 %	0.37	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	180 V	1	1	50 mA	25 mA
6	50 %	0.28	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	350 V	1	1	50 mA	25 mA
7	50 %	0.37	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	180 V	1	1	50 mA	25 mA
8	50 %	0.37	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	350 V	1	1	50 mA	25 mA
9	75 %	0.44	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	180 V	1	1	50 mA	25 mA
10	75 %	0.28	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	350 V	1	1	50 mA	25 mA
11	75 %	0.50	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	180 V	1	1	50 mA	25 mA
12	75 %	0.37	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	350 V	1	1	50 mA	25 mA
13	75 %	0.37	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	180 V	1	1	50 mA	25 mA
14	75 %	0.28	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	350 V	1	1	50 mA	25 mA
15	75 %	0.37	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	180 V	1	1	50 mA	25 mA
16	75 %	0.37	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	350 V	1	1	50 mA	25 mA
17	50 %	0.44	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	180 V	1	1	250 mA	100 mA
18	50 %	0.28	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	350 V	1	1	250 mA	100 mA
19	50 %	0.50	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	180 V	1	1	250 mA	100 mA
20	50 %	0.37	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	350 V	1	1	250 mA	100 mA
21	50 %	0.37	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	180 V	1	1	250 mA	100 mA
22	50 %	0.28	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	350 V	1	1	250 mA	100 mA
23	50 %	0.37	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	180 V	1	1	250 mA	100 mA
24	50 %	0.37	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	350 V	1	1	250 mA	100 mA
25	75 %	0.44	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	180 V	1	1	250 mA	100 mA
26	75 %	0.28	127 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	350 V	1	1	250 mA	100 mA
27	75 %	0.50	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	180 V	1	1	250 mA	100 mA
28	75 %	0.37	127 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	350 V	1	1	250 mA	100 mA
29	75 %	0.37	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	180 V	1	1	250 mA	100 mA
30	75 %	0.28	220 V	60 Hz	50 kHz	500 mA	19.34 Ω	130.18 V	350 V	1	1	250 mA	100 mA
31	75 %	0.37	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	180 V	1	1	250 mA	100 mA
32	75 %	0.37	220 V	60 Hz	50 kHz	500 mA	29.02 Ω	195.26 V	350 V	1	1	250 mA	100 mA

Table 40: Bus capacitance and $\Delta C_{\%}$ of the IDBB converter with ARC for all the studied cases

Case	*Default*	2^{nd}	4^{th}	6^{th}	8^{th}	2^{nd} and 4^{th}	2^{nd} and 6^{th}	2^{nd} and 8^{th}	4^{th} and 6^{th}	4^{th} and 8^{th}	6^{th} and 8^{th}
1	105 μF	27 μF (74.3%)	105 μF (-0.0%)	105 μF (-0.0%)	105 μF (-0.0%)	16 μF (84.8%)	27 μF (74.3%)	27 μF (74.3%)	105 μF (-0.0%)	105 μF (-0.0%)	105 μF (-0.0%)
2	28 μF	8 μF (71.4%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)	8 μF (71.4%)	8 μF (71.4%)	8 μF (71.4%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)
3	157 μF	36 μF (77.1%)	157 μF (-0.0%)	157 μF (-0.0%)	157 μF (-0.0%)	24 μF (84.7%)	36 μF (77.1%)	36 μF (77.1%)	157 μF (-0.0%)	157 μF (-0.0%)	157 μF (-0.0%)
4	42 μF	10 μF (76.2%)	42 μF (-0.0%)	42 μF (-0.0%)	42 μF (-0.0%)	10 μF (76.2%)	10 μF (76.2%)	10 μF (76.2%)	42 μF (-0.0%)	42 μF (-0.0%)	42 μF (-0.0%)
5	105 μF	24 μF (77.1%)	105 μF (-0.0%)	105 μF (-0.0%)	105 μF (-0.0%)	24 μF (77.1%)	24 μF (77.1%)	24 μF (77.1%)	105 μF (-0.0%)	105 μF (-0.0%)	105 μF (-0.0%)
6	28 μF	8 μF (71.4%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)	8 μF (71.4%)	8 μF (71.4%)	8 μF (71.4%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)
7	156 μF	36 μF (76.9%)	156 μF (-0.0%)	156 μF (-0.0%)	156 μF (-0.0%)	27 μF (82.7%)	36 μF (76.9%)	36 μF (76.9%)	156 μF (-0.0%)	156 μF (-0.0%)	156 μF (-0.0%)
8	42 μF	10 μF (76.2%)	42 μF (-0.0%)	42 μF (-0.0%)	42 μF (-0.0%)	10 μF (76.2%)	10 μF (76.2%)	10 μF (76.2%)	42 μF (-0.0%)	42 μF (-0.0%)	42 μF (-0.0%)
9	106 μF	25 μF (76.4%)	106 μF (-0.0%)	106 μF (-0.0%)	106 μF (-0.0%)	18 μF (83.0%)	25 μF (76.4%)	25 μF (76.4%)	106 μF (-0.0%)	106 μF (-0.0%)	106 μF (-0.0%)
10	28 μF	7 μF (75.0%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)	7 μF (75.0%)	7 μF (75.0%)	7 μF (75.0%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)
11	158 μF	37 μF (76.6%)	158 μF (-0.0%)	158 μF (-0.0%)	158 μF (-0.0%)	27 μF (82.9%)	37 μF (76.6%)	37 μF (76.6%)	158 μF (-0.0%)	158 μF (-0.0%)	158 μF (-0.0%)
12	42 μF	10 μF (76.2%)	42 μF (-0.0%)	42 μF (-0.0%)	42 μF (-0.0%)	7 μF (83.3%)	10 μF (76.2%)	10 μF (76.2%)	42 μF (-0.0%)	42 μF (-0.0%)	42 μF (-0.0%)
13	105 μF	24 μF (77.1%)	105 μF (-0.0%)	105 μF (-0.0%)	105 μF (-0.0%)	18 μF (82.9%)	24 μF (77.1%)	24 μF (77.1%)	105 μF (-0.0%)	105 μF (-0.0%)	105 μF (-0.0%)
14	28 μF	7 μF (75.0%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)	7 μF (75.0%)	7 μF (75.0%)	7 μF (75.0%)	28 μF (-0.0%)	28 μF (-0.0%)	28 μF (-0.0%)
15	157 μF	36 μF (77.1%)	157 μF (-0.0%)	157 μF (-0.0%)	157 μF (-0.0%)	27 μF (82.8%)	36 μF (77.1%)	36 μF (77.1%)	157 μF (-0.0%)	157 μF (-0.0%)	157 μF (-0.0%)
16	42 μF	10 μF (76.2%)	42 μF (-0.0%)	42 μF (-0.0%)	42 μF (-0.0%)	7 μF (83.3%)	10 μF (76.2%)	10 μF (76.2%)	42 μF (-0.0%)	42 μF (-0.0%)	42 μF (-0.0%)
17	21 μF	10 μF (52.4%)	21 μF (-0.0%)	19 μF (9.5%)	21 μF (-0.0%)	7 μF (66.7%)	10 μF (52.4%)	10 μF (52.4%)	19 μF (9.5%)	21 μF (-0.0%)	19 μF (9.5%)
18	6 μF	3 μF (50.0%)	6 μF (-0.0%)	6 μF (-0.0%)	6 μF (-0.0%)	2 μF (66.7%)	3 μF (50.0%)	3 μF (50.0%)	6 μF (-0.0%)	6 μF (-0.0%)	6 μF (-0.0%)
19	31 μF	15 μF (51.6%)	31 μF (-0.0%)	28 μF (9.7%)	31 μF (-0.0%)	12 μF (61.3%)	15 μF (51.6%)	15 μF (51.6%)	28 μF (9.7%)	31 μF (-0.0%)	28 μF (9.7%)
20	8 μF	4 μF (50.0%)	8 μF (-0.0%)	8 μF (-0.0%)	8 μF (-0.0%)	3 μF (62.5%)	4 μF (50.0%)	4 μF (50.0%)	8 μF (-0.0%)	8 μF (-0.0%)	8 μF (-0.0%)
21	21 μF	10 μF (52.4%)	21 μF (-0.0%)	21 μF (-0.0%)	21 μF (-0.0%)	8 μF (61.9%)	10 μF (52.4%)	10 μF (52.4%)	21 μF (-0.0%)	21 μF (-0.0%)	21 μF (-0.0%)
22	6 μF	3 μF (50.0%)	6 μF (-0.0%)	6 μF (-0.0%)	6 μF (-0.0%)	2 μF (66.7%)	3 μF (50.0%)	3 μF (50.0%)	6 μF (-0.0%)	6 μF (-0.0%)	6 μF (-0.0%)
23	31 μF	15 μF (51.6%)	31 μF (-0.0%)	31 μF (-0.0%)	31 μF (-0.0%)	12 μF (61.3%)	14 μF (54.8%)	15 μF (51.6%)	31 μF (-0.0%)	31 μF (-0.0%)	31 μF (-0.0%)
24	8 μF	4 μF (50.0%)	8 μF (-0.0%)	8 μF (-0.0%)	8 μF (-0.0%)	3 μF (62.5%)	4 μF (50.0%)	4 μF (50.0%)	8 μF (-0.0%)	8 μF (-0.0%)	8 μF (-0.0%)
25	21 μF	10 μF (52.4%)	21 μF (-0.0%)	18 μF (14.3%)	21 μF (-0.0%)	10 μF (52.4%)	10 μF (52.4%)	10 μF (52.4%)	18 μF (14.3%)	21 μF (-0.0%)	18 μF (14.3%)
26	6 μF	3 μF (50.0%)	6 μF (-0.0%)	5 μF (16.7%)	6 μF (-0.0%)	3 μF (50.0%)	3 μF (50.0%)	3 μF (50.0%)	5 μF (16.7%)	6 μF (-0.0%)	5 μF (16.7%)
27	31 μF	15 μF (51.6%)	30 μF (3.2%)	27 μF (12.9%)	31 μF (-0.0%)	14 μF (54.8%)	15 μF (51.6%)	15 μF (51.6%)	27 μF (12.9%)	30 μF (3.2%)	27 μF (12.9%)
28	8 μF	4 μF (50.0%)	8 μF (-0.0%)	7 μF (12.5%)	8 μF (-0.0%)	4 μF (50.0%)	4 μF (50.0%)	4 μF (50.0%)	7 μF (12.5%)	8 μF (-0.0%)	7 μF (12.5%)
29	21 μF	10 μF (52.4%)	21 μF (-0.0%)	18 μF (14.3%)	21 μF (-0.0%)	10 μF (52.4%)	10 μF (52.4%)	10 μF (52.4%)	18 μF (14.3%)	21 μF (-0.0%)	18 μF (14.3%)
30	6 μF	3 μF (50.0%)	6 μF (-0.0%)	5 μF (16.7%)	6 μF (-0.0%)	3 μF (50.0%)	3 μF (50.0%)	3 μF (50.0%)	5 μF (16.7%)	6 μF (-0.0%)	5 μF (16.7%)
31	31 μF	15 μF (51.6%)	31 μF (-0.0%)	28 μF (9.7%)	31 μF (-0.0%)	15 μF (51.6%)	15 μF (51.6%)	15 μF (51.6%)	28 μF (9.7%)	31 μF (-0.0%)	28 μF (9.7%)
32	8 μF	4 μF (50.0%)	8 μF (-0.0%)	7 μF (12.5%)	8 μF (-0.0%)	4 μF (50.0%)	4 μF (50.0%)	4 μF (50.0%)	7 μF (12.5%)	8 μF (-0.0%)	7 μF (12.5%)

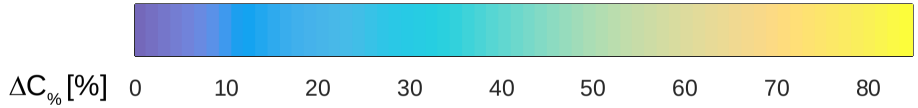
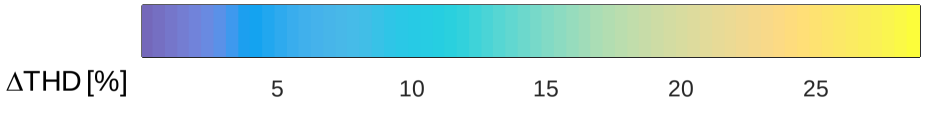


Table 41: THD and ΔTHD of the IDBB converter with ARC for all the studied cases

Case	*Default*	2^{nd}	4^{th}	6^{th}	8^{th}	2^{nd} and 4^{th}	2^{nd} and 6^{th}	2^{nd} and 8^{th}	4^{th} and 6^{th}	4^{th} and 8^{th}	6^{th} and 8^{th}
1	0.0%	9.2% (+9.2%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)	19.0% (+19.0%)	9.2% (+9.2%)	9.2% (+9.2%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)
2	0.0%	7.0% (+7.0%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	7.0% (+7.0%)	7.0% (+7.0%)	7.0% (+7.0%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
3	0.0%	12.0% (+12.0%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	19.8% (+19.8%)	12.0% (+12.0%)	12.0% (+12.0%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
4	0.0%	10.7% (+10.7%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)	10.7% (+10.7%)	10.7% (+10.7%)	10.7% (+10.7%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)
5	0.0%	10.9% (+10.9%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	10.9% (+10.9%)	10.9% (+10.9%)	10.9% (+10.9%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
6	0.0%	7.0% (+7.0%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	7.0% (+7.0%)	7.0% (+7.0%)	7.0% (+7.0%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
7	0.0%	10.9% (+10.9%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)	16.5% (+16.5%)	10.9% (+10.9%)	10.9% (+10.9%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)
8	0.0%	10.7% (+10.7%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)	10.7% (+10.7%)	10.7% (+10.7%)	10.7% (+10.7%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)
9	0.0%	12.2% (+12.2%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)	15.5% (+15.5%)	12.2% (+12.2%)	12.2% (+12.2%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)
10	0.0%	9.4% (+9.4%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (+0.0%)	9.4% (+9.4%)	9.4% (+9.4%)	9.4% (+9.4%)	0.0% (-0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
11	0.0%	10.7% (+10.7%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	16.7% (+16.7%)	10.7% (+10.7%)	10.7% (+10.7%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
12	0.0%	10.7% (+10.7%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	14.6% (+14.6%)	10.7% (+10.7%)	10.7% (+10.7%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
13	0.0%	10.9% (+10.9%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	15.0% (+15.0%)	10.9% (+10.9%)	10.9% (+10.9%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
14	0.0%	9.4% (+9.4%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	9.4% (+9.4%)	9.4% (+9.4%)	9.4% (+9.4%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
15	0.0%	10.9% (+10.9%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)	15.0% (+15.0%)	10.9% (+10.9%)	10.9% (+10.9%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)
16	0.0%	10.7% (+10.7%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	14.6% (+14.6%)	10.7% (+10.7%)	10.7% (+10.7%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
17	0.0%	23.9% (+23.9%)	0.0% (-0.0%)	6.5% (+6.5%)	0.0% (-0.0%)	23.1% (+23.1%)	28.5% (+28.5%)	23.9% (+23.9%)	6.5% (+6.5%)	0.0% (-0.0%)	6.5% (+6.5%)
18	0.0%	21.9% (+21.9%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	25.9% (+25.9%)	21.9% (+21.9%)	21.9% (+21.9%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
19	0.0%	25.0% (+25.0%)	0.0% (+0.0%)	5.6% (+5.6%)	0.0% (+0.0%)	26.8% (+26.8%)	25.2% (+25.2%)	25.0% (+25.0%)	5.6% (+5.6%)	0.0% (+0.0%)	5.6% (+5.6%)
20	0.0%	22.3% (+22.3%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)	27.5% (+27.5%)	28.2% (+28.2%)	22.3% (+22.3%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)
21	0.0%	22.8% (+22.8%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	26.4% (+26.4%)	28.8% (+28.8%)	22.8% (+22.8%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
22	0.0%	21.9% (+21.9%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)	25.9% (+25.9%)	21.9% (+21.9%)	21.9% (+21.9%)	0.0% (+0.0%)	0.0% (+0.0%)	0.0% (+0.0%)
23	0.0%	22.8% (+22.8%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)	28.2% (+28.2%)	28.8% (+28.8%)	22.8% (+22.8%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)
24	0.0%	22.3% (+22.3%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)	27.5% (+27.5%)	28.2% (+28.2%)	22.3% (+22.3%)	0.0% (-0.0%)	0.0% (-0.0%)	0.0% (-0.0%)
25	0.0%	19.1% (+19.1%)	4.3% (+4.3%)	4.3% (+4.3%)	0.0% (-0.0%)	15.7% (+15.7%)	19.1% (+19.1%)	19.1% (+19.1%)	4.3% (+4.3%)	4.3% (+4.3%)	4.3% (+4.3%)
26	0.0%	19.5% (+19.5%)	0.0% (+0.0%)	6.6% (+6.6%)	0.0% (+0.0%)	19.5% (+19.5%)	19.5% (+19.5%)	19.5% (+19.5%)	6.6% (+6.6%)	0.0% (+0.0%)	6.6% (+6.6%)
27	0.0%	19.5% (+19.4%)	3.8% (+3.8%)	3.8% (+3.8%)	0.0% (+0.0%)	17.1% (+17.1%)	19.5% (+19.4%)	19.5% (+19.4%)	3.8% (+3.8%)	3.8% (+3.8%)	3.8% (+3.8%)
28	0.0%	18.5% (+18.5%)	5.0% (+5.0%)	5.0% (+5.0%)	0.0% (+0.0%)	16.1% (+16.1%)	18.5% (+18.5%)	18.5% (+18.5%)	5.0% (+5.0%)	5.0% (+5.0%)	5.0% (+5.0%)
29	0.0%	19.0% (+19.0%)	5.1% (+5.1%)	5.1% (+5.1%)	0.0% (+0.0%)	16.4% (+16.4%)	19.0% (+19.0%)	19.0% (+19.0%)	5.1% (+5.1%)	5.1% (+5.1%)	5.1% (+5.1%)
30	0.0%	19.5% (+19.5%)	0.0% (+0.0%)	6.6% (+6.6%)	0.0% (+0.0%)	19.5% (+19.5%)	19.5% (+19.5%)	19.5% (+19.5%)	6.6% (+6.6%)	0.0% (+0.0%)	6.6% (+6.6%)
31	0.0%	19.0% (+19.0%)	5.1% (+5.1%)	5.1% (+5.1%)	0.0% (-0.0%)	16.4% (+16.4%)	19.0% (+19.0%)	19.0% (+19.0%)	5.1% (+5.1%)	5.1% (+5.1%)	5.1% (+5.1%)
32	0.0%	18.5% (+18.5%)	5.0% (+5.0%)	5.0% (+5.0%)	0.0% (+0.0%)	16.1% (+16.1%)	18.5% (+18.5%)	18.5% (+18.5%)	5.0% (+5.0%)	5.0% (+5.0%)	5.0% (+5.0%)



It is worth mentioning that among the studied integrated converters, the IDBB topology is the one that presented the higher values of ΔTHD. Nevertheless, in general, the absolute value of the THD of this circuit remained lower than the other topologies for a same level of capacitance reduction.

Table 35 summarizes the results obtained from the optimization procedure. Owing to the ΔTHD, the FoM values of the IDBB converter were slightly worse than the others integrated topologies. However, the data of Table 35 attested the superior performance of the IDBB topology compared with the single-stage flyback converter. Furthermore, the table also shows that the best configuration for the IDBB converter is the combination of the second and the fourth harmonic component, although the results obtained using only the second harmonic in the duty cycle were similar.

It is important to highlight that the theoretical analysis presented in this section has a good agreement with the experimental results of the IDBB converter (see Chapter 4), since the capacitance reduction and the THD of the input current obtained in the experiments were 46.3% and 14%, respectively. Those values are similar to the ones obtained in this chapter for a ripple criterion of 50% (the same adopted in the experiments).

Table 42: Summary of the optimization results for the IDBB converter with ARC

Harmonic	Capacitance Reduction $\Delta C_{\%}$			ΔTHD			Average FoM
	Mean	STD	K-S test	Mean	STD	K-S test	($K_1 = 2$ and $K_2 = 1$)
2^{nd}	63.3%	12.6%	true	15.6%	5.7%	true	1.97
4^{th}	0.1%	0.6%	true	0.9%	1.9%	true	0.99
6^{th}	4.0%	6.2%	true	1.7%	2.6%	true	1.06
8^{th}	0.0%	0.0%	true	0.0%	0.0%	true	1.00
2^{nd} and 4^{th}	68.5%	12.5%	true	17.5%	6.2%	true	2.03
2^{nd} and 6^{th}	63.4%	12.5%	true	16.5%	7.1%	true	1.97
2^{nd} and 8^{th}	63.3%	12.6%	true	15.6%	5.7%	true	1.97
4^{th} and 6^{th}	4.0%	6.2%	true	1.7%	2.6%	true	1.06
4^{th} and 8^{th}	0.1%	0.6%	true	0.9%	1.9%	true	0.99
6^{th} and 8^{th}	4.0%	6.2%	true	1.7%	2.6%	true	1.06

5.7 Summary

This chapter presented a generalized study of the Active Ripple Compensation technique applied to some PFC off-line LED drivers. Four topologies were investigated: a single-stage flyback converter and three integrated topologies. Differently from Chap-

ter 4, the analyses presented in this chapter considered that the duty cycle function is composed not only by a dc level plus a second harmonic, but may also contain the fourth, sixth and eighth harmonic components. Since this consideration makes the sizing of the converter elements by means of design abacuses a complex task, the whole design procedure was modeled as a non-linear constrained optimization problem. In this approach, all the design requirements, such as the maximum output current ripple and the limits for the input current harmonic components, are compiled in a matrix of constraints, which is evaluated by the optimization algorithm to find the optimum solution for a certain performance criterion. The objective function was defined so that the optimum solution minimizes the capacitance sized to filter the low-frequency ripple of the circuit output current.

In order to solve the optimization problem, it was necessary to find the mathematical description of all the studied converter considering the duty cycle modulation. It is important to highlight that, differently from the conventional strategies, the design of the converter by means of the optimization approach can be performed using equations of analysis. In other words, it was not necessary to obtain design equations or mathematical models with a close-form solution. For example, the use of differential equations to describe the bus voltage can be used instead of a expression for sizing the bus capacitance. This approach results in a precise mathematical description of the low frequency behavior of the circuit, as attested by the simulations results.

The optimization results demonstrated that the performance of the ARC technique in the integrated converters was better when compared to the flyback topology. Furthermore, the analysis showed that the second harmonic is the component that has a major impact on the ARC technique behavior, although the inclusion of the forth or the sixth ones could improve the performance in some cases.

A Figure of Merit (FoM) was proposed to quantify the performance of the duty cycle modulation. By means of this parameter, it was possible to see that the IBoBu converter presented the best results, since for this topology, the ARC technique allowed for a huge capacitance reduction at the cost of a small additional input current distortion.

6 OPTIMIZED DESIGN OF A WIDE-BANDWIDTH CONTROLLER FOR LOW-FREQUENCY RIPPLE COMPENSATION

6.1 INTRODUCTION

The last two chapters presented an approach for reducing the low-frequency ripple in VMC off-line LED drivers. The strategy was based on a controlled modulation of the duty cycle signal so that the output current ripple of the driver could be reduced. Chapter 4 showed that the ARC technique could be implemented by means of an additional control branch for each desired harmonic in the duty cycle function. For example, if the signal $d(t)$ is composed by a dc value and an ac portion oscillating at twice the line frequency, two branches would be required for the control loop: one for stabilizing the average value of the output current and another for reducing the low-frequency ripple.

Chapter 5 showed that it is possible to improve the performance of the ARC technique in some cases by adding other harmonic components to the duty cycle signal. However, this strategy would lead to a complex implementation, since the controller would have more branches.

This chapter presents an alternative implementation of the ARC technique by means of a single wide-bandwidth controller, which will be responsible for performing both the control of the average current and also the reduction of the output current ripple. This strategy will allow for the injection of more harmonic components to the duty cycle signal without the use of several branches in the control structure. However, owing to the lack of degrees of freedom in the design using a single compensator, it is not possible to choose the amplitudes and phases of each harmonic component, demanding a new approach for designing the converter.

Although the design of the ARC with a single compensator differs from the strategy presented in the previous chapters, the use of the optimization approach remains suitable for this case, since it allows for a complete evaluation of the system. As will be discussed along the chapter, the design procedure in this situation must deal with

the sizing of the parameters of the control circuit simultaneously with the elements of the converter, which differs a little from the approach presented in Chapter 4.

This chapter is divided as follows. Section 6.2 presents a qualitative analysis of the implementation of the ARC technique using a single controller, addressing the main aspects and highlighting the differences between this approach and the one presented in Chapter 4. Section 6.3 presents the modeling of the design procedure as a non-linear optimization problem. The design strategy was then employed for sizing a converter based on the IDBB topology, whose main equations are outlined in Section 6.4. Section 6.5 presents the application characteristics and the search-space for the optimization problem. Section 6.6 describes the optimization algorithm , while the design results are presented in Section 6.7. Finally, sections 6.8 and 6.9 address the simulation and experimental results. The chapter is then summarized in Section 6.10.

6.2 ANALYSIS OF THE IMPLEMENTATION OF THE ARC TECHNIQUE WITH A SINGLE CONTROLLER

As already introduced in the two previous chapters, the duty cycle of a VMC converter can be used to modify its large-signal behavior. This property allowed for the design of converters with reduced storage capacitance by using an ARC technique that relied on the proper modulation of the converter control signal. The design methodology presented in Chapter 4 was divided in two parts. First, the elements of the circuit as well as the duty cycle function were designed. After, the controllers were sized so that the duty cycle function assumed the form defined in the previous step. The main advantages of this approach is the independence between the design of the converter elements and the control circuit. Furthermore, since the duty cycle function was known *a priori*, the operating mode could be ensured without the need of solving the equations of the circuit.

The design procedure using a single controller is different from the one described above, since it is not possible to predict the duty cycle function before solving the converter equations. This means that the whole system (*i.e.,* the power and the control circuits) must be evaluated simultaneously in order to obtain the large signal behavior of the converter. The fact that the duty cycle is unknown *a priori* and cannot be calculated by means of the design parameters, such as the load and grid data, represents a new paradigm for designing PWM converters, since the main large-signal equations are represented in terms of the duty cycle.

Figure 102 illustrates a HPF VMC LED driver with a wide-bandwidth PI controller. The analysis carried out in this section considers that the driver is based on a single-stage converter or an integrated topology, which are the cases addressed in this work. Furthermore, the PI controller was chosen because it is well-established in the industry and has a good performance in terms of dynamic response. The main low-frequency waveforms of the circuit are depicted in Figure 102 in order to explain the behavior of the converter.

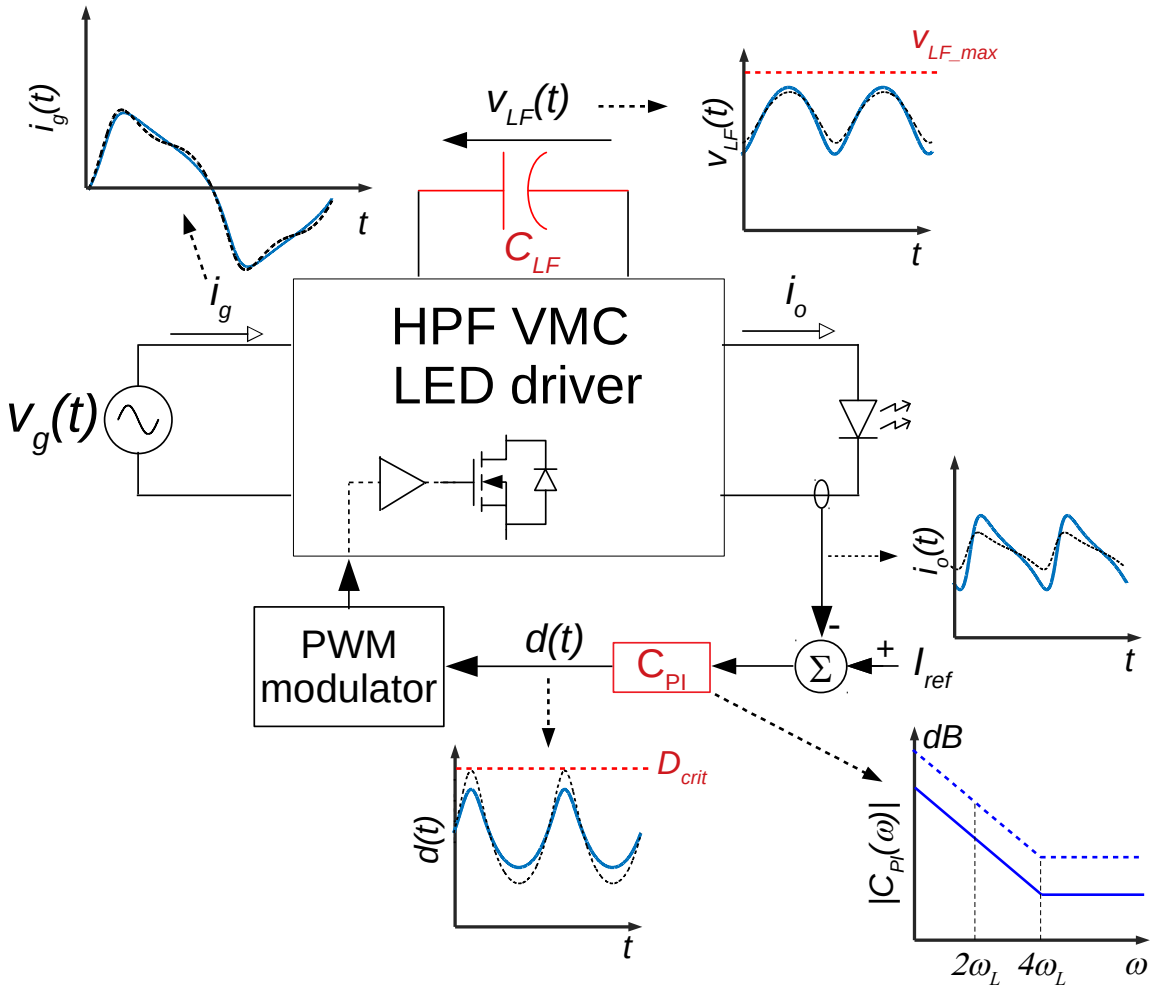


Figure 102: HPF LED driver with a wide-bandwidth PI controller.

From the analysis of Figure 102, it is possible to note that the controller is tunned so that the low-frequency ripple of the output current is compensated. Nevertheless, this compensation affects not only the output current waveform, but all the low-frequency behavior of the converter. The other element of the system that affects directly the shape of the low-frequency waveforms is the capacitor C_{LF}, which is the element in the power circuit sized to filter its input-to-output instantaneous power imbalance. Thus, these two elements must be sized together since they have a mutual influence upon the

low-frequency behavior of the converter. As can be seen in Figure 102, two possible designs for the PI controller were considered and the difference between them is that the first case (solid lines) has a lower dc gain than the second one (dashed lines).

The sketched waveforms indicate that when the dc gain of the PI controller is higher, the gain that the compensator gives to the second and the fourth harmonic components of the error signal ε is also higher. As a consequence, the amplitude of the duty cycle modulation increases so that the bus voltage and the output current ripples become lower. On the other hand, the rise of the duty cycle modulation reflects negatively in the input current, since it becomes more distorted when compared to the case in which the PI has a lower gain. It is important to highlight that this phenomena was already discussed in the previous chapters, which showed that higher amplitudes of the duty cycle harmonics increase the distortion of the input current.

The analysis outlined above discussed the influence of the controller design upon the low-frequency behavior of the circuit. However, as the compensator, the capacitor C_{LF} can change dramatically the characteristic of the circuit waveforms. For example, if the controller remains unchanged and the capacitor is decreased, the effects on the waveforms would be similar to the ones verified in the case which the gain of the compensator was higher. This occurs because the harmonic components of the error signal will be higher owing to the increase in the output current low frequency ripple. Therefore, since the gain of the PI controller remained the same, the amplitudes of the harmonic components of the duty cycle will grow. By summarizing, both the compensator and the capacitor C_{LF} influences on the harmonic components of the duty cycle function.

Figure 102 also highlights two operational constrains that must be taken into account when designing the converter. The first one is regarding the maximum duty cycle D_{crit}. Differently from the ARC technique presented in Chapters 4 and 5, in the approach involving a wide-bandwidth controller, it is necessary to solve the circuit equations in order to obtain the function $d(t)$, since the duty cycle is not a parameter neither a variable in the design process. In this case, the characteristic of $d(t)$ derives from the chosen values of the capacitor C_{LF} and the compensator. Therefore, the verification of the DCM operation of the converter, *i.e.*, if $d(t) < D_{crit} \ \forall \ t$, can be accomplished only after solving the equations of the circuit.

The second constraint that must be analyzed by the designer is regarding the voltage across the capacitor C_{LF}. If the capacitance of this element decreases, the voltage

ripple tends to increase. Therefore, it is necessary to check if $v_{LF}(t) < V_{LF\_max} \ \forall \ t$ as long as the circuit equations have been solved in order to ensure the safe operation of the capacitor.

Other important aspect regarding the ARC technique using a wide-bandwidth controller is that, differently from the control structure presented in Chapter 4, it is not possible to control the harmonic content of the duty cycle precisely. As shown in Figure 102, a wide-bandwidth controller will compensate several harmonic components of the error signal (*e.g.,* the second, fourth, etc) and not only one, as the case of the approach presented in Chapter 4. Therefore, instead of sizing the amplitudes of the duty cycle harmonic components, the design methodology consists on tuning the compensator directly in order to obtain the desired low-frequency behavior, a procedure that is outlined in the next section.

6.3 DESIGN PROCEDURE

As presented in the previous section, the design of a HPF LED driver with a high-bandwidth controller must deal with the sizing of the elements of the power circuit simultaneously with the calculation of the compensator. As already addressed in Chapter 5, the optimization approach is also suitable in this case because it allows for the consideration of several design constraints and does not need analytical equations for its implementation.

In order to present the design methodology, the circuit illustrated in Figure 103 has been chosen. One can note that the studied driver is based on the IDBB converter, already explored in the previous chapters, and the control structure is implemented by means of an analog circuit composed by operational amplifiers and a classical PWM modulator: the TL494. As addressed in the previous section, the low-frequency behavior of the circuit depends mostly on the capacitor sized to filter the low-frequency, *i.e.*, C_B, and the controller, characterized by the resistors R_1, R_2 and the capacitor C_1.

Based on the directives discussed in Section 6.2, the design of the converter with a wide-bandwidth controller was modeled as an optimization problem, defined in terms of the optimization variables vector x, as shown in the following:

$$\begin{aligned} &\min f(x) = w_{opt}\overline{c_1(x)} + (1 - w_{opt})\,\overline{c_2(x)} \\ &subject\,to \quad H(x) \leqslant 0_{12x1} \end{aligned} \tag{6.1}$$

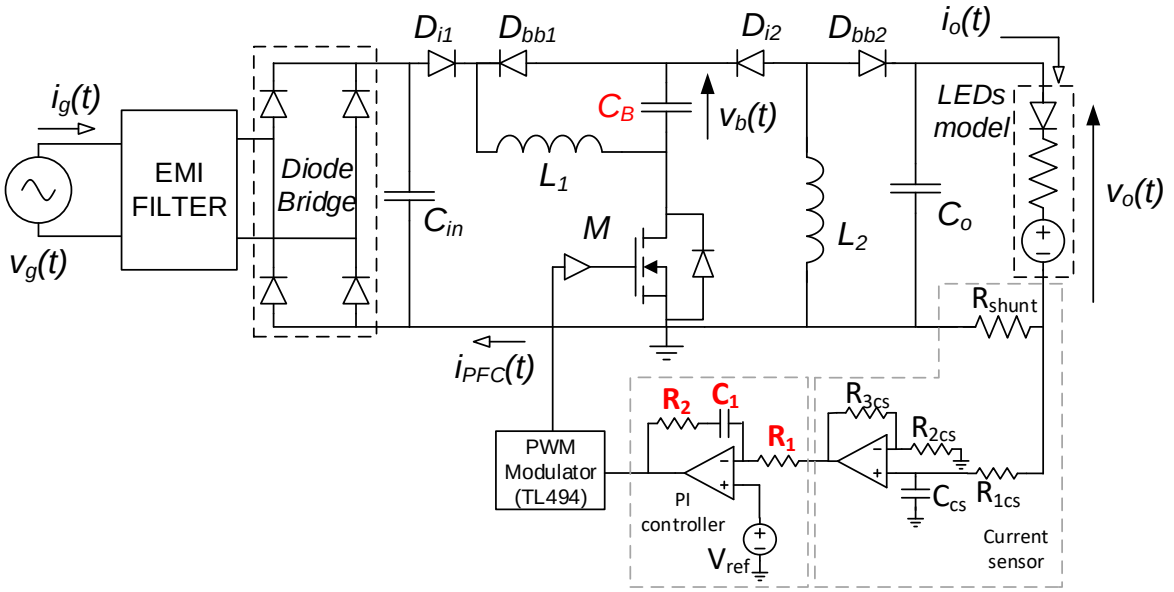


Figure 103: Schematic of the IDBB with a PI controller.

One can note that the optimization problem was defined in terms of w_{opt}, which varies from 0 to 1 and represents the weight that characterizes the optimization strategy. On the other hand, $\overline{c_1(x)}$ and $\overline{c_2(x)}$ are the Normalized Single-Objective Cost (NSOC) functions, given by (6.2) and (6.3), respectively.

$$\overline{c_1(x)} = \frac{c_1(x)}{N_{f1}} = \frac{C_B\left(10^6 F^{-1}\right) + \Delta I_{o\_LF}\left(A^{-1}\right)}{N_{f1}} \tag{6.2}$$

$$\overline{c_2(x)} = \frac{c_2(x)}{N_{f2}} = \frac{\max(THD, 1\%)}{N_{f2}}, \tag{6.3}$$

where $\max(arg1,arg2)$ is a function that returns the maximum value of two arguments.

From the definition of the NSOC functions, it is possible to observe that $\overline{c_1(x)}$ is related to the capacitor C_B and the low-frequency ripple of the output current. On the other hand, $\overline{c_2(x)}$ accounts the THD of the input current of the circuit. It is important to highlight that the Single-Objective Cost (SOC) functions $c_1(x)$ and $c_2(x)$ must be normalized in this case because they have different orders of magnitude. Therefore, the normalization allows the designer to configure the optimization strategy just by setting the weight w_{opt}. The normalization factors N_{f1} and N_{f2} can be found by means of (6.4) and (6.5), respectively.

$$\begin{aligned} &N_{f1} = \min\{c_1(x)\} \\ &\text{subjected to } H(x) \leq 0_{12x1} \end{aligned} \tag{6.4}$$

$$\begin{aligned} &N_{f2} = \min\{c_2(x)\} \\ &\text{subjected to } H(x) \leq 0_{12x1} \end{aligned} \tag{6.5}$$

The function max was used to defined a threshold for the THD, *i.e.*, if the THD is lower than 1%, the SOC function $c_2(x)$ will be equal 1%. This strategy was implemented in order to avoid numerical errors during the optimization procedure, since the theoretical value of $c_2(x)$ for the IDBB converter can be zero for some values of x.

The matrix H, given by (6.6), compiles the constraints of the optimization problem, which are the same as those presented in Chapter 4, except the last four. The constraint regarding the convergence time t_c evaluates the time required by the system to null the steady state error of the output current. If this time is greater than a limit determined by t_{c_max}, the constraint is violated. By inserting this requirement, it is possible to avoid solutions which lead the system to a slow dynamic response. On the other hand, the constraint related to the bus voltage $v_b(t)$ ensures the safe operation of the bus capacitor, as already discussed in Section 6.2.

The two last constraints of matrix H are related to the stability of the closed-loop system. According to Aström and Murray (2010), a phase margin Pm above 30° and a gain margin Gm above 2 are reasonable assumptions for defining the stability criterion. The equations used for obtaining the phase and gain margins are presented in the next subsection.

$$H(x) = \begin{pmatrix} \Delta Io_{LF} - \Delta Io_{LF\_max} \\ d(t) - 0.9D_{crit} \\ I_3 - 0.3PFI_1 \\ I_5 - 0.1I_1 \\ I_7 - 0.07I_1 \\ I_9 - 0.05I_1 \\ I_{11} - 0.03I_1 \\ I_{13} - 0.03I_1 \\ t_c - t_{c\_max} \\ v_b(t) - 0.95V_{B\_max} \\ 30^\circ - Pm \\ 2 - Gm \end{pmatrix}, \tag{6.6}$$

Finally, it is necessary to define the vector containing the optimization variables x, given by:

$$x = \begin{bmatrix} C_B & R_1 & R_2 & C_1 \end{bmatrix}. \tag{6.7}$$

One can note from (6.7) that the optimization variables are the bus capacitance of the converter, sized to filter the low-frequency ripple of the circuit, and the elements that characterize the PI controller.

By summarizing, the optimization algorithm must search the value of the bus capacitance, as well as the components of the PI controller that minimize the multi-objective function $f(x)$ defined in (6.1), subject to the constraints compiled in $H(x)$.

It is worth mentioning that the optimization problem defined in this chapter can be considered multi-objective because it concerns two different aspects of the converter design: the capacitance C_B and input current THD. Such approach gives a flexibility for choosing the best strategy for the application, since the ARC technique introduce a trade-off between capacitance reduction and input current distortion.

Next section outlines the main equations used for solving (6.1).

6.4 MAIN EQUATIONS

In order to solve the optimization problem described in the previous section, it is necessary to derive the main equations of the converter. Differently from the previous chapters, the mathematical description of the circuit must take into account the control loop. Since the equations of the IDBB converter with large signal modulation were already discussed, the analysis presented in this section will only highlight the main differences, presenting the expressions in a straightforward way.

- Critical duty cycle D_{crit}

The methodology for calculating the critical duty cycle of the IDBB converter was already presented in section 4.2.2.1 and remains the same for the case with more than one harmonic component in the duty cycle signal. The value of D_{crit} is used by the optimization algorithm to evaluate the second constraint of matrix H, which ensures the DCM operation.

Differently from the methodology shown in the previous chapter, the evaluation

of the aforementioned design constraint cannot be performed *a priori*. This occurs because the duty cycle function is unknown at the beginning of the design procedure and depends on the other elements of the system, such as the bus capacitance and the parameters of the PI controller.

- Input current i_g

The input current of the IDBB converter was already discussed in the previous chapters and can be calculated by means of:

$$i_g(t) = \frac{v_g(t)d(t)^2}{2L_1 f_s}. \tag{6.8}$$

As can be seen, the calculation of the input current demands the duty cycle function $d(t)$, which is unknown *a priori*. Therefore, in order to obtain the input current of the converter, (6.8) must be used in a recursive algorithm, as will be shown along this chapter.

- Inductances L_1 and L_2

As already shown in Section 5.6.1, the duty cycle function influence on the calculation of the inductances, since it changes the power processed by the converter. This issue represents a problem in this case because d(t) is unknown *a priori*. Nevertheless, it was shown in Chapter 4 that if the duty cycle harmonic components have a small amplitude, it is possible to use the only the average value of the duty cycle for calculating the inductances with an acceptable error. Furthermore, Chapter 5 showed that integrated converters does not demand a large modulation of the duty cycle for compensating the ripple. Therefore, the calculation of the inductances of the IDBB converter with a wide-bandwidth compensator will be done considering only the average value of the duty cycle D_0, as shown in (6.9) and (6.10).

$$L_1 = \eta_{PFC}\eta_{PC}\frac{{D_0}^2 V_G^2}{4P_o f_s}, \tag{6.9}$$

$$L_2 = \frac{2L_1}{\sqrt{\eta_{PFC}}\left(\frac{\sqrt{2}V_G}{V_B}\right)^2} \tag{6.10}$$

It is worth mentioning that owing to the PI controller operation, the power processed by the converter will remain at the desired value. Furthermore, the design

procedure ensures the DCM operation by means of the second constraint of the matrix H. Thus, the effects of using only D_0 for calculating the inductances will be negligible.

Another important observation is that the average value of the duty cycle remains as a design parameter of the optimization problem, since it defines the approximated operating point of the circuit. In a practical implementation, the value of D_0 will be corrected by the controller in order to compensate the converter losses and the influence of the duty cycle modulation upon the power processed by the driver.

- High-frequency capacitor

The methodology for designing the IDBB converter output capacitor remains the same of Chapter 4. Therefore, this element can be calculated by means of (4.52), which is repeated here for the reader convenience.

$$\Delta I_{o\_HF} = \frac{1}{f_s C_o r_d}\left(I_o + \frac{\Delta I_{o\_LF}}{2}\right)\left(1 - D_0\frac{V_B}{V_o}\right). \tag{6.11}$$

- Low-frequency output current ripple ΔIo_{LF}

Regarding the output current ripple, the procedure is the same as outlined in Chapter 5. Therefore, the output current of the IDBB converter can be calculated by means of:

$$i_o(t) = \frac{v_o(t) - V_t}{r_d}. \tag{6.12}$$

$$\frac{dv_o(t)}{dt} = \frac{1}{C_o}\left(\eta_{PC}\frac{v_b(t)^2 d(t)^2}{2 f_s v_o(t) L_2} - \frac{v_o(t) - V_t}{r_d}\right). \tag{6.13}$$

On the other hand, the bus voltage can be obtained as follows:

$$\frac{dv_b(t)}{dt} = \frac{1}{2C_B f_s}\left(\eta_{PFC}\frac{v_g(t)^2 d(t)^2}{L_1 v_b\,(t)} - \frac{v_b\,(t)\,d(t)^2}{L_2}\right). \tag{6.14}$$

Therefore, the value of the low-frequency output current ripple can be obtained by solving numerically the equation system formed by (6.12) - (6.14).

- Duty cycle function

In order to calculate the duty cycle function, it is necessary to evaluate the control circuit, which can be done by means of the equation system shown in (6.15).

$$\begin{cases} \frac{dv_{cs}(t)}{dt} = \omega_{cs}\left(K_{cs}i_o(t) - v_{cs}(t)\right) \\ \frac{dv_{PI}(t)}{dt} = \frac{K_P}{T_i}V_{REF} - K_P K_{cs}\omega_{cs}i_o(t) + v_{cs}(t)\left(K_P\omega_{cs} - \frac{K_P}{T_i}\right) \\ d(t) = \frac{v_{PI}(t)}{V_{PWM}} \end{cases} \tag{6.15}$$

where:

$v_{cs}(t)$ - instantaneous output voltage of the current sensor

K_{cs} - gain of the current sensor, given by (6.16) in terms of the current sensor resistors R_{2cs}, R_{3cs} and the shunt resistor R_s.

ω_{cs} - cutoff angular frequency of the current sensor, given by (6.17) in terms of the current sensor resistor R_{1cs} and capacitor C_{cs}.

$v_{PI}(t)$ - instantaneous output voltage of the PI controller.

K_P - proportional gain of the PI controller, given by (6.18) in terms of the PI controller resistors R_1 and R_2.

T_i - integration time of the PI controller, given by (6.19) in terms of the PI controller resistor R_2 and capacitor C_1.

V_{REF} - reference voltage, given by (6.20) in terms of the current sensor gain K_{cs} and the desired output current I_o.

V_{PWM} - peak-to-peak voltage of the sawtooth wave of the PWM modulator, which is 3V for the TL494 IC.

$$K_{cs} = \left(1 + \frac{R_{3cs}}{R_{2cs}}\right)R_s \quad [V/A] \tag{6.16}$$

$$\omega_{cs} = \frac{1}{R_{1cs}C_{cs}} \quad [rad/s] \tag{6.17}$$

$$K_P = \frac{R_2}{R_1} \quad [V/V] \tag{6.18}$$

$$T_i = R_2 C_1 \quad [s] \tag{6.19}$$

$$V_{REF} = K_{cs} I_o \quad [V] \tag{6.20}$$

In order to obtain the behavior of the converter main variables, it is necessary to solve numerically the equations addressed above. Since the differential equations that describe the circuit were already obtained, the composite midpoint rule (LEVY, 2010) can be used to calculate the main variables, similarly to the procedure outlined in Section 4.1. A MATLAB pseudo-code for calculating the behavior of the main variables of the IDBB converter is presented in Figure 104. It is important to note that this code is a part of a script that besides the calculation of the variables, also extracts some features from them, such as the input current harmonics and the output current ripple. The aforementioned program is presented in Appendix C.3.

- Phase and gain margins

In order to obtain the phase and gain margins, one must obtain the open-loop transfer function $OL(s)$ by means of the analysis of the system's block diagram, which is depicted in Figure 105.

As shown in (WU & CHEN, 1999), the output-to-control transfer function (*i.e.,* G_p) of an integrated converter depends only on the output stage. Therefore, the transfer function that describes the small-signal behavior of the IDBB converter, given by (6.21), can be obtained by using the procedure outlined in (ALONSO et al., 2013).

$$G_p(s) = \frac{i_o(s)}{d(s)} = K_{dc} \frac{1 + s/\omega_z}{1 + s/\omega_p}. \tag{6.21}$$

The dc gain of the transfer function K_{dc}, the zero defined by ω_z and the pole characterized by ω_p are defined in (6.22),(6.23) and (6.24), respectively.

$$K_{tf} = \frac{J_{Dd}}{1 - G_{Do} r_d} \tag{6.22}$$

$$\omega_z = \frac{1}{r_c C_o} \tag{6.23}$$

$$\omega_p = \frac{1 - G_{Do} r_d}{\left(r_d + r_c - G_{Do} r_d r_c\right) C_o} \tag{6.24}$$

where:

```
function [io, ig, d, vb] = IDBBEval(CB, Co, D0, VB, Kcs, wcs, VPWM, KP, Ti,
L1, L2, fs, fL, VG, rd, Vt, effPFC, effPC)

% Auxiliary parameters
ts = 1/(fL * 2000);
tf = 30/fL;
wL = 2 * π * fL;
T = 0 : ts : tf;
ig = zeros(size(T));
vb = zeros(size(T));
vo = zeros(size(T));
io = zeros(size(T));
d = zeros(size(T));
vcs = zeros(size(T));
vpi = zeros(size(T));
N = length(T) − 1;
% Initial Conditions
vb(1) = VB;
vo(1) = Vt;
vcs(1) = 0;
vpi(1) = D0 * VPWM;
d(1) = D0;

% Solution of the circuit variables
for k = 1 : N
    t = T(k);
    vg = sqrt(2) * VG * sin(wL * t);
    ig(k) = d(k)^2 * vg/(2 * fs * L1);
    vb(k + 1) = vb(k) + ts * (d(k)^2/(2 * CB * fs) * (effPFC * vg * vg/(L1 * vb(k)) −
(vb(k)/L2)));
    vo(k+1) = vo(k)+ts*(1/Co)*(effPC*vb(k+1)^2*d(k)^2/(2*fs*vo(k)*L2)−
((vo(k) − Vt)/rd));
    io(k) = (vo(k) − Vt)/rd;
    vcs(k + 1) = vcs(k) + ts * (wcs * (Kcs * io(k) − vcs(k)));
    vpi(k + 1) = vpi(k) + ts * (Kp/Ti * (Kcs * Io) − Kp * Kcs * wcs * io(k) + vcs(k) *
(Kp * wcs − Kp/Ti));
    d(k + 1) = vpi(k + 1)/VPWM;
end
```

Figure 104: MATLAB pseudo-code for calculating the main variables of the IDBB converter with a wide-bandwidth controller.

J_{Dd} - partial derivative of the average current of the pc stage diode with respect to the duty cycle, given by (6.25) (ALONSO et al., 2013), in terms of the average values of the duty cycle D_0, the bus voltage V_B, the output voltage V_o, the switching frequency f_s and the pc stage inductance L_2;

G_{Do} - partial derivative of the average current of the PC stage diode with respect

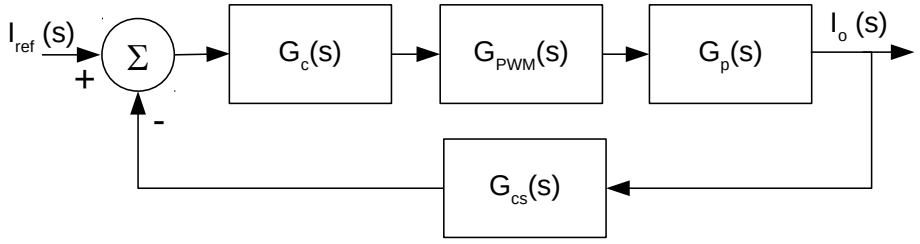


Figure 105: Block diagram of the system.

to the output voltage, given by (6.26) (ALONSO et al., 2013);

r_c - equivalent series resistance of the output capacitor.

$$J_{Dd} = \frac{D_0 V_B^2}{L_2 f_s V_o} \tag{6.25}$$

$$G_{Do} = \frac{-D_0^2 V_B^2}{2 L_2 f_s V_o^2} \tag{6.26}$$

The transfer functions of the PWM modulator $G_{PWM}(s)$, the PI controller $G_c(s)$ and the current sensor $G_{cs}(s)$ are given by (6.27), (6.28) and (6.29), respectively.

$$G_{PWM}(s) = \frac{1}{V_{PWM}} \tag{6.27}$$

$$G_c(s) = K_p \frac{s + T_i}{T_i s} \tag{6.28}$$

$$G_{cs}(s) = K_{cs} \frac{\omega_{cs}}{s + \omega_{cs}} \tag{6.29}$$

Finally, according to Aström and Murray (2010), the phase and gain margins can be calculated by means of (6.30) and (6.31), respectively.

$$Pm = 180^\circ + \angle OL\left(i\omega_{gc}\right), \tag{6.30}$$

$$Gm = \frac{1}{\left|OL\left(i\omega_{pc}\right)\right|}, \tag{6.31}$$

where $\angle OL\left(i\omega_{gc}\right)$ is the phase of the open-loop transfer function, given by (6.32), at the gain crossover frequency ω_{gc}, and $\left|OL\left(i\omega_{pc}\right)\right|$ is the gain of the open-loop transfer

function at the phase crossover frequency ω_{gc}.

$$OL(s) = G_c(s)G_{PWM}(s)G_p(s)G_{cs}(s). \tag{6.32}$$

6.5 DEFINITION OF THE DESIGN PARAMETERS AND THE SEARCH SPACE

In order to solve the optimization problem defined in (6.1), it is necessary to define the parameters of the application and also the search-space. Table 43 summarizes the design parameters. The load, whose equivalent parameters are shown in the table, is composed by four LED modules. Each module consists of the series connection of 12 Phillips LUXEON Rebel LEDs.

Table 43: Parameters for the design of the IDBB converter

Item	Description	Value
V_G	RMS value of the input voltage	220 V ±10%
f_L	frequency of the mains voltage	60 Hz
f_s	switching frequency	50 kHz
D_0	Average value of the duty cycle	75% D_{crit}
I_o	Average output current	500 mA
V_o	Average output voltage	139.9 V
P_o	Average output power	74.3 W
V_t	threshold voltage of the LED string	129.37 V
r_d	dynamic resistance of the LED string	38.46 Ω
r_c	equivalent series resistance of the output capacitor	0.1 Ω
ΔIo_{LF_max}	maximum peak-to-peak ripple of the output current	50 mA (10%)
ΔIo_{HF_max}	maximum high frequency ripple of the output current	25 mA (5%)
V_B	Nominal bus voltage	160 V
V_{B_max}	Maximum bus voltage	200 V
t_{c_max}	Maximum convergence time	0.5 s
η_{PFC}	Efficiency of the PFC stage	0.922
η_{PC}	Efficiency of the PC stage	0.922

By using the values presented in Table 43 in (4.44) it is possible to calculate the critical duty cycle as $D_{crit} = 0.3396$. Therefore, the average value of $d(t)$ was $D_0 = 0.2547$, as defined in Table 43. The value of D_0 was chosen in order to ensure the DCM operation and also to allow for the duty cycle modulation. If one choose a higher value of D_0, the maximum amplitude of the ac part of $d(t)$ would be limited, decreasing the potential of capacitance reduction of the ARC technique. On the other hand, small values of D_0 can lead to high current stresses through the circuit switches. An important observation is that the real value of D_0 will differ a little from the one afore defined, since the duty cycle modulation will also affect the power processed by

the converter. Therefore, the PI controller will adjust the value of D_0 for ensuring null steady-state error of the output current.

Since the value of D_0 is defined, the inductances of the IDBB converter can be calculated by means of (6.9), (6.10) and the parameters of Table 43, yielding $L_1 = 359\,\mu H$ and $L_2 = 206\,\mu H$. The calculation of the output capacitance also does not demand the values of C_B and the parameters of the PI controller. Therefore, by using the data of Table 43 in (6.11), one can obtain $C_o = 7.92\,\mu F$. Owing to the laboratory availability, it was chosen $C_o = 12\,\mu F$.

Table 44 defines the values of the current sensor, yielding a gain $K_{cs} = 2.75\ [V/V]$ and $\omega_{cs} = 30{,}303$ rad/s ($f_{cs} = 4823$ Hz) according to (6.18) and (6.17), respectively. Those values were chosen in order to minimize the losses in the shunt resistor and to mitigate the influence of the switching harmonics upon the control circuit operation.

Table 44: Components of the current sensor

Item	Value
R_s	0.25 Ω
R_{1cs}	3.3 kΩ
R_{2cs}	3.3 kΩ
R_{3cs}	33 kΩ
C_{cs}	10 nF

As presented in the previous section, the optimization variables are the bus capacitance C_B and the components of the PI controller, *i.e.*, the resistors R_1 and R_2 as well as the capacitance C_1. As already commented in the previous chapter, the search space of the optimization problem is the combination of all the possibilities of each optimization variable. Table 45 shows the possible values for each element of vector x.

Table 45: Range of the optimization variables.

Variable	Possible Values
C_B	$\{10, 22, 33, 47, 100, 150, 220, 330\}\ [\mu F]$
C_1	$\{E12 \times 10^{-9}\} + \{E12 \times 10^{-8}\} + \{E12 \times 10^{-7}\}\ [F]$
R_1	$\{E12 \times 10^{-9}\} + \{E12 \times 10^{-8}\} + \{E12 \times 10^{-7}\}\ [F]$
R_2	$\{E12 \times 10^{3}\} + \{E12 \times 10^{4}\} + \{E12 \times 10^{5}\}\ [\Omega]$

where $E12$ represents the set of values standardized in the E12 series of preferred numbers (IEC, 2015). One can note that the optimization variables can assume only commercial values, making the experimental implementation more straightforward, since it will not be necessary to associate components to achieve the desired values.

By using the fundamental principle of counting and considering the ranges defined in Table 45, it is possible to calculate a number of possibilities for the vector x equals to 373,248, which is the size of the search-space. Similarly to Chapter 5, the solution of the optimization problem defined in (6.1) was accomplished by means of the exhaustive-search algorithm. Therefore, for each possible value of x, all the constraints and SOC functions must be calculated, as will be discussed in the next section.

6.6 THE OPTIMIZATION ALGORITHM

The optimization algorithm flowchart is presented in Figure 106. One can note that the procedure is very similar to the one presented in the previous chapter. The main differences are related to the calculation of the variables necessary to evaluate $f(x)$ and the constraints, such as the input and output currents. In this case, such calculations demand the evaluation of the whole system, which includes the solution of the power and the control circuits, as addressed in Section 6.4. Furthermore, instead of storing only the result with the lowest value of $f(x)$ (as in Chapter 5), the algorithm was developed so that all the points in the search space that meet the constraints are retained in a matrix of results R, which has the form shown in (6.33).

$$R = \begin{bmatrix} c_1(x1) & c_2(x1) & \Delta Io_{LF}(x1) & x1_{1\times 4} \\ c_1(x2) & c_2(x2) & \Delta Io_{LF}(x2) & x2_{1\times 4} \\ \vdots & \vdots & \ddots & \vdots \\ c_1(xn) & c_2(xn) & \Delta Io_{LF}(xn) & xn_{1\times 4} \end{bmatrix} \tag{6.33}$$

As can be seen in (6.33), the matrix R stores the SOC functions and also the points of the search space (*i.e.,* $x1, x2, \ldots, xn$) which meet the design requirements. By considering the whole optimization algorithm, the procedure for obtaining the matrix R is the most computational-intensive, since it is necessary to evaluate all the equations addressed in Section 6.4 for each point in the search-space. It is important to highlight that the parameters and also the search-space definition changes the matrix R whereas the weight w_{opt} does not influence it.

As long as the matrix R is obtained, the objective function for each point can be calculated by means of:

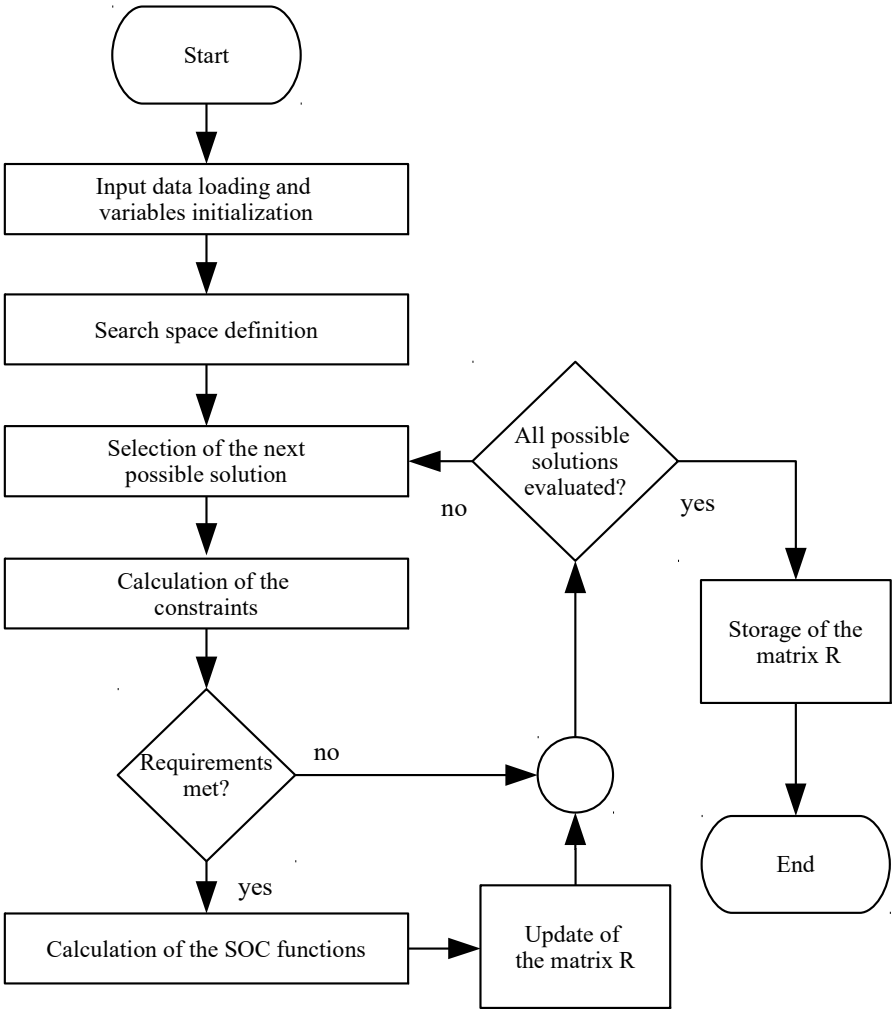


Figure 106: Flowchart of the matrix R calculation.

$$F = \frac{w_{opt}}{\min\left(R_{i1}\right)} \times R_{i1} + \frac{(1 - w_{opt})}{\min\left(R_{i2}\right)} \times R_{i2} = \begin{bmatrix} f(x1) \\ f(x2) \\ \vdots \\ f(xn) \end{bmatrix}, \tag{6.34}$$

where:

i - *i-th* line of the matrix R. $i = 1, 2, \ldots, n$

n - number of possible solutions that meet the constraints of the optimization problem.

Finally, the matrix with the solution of the optimization problem S can be obtained by concatenating the column-vector F with the matrix R, and then by sorting the rows of S according to the value of the objective function, as shown in (6.35).

$$S = sortrows\left([F|R], 1\right) \tag{6.35}$$

where $sortrows\left(arg1, arg2\right)$ is a function that sorts the matrix indicated in $arg1$ according to the value of the column defined in $arg2$. In this study, $arg2$ is equal to one because it represents the column with the values of the objective function for each point (*i.e.*, the column-vector F). Therefore, the solution with the lowest value of the objective function can be found in the first row of matrix S.

One can note that the calculation of S demands as input data the matrix R and the weight w_{opt}. This procedure is straightforward and does not demand a large computational effort. Therefore, if the designer decides to change the design directives, which are represented by the w_{opt}, the new solution of the optimization problem can be found quickly, *i.e.,* without the need of calculating the constraints and the SOC functions again.

6.7 OPTIMIZATION RESULTS

In order to solve the optimization procedure defined in (6.1), a set of MATLAB scripts were produced based on the optimization algorithm outlined in the previous section. Such pieces of software can be found in Appendix C.

By running the aforementioned code with the parameters and the search-space defined in Section 6.5, a matrix R with 162,981 lines is obtained, which means that approximately 44 % of the search-space meet all the constraints compiled in the matrix H.

As already commented, by varying the weight w_{opt} from zero to one, it is possible to obtain different solutions for the optimization problem. Figure 107 shows the behavior of the bus capacitance and the THD according to the weight w_{opt}. The aforementioned graph was plotted by using the values of the first row of the matrix S for each w_{opt} value.

From Figure 107 it is possible to observe that when a designer selects a directive that gives full priority to reduce the THD ($w_{opt} = 0$), this parameter remains at 1% whereas the bus capacitance was 150 μF. On the other hand, when the design is focused only on minimizing the bus capacitance ($w_{opt} = 1$), the total harmonic distortion of the input current was 19.55 % while the bus capacitance can be reduced to 22 μF. The results shown in Figure 107 are in agreement with the discussion presented in Section

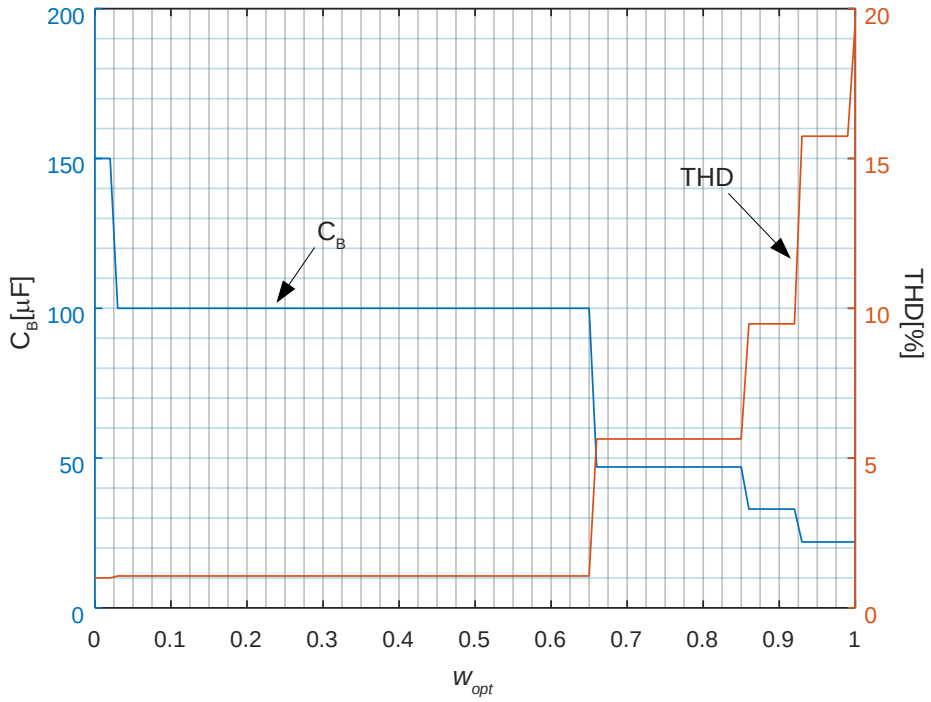


Figure 107: Behavior of the bus capacitance and the THD of the input current according to the weight w_{opt}.

6.2, since as the bus capacitance decreases, the THD of the input current increases. This means that the reduction of the capacitance induces a larger modulation of the duty cycle, which consequently increases the distortion of the input current.

An interesting aspect that could be noted from the results is that there are several combinations of the PI controller that lead to a similar value of the objective function. Figure 108 shows the histogram of the objective function values for $w_{opt} = 1$, which shows that more than eleven thousand points in the search-space produced a similar value of the objective function $f(x)$. All these points have the same bus capacitance and similar values of THD and low-frequency ripple, as indicated in the figure. Therefore, instead of an unique optimal solution, the optimization procedure led to an optimal region, which is characterized by a bus capacitance of 22 μF. The parameters of the PI controller of the solutions that belong to this optimal region are shown in a Figure 109. In order to aid the visualization, the scatter plot of the PI controller parameters was represented in a log-log scale, since the optimal region is approximately 3 % of the search-space[1].

As already commented, the low-frequency behavior of the converter will be similar for all the PI parameters within the optimal region. In order to attest the theoreti-

[1]The optimal region for $w_{opt} = 1$ has 11,783 points whereas the search-space is composed by 373,248 possibilities of x.

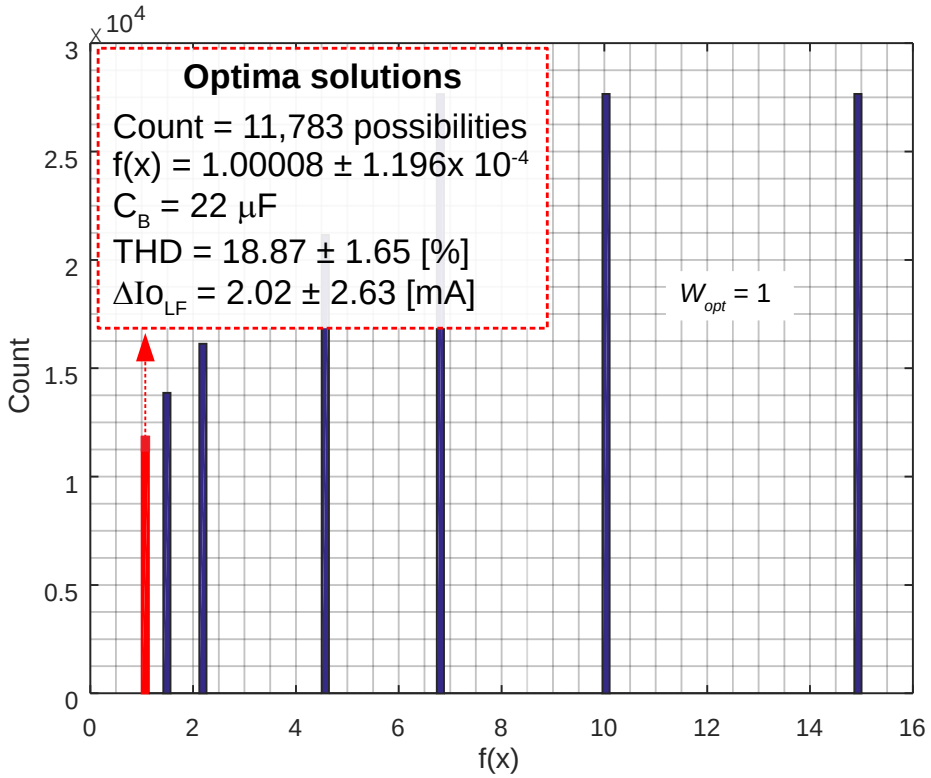


Figure 108: Histogram of the objective function for $w_{opt} = 1$.

cal analysis and the optimization results, the PI parameters of the point highlighted in Figure 109 were chosen, yielding the optimal solution shown in (6.36). Computational simulations and also experimental results will be carried out in the next sections considering this solution.

$$x^*_{w_{opt}=1} = \begin{bmatrix} 22\mu F & 5.6k\Omega & 22k\Omega & 4.7nF \end{bmatrix} \tag{6.36}$$

Figure 110 shows the histogram of the objective function for $w_{opt} = 0$. In this case, the variable of interest is the THD so that the values of the capacitance C_B and the low-frequency ripple do not impact on the result. As can be seen in the graph, there are 22,516 points in the search-space that presented $f(x) = 1$ and the THD = 1 %. This occurred because of the threshold applied to the function $c_2(x)$, which was defined so that the minimum THD was 1 %. One can note in Figure 110 that among the optima solutions, there are cases with $C_B = 150\mu F$, $C_B = 220\mu F$ and $C_B = 330\mu F$. Furthermore, the low-frequency ripple was much higher in the strategy with $w_{opt} = 1$, which was expected since the directive characterized by $w_{opt} = 0$ does not lead to a minimization of C_B neither ΔIo_{LF}.

The scatter plot of the PI controller parameters for $w_{opt} = 0$ is presented in Fig-

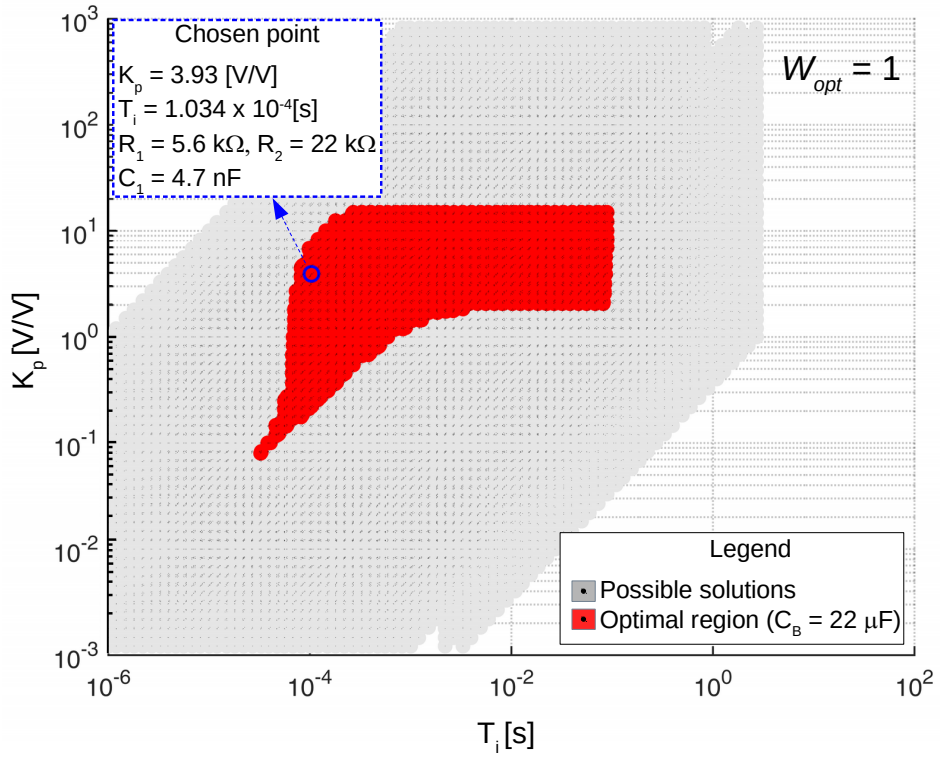


Figure 109: Scatter plot of the PI controller parameters for $w_{opt} = 1$.

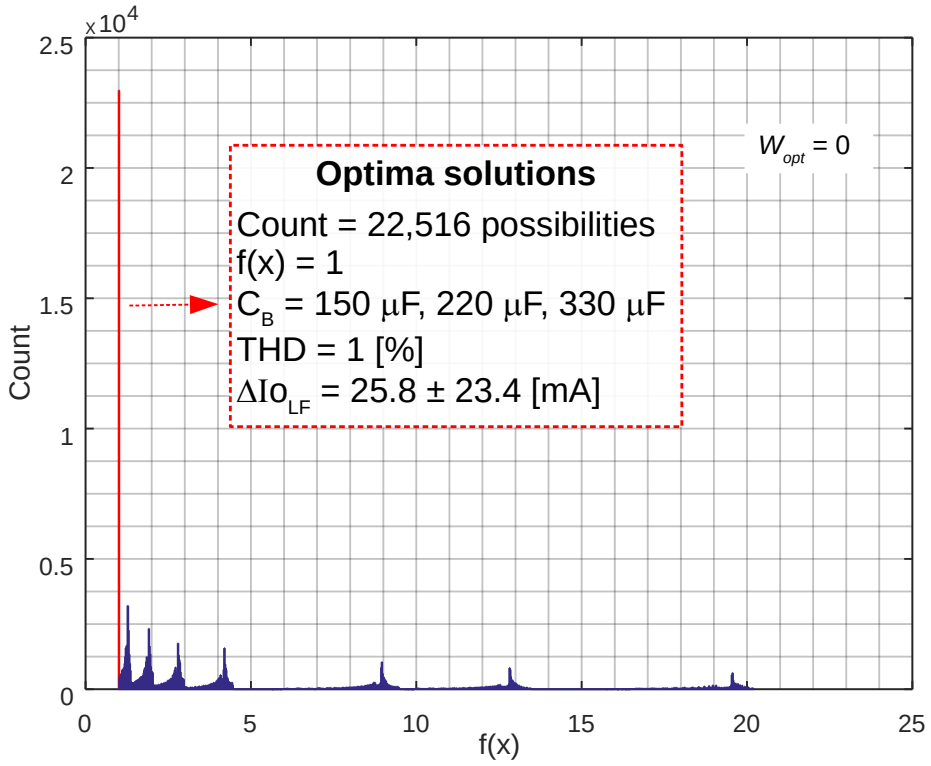


Figure 110: Histogram of the objective function for $w_{opt} = 0$.

ure 111. The figure shows that there are three optima regions in the graph, which depend on the value of the bus capacitance. As can be seen, as the value of C_B in-

creases, the optimum region for the PI parameters also grows. This behavior was explained in Section 6.2: for higher capacitances, the low-frequency ripple is lower, allowing for the use of greater proportional gains and lower integration times, so that the input current distortion is not increased.

By comparing figures 109 and 111, it is possible to observe that the strategy with $w_{opt} = 1$ leads to wider bandwidth PI controllers (*i.e.,* higher K_p and lower T_i), since this design directive pursues the capacitance and ripple reduction. On the other hand, when w_{opt} is set to be zero, the optimization algorithm will seek the points in the search-space that minimize the duty cycle modulation in order to keep the input current waveform with a low distortion. It is important to highlight that the strategy with $w_{opt} = 0$ is similar to the conventional design approach for VMC LED drivers, in which the output current ripple compensation is not considered, as in Alonso et al. (2011a).

The chosen point for $w_{opt} = 0$ yields the following optimal solution:

$$x^*_{w_{opt}=0} = \begin{bmatrix} 150\mu F & 270k\Omega & 2.7k\Omega & 470nF \end{bmatrix} \tag{6.37}$$

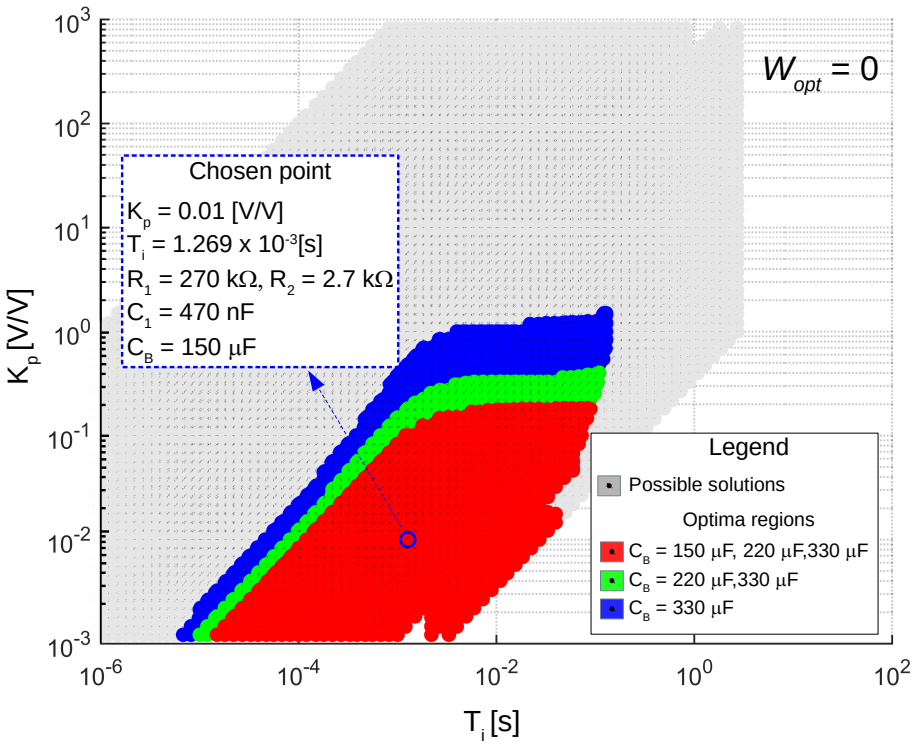


Figure 111: Scatter plot of the PI controller parameters for $w_{opt} = 0$.

By comparing the design results with $w_{opt} = 0$ and $w_{opt} = 1$, one can note that the use of a PI controller sized to compensate the low-frequency current ripple leads to a

capacitance 85 % lower at the cost of a THD increment of 19.56 %.

6.8 SIMULATION RESULTS

In order to verify the optimization results, a PSIM simulation of the IDBB converter with a PI controller was carried out. Table 46 summarizes the main simulation parameters whereas the circuit is shown in Figure 112. As can be seen, a resistor R_{loss} was placed in parallel with the bus capacitor in order to represent the converter losses. Two simulation results will be presented next: the first one is regarding the optimization results considering $w_{opt} = 1$ and the other for $w_{opt} = 0$. One can note from Table 46 that the difference between both simulations are only the optimization variables, *i.e.*, the bus capacitor C_B and the PI controller parameters. Figure 112 also shows that a zener diode was placed in the output of the PI controller in order to limit the duty cycle of the converter. Furthermore, the low-frequency behavior of the input and output currents was obtained by using the same strategy of Chapter 5, *i.e.,* by means of a low-pass filter.

Figures 113 and 114 present the main waveforms obtained from the simulation of

Table 46: Values used in the simulation of the IDBB converter.

General Parameters		
f_s	50 kHz	
L_1	359.2 μH	
L_2	206.1 μH	
C_o	12 μF	
r_d	38.46 Ω	
V_t	129.37 V	
I_o	500 mA (nominal)	
R_{loss}	1961 Ω	
Simulation step	0.1 μs	
Current Sensor		
R_s	0.25 Ω	
R_{1cs}	3.3 kΩ	
R_{2cs}	3.3 kΩ	
R_{3cs}	33 kΩ	
C_{cs}	10 nF	
Optimization Variables		
	$w_{opt} = 1$	$w_{opt} = 0$
C_B	22 μF	150 μF
R_1	5.6 kΩ	270 kΩ
R_2	22 kΩ	2.7 kΩ
C_1	4.7 nF	470 nF

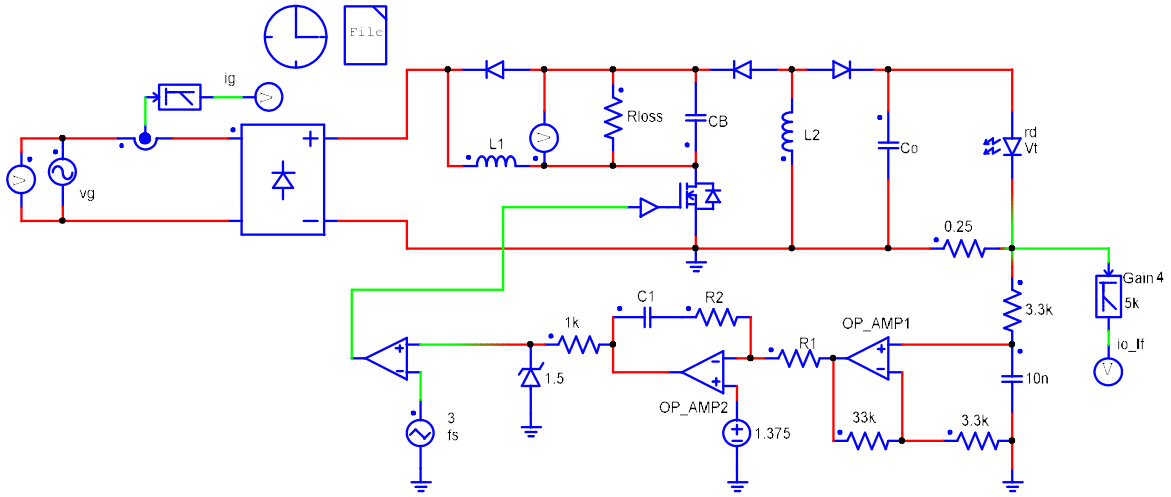


Figure 112: Circuit used in the simulation of the IDBB converter with an analog PI controller

the converter compared with the theoretical model for $w_{opt} = 1$. From Figure 113 it is possible to see that the simulation results regarding the bus voltage and the input current are similar to the waveforms predicted by the equations presented in section 6.4. The small differences between the theoretical and simulated results are related to the losses modeling. In the theoretical analysis, the losses are distributed between the PFC and the PC stages equally. On the other hand, the simulation was carried out considering that the losses are concentrated and represented by a single element. Figure 114 shows that the predicted low-frequency behavior of the output current is also similar to the results gathered in the circuit simulation.

Table 47 presents a comparison between some values obtained from the simulation and the theoretical values. One can note that the mathematical model yielded a good prediction of the low-frequency behavior of the converter.

Table 47: Simulation results of the IDBB converter for $w_{opt} = 1$.

Item	Description	PSIM Result	Mathematical Model
I_o	Average output current	500 mA	500 mA
ΔIo_{LF}	Low-frequency output current ripple	3.2 mA	2.8 mA
ΔIo_{HF}	High-frequency output current ripple	18.5 mA	25 mA
V_B	Average bus voltage	152.14 V	158.68 V
THD	Total Harmonic Distortion	22.6 %	19.56%
PF	Power Factor	0.956	0.9635

The main waveforms for the case with $w_{opt} = 0$ are presented in Figures 115 and 116. Similarly to the previous design directive, the shape of all variables obtained from the simulation is quite similar to the ones predicted by the equations presented in

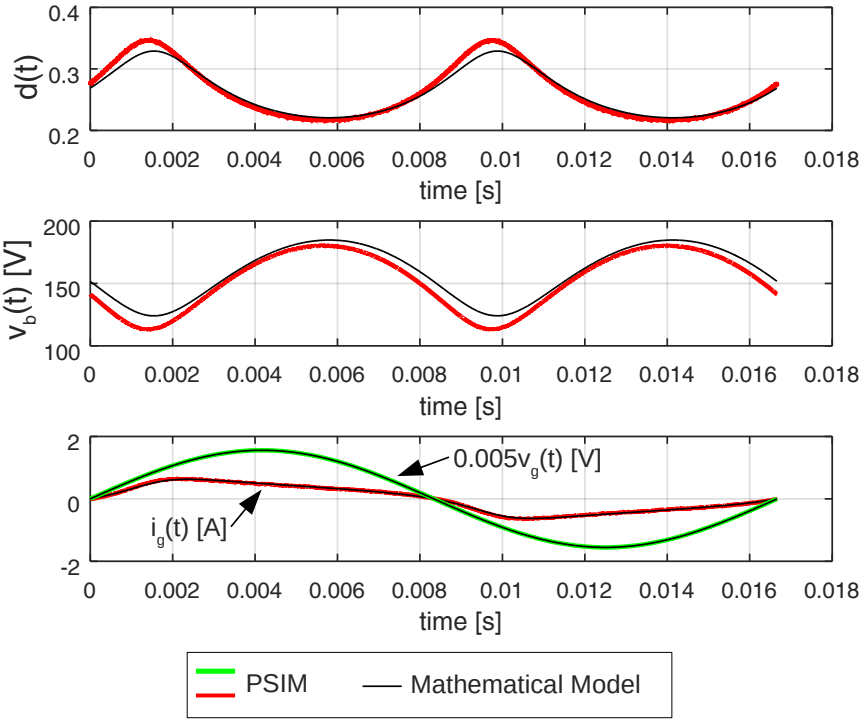


Figure 113: Comparison between the simulated waveforms with the theoretical model of the IDBB converter for $w_{opt} = 1$.

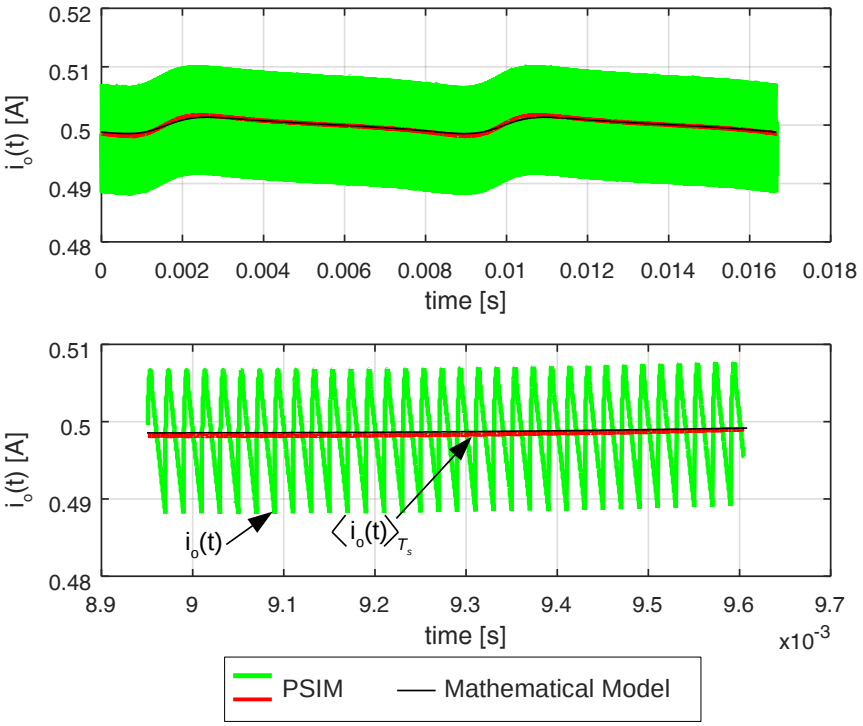


Figure 114: Comparison between the simulated waveforms of the IDBB converter output current with the theoretical model for $w_{opt} = 1$. (a) Low-frequency behavior; (b) High-frequency waveforms.

Section 6.4. The larger difference between the mathematical model and the simulation results occurred in the bus voltage waveform owing to the losses modeling. Since all the converter losses were represented by a resistor in parallel with the bus capacitor, the voltage across this element was lower than the one predicted by the mathematical model.

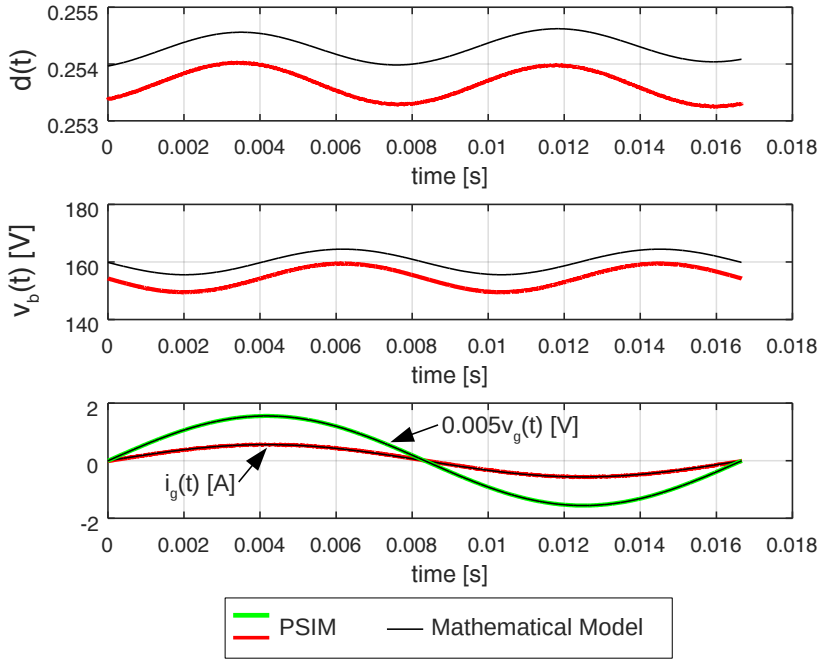


Figure 115: Comparison between the simulated waveforms with the theoretical model of the IDBB converter for $w_{opt} = 0$.

Finally, Table 48 shows a comparison between the values of some variables considering the mathematical model and PSIM simulation. The results attested that the theoretical analysis provides a good description of the low-frequency behavior of the converter.

Table 48: Simulation results of the IDBB converter for $w_{opt} = 0$.

Item	Description	PSIM Result	Mathematical Model
I_o	Average output current	501 mA	499 mA
ΔIo_{LF}	Low-frequency output current ripple	53.6 mA	46.2 mA
ΔIo_{HF}	High-frequency output current ripple	19.5 mA	25 mA
V_B	Average bus voltage	154.56 V	160.05 V
THD	Total Harmonic Distortion	1.34 %	less than 1%
PF	Power Factor	0.999	1

6.9 EXPERIMENTAL RESULTS

In order to validate the theoretical analysis of the proposed design technique, a laboratory prototype was built. The prototype's components values are given in Table 49 and a photograph of it is shown in Figure 117, which was taken for the case in which $C_B = 22\mu$F. The capacitance for the design with $w_{opt} = 0$ was obtained by using a parallel connection of two capacitors: 100 μF/200V and 47 μF/200V.

Figure 118 presents some experimental results of the IDBB converter designed for $w_{opt} = 1$ (Figure 118a) compared with the design with $w_{opt} = 0$ (Figure 118b). By means of the depicted dashed lines, which represent the theoretical waveforms, it is possible to observe that the experimental results are in agreement with the theoretical analysis.

The low-frequency output current ripple gathered from the experiments for the design with $w_{opt} = 1$ was 4 mA and 52 mA for the case with $w_{opt} = 0$. Those results are similar to the theoretical prediction, which showed that these quantities would assume the values of 2.8 mA and 46.2 mA, respectively. On the other hand, the measured THD of the input current was 18.2 % for $w_{opt} = 1$ and 2.64% for $w_{opt} = 0$, which are also similar to the predicted values, *i.e.,* 19.56 % for $w_{opt} = 1$ and less than 1% for

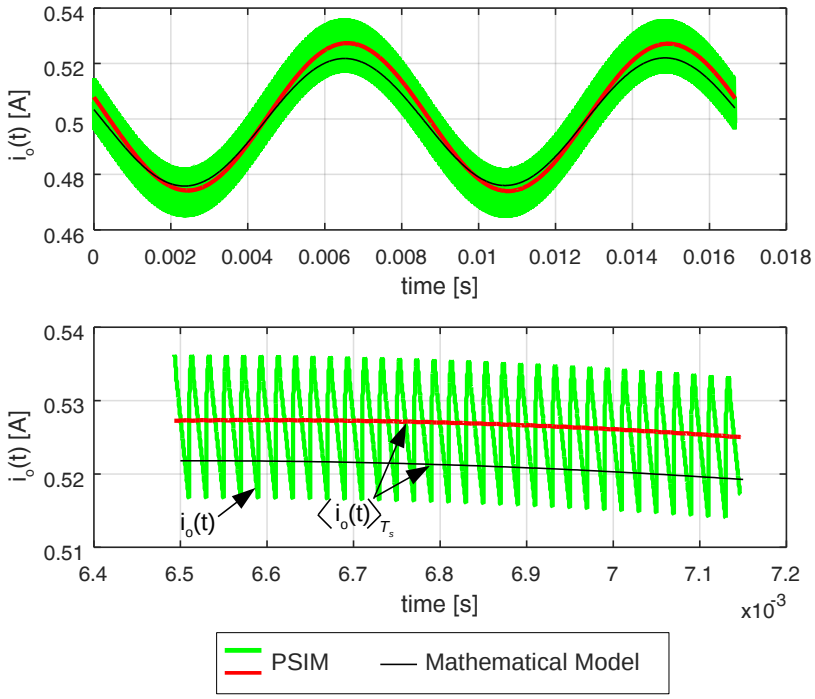


Figure 116: Comparison between the simulated waveforms of the IDBB converter output current with the theoretical model for $w_{opt} = 0$. (a) Low-frequency behavior; (b) High-frequency waveforms

Table 49: Prototype parameters

Item	Description	Value
EMI	EMI Filter	CM:5.2 mH / DM: 3 mH /2 x 220nF
DB	diode bridge	GBU4J
L_1	PFC inductor	360 μH (E30 core)
L_2	PC inductor	199 μH (E30 core)
C_B	bus capacitor for $w_{opt} = 1$	22 μF/200 V (electrolytic)
C_B	bus capacitor for $w_{opt} = 0$	147 μF/200 V (electrolytic)
C_o	output capacitor	12 μF/ 450 V (polypropylene film)
M	main switch	SPP08N80C3
D_{bb1},D_{bb2},D_{i1},D_{i2}	diodes of the power circuit	MUR460
$U1$	operational Amplifier	MCP602
$U2$	PWM modulator	TL494
-	control circuit resistors	0805 thick film resistors
-	control circuit capacitors	0805 ceramic capacitors

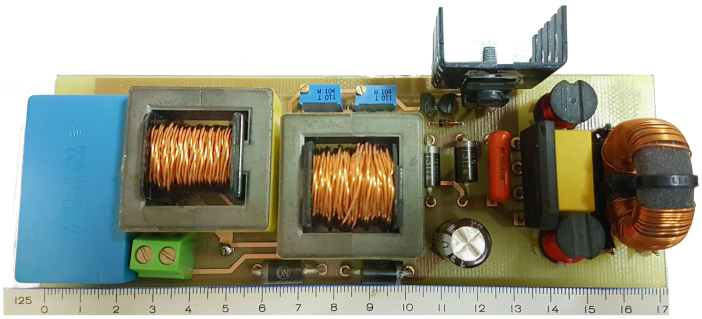


Figure 117: Top-view of the prototype with $C_B = 22$ μF. Ruler in centimeters.

$w_{opt} = 0$. Figure 118c presents some waveforms of the circuit operating in open-loop with a bus capacitor of 22 μF[2], showing that if the wide-bandwidth PI controller is not used, the ripple requirements are not met.

The results presented in Figure 118 show that the output current ripple of the circuit was lower for the design with $w_{opt} = 1$ at the cost of an increase of the input current distortion. Nevertheless, this distortion was predicted during the design procedure so that the harmonic content of the input current remains in compliance with the IEC 61000-3-2:2014 standard, as shown in Figure 119.

The behavior of the output current ripple and the THD owing to variations in the output power (dimming) is presented in Figure 120. The results showed that the design with $w_{opt} = 1$ ensured a small current ripple for all the analyzed levels. Nevertheless, the THD increased as the output current rose, indicating a larger modulation of the duty cycle for higher current levels. On the other hand, Figure 120b shows that for

[2]the same power circuit of the design with $w_{opt} = 1$

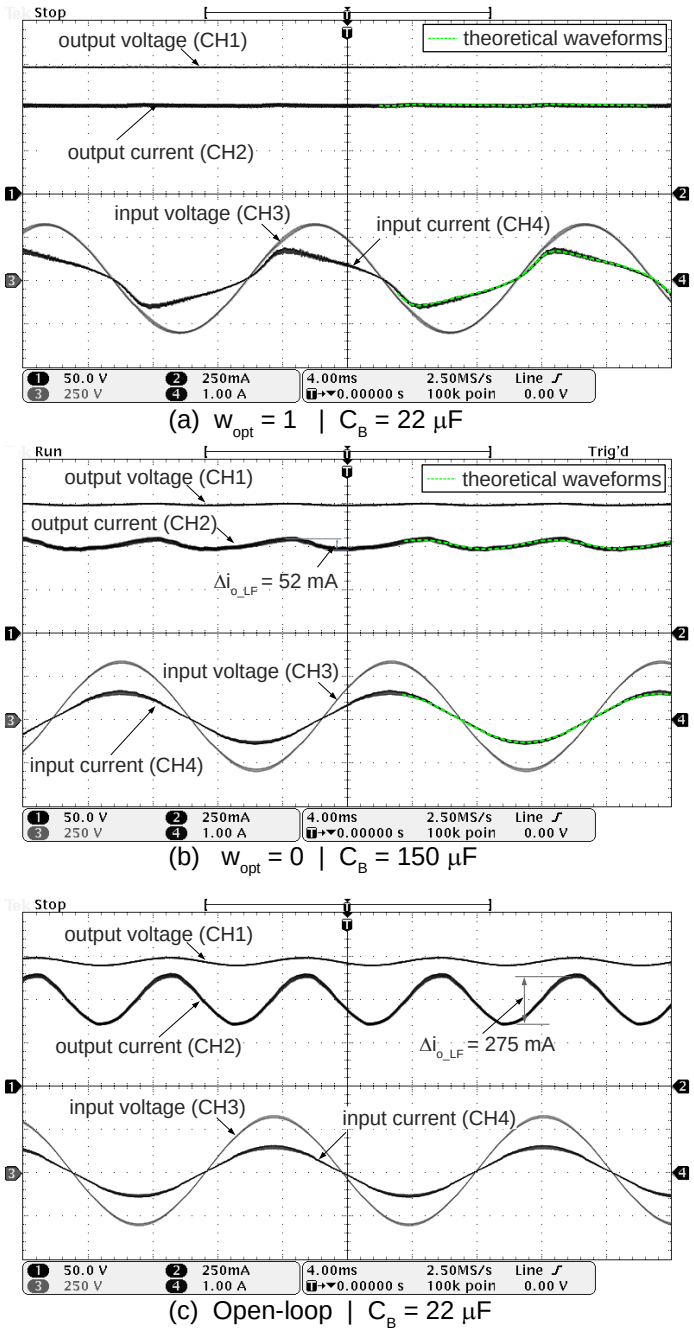


Figure 118: Experimental waveforms obtained for the design with $w_{opt} = 1$(a) and $w_{opt} = 0$ (b). (c) Results obtained for the circuit operating in open-loop with $C_B = 22$ μF. Output voltage (CH1 - 50V/div), output current(CH2 - 250 mA/div), input voltage (CH3 - 250V/div) and input current (1A/div). Horiz. scale: 4 ms/div.

$w_{opt} = 0$, the THD remains small for all the cases while the current ripple increases for higher output power conditions, which means that the low-frequency ripple is not compensated by the PI controller. All the results of Figure 120 were obtained for $V_G = 220$ V.

The output of the PI controller at steady-state operation can be seen in Figure 121.

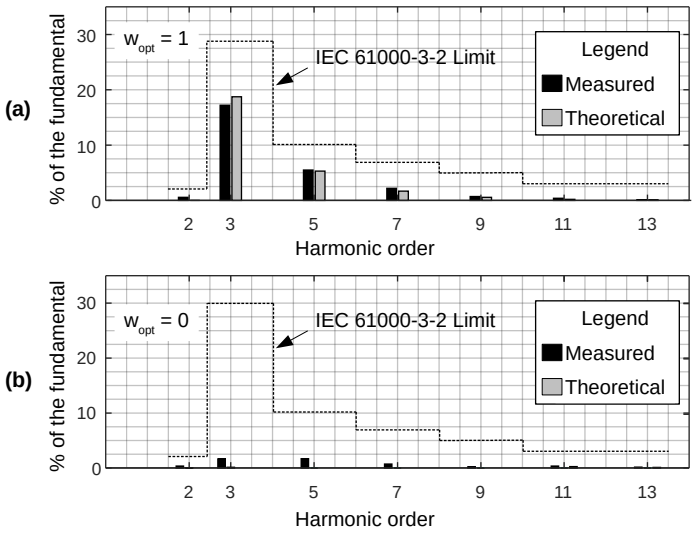


Figure 119: Harmonic content of the input current for $w_{opt} = 1$(a) and $w_{opt} = 0$(b).

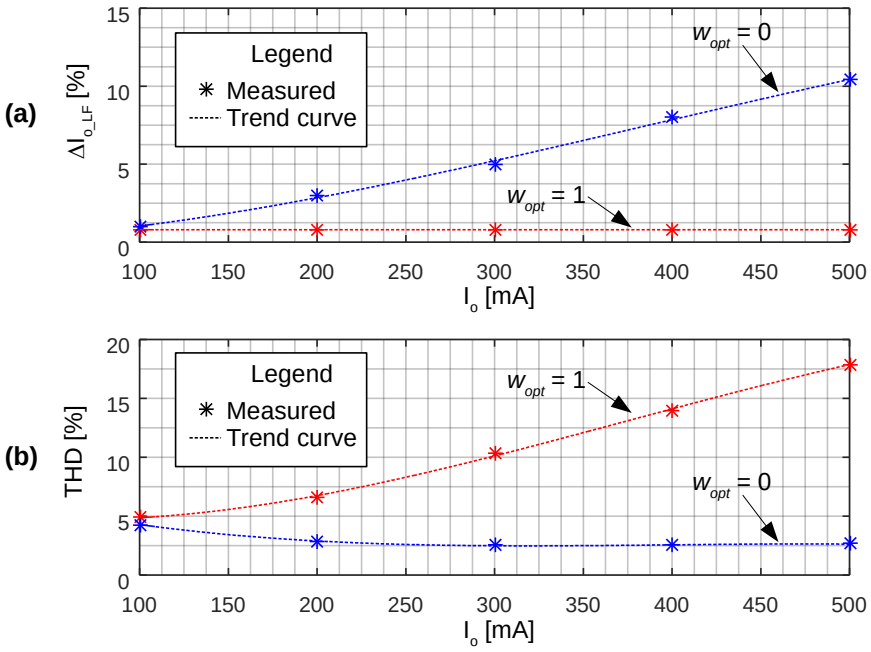


Figure 120: Behavior of the output current ripple (a) and the THD of the input current (b) for variations in the output power.

One can see that, as predicted in theoretical analysis, the PI controller of the design with $w_{opt} = 1$ modulates the duty cycle of the converter in order to compensate the output current ripple. On the other hand, for the case with $w_{opt} = 0$, the input voltage of the PWM modulator is almost constant, leading to the desired condition, *i.e.*, a low distortion of converter's input current.

Figure 122 presents the behavior of the converter's efficiency according to variations in the input voltage (Figure 122a) and also in the output current (Figure 122b). The

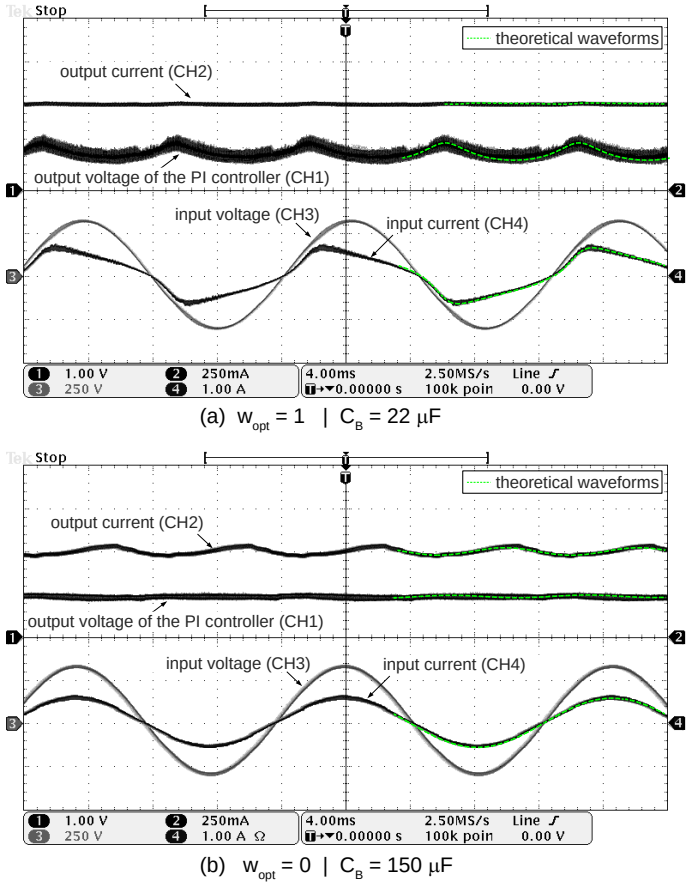


Figure 121: Behavior of the duty cycle in steady-state for $w_{opt} = 1$(a) and $w_{opt} = 0$(b). Output voltage of the PI controller(CH1 - 1V/div), output current(CH2 - 250 mA/div), input voltage (CH3 - 250V/div) and input current (1A/div). Horiz. scale: 4 ms/div.

results show that the efficiency of the circuit with $w_{opt} = 0$ was slightly higher than the design with $w_{opt} = 1$, however, the difference was lower than 0.5% for all the conditions, so that it could be concluded that the influence of the duty cycle modulation upon this parameter is negligible. Figure 122 also showed that the efficiency of the circuit increases as the input voltage grows and the output current decreases. This characteristic is expected for the IDBB converter, which is a topology with a high current stress on the semiconductors due to the integration of the PFC and PC stages.

Figure 123 shows the bus voltage for two output power conditions: full load and 20% of the full load. One can note that both conditions were compiled in a single picture by using the memory function of the oscilloscope. As expected, the average value of the bus voltage remained nearly constant for both load conditions and was also similar for both design cases. The experiments showed that the bus voltage ripple was always higher for the design with $w_{opt} = 1$, which occurs because the capacitance in this case is much lower. However, owing to the duty cycle modulation (see Figure 121),

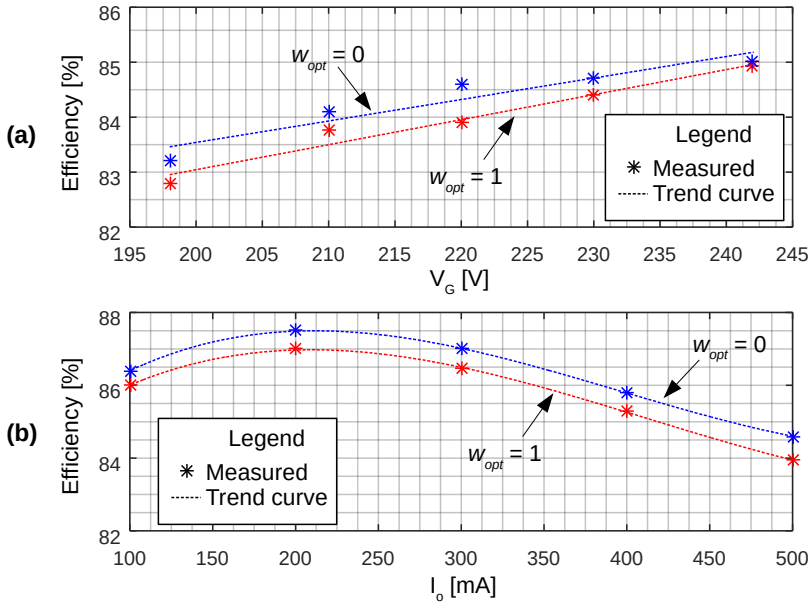


Figure 122: Efficiency of the converter according to variations in the input voltage (a) and the output current (b). Data taken with $V_G = 220$ V.

the output current ripple of the case with a wider-bandwidth controller was always lower than the design with $w_{opt} = 0$.

The waveforms obtained from the MOSFET M can be observed in Figure 124. The results attest the full DCM operation because the current through M is the sum of the currents through both inductors during the on-time. Therefore, it ramps up from zero only if both stages are in DCM. Those waveforms were taken from the prototype designed with $w_{opt} = 1$ at the peak of the rectified line voltage for nominal conditions.

Finally, Figure 125 shows the dynamic performance of the converter during steps of the input voltage and the load for both design conditions. One can note from Figure 125a that the PI controller with a wider-bandwidth was able to stabilize the output current in less than a quarter line voltage cycle after a short-circuit in 1 LED module (25% of the load). On the other hand, the PI controller for the case with $w_{opt} = 0$ spent approximately 5 cycles to accomplish the same task. Furthermore, the superior dynamic performance of the design with $w_{opt} = 1$ can be verified by analyzing the parts (c) and (d) of Figure 125, since it was able to reject perturbations in the line voltage so that the output current did not present any overshoot. Figure 125d shows that controller designed with $w_{opt} = 0$ was also able to stabilize the output current after steps in the converter's input voltage, however, the dynamic response was slower compared to the wider-bandwidth PI controller.

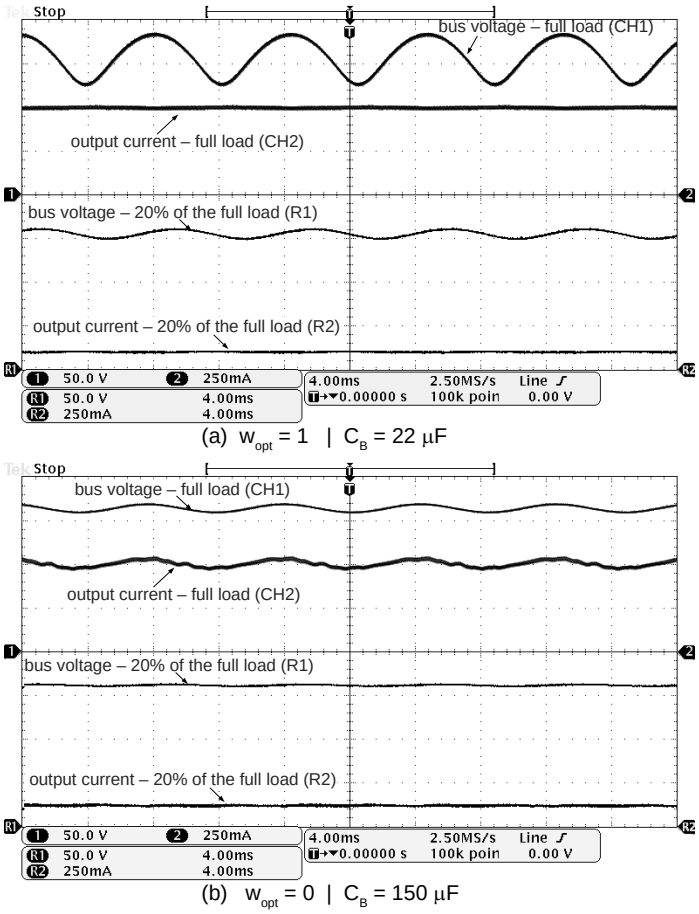


Figure 123: Behavior of the bus voltage according to load variations for an input voltage of 220 V. Bus voltage for full load (CH1 - 50 V/div); Bus voltage for 20% of the full load (R1 - 50 V/ div); Output current for full load (CH2 - 250 mA/div); Output current for 20% of the full load (R2 - 250 mA/div). Time scale: 4 ms.

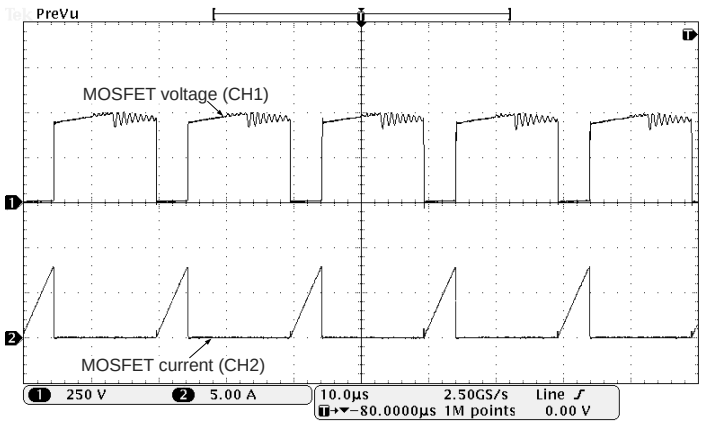


Figure 124: MOSFET voltage (CH1 - 250 V/div) and current (CH2 - 5A/div). Horiz. scale: 10 μs/div.

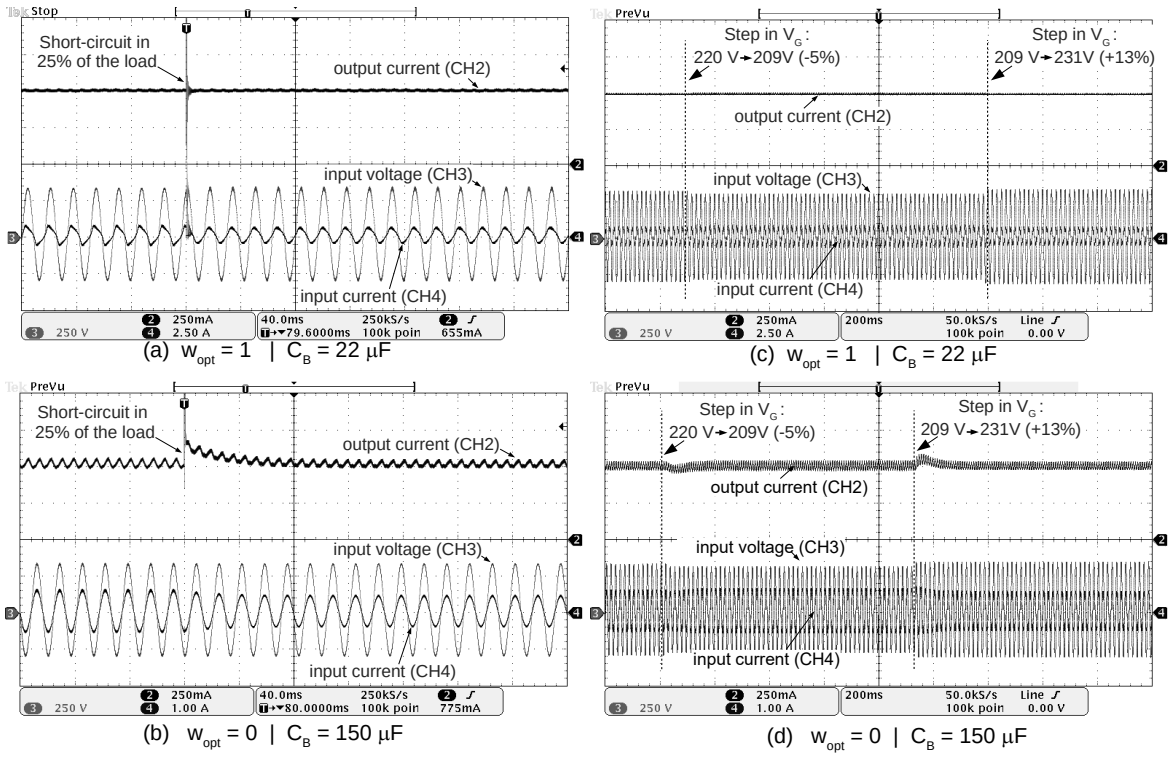


Figure 125: Dynamic behavior of the converter during steps of the input voltage (a) and the load(b). Output voltage (CH1: 50V/div), output current(CH2: 100 mA/div in (a) - 200 mA/div in(b)), input voltage (CH3: 250V/div) and input current (1A/div). Horiz. scale: 200 ms/div in (a) and 50 ms/div in (b).

6.10 SUMMARY

This chapter presented an alternative implementation of the ARC technique by means of PI controller with a wide-bandwidth. First, a qualitative analysis was presented showing the main aspects of the circuit operation when the controller of the converter is sized to compensate the output current ripple.

The design procedure was modeled as an optimization problem, so that the requirements and design objectives could be characterized in a straightforward and quantitative way. The proposed objective function evaluates simultaneously the capacitance, output current ripple and the THD. Those terms were weighted by a factor called w_{opt}, which can vary from zero (priority for minimizing the THD of the circuit) to one (priority for minimizing the capacitance).

The design procedure was studied in an IDBB converter, whose main equations were outlined along the chapter, including the expressions for evaluating the behavior of the control circuit under the large signal modulation of the duty cycle.

In order to validate experimentally the proposed design procedure, two cases were studied. The first one aimed to the capacitance reduction ($w_{opt} = 1$) whereas the other had a design directive that pursued a low THD of the input current, which is similar to the conventional design strategy for off-line VMC LED drivers, *i.e.*, the low-frequency output current ripple compensation is not considered. The design results showed that a capacitance reduction of 85 % can be achieved by using a PI controller sized to compensate the low-frequency current ripple.

The experimental results were in agreement with the theoretical analysis, showing the validity of the proposed design technique. Furthermore, the experiments showed that both designs met the requirements stated in the optimization problem.

7 CONCLUSIONS AND PROPOSALS FOR FUTURE WORKS

This work proposed an approach for designing LED drivers with reduced storage capacitance by means of the modulation of the converter's duty cycle. Nevertheless, before discussing the technique, some aspects of LED lighting technology were addressed.

In Chapter 1, a review regarding the characteristics of the LED lighting system was presented, highlighting the desired features for the driver: one of the most important components in the aforementioned system. It was shown that a good design approach for this electronic circuit must be guided by performance parameters that rule the behavior of the converter regarding its input and output variables. When concerning the input variables, the designer must be aware of the power factor of the circuit and the harmonic content of the input current, so that the compliance with the standards can be met. On the other hand, the main design requirements regarding the output variables are related to the average value of the load voltage and current as well as the limitation of the low-frequency ripple. The latter could be a problem since it normally demands the use of bulky storage elements and the conventional solutions employ electrolytic capacitors, which can reduce the reliability of the system, or film capacitors, which have a poor energy density. Other requirements for designing the LED driver are related to the economic attractiveness of the whole SSL system, which normally leads to a choice of topologies with a low component count, allowing for a low cost implementation.

In light of the above mentioned characteristics, some techniques for power factor correction and capacitance reduction in off-line drivers were revisited in chapters 2 and 3, respectively, so that a novel solution that complies with the requirements of the application could be developed.

Chapter 4 outlined the use of the low-frequency duty cycle modulation for capacitance reduction. The solution, called Active Ripple Compensation (ARC), was devised to be applied in off-line voltage-mode controlled LED drivers and allows for a significant reduction of the required filtering capacitances. The preliminary studies included

the investigation of the proposed technique in a classical flyback-based driver and also in an integrated topology. The results showed in Chapter 4 attested the potential of the ARC technique for reducing the capacitance in off-line LED drivers, since it allowed for a capacitance reduction of 24.2 % in the flyback converter and 46.3% in the IDBB topology at the cost of an increase in the THD of 25.54% and 14%, respectively. Furthermore, Chapter 4 showed that the ARC technique is easy to implement, since it requires only an additional branch in the conventional control structure of the converter.

In Chapter 5, the study of the ARC technique was extended to other topologies and design conditions. A generalized investigation was accomplished by modeling the design procedure as an optimization problem, so that the evaluation of all the cases could be performed in a systematic way. The results confirmed the preliminary studies, showing that the ARC can lead to large reductions of the converter capacitance in several topologies and also for various application characteristics. Furthermore, it was shown that the use of the ARC in two-stage topologies leads to a better performance when compared to single-stage converters.

Finally, Chapter 6 discussed an alternative implementation of the ARC technique by means of a wide-bandwidth controller. In this approach, both the output average current regulation and also the ripple compensation are performed by a single compensator. As in Chapter 5, the design procedure was modeled as an optimization problem, so that the capacitance sized to filter the low-frequency ripple and also the controller parameters could be designed simultaneously. Furthermore, the objective function was devised so that the designer could choose which strategy must be used by the search algorithm: capacitance reduction or THD minimization. The proposed design technique was employed to size an IDBB converter and the results showed that a capacitance reduction of 85 % can be achieved by compensating the low-frequency ripple.

It is important to highlight that the approaches presented in Chapter 4 and Chapter 6 are both based on the same principle: the controlled modulation of the converter's duty cycle. The strategy presented in Chapter 4 has the advantage of allowing for a fine control of the duty cycle harmonic components, and also an independent design of the converter elements and the controller. On the other hand, the implementation of the ARC technique by means of a single controller is easier and has a low-component count, although has a more complex design procedure, since the equations of the power and control circuit must be evaluated simultaneously.

Some proposals for future works are presented in the following:

- Study of the proposed technique in topologies with higher efficiencies, such as resonant converters;
- Evaluation of the controlled frequency modulation instead of the duty cycle modulation for reducing the filtering capacitances;
- Study of the duty cycle modulation aiming to the reduction of the crossover distortion in boost-based and buck-based VMC PFC pre-regulators;
- Investigation of the ARC technique in converters with primary-side regulation;
- The design strategy based on the optimization approach can be expanded in order to evaluate other converter parameters, such as the efficiency;
- Development of high-power-density converters based on the design via the optimization approach;
- Other optimization algorithms can be explored to reduce the computational time or to enlarge the search-space;
- Investigation of analytical solutions for the optimization problem based on the input parameters of the applications, so that the numerical optimization procedure could be avoided in some situations.

The papers published or accepted for publication as a direct or indirect result of this work are listed in the following.

- Papers published in journals

1. SOARES, GUILHERME M.; ALMEIDA, PEDRO S.; BRAGA, HENRIQUE A. C. ; ALONSO, J. M., Capacitance Minimization in Integrated Off-line LED Drivers Using an Active-Ripple-Compensation Technique. IEEE Transactions on Power Electronics, v. 34, p. 1-1, 2017.
2. SOARES, GUILHERME M.; ALMEIDA, PEDRO S. ; BRAGA, HENRIQUE A. C., A Fully Digital Smart LED Luminaire with Remote Management and Embedded Power Quality Analysis System. JOURNAL OF CONTROL, AUTOMATION AND ELECTRICAL SYSTEMS, v. 1, p. 1, 2017.

- Papers published in conferences

1. SOARES, G. M.; ALMEIDA, PEDRO S. ; ALONSO, J. MARCOS ; BRAGA, HENRIQUE A. C. DCM Integrated Double Buck-Boost led driver with reduced storage capacitance. In: 2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC), 2015, Fortaleza. 2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC), 2015. p. 1.

- Papers accepted for publication

1. SOARES, G. M.; BRAGA, HENRIQUE A. C. ; ALONSO, J. M, Investigation of the Active Ripple Compensation Technique to Reduce Bulk Capacitance in Off-line Flyback-Based LED Drivers. IEEE Transactions on Power Electronics, 2017.

2. NOGUEIRA, F. ; SOARES, G. M. ; BRAGA, H. A. C. ; FERRAZ, R. M. ; RESENDE, L. H. G. ; SILVA, E. . Modelagem e Controle de um Driver de LEDs de Baixa Frequência Baseado no Pré-Regulador Boost. REVISTA ELETRÔNICA DE POTÊNCIA, 2017.

REFERENCES

ABNT. *NBR 16026 – Dispositivo de controle eletrônico c.c. ou c.a. para módulos de LED – Requisitos de desempenho*. 2012.

ALBERTSEN, A. *Electrolytic capacitor lifetime estimation*. 2010. Available from Internet: <http://jianghai-america.com/uploads/technology/JIANGHAI_Elcap_Lifetime_-_Estimation_AAL.pdf>.

ALMEIDA, P. S. *Síntese de Conversores Ressonantes com Alto Fator de Potência e Alta Eficiência para o Acionamento de Diodos Emissores de Luz*. Ph.D. Thesis (Ph.D.) — Universidade Federal de Juiz de Fora, 2014.

ALMEIDA, P. S. et al. Static and dynamic photoelectrothermal modeling of led lamps including low-frequency current ripple effects. *IEEE Transactions on Power Electronics*, IEEE, v. 30, n. 7, p. 3841–3851, 2015.

ALMEIDA, P. S. et al. Offline soft-switched led driver based on an integrated bridgeless boost–asymmetrical half-bridge converter. *Industry Applications, IEEE Transactions on*, IEEE, v. 51, n. 1, p. 761–769, 2015.

ALMEIDA, P. S. et al. Application of series resonant converters to reduce ripple transmission to led arrays in offline drivers. *Electronics Letters*, IET, v. 49, n. 6, p. 414–415, 2013.

ALMEIDA, P. S. et al. An experimental study on the photometrical impacts of several current waveforms on power white leds. In: IEEE. *XI Brazilian Power Electronics Conference*. 2011. p. 728–733.

ALMEIDA, P. S.; SOARES, G. M.; BRAGA, H. A. Storage capacitance minimization in led drivers based on photometrical constraints and converter integration. *Eletrônica de Potência*, v. 18, n. 2, p. 962–971, 2013.

ALONSO, J. et al. Investigation of a novel high-power-factor electronic ballast based on the input current shaper. In: IEEE. *Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE*. 1999. v. 2, p. 1109–1114.

ALONSO, J. et al. Analysis and design of the integrated double buck-boost converter operating in full dcm for led lighting applications. In: IEEE. *IECON 2011-37th Annual Conference on IEEE Industrial Electronics Society*. 2011. p. 2889–2894.

ALONSO, J. M. et al. A long-life high-power-factor hps-lamp led retrofit converter based on the integrated buck-boost buck topology. In: IEEE. *IECON 2011-37th Annual Conference on IEEE Industrial Electronics Society*. 2011. p. 2860–2865.

ALONSO, J. M. et al. Reducing storage capacitance in off-line led power supplies by using integrated converters. In: IEEE. *Industry Applications Society Annual Meeting (IAS), 2012 IEEE*. 2012. p. 1–8.

ALONSO, J. M. et al. A straightforward methodology to modeling high power factor ac–dc converters. *IEEE Transactions on Power Electronics*, IEEE, v. 28, n. 10, p. 4723–4731, 2013.

ALONSO, J. M. et al. Analysis and design of the integrated double buck–boost converter as a high-power-factor driver for power-led lamps. *Industrial Electronics, IEEE Transactions on*, IEEE, v. 59, n. 4, p. 1689–1697, 2012.

ALWITT, R. S.; HILLS, R. The chemistry of failure of aluminum electrolytic capacitors. *Parts, Materials and Packaging, IEEE Transactions on*, IEEE, v. 1, n. 2, p. 28–34, 1965.

ASTRÖM, K. J.; MURRAY, R. M. *Feedback systems: an introduction for scientists and engineers*. : Princeton university press, 2010.

BARDSLEY, N. et al. Manufacturing roadmap solid-state lighting research and development. *US Department of Energy*, 2014.

BARDSLEY, N. et al. Solid-state lighting research and development multi-year program plan. *US Department of Energy*, 2014.

BIBER, C. Led light emission as a function of thermal conditions. In: IEEE. *Semiconductor Thermal Measurement and Management Symposium, 2008. Semi-Therm 2008. Twenty-fourth Annual IEEE*. 2008. p. 180–184.

BUIATTI, G. M. et al. Condition monitoring of metallized polypropylene film capacitors in railway power trains. *Instrumentation and Measurement, IEEE Transactions on*, IEEE, v. 58, n. 10, p. 3796–3805, 2009.

BUSO, S.; MATTAVELLI, P. Digital control in power electronics. *Synthesis Lectures on Power Electronics*, Morgan & Claypool Publishers, v. 5, n. 1, p. 1–229, 2015.

CAMPONOGARA, D. et al. Offline led driver for street lighting with an optimized cascade structure. *Industry Applications, IEEE Transactions on*, IEEE, v. 49, n. 6, p. 2437–2443, 2013.

CAMPONOGARA, D. et al. Capacitance reduction with an optimized converter connection applied to led drivers. *Industrial Electronics, IEEE Transactions on*, IEEE, v. 62, n. 1, p. 184–192, 2015.

CHEMI-CON, N. *Aluminum capacitors catalogue-Technical note on judicious use of aluminum electrolytic capacitors*. 2013. Available from Internet: <http://www.chemi-con.com/2013AluminumElectrolyticCatalog.pdf>.

CHEN, H. T.; TAO, X. H.; HUI, S. R. Estimation of optical power and heat-dissipation coefficient for the photo-electro-thermal theory for led systems. *IEEE Transactions on Power Electronics*, IEEE, v. 27, n. 4, p. 2176–2183, 2012.

CHENG, C.-A. et al. A novel single-stage high power leds driver. In: IEEE. *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*. 2011. p. 2733–2740.

CHIU, H.-J. et al. A high-efficiency dimmable led driver for low-power lighting applications. *IEEE Transactions on Industrial Electronics*, v. 57, n. 2, p. 735 – 743, feb. 2010. ISSN 0278-0046.

CRAFORD, G. Current state of the art in high brightness leds. In: *APS March Meeting Abstracts*. 2007. v. 1, p. 3001.

DALLA COSTA, M. A. et al. A single-stage high-power-factor electronic ballast based on integrated buck flyback converter to supply metal halide lamps. *IEEE Transactions on Industrial Electronics*, v. 55, n. 3, p. 1112 – 1122, Mar. 2008. ISSN 0278-0046.

DOE. *Lifetime and reliability*. 2013.

DREYFUS, G.; GALLINAT, C. *Rise and Shine: Lighting the World with 10 Billion LED Bulbs*. 2015. Available from Internet: <https://www.energy.gov/articles/rise-and-shine-lighting-world-10-billion-led-bulbs>.

DUBILIER, C. *Application guide, aluminum electrolytic capacitors*. 2002. Available from Internet: <http://www.cde.com/catalogs/AEappGUIDE.pdf>.

EPCOS. *Data Book-Aluminum Electrolytic Capacitors*. 2012.

EPCOS. *Film Capacitors – General technical information*. 2015. Available from Internet: <http://www.epcos-china.com/blob/541236/download /4/pdf-generaltechnicalinformation.pdf>.

ERICKSON, R. W.; MAKSIMOVIC, D. *Fundamentals of Power Electronics*. : Springer, 2001. ISBN 978-0792372707.

FAIRCHILD. *Reference Design RD-L012*. 2011.

FRAYTAG, J. et al. A comparative performance investigation of single-stage dimmable electronic ballasts for electrodeless fluorescent lamp applications. *IEEE Transactions on Power Electronics*, IEEE, v. 30, n. 4, p. 2239–2252, 2015.

GACIO, D. et al. A universal-input single-stag2e high-power-factor power supply for hb-leds based on integrated buck–flyback converter. *Industrial Electronics, IEEE Transactions on*, IEEE, v. 58, n. 2, p. 589–599, 2011.

GACIO, D. et al. Optimization of a front-end dcm buck pfp for an hpf integrated single-stage led driver. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, IEEE, v. 3, n. 3, p. 666–678, 2015.

GARCIA, J. et al. An estimator of luminous flux for enhanced control of high brightness leds. In: IEEE. *2008 IEEE Power Electronics Specialists Conference*. 2008. p. 1852–1856.

GU, L. et al. Means of eliminating electrolytic capacitor in ac/dc power supplies for led lightings. *IEEE Transactions on Power Electronics*, IEEE, v. 24, n. 5, p. 1399–1408, 2009.

HUELSMAN, L. P.; ALLEN, P. E. *Introduction to the theory and design of active filters*. : McGraw-Hill College, 1980.

HUI, S.; QIN, Y. A general photo-electro-thermal theory for light emitting diode (led) systems. *IEEE Transactions on Power electronics*, IEEE, v. 24, n. 8, p. 1967–1976, 2009.

HUI, S. Y. et al. A novel passive offline led driver with long lifetime. *IEEE Transactions on Power Electronics*, v. 25, n. 10, p. 2665 – 2672, oct. 2010. ISSN 0885-8993.

IEC. *CISPR 22 : Information Technology Equipment - Radio disturbance characteristics - Limits and methods of measurement*. 2008.

IEC. *IEC 61000-3-2 : Electromagnetic compatibility (EMC) – Part 3 – 2: Limits – Limits for harmonic current emissions (equipment input current ≤ 16 A per phase)*. 2014.

IEC. *IEC 60063:2015 Standard : Preferred number series for resistors and capacitors*. 2015.

IHS. *LED Market Overview: LEDs & the SSL Ecosystem*. 2013.

INMETRO. *Portaria nº 144, de 13 de março de 2015*. 2015.

INMETRO. *Portaria n.º 20, de 15 de fevereiro de 2017*. 2017.

JIA, L.; LIU, Y.-F.; FANG, D. High power factor single stage flyback converter for dimmable led driver. In: *IEEE Energy Conversion Congress and Exposition (ECCE)*. 2015. p. 3231–3238.

JR, S. G. P.; DUBILIER, P. C. Deriving life multipliers for electrolytic capacitors. *IEEE Power Electronics Society Newsletter*, v. 16, n. 1, p. 11–12, 2004.

JR, S. G. P.; DUBILIER, P. C. *Reliability of CDE aluminum electrolytic capacitors*. 2004. Available from Internet: <http://www.cde.com/resources/technical-papers/reliability.pdf>.

KIM, J.-W.; YI, J.-H.; CHO, B.-H. Enhanced variable on-time control of critical conduction mode boost power factor correction converters. *Journal of Power Electronics*, v. 14, n. 5, p. 2890–898, sept. 2014. ISSN 1598-2092.

LAMAR, D. G. et al. On the limit of the output capacitor reduction in power-factor correctors by distorting the line input current. *IEEE Transactions on Power Electronics*, IEEE, v. 27, n. 3, p. 1168–1176, 2012.

LEE, B. et al. Robust passive led driver compatible with conventional rapid-start ballast. *IEEE Transactions on Power Electronics*, v. 26, n. 12, p. 3694 – 3706, dec. 2011. ISSN 0885-8993.

LEE, E. S. et al. Temperature-robust lc^3 passive led drivers with low thd, high efficiency and pf, and long life. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, v. 3, n. 3, p. 829 – 840, jun. 2015. ISSN 2168-6777.

LEHMAN, B.; WILKINS, A. J. Designing to mitigate effects of flicker in led lighting: Reducing risks to health and safety. *IEEE Power Electronics Magazine*, IEEE, v. 1, n. 3, p. 18–26, 2014.

LEVY, D. Introduction to numerical analysis. *Department of Mathematics and Center for Scientific Computation and Mathematical Modeling, CSCAMM, University of Maryland*, 2010.

LUZ, P. C. et al. An integrated insulated buck-boost-flyback converter to feed led's lamps to street lighting with reduced capacitances. In: IEEE. *Industry Applications (INDUSCON), 2014 11th IEEE/IAS International Conference on*. 2014. p. 1–6.

MARCHESAN, T. B. *Integração de conversores estáticos aplicados a sistemas de iluminação publica*. Ph.D. Thesis (Ph.D.) — Thesis (Ph. D. in Electrical Engineering), Universidade Federal de Santa Maria, Santa Maria, RS, Brasil, 2007.

MARCHESAN, T. B. et al. Two flyback-based integrated converters for the implementation of lfsw electronic ballasts. In: IEEE. *Industry Applications Conference, 2007. 42nd IAS Annual Meeting. Conference Record of the 2007 IEEE*. 2007. p. 463–470.

MÄRZ, M. et al. Power electronics system integration for electric and hybrid vehicles. In: IEEE. *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*. 2010. p. 1–10.

Massey Jr.; Frank J. The kolmogorov-smirnov test for goodness of fit. *Journal of the American statistical Association*, Taylor & Francis Group, v. 46, n. 253, p. 68–78, 1951.

MELO, M. D. et al. Analysis of low-frequency current ripple transmission in series-resonant led drivers. *Electronics Letters*, IET, v. 51, n. 9, p. 716–717, 2015.

NOGUEIRA, F. J. et al. Influência da temperatura no desempenho de luminárias led. In: *International Conference on Industry Applications (IEEE/IAS 10th INDUSCON)*. 2012.

NXP. *Datahseet of SSL4120T - Resonant power supply control IC with PFC*. 2012.

OGATA, K.; YANG, Y. *Modern control engineering*. : Prentice-Hall Englewood Cliffs, 1970.

PEREIRA, G. G. et al. Led driver based on input current shaper without electrolytic capacitor. *IEEE Transactions on Industrial Electronics*, IEEE, v. 64, n. 6, p. 4520–4529, 2017.

PEREIRA, G. G. et al. High-power-factor led driver based on input current shaper using a flyback converter. In: IEEE. *Industry Applications Society Annual Meeting, 2015 IEEE*. 2015. p. 1–6.

POPLAWSKI, M.; MILLER, N. J.; FIES, F. Exploring flicker in solidstate lighting: What you might find, and how to deal with it. *Pacific Northwest National Laboratory*, 2011.

POWER, E. N. Capacitors age and capacitors have an end of life. *White paper*, 2012.

QU, X.; WONG, S.-C.; TSE, C. K. Noncascading structure for electronic ballast design for multiple led lamps with independent brightness control. *IEEE Transactions on Power Electronics*, v. 25, n. 2, p. 331 – 340, feb. 2010. ISSN 0885-8993.

RASMUSSEN, S. *Production economics: the basic theory of production optimisation.* : Springer Science & Business Media, 2012.

RODRIGUES, C. R. et al. Experimental characterization regarding two types of phosphor-converted white high-brightness leds: low power and high power devices. In: IEEE. *XI Brazilian Power Electronics Conference*. 2011. p. 734–740.

RODRIGUES, C. R. et al. An experimental comparison between different technologies arising for public lighting: Led luminaires replacing high pressure sodium lamps. In: IEEE. *2011 IEEE International Symposium on Industrial Electronics*. 2011. p. 141–146.

RODRIGUES, C. R. B. S. *Contribuições ao uso de Diodos Emissores de Luz em Iluminação Pública*. Ph.D. Thesis (Ph.D.) — Thesis (Ph. D. in Electrical Engineering), Universidade Federal de Juiz de Fora, Juiz de Fora, MG, Brasil, 2012.

RODRIGUEZ, C.; AMARATUNGA, G. A. Long-lifetime power inverter for photovoltaic ac modules. *Industrial Electronics, IEEE Transactions on*, IEEE, v. 55, n. 7, p. 2593–2601, 2008.

ROUND, H. J. A note on carborundum. *Electrical world*, v. 49, n. 6, p. 309, 1907.

S-KEI. *Schematic diagrams of Light Emitting Diodes (LED)*. 2011. Available from Internet: <https://commons.wikimedia.org>.

Samsung Electronics. *Samsung Achieves 220 Lumens per Watt with New Mid-Power LED Package*. 2017. Available from Internet: <https://news.samsung.com/global/samsung-achieves-220-lumens-per-watt-with-new-mid-power-led-package>.

SCHUBERT, E. F.; GESSMANN, T.; KIM, J. K. *Light emitting diodes*. : Wiley Online Library, 2005.

SHUR, M. S.; ZUKAUSKAS, R. Solid-state lighting: toward superior illumination. *Proceedings of the IEEE*, IEEE, v. 93, n. 10, p. 1691–1703, 2005.

SOARES, G. M. et al. A comparative study between two single-stage led drivers: A sole converter versus an integrated topology. In: IEEE. *Industry Applications (INDUSCON), 2012 10th IEEE/IAS International Conference on*. 2012. p. 1–8.

SOARES, G. M. et al. A single-stage high efficiency long-life off-line led driver based on the dcm cuk converter. In: IEEE. *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society*. 2012. p. 4509–4514.

SOMNUSDE. *Countries of the world, colored according to their nominal power net voltage and frequency*. 2009. Available from Internet: <https://commons.wikimedia.org>.

SPIAZZI, G.; BUSO, S.; MENEGHESSO, G. Analysis of a high-power-factor electronic ballast for high brightness light emitting diodes. In: IEEE. *Power Electronics Specialists Conference, 2005. PESC'05. IEEE 36th*. 2005. p. 1494–1499.

STMICROELECTRONICS. *STEVAL-ILL052V1 - 48 V - 130 W high efficiency converter with PFC for LED street lighting applications based on L6562 and L6599 - European version*. 2012.

TSAO, J. Y. Solid-state lighting: lamps, chips, and materials for tomorrow. *IEEE Circuits and Devices Magazine*, IEEE, v. 20, n. 3, p. 28–37, 2004.

TUSTIN, A. A method of analysing the behaviour of linear systems in terms of time series. *Electrical Engineers-Part IIA: Automatic Regulators and Servo Mechanisms, Journal of the Institution of*, IET, v. 94, n. 1, p. 130–142, 1947.

USDOD. *MIL-HDBK-217F - Military Handbook - Reliability Prediction of Electronic Equipment*. 1991.

WANG, B. et al. A method of reducing the peak-to-average ratio of led current for electrolytic capacitor-less ac–dc drivers. *IEEE Transactions on Power Electronics*, IEEE, v. 25, n. 3, p. 592–601, 2010.

WANG, H.; BLAABJERG, F. Reliability of capacitors for dc-link applications in power electronic converters?an overview. *Industry Applications, IEEE Transactions on*, IEEE, v. 50, n. 5, p. 3569–3578, 2014.

WANG, Y. et al. A single-stage led driver based on interleaved buck–boost circuit and llc resonant converter. *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, IEEE, v. 3, n. 3, p. 732–741, 2015.

WANG, Y. et al. A single-stage led driver based on bcm boost circuit and converter for street lighting system. *Industrial Electronics, IEEE Transactions on*, IEEE, v. 62, n. 9, p. 5446–5457, 2015.

WANG, Y. et al. Single-stage led driver with low bus voltage. *Electronics Letters*, IET, v. 49, n. 7, p. 455–457, 2013.

WEI, H.; BATARSEH, I. Comparison of basic converter topologies for power factor correction. In: *Proceedings of IEEE Southeastcon '98*. 1998. p. 348 – 353.

WILKINS, A.; VEITCH, J.; LEHMAN, B. Led lighting flicker and potential health concerns: Ieee standard par1789 update. In: IEEE. *2010 IEEE Energy Conversion Congress and Exposition*. 2010. p. 171–178.

WONG, C. et al. An alternative approach to led driver design based on high-voltage driving. *Power Electronics, IEEE Transactions on*, IEEE, v. 31, n. 3, p. 2465–2475, 2016.

WU, T.-F.; CHEN, Y.-K. Modeling of single-stage converters with high power factor and fast regulation. *IEEE Transactions on Industrial Electronics*, IEEE, v. 46, n. 3, p. 585–593, 1999.

YAN, B. et al. Can junction temperature alone characterize thermal performance of white led emitters? *IEEE Photonics Technology Letters*, IEEE, v. 23, n. 9, p. 555–557, 2011.

YIM, S. et al. A behavioral model of a two-stage average-current-mode-controlled pfc converter for dimmable mr16 led lamps. In: *International SoC Design Conference (ISOCC)*. 2013. p. 380–383.

ZHOU, Y. et al. A remaining useful life prediction method based on condition monitoring for led driver. In: IEEE. *Prognostics and System Health Management (PHM), 2012 IEEE Conference on*. 2012. p. 1–5.

APPENDIX A – SUPPLEMENTARY MATERIAL OF CHAPTER 4

A.1 Mathematical proof of the flyback-based converter input current with duty cycle modulation

The input current of the flyback-based converter is given by (1), as shown in Chapter 4.

$$|i_g(t)| = \frac{|v_g(t)|\, d(t)^2}{2L_m f_s}. \tag{1}$$

By considering the diode bridge, one can write:

$$i_g\,(t) = \begin{cases} |i_g(t)|\,,\; if\; v_g\,(t) \geq 0 \\ -\,|i_g(t)|\,,\; if\; v_g\,(t) < 0 \end{cases} \tag{2}$$

Since the term $d(t)^2/\,(2L_m f_s)$ is always a positive number, the input current of the driver can be expressed as:

$$i_g(t) = \frac{v_g(t) d(t)^2}{2L_m f_s}. \tag{3}$$

By replacing the definition of the input voltage, given by (4), and the duty cycle, given by (5), in (3), the input current can be written as (6).

$$v_g(t) = \sqrt{2} V_G \sin\left(2\pi f_L t\right). \tag{4}$$

$$d(t) = D_0 + D_2 \sin(2\omega_L t + \phi_2). \tag{5}$$

$$i_g\,(t) = \frac{\sqrt{2} V_G}{2L_m f_s} \sin\left(\omega_L t\right) \left[D_0 + D_2 \sin\left(2\omega_L t + \phi_2\right)\right]^2, \tag{6}$$

which can be rewritten as:

$$
\begin{aligned}
i_g(t) &= \frac{\sqrt{2}V_G}{2L_m f_s}\sin(\omega_L t)\left[{D_0}^2 + 2D_0D_2\sin(2\omega_L t+\phi_2) + {D_2}^2\sin^2(2\omega_L t+\phi_2)\right] = \\
&= \frac{\sqrt{2}V_G}{2L_m f_s}\sin(\omega_L t)\left\{{D_0}^2 + 2D_0D_2\sin(2\omega_L t+\phi_2) + \frac{{D_2}^2}{2}\left[1-\cos(4\omega_L t+2\phi_2)\right]\right\} = \\
&= \frac{\sqrt{2}V_G}{2L_m f_s}\left\{{D_0}^2\sin(\omega_L t) + D_0D_2\left[\cos(\omega_L t+\phi_2)-\cos(3\omega_L t+\phi_2)\right] + \frac{{D_2}^2}{2}\left[\sin(\omega_L t)-\cos(4\omega_L t+2\phi_2)\sin(\omega_L t)\right]\right\} = \\
&= \frac{\sqrt{2}V_G}{2L_m f_s}\left\{{D_0}^2\sin(\omega_L t) + D_0D_2\left[\cos(\omega_L t+\phi_2)-\cos(3\omega_L t+\phi_2)\right] + \frac{{D_2}^2}{2}\left[\sin(\omega_L t)-\frac{1}{2}\left(\sin(5\omega_L t+2\phi_2)-\sin(3\omega_L t+2\phi_2)\right)\right]\right\} = \\
&= \frac{\sqrt{2}V_G}{2L_m f_s}\left\{{D_0}^2\sin(\omega_L t) + D_0D_2\left[\cos(\omega_L t+\phi_2)-\cos(3\omega_L t+\phi_2)\right] + \frac{{D_2}^2}{2}\sin(\omega_L t) - \frac{{D_2}^2}{4}\sin(5\omega_L t+2\phi_2) + \frac{{D_2}^2}{4}\sin(3\omega_L t+2\phi_2)\right\}
\end{aligned}
\tag{7}
$$

Equation (7) can be rewritten in terms of its harmonic components, as shown in:

$$
i_g(t) = i_{g1}(t) + i_{g3}(t) + i_{g5}(t), \tag{8}
$$

in which the first harmonic $i_{g1}(t)$, the third $i_{g3}(t)$ and the fifth $i_{g5}(t)$ are given by (9), (10) and (11), respectively.

$$
\begin{aligned}
i_{g1}(t) &= \frac{\sqrt{2}V_G}{2L_m f_s}\left[\left({D_0}^2+\frac{{D_2}^2}{2}\right)\sin(\omega_L t)+D_0D_2\cos(\omega_L t+\phi_2)\right]= \\
&= \frac{\sqrt{2}V_G}{2L_m f_s}\left[\left({D_0}^2+\frac{{D_2}^2}{2}\right)\sin(\omega_L t)+D_0D_2\left(\cos(\omega_L t)\cos(\phi_2)-\sin(\omega_L t)\sin(\phi_2)\right)\right] \\
&= \frac{\sqrt{2}V_G}{2L_m f_s}\left[\left({D_0}^2+\frac{{D_2}^2}{2}-D_0D_2\sin(\phi_2)\right)\sin(\omega_L t)+D_0D_2\cos(\omega_L t)\cos(\phi_2)\right] \\
&= \underbrace{\frac{\sqrt{2}V_G}{2L_m f_s}\left[\left({D_0}^2+\frac{{D_2}^2}{2}-D_0D_2\sin(\phi_2)\right)^2+\left(D_0D_2\cos(\phi_2)\right)^2\right]^{\frac{1}{2}}}_{I_1}\sin\left(\omega_L t+\underbrace{\tan^{-1}\left(\frac{2D_0D_2\cos(\phi_2)}{2{D_0}^2+{D_2}^2-2D_0D_2\sin(\phi_2)}\right)}_{\theta_1}\right)
\end{aligned}
\tag{9}
$$

$$
\begin{aligned}
i_{g3}(t) &= \frac{\sqrt{2}V_G}{2L_m f_s}\left[\frac{{D_2}^2}{4}\sin(3\omega_L t+2\phi_2)-D_0D_2\cos(3\omega_L t+\phi_2)\right]= \\
&= \frac{\sqrt{2}V_G}{2L_m f_s}\left[\frac{{D_2}^2}{4}\left(\sin(3\omega_L t)\cos(2\phi_2)+\cos(3\omega_L t)\sin(2\phi_2)\right)-D_0D_2\left(\cos(3\omega_L t)\cos(\phi_2)-\sin(3\omega_L t)\sin(\phi_2)\right)\right] \\
&= \frac{\sqrt{2}V_G}{4L_m f_s}\left[\left(\frac{{D_2}^2}{2}\cos(2\phi_2)+2D_0D_2\sin(\phi_2)\right)\sin(3\omega_L t)+\left(\frac{{D_2}^2}{2}\sin(2\phi_2)-2D_0D_2\cos(\phi_2)\right)\cos(3\omega_L t)\right] \\
&= \underbrace{\frac{\sqrt{2}V_G}{4L_m f_s}\left[\left(\frac{{D_2}^2}{2}\cos(2\phi_2)+2D_0D_2\sin(\phi_2)\right)^2+\left(\frac{{D_2}^2}{2}\sin(2\phi_2)-2D_0D_2\cos(\phi_2)\right)^2\right]^{\frac{1}{2}}}_{I_3}\sin\left(3\omega_L t+\underbrace{\tan^{-1}\left(\frac{\frac{{D_2}^2}{2}\sin(2\phi_2)-2D_0D_2\cos(\phi_2)}{\frac{{D_2}^2}{2}\cos(2\phi_2)+2D_0D_2\sin(\phi_2)}\right)}_{\theta_3}\right)
\end{aligned}
\tag{10}
$$

$$i_{g5}(t) = -\frac{\sqrt{2}V_G {D_2}^2}{8L_m f_s}\sin(5\omega_L t + 2\phi_2) = \underbrace{\frac{\sqrt{2}V_G {D_2}^2}{8L_m f_s}}_{I_5}\sin\left(5\omega_L t + \underbrace{2\phi_2 + \pi}_{\theta_5}\right) \tag{11}$$

A.2 Schematic of the Control Board

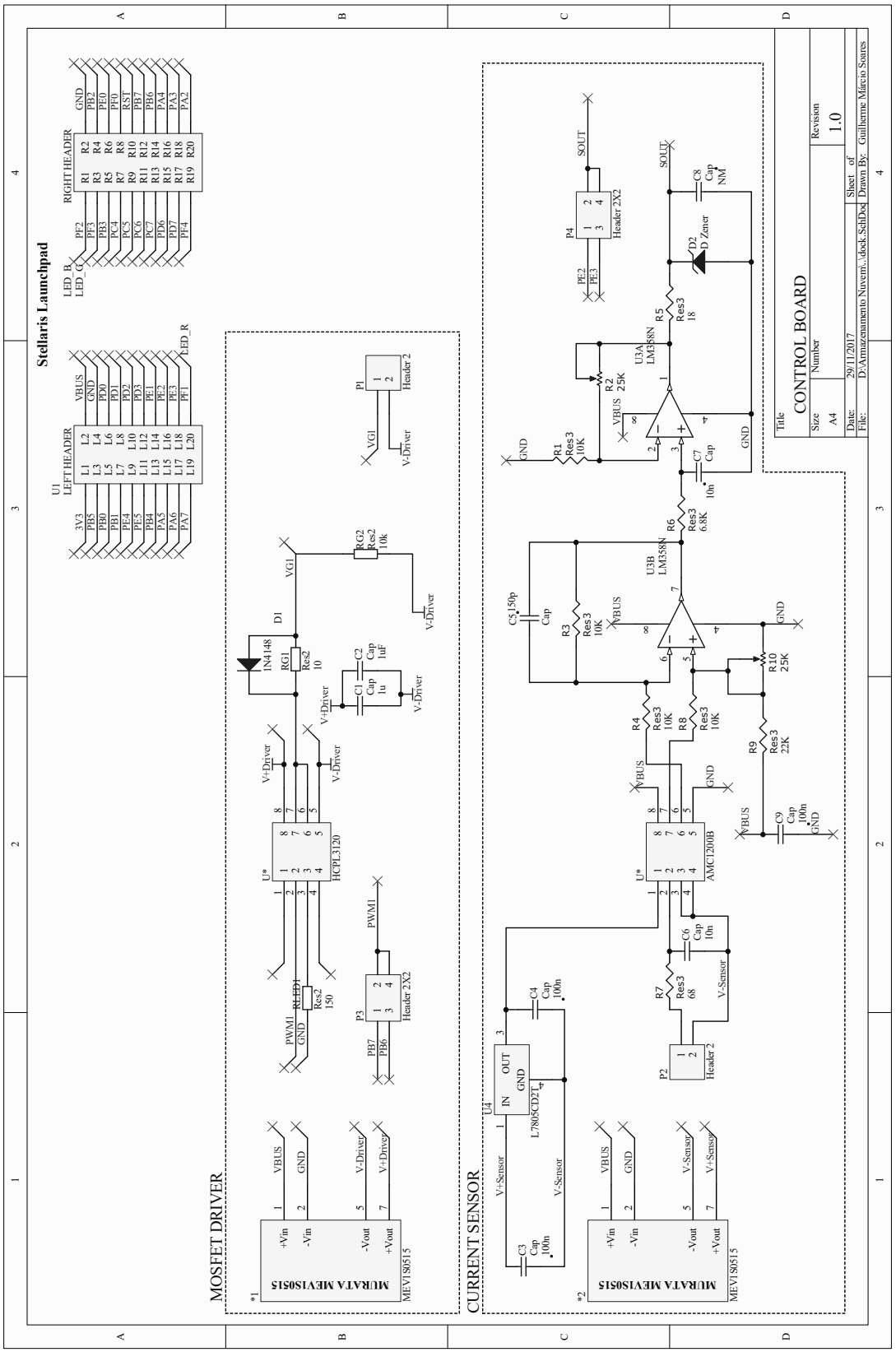


Figure 126: Schematic of the control board.

A.3 Content of the C-block Used in the Simulation of Chapter 4

The content of the C-block used in the simulation of the ARCT is presented in figures 127 and 128.

```
# include <Stdlib.h>
#include <String.h>

#define Fs 5000

#define Nbp1 0.012341106167435646
#define Nbp2 0
#define Nbp3 -0.012341106167435646
#define Dbp2 -1.952917218208313
#define Dbp3 0.9751778841018677
#define Nap1 0.64599
#define Nap2 -0.5424
#define Dap2 -0.87755

#define N11 2.000000e-003
#define N21 2.000000e-003
#define D11 -1

int adc = 0, tsim=0;
double x[5]=0,0,0,0,0;
double yap[2]=0,0;
double ybp[3]=0,0,0;
double ymv[2]=0,0;
double yt;
double a1,a2,b0,b2;

int g_nInputNodes=0;
int g_nOutputNodes=0;

int g_nStepCount=0;
```

Figure 127: C-block - Variable/Function definitions.

```
void RunSimUser(double t, double delt, double *in, double *out, int *pnError, char *
szErrorMsg)
{
tsim++; %Auxiliary variable used to implement the sampling rate

if(tsim>(1/delt)/Fs)
{
tsim =0;
//Implementation of the ARCT branch
x[3]=x[2];
x[2]=x[1];
x[1]=x[0];
x[0]= in[0];
ybp[2]=ybp[1];
ybp[1]=ybp[0];
yap[1]=yap[0];
ybp[0] =Nbp1*x[0]+Nbp2*x[1]+Nbp3*x[2]-Dbp2*ybp[1]-Dbp3*ybp[2];
yap[0] = Nap1*ybp[0]+Nap2*ybp[1]-Dap2*yap[1];

//Implementation of the controller for compensating the average value of the output
current
ymv[1]=ymv[0];
ymv[0] = N11*x[0]+ N21*x[1]-D11*ymv[1];

// Calculation of the new duty-cycle
yt = yap[0]+ymv[0];
out[1]=yt;

}
}
```

Figure 128: C-block - Implementation of the RunSimUser Fcn

APPENDIX B – MATLAB SCRIPTS USED IN THE OPTIMIZATION ALGORITHM OF CHAPTER 5

This appendix compiles the main scripts used for solving the optimization algorithm proposed in Chapter 5. The codes are presented in the following. One can note that the main features of each routine were commented to help the understanding of the program.

B.1 Main routine

```
1
2  clearvars;clc;
3  %% Parameters range - Definition of the parameters used in the ...
       optimization routine
4
5  Par.d0 = [0.5 0.75];
6  Par.Nleds = 48:24:72;
7  Par.VG = sqrt(2)*[127 220];
8  Par.fl = 60;
9  Par.Ne = 1;
10 Par.VBbuckR = [0.8*sind(25) 0.6*sind(25)];
11 Par.VBboostR = [1.5 1.7];
12 Par.VBbuckboost = [180 350];
13 Par.fs = 50e3;
14 Par.eff_pfc = 1;
15 Par.eff_pc = 1;
16 Par.rdLED = 0.4030;
17 Par.VtLED = 2.7120;
18 Par.Io = 0.5;
19 Par.Harm = [0 2;0 4;0 6;0 8;2 4;2 6;2 8;4 6;4 8;6 8];
20 Par.LFR = Par.Io*[0.1 0.5];
21 Par.HFR = Par.Io*[0.05 0.2];
22
```

```
%% Algorithm parameters
%Step for the amplitude of the duty cycle harmonic components
AlgVars.dstep = 0.01;
%Step for the phase of the duty cycle harmonic components
AlgVars.phistep = deg2rad(10);
%Number of capacitors to be evaluated
AlgVars.numcaps = 50;
%Initial value of Cdef
AlgVars.capinit = 100e-6;


%% Configuration of the cluster
% Parameters for configurating the cluster
delete(gcp('nocreate'));
JOB_STORAGE_LOCATION = '/home/guilhermem/clusterfiles';
walltime = '999:00:00';
cluster = clusterConfig(JOB_STORAGE_LOCATION, walltime);
pool = parpool(cluster,96, 'IdleTimeout', 99999);
pathTempG = '/home/guilhermem/Cluster/ProgramThesis/temp/';
pathReport = ...
    '/home/guilhermem/Cluster/ProgramThesis/reports/status.txt';

%% Distribution of the cases in the parallel pool
% Each analyzed case will be assigned to a process and will be ...
    executed on
% the computer cluster if there is a resourse availabe

Converters = [{'Flyback'} {'IDBB'} {'IBoBu'} {'IBuFly'} ]; % ...
    Converters that will be analyzed
k = 1;
for conv = 1:length(Converters)
    Converter = Converters{conv};
    pathTemp = [pathTempG Converter '/'];
    Cases{conv} = GenCases(Par,Converter); %Function for ...
        generating the cases (Tables 15, 23, 31 and 37)
    NotExecuted = verifyNE(size(Cases{conv},1),Par.Harm,pathTemp); ...
        %Function for that verifies which cases were not executed
    for i = 1:size(NotExecuted,1) % Assigns the cases for a ...
        process to be executed in the cluster
        F(k)=parfeval(pool,@exsearch,0,Converter, ...
            Cases{conv}(NotExecuted(i,3),:),NotExecuted(i,3), ...
            NotExecuted(i,1:2),AlgVars,pathTemp);
        k = k+1;
```

```
58
59      end
60  end
61
62  NotExecutedAll = ones(1,length(Converters));
63
64  %%Loop that wait the execution of all the cases and prints a ...
        report file
65  while(max(NotExecutedAll)≠0)
66      for conv = 1:length(Converters)
67          Converter = Converters{conv};
68          pathTemp = [pathTempG Converter '/'];
69          NExec = verifyNE(size(Cases{conv},1),Par.Harm, pathTemp);
70          if(isempty(NExec))
71              NotExecutedAll(conv) = 0;
72          else
73              NotExecutedAll(conv) = size(NExec,1);
74          end
75          Updatereport(F, pathReport);
76          pause(30);
77      end
78  end
79  delete(pool);
```

B.1.1 Function for the Generation of the studied cases

```
1   function Cases = GenCases(Par,Converter)
2   %% Function that groups the design parameters, creating the ...
        several cases to be studied
3
4   k=1;
5   for lfri = 1:length(Par.LFR)
6       for d0i = 1:length(Par.d0)
7           for vgi = 1: length(Par.VG)
8               for ni = 1:length(Par.Nleds)
9                   rd = Par.rdLED*Par.Nleds(ni);
10                  Vt = Par.VtLED*Par.Nleds(ni);
11                  Vo = rd*Par.Io + Vt;
12                  switch Converter
13                      case 'Flyback'
```

```
14                          Cases(k,:) = [Par.d0(d0i) ...
                                dcrit_fly(Par.VG(vgi) , Par.Ne, Vo) ...
                                Par.VG(vgi) Par.fl Par.fs Par.Io rd Vt ...
                                0 Par.Ne Par.eff_pfc Par.eff_pc ...
                                Par.LFR(lfri) Par.HFR(lfri)];
15                          k = k+1;
16                      case 'IBuFly'
17                          for vbi=1:length(Par.VBbuckR)
18                              Cases(k,:) = [Par.d0(d0i) ...
                                    dcrit_ibufly(Par.VG(vgi), ...
                                    Par.VBbuckR(vbi)*Par.VG(vgi), Vo, ...
                                    Par.Ne) Par.VG(vgi) Par.fl Par.fs ...
                                    Par.Io rd Vt ...
                                    Par.VBbuckR(vbi)*Par.VG(vgi) Par.Ne ...
                                    Par.eff_pfc 1 Par.LFR(lfri) ...
                                    Par.HFR(lfri)];
19                              k = k+1;
20                          end
21                      case 'IBoBu'
22                          for vbi=1:length(Par.VBboostR)
23                              Cases(k,:) = [Par.d0(d0i) ...
                                    dcrit_ibobu(Par.VG(vgi), ...
                                    Par.VBboostR(vbi)*Par.VG(vgi), Vo) ...
                                    Par.VG(vgi) Par.fl Par.fs Par.Io rd ...
                                    Vt Par.VBboostR(vbi)*Par.VG(vgi) 0 ...
                                    Par.eff_pfc Par.eff_pc ...
                                    Par.LFR(lfri) Par.HFR(lfri)];
24                              k = k+1;
25                          end
26                      case 'IDBB'
27                          for vbi=1:length(Par.VBbuckboost)
28                              Cases(k,:) = [Par.d0(d0i) ...
                                    dcrit_idbb(Par.VG(vgi) , ...
                                    Par.VBbuckboost(vbi), Vo) ...
                                    Par.VG(vgi) Par.fl Par.fs Par.Io rd ...
                                    Vt Par.VBbuckboost(vbi) 0 ...
                                    Par.eff_pfc Par.eff_pc ...
                                    Par.LFR(lfri) Par.HFR(lfri)];
29                              k = k+1;
30                          end
31                  end
32              end
33          end
```

```
34      end
35  end
36  end
```

B.2 Function that Implements the Exhaustive Search Algorithm

```
1  function [] = exsearch(Converter, Case, CaseNumber, Harm, AlgVars, ...
       pathTemp)
2
3  %Function that Implements the Exhaustive Search Algorithm
4
5  SS = GenSS(Converter,Case,Harm,AlgVars); %Function for generating ...
       the search space
6
7  fob_min = 1e6; %Initial value for the fob
8
9  j=1;
10 for i = 1:size(SS,1)
11
12     % Calculation of the converter variables
13     switch Converter
14         case 'Flyback'
15             [Ripple, I1, I3, I5, I7, I9 , I11, I13, PF, THD, ...
                   Inductors, Chf] = calc_fly(Case, SS(i,:));
16         case 'IBuFly'
17             [Ripple, I1, I3, I5, I7, I9 , I11, I13, PF, THD, ...
                   Inductors, Chf] = calc_ibufly(Case, SS(i,:));
18         case 'IBoBu'
19             [Ripple, I1, I3, I5, I7, I9 , I11, I13, PF, THD, ...
                   Inductors, Chf] = calc_ibobu(Case, SS(i,:));
20         case 'IDBB'
21             [Ripple, I1, I3, I5, I7, I9 , I11, I13, PF, THD, ...
                   Inductors, Chf] = calc_idbb(Case, SS(i,:));
22     end
23
24     %Calculation of the matrix H
25     H = [Ripple - Case(13);
26         -PF     + 0.92;
27         I3      - 0.3*PF*I1;
28         I5      - 0.1*I1;
29         I7      - 0.07*I1;
```

```
30          I9      - 0.05*I1;
31          I11     - 0.03*I1;
32          I13     - 0.03*I1];
33
34
35      if(max(H)<0) % Evaluation of the constraints
36          fob = SS(i,9)*1e6 + Ripple; % Calculation of f(x)
37          if(fob<fob_min)
38              % If fob< fob_min -> x* = x
39              % Store the results
40              fob_min = fob;
41              Solution.x = SS(i,:);
42              Solution.Inductors = Inductors;
43              Solution.Chf = Chf;
44              Solution.Performance = [Ripple THD];
45          end
46      end
47
48  end
49
50  if(¬exist('Solution'))
51      Solution = 0;
52  end
53  %save the solution for the studied case
54  save([pathTemp num2str(Harm(1)) num2str(Harm(2)) ...
        num2str(CaseNumber)],'Solution');
55  end
```

B.3 Function for generating the search space

```
1   function SS = GenSS(Converter,Case,Harm,AlgVars)
2
3   %% Function for creating the search space
4   Cbx = AlgVars.capinit;
5   ripple = 2*Case(13);
6
7   % Calculation of Cdef by means of the modified Newton-Raphson ...
        Algorithm
8   while(¬(ripple>0.95*Case(13)&&ripple≤Case(13)))
9
10          switch Converter
```

```
11          case 'Flyback'
12              ripple = calc_fly(Case, [0 0 0 0 0 0 0 0 Cbx]);
13              ripl = calc_fly(Case, [0 0 0 0 0 0 0 0 Cbx*1.01]);
14              drip = (ripl - ripple)/(Cbx*0.01);
15          case 'IBuFly'
16              ripple = calc_ibufly(Case, [0 0 0 0 0 0 0 0 Cbx]);
17              ripl = calc_ibufly(Case, [0 0 0 0 0 0 0 0 Cbx*1.01]);
18              drip = (ripl - ripple)/(Cbx*0.01);
19          case 'IBoBu'
20              ripple = calc_ibobu(Case, [0 0 0 0 0 0 0 0 Cbx]);
21              ripl = calc_ibobu(Case, [0 0 0 0 0 0 0 0 Cbx*1.01]);
22              drip = (ripl - ripple)/(Cbx*0.01);
23          case 'IDBB'
24              ripple = calc_idbb(Case, [0 0 0 0 0 0 0 0 Cbx]);
25              ripl = calc_idbb(Case, [0 0 0 0 0 0 0 0 Cbx*1.01]);
26              drip = (ripl - ripple)/(Cbx*0.01);
27          end
28
29          aux = (Case(13)- ripple)/(-drip);
30          if(abs(aux)>0.8*Cbx)
31              Cbx = Cbx - 0.8*Cbx*aux/abs(aux);
32          else
33              Cbx = Cbx - aux;
34          end
35
36
37
38  end
39
40  %Definition of the search space for the capacitor C_LF
41  Cbx = ceil(Cbx*1e6)/1e6;
42  capopt = linspace(0.01*Cbx,Cbx,AlgVars.numcaps);
43
44
45  k=1;
46  d0 = Case(1)*Case(2);
47  dmax = 0.9*Case(2) - d0;
48
49  %Definition of the search space of the amplitudes and phases of ...
        the duty
50  %cycle function
51
52  ssd = 0:AlgVars.dstep:dmax;
```

```
53 dopt = length(ssd);
54 ssphi = -pi:AlgVars.phistep:pi;
55 phiopt = length(ssphi);
56
57 %Definition of the harmonics that will be analyzed in the actual case
58 if(any(Harm == 2))
59     nopt2 = dopt;
60     nphi2 = phiopt;
61 else
62     nopt2 = 1;
63     nphi2 = 1;
64 end
65
66 if(any(Harm== 4))
67     nopt4 = dopt;
68     nphi4 = phiopt;
69 else
70     nopt4 = 1;
71     nphi4 = 1;
72 end
73
74 if(any(Harm == 6))
75     nopt6 = dopt;
76     nphi6 = phiopt;
77 else
78     nopt6 = 1;
79     nphi6 = 1;
80 end
81
82 if(any(Harm == 8))
83     nopt8 = dopt;
84     nphi8 = phiopt;
85 else
86     nopt8 = 1;
87     nphi8 = 1;
88 end
89 num =1;
90
91 %Definition of the search space of the optimization algorithm by ...
       combining
92 %the search spaces of each variable of the vector x
93
```

```
94  SS = ...
        zeros(nopt2*nopt4*nopt6*nopt8*nphi2*nphi4*nphi6*nphi8*AlgVars.numcaps,9);
95  for d2=1:nopt2
96      for phi2=1:nphi2
97          if(ssd(d2) ==0 && ssphi(phi2)≠ssphi(1))
98              break;
99          end
100         for d4=1:nopt4
101             for phi4=1:nphi4
102                 if(ssd(d4) ==0 && ssphi(phi4)≠ssphi(1))
103                     break;
104                 end
105                 for d6=1:nopt6
106                     for phi6=1:nphi6
107                         if(ssd(d6) ==0 && ssphi(phi6)≠ssphi(1))
108                             break;
109                         end
110                         for d8=1:nopt8
111                             for phi8=1:nphi8
112                                 if(ssd(d8) ==0 && ...
                                        ssphi(phi8)≠ssphi(1))
113                                     break;
114                                 end
115                                 if(checkduty(0.9*Case(2), ...
                                        d0,Case(4), ssd(d2), ...
                                        ssphi(phi2), ssd(d4), ...
                                        ssphi(phi4), ssd(d6), ...
                                        ssphi(phi6), ssd(d8), ssphi(phi8)))
116                                     break;
117                                 end
118                                 for cap=1:AlgVars.numcaps
119                                     SS(num,:) = [ssd(d2) ...
                                            ssphi(phi2) ssd(d4) ...
                                            ssphi(phi4) ssd(d6) ...
                                            ssphi(phi6) ssd(d8) ...
                                            ssphi(phi8) capopt(cap)];
120                                     num = num + 1;
121                                 end
122                             end
123                         end
124                     end
125                 end
126             end
```

```
127         end
128     end
129 end
130
131 SS(num:size(SS,1),:) = [];
132 end
```

B.4 Function for evaluating the flyback converter

B.4.1 Main code

```
1  function [Ripple, I1, I3, I5, I7, I9 , I11, I13, PF, THD, Lm, Chf] ...
       = calc_fly(Case, x)
2
3  %% Function for evaluating the main variables of the flyback converter
4  Chf = 0;
5  % Parameters loading
6  d0 = Case(1)*Case(2);
7  Vt = Case(8);
8  rd = Case(7);
9  fs = Case(5);
10 fl = Case(4);
11 VG = Case(3);
12 eff = Case(11);
13 Po = Case(6)^2*rd + Case(6)*Vt;
14
15 % Optimization variables
16 d2 = x(1);
17 phi2 = x(2);
18 d4 = x(3);
19 phi4 = x(4);
20 d6 = x(5);
21 phi6 = x(6);
22 d8 = x(7);
23 phi8 = x(8);
24 C = x(9);
25
26 %Function for calculating the magnetizing inductance
27 Lm = LmDesign(d0, x, fs, fl, VG, Po, eff);
28
29 % Auxiliary variables
```

```
ppc = 1000;
wl = 2*pi*fl;
Os = 2*pi/ppc;
Of = 28*pi;
O = 0:Os:Of;
N = length(O);

vo = zeros(1,N);
io = zeros(1,N);
ig = zeros(1,N);

%Initial conditions
vo(1) = Vt;
jj = 0;
iomed = zeros(1,3);

%% Numerical solution of the main variables of the converter
for k = 1:N
    o = O(k);
    d = d0 + d2*sin(2*o+phi2) + d4*sin(4*o+phi4) + ...
        d6*sin(6*o+phi6) + d8*sin(8*o+phi8);
    vg = VG*sin(o);
    ig(k) = d^2*vg/(2*fs*Lm);
    vo(k+1) = vo(k) + Os/(wl*C)*(eff*vg*vg*d*d/(2*fs*vo(k)*Lm) - ...
        ((vo(k)-Vt)/rd));
    io(k)=(vo(k+1)-Vt)/rd;

    %Detection of steady state for stoping the solution
    %(if the mean of the output current remains constant for 3 ...
        cycles it means that the numerical solution achieved the ...
        steady state)
    if(mod(k,ppc)==0)
        jj = mod((jj),3)+1;
        iomed(jj) = mean(io(k-ppc+1:k));
        if(max(abs(diff(iomed)))<1e-3)
            break;
        end
    end
end

% Exclusion of the data regarding the transitory state
ig = ig(k-ppc+1:k);
t = O(k-ppc+1:k)/(2*pi*fl);
```

```
69 io = io(k-ppc+1:k);
70
71 % Calculation of the low-frequency current ripple
72 Ripple = max(io)-min(io);
73
74
75 % Calculation of the harmonic components of the input current ...
       using the
76 % function fouriercoeff
77
78 [a1, b1] = fouriercoeff(t, ig, 1, 2*pi*fl);
79 I1 = sqrt(a1^2+b1^2);
80 phi1 = atan(a1/b1);
81
82 [a3, b3] = fouriercoeff(t, ig, 3, 2*pi*fl);
83 I3 = sqrt(a3^2 + b3^2);
84
85 [a5, b5] = fouriercoeff(t, ig, 5, 2*pi*fl);
86 I5 = sqrt(a5^2 + b5^2);
87
88 [a7, b7] = fouriercoeff(t, ig, 7, 2*pi*fl);
89 I7 = sqrt(a7^2 + b7^2);
90
91 [a9, b9] = fouriercoeff(t, ig, 9, 2*pi*fl);
92 I9 = sqrt(a9^2 + b9^2);
93
94 [a11, b11] = fouriercoeff(t, ig, 11, 2*pi*fl);
95 I11 = sqrt(a11^2 + b11^2);
96
97 [a13, b13] = fouriercoeff(t, ig, 13, 2*pi*fl);
98 I13 = sqrt(a13^2 + b13^2);
99
100 %Calculation of the THD and the Power factor of the input current
101 THD = sqrt(0.5*(I3^2+I5^2+I7^2+I9^2+I11^2+I13^2))/(I1/sqrt(2));
102
103 PF = abs(cos(phi1)/(sqrt(1+THD^2)));
104
105 end
```

B.4.2 Routine for calculating the inductance

```
function Lm = LmDesign(d0, x, fs, fl, VG, Po, eff)

%Calculation of the magnetizing inductance of the flyback converter
d2 = x(1);
phi2 = x(2);
d4 = x(3);
phi4 = x(4);
d6 = x(5);
phi6 = x(6);
d8 = x(7);
phi8 = x(8);

T = 1/fl;
t = 0:1e-6:T;
vg = VG*sin(2*pi*fl*t);
w = 2*pi*fl*t;

d = d0 + d2*sin(2*w + phi2) + d4*sin(4*w + phi4) + d6*sin(6*w + ...
    phi6)+ d8*sin(8*w + phi8);

Integrando = eff*vg.*vg.*d.*d/(2*Po*fs);

Lm = trapz(t,Integrando)/T;

end
```

B.5 Function for evaluating the IBuFly converter

B.5.1 Main code

```
function [Ripple, I1, I3, I5, I7, I9 , I11, I13, PF, THD, ...
    Indutores, Chf] = calc_ibufly(Case, x)
%% Function for evaluating the main variables of the IBuFly converter

% Parameters loading
d0 = Case(1)*Case(2);
Vt = Case(8);
rd = Case(7);
fs = Case(5);
fl = Case(4);
VG = Case(3);
```

```
11 VB = Case(9);
12 Io = Case(6);
13 Ne = Case(10);
14 Vo = rd*Io + Vt;
15 eff_pfc = Case(11);
16 eff_pc = Case(12);
17 Po = Io*Vo;
18
19 %Function for calculating the magnetizing inductance
20 [Li, Lm] = LIBuFlyDesign(d0, x, fs, fl, VG, VB, Po, eff_pfc, eff_pc);
21
22 Indutores(1) = Li;
23 Indutores(2) = Lm;
24
25
26 %Calculation of the output capacitor (high-frequency)
27 Chf = -(Ne*(d0*VB - Lm*fs*(Case(13) + Io))*(Case(13) + Io - ...
       (d0*VB)/(Lm*Ne*fs)))/(2*Case(14)*Vo*fs*rd);
28 Chf = ceil(Chf*1e6)/1e6;
29
30
31 % Optimization variables
32 d2 = x(1);
33 phi2 = x(2);
34 d4 = x(3);
35 phi4 = x(4);
36 d6 = x(5);
37 phi6 = x(6);
38 d8 = x(7);
39 phi8 = x(8);
40 C = x(9);
41
42 % Auxiliary variables
43 ppc = 1000;
44 wl = 2*pi*fl;
45 Os = 2*pi/ppc;
46 Of = 28*pi;
47 O = 0:Os:Of;
48 N = length(O);
49
50 ig = zeros(1,N);
51 vb = zeros(1,N);
52 io = zeros(1,N);
```

```
53 vo = zeros(1,N);
54
55 %Initial conditions
56 vb(1) = VB;
57 vo(1) = Vt;
58 jj = 0;
59 iomed = zeros(1,3);
60
61
62 %% Numerical solution of the main variables of the converter
63 for k = 1:N
64     o = O(k);
65     d = d0 + d2*sin(2*o+phi2) + d4*sin(4*o+phi4) + ...
           d6*sin(6*o+phi6) + d8*sin(8*o+phi8);
66     vg = VG*sin(o);
67     th1 = asin(vb(k)/VG);
68
69     o_aux = mod(o,2*pi);
70
71     if(o_aux ≤ th1)
72         IL = 0;
73         ig(k) = 0;
74     else if (o_aux > th1 && o_aux ≤(pi-th1))
75             IL = (abs(vg)/(2*Li*fs*vb(k)/d^2))*(abs(vg)-vb(k));
76             ig(k) = (abs(vg)-vb(k))/(2*Li*fs/d^2);
77         else if (o_aux > (pi-th1) && o_aux ≤ (pi+th1))
78                 IL = 0;
79                 ig(k) = 0;
80             else if(o_aux > (pi+th1) && o_aux ≤ (2*pi-th1))
81                     IL = ...
                           (abs(vg)/(2*Li*fs*vb(k)/d^2))*(abs(vg)-vb(k));
82                     ig(k) = -(abs(vg)-vb(k))/(2*Li*fs/d^2);
83                 else if (o_aux > (2*pi-th1) && o_aux ≤ 2*pi)
84                         IL = 0;
85                         ig(k) = 0;
86                     end
87                 end
88             end
89         end
90     end
91
92     vb(k+1) = vb(k) + (Os/(C*wl))*(eff_pfc*IL - ...
           (d*d*vb(k)/(2*Lm*fs)));
```

```
93
94      vo(k+1) = vo(k) + ...
            Os/(wl*Chf)*(eff_pc*vb(k+1)*vb(k+1)*d*d/(2*fs*vo(k)*Lm) - ...
            ((vo(k)-Vt)/rd));
95      io(k)=(vo(k+1)-Vt)/rd;
96
97      %Detection of steady state for stoping the solution
98      %(if the mean of the output current remains constant for 1 ...
            cycle it means that the numerical solution achieved the ...
            steady state)
99      if(mod(k,ppc)==0)
100         jj = mod((jj),3)+1;
101         iomed(jj) = mean(io(k-ppc+1:k));
102         if(max(abs(diff(iomed)))<1e-3)
103             break;
104         end
105     end
106 end
107
108 % Exclusion of the data regarding the transitory state
109 ig = ig(k-ppc+1:k);
110 t = O(k-ppc+1:k)/(2*pi*fl);
111 io = io(k-ppc+1:k);
112
113 % Calculation of the low-frequency current ripple
114 Ripple = max(io)-min(io);
115
116 % Calculation of the harmonic components of the input current ...
        using the
117 % function fouriercoeff
118
119 [a1, b1] = fouriercoeff(t, ig, 1, 2*pi*fl);
120 I1 = sqrt(a1^2+b1^2);
121 phi1 = atan(a1/b1);
122
123 [a3, b3] = fouriercoeff(t, ig, 3, 2*pi*fl);
124 I3 = sqrt(a3^2 + b3^2);
125
126 [a5, b5] = fouriercoeff(t, ig, 5, 2*pi*fl);
127 I5 = sqrt(a5^2 + b5^2);
128
129 [a7, b7] = fouriercoeff(t, ig, 7, 2*pi*fl);
130 I7 = sqrt(a7^2 + b7^2);
```

```
131
132 [a9, b9] = fouriercoeff(t, ig, 9, 2*pi*fl);
133 I9 = sqrt(a9^2 + b9^2);
134
135 [a11, b11] = fouriercoeff(t, ig, 11, 2*pi*fl);
136 I11 = sqrt(a11^2 + b11^2);
137
138 [a13, b13] = fouriercoeff(t, ig, 13, 2*pi*fl);
139 I13 = sqrt(a13^2 + b13^2);
140
141
142 %Calculation of the THD and the Power factor of the input current
143
144 THD = sqrt(0.5*(I3^2+I5^2+I7^2+I9^2+I11^2+I13^2))/(I1/sqrt(2));
145
146 PF = abs(cos(phi1)/(sqrt(1+THD^2)));
147
148 end
```

B.5.2 Routine for calculating the inductance

```
1  function [Li, Lm] = LIBuFlyDesign(d0, x, fs, fl, VG, VB, Po, ...
       eff_pfc, eff_pc)
2  %Calculation of the IBuFly converter inductances
3  d2 = x(1);
4  phi2 = x(2);
5  d4 = x(3);
6  phi4 = x(4);
7  d6 = x(5);
8  phi6 = x(6);
9  d8 = x(7);
10 phi8 = x(8);
11
12 %% Calculation of the flyback converter magnetizing inductance
13 T = 1/fl;
14 t = 0:1e-4:T;
15 w = 2*pi*fl*t;
16 d = d0 + d2*sin(2*w + phi2) + d4*sin(4*w + phi4) + d6*sin(6*w + ...
       phi6)+ d8*sin(8*w + phi8);
17 integFly = eff_pc*VB^2.*d.*d/(2*Po*fs);
18 Lm = trapz(t,integFly)/T;
```

```
19
20 %% Calculation of the buck converter inductance
21 th1 = asin(VB/VG);
22 th = th1:1e-3:pi-th1;
23 vg = VG*sin(th);
24 d = d0 + d2*sin(2*th + phi2) + d4*sin(4*th + phi4) + d6*sin(6*th + ...
       phi6)+ d8*sin(8*th + phi8);
25 integbu = ((vg - VB).*vg.*d.*d)/(2*fs);
26 Li = (1/(pi*Po/(eff_pfc*eff_pc)^2))*trapz(th,integbu);
27
28 end
```

B.6 Function for evaluating the IBoBu converter

B.6.1 Main code

```
1  function [Ripple, I1, I3, I5, I7, I9 , I11, I13, PF, THD, ...
       Indutores, Chf] = calc_ibobu(Case, x)
2  %% Function for evaluating the main variables of the IBoBu converter
3
4  % Parameters loading
5  d0 = Case(1)*Case(2);
6  Vt = Case(8);
7  rd = Case(7);
8  fs = Case(5);
9  fl = Case(4);
10 VG = Case(3);
11 VB = Case(9);
12 eff_pfc = Case(11);
13 eff_pc = Case(12);
14 Io = Case(6);
15 Vo = Vt + rd*Io;
16 Po = Io^2*rd + Io*Vt;
17
18 %Function for calculating the magnetizing inductance
19 [Li, Lo] = LIBoBuDesign(d0, x, fs, VG, VB, Vo, Po, eff_pfc, eff_pc);
20
21 Indutores(1) = Li;
22 Indutores(2) = Lo;
23
24 %Calculation of the output capacitor (high-frequency)
```

```
25 Chf = (((Io+Case(13)/2) - (d0*(VB - Vo))/(Lo*fs))*(Vo*(d0*VB - ...
       Case(14)*Lo*fs) - d0*VB^2 + (Case(14)*Lo*VB*fs)/2 + ...
       (Io+Case(13)/2)*Lo*VB*fs))/(2*Case(14)*Vo*fs*rd*(VB - Vo));
26 Chf = ceil(Chf*1e6)/1e6;
27
28 % Optimization variables
29 d2 = x(1);
30 phi2 = x(2);
31 d4 = x(3);
32 phi4 = x(4);
33 d6 = x(5);
34 phi6 = x(6);
35 d8 = x(7);
36 phi8 = x(8);
37 C = x(9);
38
39 % Auxiliary variables
40 ppc = 1000;
41 wl = 2*pi*fl;
42 Os = 2*pi/ppc;
43 Of = 28*pi;
44 O = 0:Os:Of;
45 N = length(O);
46
47 ig = zeros(1,N);
48 vb = zeros(1,N);
49 io = zeros(1,N);
50 vo = zeros(1,N);
51
52 %Initial conditions
53 vb(1) = VB;
54 vo(1) = Vt;
55 jj = 0;
56 iomed = zeros(1,3);
57
58 %% Numerical solution of the main variables of the converter
59 for k = 1:N
60
61     o = O(k);
62     d = d0 + d2*sin(2*o+phi2) + d4*sin(4*o+phi4) + ...
           d6*sin(6*o+phi6) + d8*sin(8*o+phi8);
63     vg = VG*sin(o);
64
```

```
65      if(vg ≥ 0)
66          ig(k) = (1/(2*Li*fs))*d^2*(abs(vg)*vb(k))/(vb(k)-abs(vg));
67      else
68          ig(k) = -(1/(2*Li*fs))*d^2*(abs(vg)*vb(k))/(vb(k)-abs(vg));
69      end
70
71      vb(k+1) = vb(k) + ...
            (Os/(C*wl))*((d*d*vg*vg)/(2*Li*fs*(vb(k)-abs(vg))) - ...
            d^2*(vb(k)-vo(k))/(2*Lo*fs));
72      IL = (vb(k)*d^2/(2*Lo*fs*vo(k)))*(vb(k)-vo(k));
73      io(k) = (vo(k) - Vt)/rd;
74      vo(k+1) = vo(k) + (Os/(Chf*wl))*(IL - io(k));
75
76
77
78      %Detection of steady state for stoping the solution
79      %(if the mean of the output current remains constant for 1 ...
            cycle it means that the numerical solution achieved the ...
            steady state)
80      if(mod(k,ppc)==0)
81          jj = mod((jj),3)+1;
82          iomed(jj) = mean(io(k-ppc+1:k));
83          if(max(abs(diff(iomed)))<1e-3)
84              break;
85          end
86      end
87
88  end
89
90  % Exclusion of the data regarding the transitory state
91  ig = ig(k-ppc+1:k);
92  t = O(k-ppc+1:k)/(2*pi*fl);
93  io = io(k-ppc+1:k);
94
95  % Calculation of the low-frequency current ripple
96  Ripple = max(io)-min(io);
97
98  % Calculation of the harmonic components of the input current ...
        using the
99  % function fouriercoeff
100
101 [a1, b1] = fouriercoeff(t, ig, 1, 2*pi*fl);
102 I1 = sqrt(a1^2+b1^2);
```

```
103 phi1 = atan(a1/b1);
104
105 [a3, b3] = fouriercoeff(t, ig, 3, 2*pi*fl);
106 I3 = sqrt(a3^2 + b3^2);
107
108 [a5, b5] = fouriercoeff(t, ig, 5, 2*pi*fl);
109 I5 = sqrt(a5^2 + b5^2);
110
111 [a7, b7] = fouriercoeff(t, ig, 7, 2*pi*fl);
112 I7 = sqrt(a7^2 + b7^2);
113
114 [a9, b9] = fouriercoeff(t, ig, 9, 2*pi*fl);
115 I9 = sqrt(a9^2 + b9^2);
116
117 [a11, b11] = fouriercoeff(t, ig, 11, 2*pi*fl);
118 I11 = sqrt(a11^2 + b11^2);
119
120 [a13, b13] = fouriercoeff(t, ig, 13, 2*pi*fl);
121 I13 = sqrt(a13^2 + b13^2);
122
123 %Calculation of the THD and the Power factor of the input current
124
125 THD = sqrt(0.5*(I3^2+I5^2+I7^2+I9^2+I11^2+I13^2))/(I1/sqrt(2));
126
127 PF = abs(cos(phi1)/(sqrt(1+THD^2)));
128 end
```

B.6.2 Routine for calculating the inductance

```
1  function [Li, Lo] = LIBoBuDesign(d0, x, fs, VG, VB, Vo, Po, ...
       eff_pfc, eff_pc)
2  %Calculation of the IBoBu converter inductances
3  d2 = x(1);
4  phi2 = x(2);
5  d4 = x(3);
6  phi4 = x(4);
7  d6 = x(5);
8  phi6 = x(6);
9  d8 = x(7);
10 phi8 = x(8);
11
```

```
12 %% Calculation of the boost converter inductance
13 theta = 0:0.001:pi;
14 vg = VG*sin(theta);
15 d = d0 + d2*sin(2*theta + phi2) + d4*sin(4*theta + phi4) + ...
       d6*sin(6*theta + phi6)+ d8*sin(8*theta + phi8);
16 integbo = (d.*d/(2*fs)).*((vg*VB)./(VB - vg)).*vg;
17 Li = 1/(pi*Po/(eff_pfc*eff_pc))*trapz(theta,integbo);
18
19 %% Calculation of the buck converter inductance
20 integbu = ((VB - Vo)*VB.*d.*d)/(2*fs);
21 Lo = (1/(pi*Po/eff_pc))*trapz(theta,integbu);
22
23 end
```

B.7 Function for evaluating the IDBB converter

B.7.1 Main code

```
1  function [Ripple, I1, I3, I5, I7, I9 , I11, I13, PF, THD, ...
       Indutores, Chf] = calc_idbb(Case, x)
2  %% Function for evaluating the main variables of the IDBB converter
3
4  % Parameters loading
5  d0 = Case(1)*Case(2);
6  Vt = Case(8);
7  rd = Case(7);
8  fs = Case(5);
9  fl = Case(4);
10 VG = Case(3);
11 VB = Case(9);
12 eff_pfc = Case(11);
13 eff_pc = Case(12);
14 Io = Case(6);
15 Vo = Vt + rd*Io;
16 Po = Io^2*rd + Io*Vt;
17
18 %Function for calculating the magnetizing inductance
19 [Li, Lo] = LIDBBDesign(d0, x, fs, fl, VG, VB, Po, eff_pfc, eff_pc);
20 Indutores(1) = Li;
21 Indutores(2) = Lo;
22
```

```
%Calculation of the output capacitor (high-frequency)
Chf = (1/((Case(14))*fs*rd))*(Io+(Case(13))/2)*(1-d0*VB/Vo);
Chf = ceil(Chf*1e6)/1e6;

% Optimization variables
d2 = x(1);
phi2 = x(2);
d4 = x(3);
phi4 = x(4);
d6 = x(5);
phi6 = x(6);
d8 = x(7);
phi8 = x(8);
C = x(9);

% Auxiliary variables
ppc = 1000;
wl = 2*pi*fl;
Os = 2*pi/ppc;
Of = 28*pi;
A = 2*C*wl*Li*fs;
B = 2*C*wl*Lo*fs;
O = 0:Os:Of;
N = length(O);

ig = zeros(1,N);
vb = zeros(1,N);
vo = zeros(1,N);
io = zeros(1,N);

%Initial conditions
vb(1) = VB;
vo(1) = Vt;
jj = 0;
iomed = zeros(1,3);


%% Numerical solution of the main variables of the converter
for k = 1:N
    o = O(k);
    d = d0 + d2*sin(2*o+phi2) + d4*sin(4*o+phi4) + ...
        d6*sin(6*o+phi6) + d8*sin(8*o+phi8);
    vg = VG*sin(o);
```

```
65      ig(k) = d^2*vg/(2*fs*Li);
66      vb(k+1) = vb(k) + Os*d*d*(eff_pfc*vg*vg/(A*vb(k)) - (vb(k)/B));
67      vo(k+1) = vo(k) + ...
            Os/(wl*Chf)*(eff_pc*vb(k+1)^2*d^2/(2*fs*vo(k)*Lo) - ...
            ((vo(k)-Vt)/rd));
68      io(k)=(vo(k+1)-Vt)/rd;
69
70      %Detection of steady state for stoping the solution
71      %(if the mean of the output current remains constant for 1 ...
            cycle it means that the numerical solution achieved the ...
            steady state)
72      if(mod(k,ppc)==0)
73          jj = mod((jj),3)+1;
74          iomed(jj) = mean(io(k-ppc+1:k));
75          if(max(abs(diff(iomed)))<1e-3)
76              break;
77          end
78      end
79  end
80
81  % Exclusion of the data regarding the transitory state
82  ig = ig(k-ppc+1:k);
83  t = O(k-ppc+1:k)/(2*pi*fl);
84  io = io(k-ppc+1:k);
85
86  % Calculation of the low-frequency current ripple
87  Ripple = max(io)-min(io);
88
89  % Calculation of the harmonic components of the input current ...
        using the
90  % function fouriercoeff
91  [a1, b1] = fouriercoeff(t, ig, 1, 2*pi*fl);
92  I1 = sqrt(a1^2+b1^2);
93  phi1 = atan(a1/b1);
94
95  [a3, b3] = fouriercoeff(t, ig, 3, 2*pi*fl);
96  I3 = sqrt(a3^2 + b3^2);
97
98  [a5, b5] = fouriercoeff(t, ig, 5, 2*pi*fl);
99  I5 = sqrt(a5^2 + b5^2);
100
101 [a7, b7] = fouriercoeff(t, ig, 7, 2*pi*fl);
102 I7 = sqrt(a7^2 + b7^2);
```

```
103
104 [a9, b9] = fouriercoeff(t, ig, 9, 2*pi*fl);
105 I9 = sqrt(a9^2 + b9^2);
106
107 [a11, b11] = fouriercoeff(t, ig, 11, 2*pi*fl);
108 I11 = sqrt(a11^2 + b11^2);
109
110 [a13, b13] = fouriercoeff(t, ig, 13, 2*pi*fl);
111 I13 = sqrt(a13^2 + b13^2);
112
113 %Calculation of the THD and the Power factor of the input current
114
115 THD = sqrt(0.5*(I3^2+I5^2+I7^2+I9^2+I11^2+I13^2))/(I1/sqrt(2));
116
117 PF = abs(cos(phi1)/(sqrt(1+THD^2)));
118
119 end
```

B.7.2 Routine for calculating the inductance

```
1  function [Li, Lo] = LIDBBDesign(d0, x, fs, fl, VG, VB, Po, ...
       eff_pfc, eff_pc)
2
3  %Calculation of the IDBB converter inductances
4  d2 = x(1);
5  phi2 = x(2);
6  d4 = x(3);
7  phi4 = x(4);
8  d6 = x(5);
9  phi6 = x(6);
10 d8 = x(7);
11 phi8 = x(8);
12
13 %% Calculation of the PFC stage inductance
14 T = 1/fl;
15 t = 0:1e-6:T;
16 vg = VG*sin(2*pi*fl*t);
17 w = 2*pi*fl*t;
18 d = d0 + d2*sin(2*w + phi2) + d4*sin(4*w + phi4) + d6*sin(6*w + ...
       phi6)+ d8*sin(8*w + phi8);
19 Integrando = (eff_pfc*eff_pc)*vg.*vg.*d.*d/(2*Po*fs);
```

```
Li = trapz(t,Integrando)/T;

%% Calculation of the PC stage inductance
Lo = (2*Li)/(sqrt(eff_pfc)*(VG/VB)^2);

end
```

B.8 Auxiliary functions

B.8.1 Function for the cluster configuration

```
function cluster = clusterConfig(JOB_STORAGE_LOCATION, walltime)

MATLAB_PATH = '/opt/MATLAB/R2015a';

cluster = ...
    parallel.cluster.Generic('JobStorageLocation',JOB_STORAGE_LOCATION);
set(cluster, 'HasSharedFilesystem', true);
set(cluster, 'ClusterMatlabRoot', MATLAB_PATH);
set(cluster, 'OperatingSystem', 'unix');
set(cluster, 'IndependentSubmitFcn', {@mySubmitIndFcn, walltime}); ...
    % If you want to run communicating jobs (including parallel ...
    pools), you must specify a CommunicatingSubmitFcn
set(cluster, 'CommunicatingSubmitFcn',{@mySubmitComFcn, walltime});
set(cluster, 'GetJobStateFcn', @getJobStateFcn);
set(cluster, 'DeleteJobFcn', @deleteJobFcn);
```

B.8.2 Function for verifying which cases were not executed

```
function NotExecuted = verifyNE(NCases,Harm,pathTemp)
%Simple function for verifying which cases were not executed by the
%algorithm
D = dir([pathTemp,'*.mat']);
k =1;
for n = 1:NCases
    for h =1:size(Harm,1)
        NotExecuted(k,:) = [Harm(h,1) Harm(h,2) n];
        k = k+1;
    end
```

```
11 end
12
13 for ii=1:length(D)
14   num = [str2double(D(ii).name(1)) str2double(D(ii).name(2)) ...
         str2double(D(ii).name(3:end-4))];
15   NotExecuted(NotExecuted(:,1) == num(1) & NotExecuted(:,2) == ...
         num(2) & NotExecuted(:,3) == num(3),:)=[];
16 end
17
18 end
```

B.8.3 Function for calculating the Fourier coefficients

```
1  function [ ax, bx] = fouriercoeff(t, ig, Or, w)
2
3  %Function for calculating the coefficients of the fourier seriers
4
5  T = 2*pi/w;
6  ts = t(2)-t(1);
7
8  th = w*t;
9
10 ax = (2/T)*trapz(ts*ig.*cos(Or*th));
11 bx = (2/T)*trapz(ts*ig.*sin(Or*th));
12
13 end
```

APPENDIX C – MATLAB SCRIPTS USED IN THE OPTIMIZATION ALGORITHM OF CHAPTER 6

This appendix compiles the main scripts used for solving the optimization algorithm proposed in Chapter 6. The codes are presented in the following. One can note that the main features of each routine were commented to help the understanding of the program.

C.1 Script for calculating the matrix S

```
1
2 %Script for calculating the solution of the optimization problem
3 clearvars;clc;close all;
4
5 load R %Load matrix R, calculated by means of the script getR.m
6 wopt = 1;
7 F = (wopt/min(R(:,1)))*R(:,1)+((1-wopt)/min(R(:,2)))*R(:,2);
8 S = sortrows([F R],1);
```

C.2 Script for calculating the matrix R

```
1
2 clearvars;clc;
3
4 %Script for obtaining the matrix R, which is used in the optimization
5 %routine
6
7
8 %% Application parameters
9
10 %Main parameters
```

```
Io = 0.5;                   % Output current
rd = 38.4645;               % Dynamic resistance of the LED lamp
Vt= 129.37;                 % Threshold voltage of the LED lamp
fl=60;                      % Line frequency
fs=50e3;                    % Switching frequency
VG  = sqrt(2)*220;          % Nominal input voltage
DIo_LF = 0.1*Io;            % Maximum low-frequency ripple of the ...
    output current
effPFC = 0.922;             % Estimated efficiency of the PFC stage
effPC = 0.922;              % Estimated efficiency of the PC stage
VBmax = 200;                % Maximum voltage of the bus capacitor
tcmax = 0.5;                % Maximum convergence time - 0.5 s
VB = 160;                   % Average bus capacitor voltage
D0r = 0.75;                 % Relative value of D0
VPWM = 3;                   % Peak voltage of the PWM modulator

% Elements calculated by using the expressions shown in Chapter 6 ...
    and the
% main parameters of the application

% Inductors
L1=3.592145e-04;
L2=2.060815e-04;

% Output capacitor
Co = 12e-6;

% Critical duty cycle

Dcrit = 0.3396;
D0 = D0r*Dcrit;

%Current sensor
Kcs = 2.75;                 %Gain of the current sensor
fcs = 4823;                 %Cutoff frequency of the current sensor

wcs = 2*pi*fcs;             %Angular cutoff frequency of the ...
    current sensor

%% Search-space definition

%Search-space of the bus capacitor
CBrange = [10 22 33 47 100 150 220 330]*1e-6;
```

```
51
52 %Search-space of the PI controller elements
53 e12 = [1 1.2 1.5 1.8 2.2 2.7 3.3 3.9 4.7 5.6 6.8 8.2];
54 r1range = [e12*1e3 e12*1e4 e12*1e5];
55 r2range = [e12*1e3 e12*1e4 e12*1e5];
56 c1range = [e12*1e-9 e12*1e-8 e12*1e-7];
57
58 %Definition of the search-space
59 SS = ...
       zeros(length(CBrange)*length(r1range)*length(r2range)*length(c1range),4);
60 k =1;
61
62 for cbi = 1:length(CBrange)
63     for r1i = 1:length(r1range)
64         for r2i = 1:length(r2range)
65             for c1i = 1:length(c1range)
66                 %             CB           R1            R2 ...
                                 C1
67                 SS(k,:) = [CBrange(cbi) r1range(r1i) r2range(r2i) ...
                       c1range(c1i)];
68                 k = k+1;
69             end
70         end
71     end
72 end
73
74 %Calculation of the size of the search-space
75 N = size(SS,1);
76
77 R = zeros(N,7); %Preallocation of Matrix R with its maximum ...
       possible size
78
79 rindex = 1;
80
81 for k=100000:N
82
83     clc;
84     fprintf('Status: %.2f %% concluded',100*k/N); %Comment lines ...
           83 and 84 for reducing the execution time
85
86     %x = [CB R1 R2 C1]
87     x = SS(k,:); %Selecting the next possible solution
88
```

```
89      % Calculation of the constraints
90      [d_const, tc_const, vb_const, Ripple, I1, I3, I5, I7, I9 , ...
           I11, I13, PF, THD, Gm, Pm] = IDBBEval(Io, rd, Vt, fl, fs, ...
           VG, effPFC, effPC, L1, L2, Co, VB, Dcrit, tcmax, VBmax,  ...
           D0, Kcs, wcs, VPWM, x);
91
92      H =     [Ripple - DIo_LF;
93               d_const
94               I3      - 0.3*PF*I1;
95               I5      - 0.1*I1;
96               I7      - 0.07*I1;
97               I9      - 0.05*I1;
98               I11     - 0.03*I1;
99               I13     - 0.03*I1;
100              tc_const;
101              vb_const;
102              30-Pm;
103              2 - Gm];
104
105     % Requirements met?
106         if(max(H)>0)
107             continue;
108         end
109
110     % Calculation of the SOC functions
111     c1 = x(1)*10e6 + Ripple;
112     c2 = THD;
113
114     %Update Matrix R
115
116     R(rindex,:) = [c1 c2 Ripple x];
117     rindex = rindex + 1;
118
119 end
120
121 R(rindex:end,:) = []; % Exclusion of the empty rows of R
122
123 % Storage of matrix R
124 save('R.mat');
```

C.3 Function for calculating the constraints

```
function [d_const, tc_const, vb_const,  Ripple, I1, I3, I5, I7, I9 ...
    , I11, I13, PF, THD, Gm, Pm] = IDBBEval(Io, rd, Vt, fl, fs, VG, ...
    effPFC, effPC, L1, L2, Co, VB, Dcrit, tcmax, VBmax,  D0, Kcs, ...
    wcs, VPWM, x)


%Optimization vector: x = [CB R1 R2 C1]

CB = x(1);
Kp = x(3)/x(2);     %Kp = R2/R1
Ti = x(3)*x(4);     %Ti = R2*C1


%AuxiL1ary parameters
ppc = 2000;
fa = (fl*ppc);
wl = 2*pi*fl;
ts = 1/fa;
tend = 31/fl;
T = 0:ts:tend;
N = length(T);

ig = zeros(1,N);
vb = zeros(1,N);
io = zeros(1,N);
vo = zeros(1,N);
vcs = zeros(1,N);
vpi = zeros(1,N);
d = zeros(1,N);

%Initial conditions
vo(1) = Vt;
vb(1) = VB; % Condição inicial para a solução da equação diferencial
vcs(1) = 0;
vpi(1) = D0*VPWM;
jj = 0;
iomed = zeros(1,3);
d(1)= D0;


```

```
38 %% Solution of the circuit variables
39 for k = 1:N
40
41     t = T(k);
42     vg = VG*sin(wl*t);
43     ig(k) = d(k)^2*vg/(2*fs*L1);
44     vb(k+1) = vb(k) + ts*d(k)^2/(2*CB*fs)*(effPFC*vg*vg/(L1*vb(k)) ...
           - (vb(k)/L2));
45     vo(k+1) = vo(k) + ...
           (ts/(Co))*(effPC*vb(k+1)^2*d(k)^2/(2*fs*vo(k)*L2) - ...
           ((vo(k)-Vt)/rd));
46     io(k)=(vo(k)-Vt)/rd;
47     vcs(k+1) = vcs(k) + ts*(wcs*(Kcs*io(k) - vcs(k)));
48     vpi(k+1) = vpi(k) + ts*(Kp/Ti*(Kcs*Io) - Kp*Kcs*wcs*io(k) + ...
           vcs(k)*(Kp*wcs - Kp/Ti));
49     d(k+1) = vpi(k+1)/VPWM;
50
51     %Saturation of the duty cycle to avoid numerical errors
52     if(d(k+1)>1)
53         d(k+1)=1;
54     else if (d(k+1)<0)
55             d(k+1)=0;
56         end
57     end
58
59     %Detection of steady state for stoping the solution
60     %(if the mean of the output current remains constant for 1 ...
           cycle it means that the numerical solution achieved the ...
           steady state)
61     if(mod(k,ppc)==0)
62         jj = mod((jj),3)+1;
63         iomed(jj) = mean(io(k-ppc+1:k));
64         if(max(abs(diff(iomed)))<1e-3)
65             break;
66         end
67     end
68 end
69
70 %Calculation of the convergence time
71 tc = k/fa;
72
73 %Exclusion of the transitory part of the variables - only the last ...
       cycle is stored.
```

```
74  ig = ig(k-ppc+1:k);
75  io = io(k-ppc+1:k);
76  vb = vb(k-ppc+1:k);
77  d = d(k-ppc+1:k);
78  t = T(k-ppc+1:k);
79
80  %Check the constraints number 2, 9 and 10
81  if(max(d)>Dcrit)
82      d_const = 1;
83      vb_const = 0;
84      tc_const = 0;
85      Ripple =0; I1=0; I3=0; I5=0; I7=0; I9=0; I11=0; I13=0; ...
            PF=0;THD=0;Gm=2;Pm=30;
86      return;
87  end
88
89  if(tc≥tcmax)
90      tc_const = 1;
91      d_const = 0;
92      vb_const = 0;
93      Ripple =0; I1=0; I3=0; I5=0; I7=0; I9=0; I11=0; I13=0; ...
            PF=0;THD=0;Gm=2;Pm=30;
94      return;
95  end
96
97  if(max(vb)>0.95*VBmax)
98      vb_const = 1;
99      d_const = 0;
100     tc_const = 0;
101     Ripple =0; I1=0; I3=0; I5=0; I7=0; I9=0; I11=0; I13=0; ...
            PF=0;THD=0;Gm=2;Pm=30;
102     return;
103 end
104
105
106 %Feature extraction section
107
108
109 Ripple = max(io) - min(io); %Calculation of the L2w ...
        frequency-ripple of the output current
110
111
112 %Calculation of the harmonic components of the input current
```

```
113
114   [a1, b1] = fouriercoeff(t, ig, 1, 2*pi*fl);
115   I1 = sqrt(a1^2+b1^2);
116   phi1 = atan(a1/b1);
117
118   [a2, b2] = fouriercoeff(t, ig, 2, 2*pi*fl);
119   I2 = sqrt(a2^2 + b2^2);
120
121   [a3, b3] = fouriercoeff(t, ig, 3, 2*pi*fl);
122   I3 = sqrt(a3^2 + b3^2);
123
124   [a5, b5] = fouriercoeff(t, ig, 5, 2*pi*fl);
125   I5 = sqrt(a5^2 + b5^2);
126
127   [a7, b7] = fouriercoeff(t, ig, 7, 2*pi*fl);
128   I7 = sqrt(a7^2 + b7^2);
129
130   [a9, b9] = fouriercoeff(t, ig, 9, 2*pi*fl);
131   I9 = sqrt(a9^2 + b9^2);
132
133   [a11, b11] = fouriercoeff(t, ig, 11, 2*pi*fl);
134   I11 = sqrt(a11^2 + b11^2);
135
136   [a13, b13] = fouriercoeff(t, ig, 13, 2*pi*fl);
137   I13 = sqrt(a13^2 + b13^2);
138
139
140      %Calculation of the power factor and the THD
141   THD = ...
         max(sqrt(0.5*(I3^2+I5^2+I7^2+I9^2+I11^2+I13^2))/(I1/sqrt(2)),0.01);
142
143   PF = abs(cos(phi1)/(sqrt(1+THD^2)));
144
145
146   %Phase margin calculation
147
148   Vo = Vt + rd*Io;
149   rc = 0.1;
150
151  JDd = D0*VB^2/(L2*fs*Vo);
152  GDo = -D0^2*VB^2/(2*L2*fs*Vo^2);
153  K = JDd/(1-GDo*rd);
154  wz = 1/(rc*Co);
```

```
155 wp = (1-GDo*rd)/((rd+rc-GDo*rd*rc)*Co);
156
157 Giod = K*tf([1/wz 1],[1/wp 1]);
158 Gc = Kp*tf([Ti 1],[Ti 0]);
159
160 H = tf([0  Kcs*wcs],[1 wcs]);
161 G = series(series(Giod,Gc/VPWM),H);
162
163 [Gm,Pm,¬,¬] = margin(G);
164
165
166 d_const = 0;
167 vb_const = 0;
168 tc_const = 0;
```

APPENDIX D – SUPPLEMENTARY MATERIAL OF CHAPTER 5

The design results for all the cases analyzed in Chapter 5 can be accessed by means of the following URLs:

https://goo.gl/8JwXDj

https://goo.gl/npEjx6

The material consists of four spreadsheets containing the design results of each analyzed converter. The files are divided in eleven sheets, each one containing the data regarding a specific harmonic configuration.